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Design of an Efficient 900 GHz Antenna in Standard CMOS Technology for Imaging Arrays

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***Abstract*—This paper describes and addresses the challenges that are encountered while designing a 900 GHz antenna for FET detectors using a standard submicron CMOS technology. The reduced metal stack, the problem of surface waves and technology-related rules are taken into account in order to properly design an efficient antenna, with the objective to couple it to field-effect transistor (FET) detectors in a focal-plane array configuration. Simulations on a 0.15-µm standard CMOS technology show that up to 58% efficiency with responsivity in the several kV/W range can be achieved.**

***Index Terms*—antenna, CMOS, imaging, self-mixing, terahertz.**

I. Introduction

Terahertz (THz) detectors based on field-effect transistors (FET) self-mixing principle implemented using CMOS technologies [1] have a number of advantages with respect to other uncooled solutions, spanning from the possibility to easily implement low cost imaging arrays with good sensitivity, to the possibility of integrating processing electronics for the signal amplification. On the other hand, technological constraints and the lossy silicon substrate complicate the design of the antenna needed to properly couple the incoming radiation.

As far as the lossy substrate is of concern, mainly two solutions can be implemented in such a way that surface waves are not jeopardizing the performance of the antenna. The use of a ground plane with patch antennas with top-side illumination [2] effectively eliminates the substrate contribution. Another option is to illuminated the sensor from the silicon side by means of a high-resistivity hyperemispherical lens [3], requiring thinning of the lossy substrate to improve efficiency and more complex assembly.

In this contribution, the design of a 900 GHz integrated CMOS antenna for FET imaging arrays is presented, taking into account all technological constraints, from the back-end-of-line (BEOL) metal stack height to the fulfilling of the manufacturing and reliability rules.

II. Antenna Design

A. Detector Impedance and Matching

The FET detector impedance is given by the equivalent transmission line representing the transistor channel and is given by

$$Z_{FET} = \sqrt{\frac{R_{DS}}{j\omega WLC_{ox}}} \parallel \frac{1}{j\omega WC_{gso}}, \quad (1)$$

where W and L are the transistor size, R_{DS} is the channel resistance, C_{ox} is the oxide area capacitance and C_{gso} is an additional parallel parasitic capacitance. This gives rise to an impedance with a strong capacitive part which is hard to compensate with matching techniques because of the high losses of the aluminum composing the metal interconnections.

Therefore, optimal coupling can be achieved by tuning the antenna frequency in a region where it presents a relevant inductive component, which in turn means designing a slightly smaller antenna for a given frequency. With the chosen technology, $Z_{FET} = 16 - 350i\ \Omega$ at the frequency of 900 GHz.

The relevant quantity for the detection principle is the squared voltage at its input port, which in general matching conditions [2] results to be proportional to the factor

$$R_{eq} = 4e_{rad}\, Re(Z_{ANT}) \left| \frac{Z_{FET}}{Z_{FET} + Z_{ANT}} \right|^2. \quad (2)$$

This expression, which has Ohm units, can be considered an equivalent resistance function of the impedance of detector Z_{FET}, of antenna Z_{ANT} and radiation efficiency e_{rad}, and can therefore be used as a parameter to be maximized.

B. Use of the Metal Stack

A 0.15-µm 6-metal CMOS process technology with thick metal option has been chosen for this design. Simulations show that conventional metal layer thickness (typically less than 1 µm thick) induces high losses in the antenna transmission, and therefore the use of a thick metal option, when available, improves significantly the efficiency.

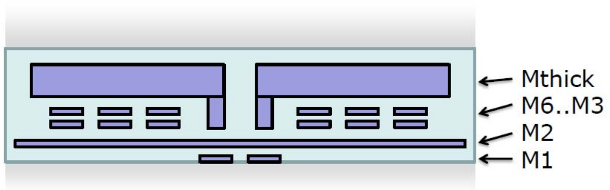

Fig. 1. Simplified cross-section of the CMOS back-end-of-line with the purpose of each layer.

At the same time, there are two opposite constraints on the choice of the metal level to be used as shield: on the one hand, the antenna-ground plane distance has to be large enough so that induced currents are not canceling out the field, and on the other hand some layers should be left available for routing and, possibly, for electronics.

Therefore, as shown in Fig. 1, thick metal option with approximately 6 μm thickness has been used for the antenna body and metal 2 for the ground plane, while metal 1 is available for the detector connection and signals routing. This choice has the advantage of avoiding any interference of these interconnections with the radiation properties of the antenna, at the expense of about 5% efficiency loss. The remaining metals, in order to fulfill the manufacturing rules, have to comply with "coverage" rules and therefore dummy patches have to be placed so as to reach about 30% of the total area.

C. Optimization of the Antenna Design

The implemented antenna is a bowtie, which resulted to be effective in maintaining a good efficiency while respecting the relatively large manufacturing rules of the thick metal. The antenna body is connected to the detector, which is on the silicon substrate, with vias passing through all metal levels, ground plane included. This interconnection introduces a small but relevant inductive component which contributes to improve the matching with the detector.

Special care had to be taken in the placement of dummy metal for manufacturing yield purposes, in such a way that their presence is not disturbing the performance of the antenna. This resulted in having a certain clearance in the feed area, while reaching the 30% target fill coverage. These dummy structures, if properly placed, not only do not reduce the antenna performance, but strongly decrease surface waves in the dielectric [4][5]. Due to the ground plane, there are no surface waves in the silicon, but the dummy metals still bring the advantage of slightly improving the effective dielectric constant of the oxide without introducing additional losses.

III. SIMULATIONS AND DISCUSSION

A parameterized model (see Fig. 2) has been setup and simulated. By means of optimization of the main dimensional parameters, the results shown in Fig. 3 have been obtained. At the center frequency of 900 GHz, the antenna shows a radiation efficiency of 58% with a maximum R_{eq} = 2330 Ω.

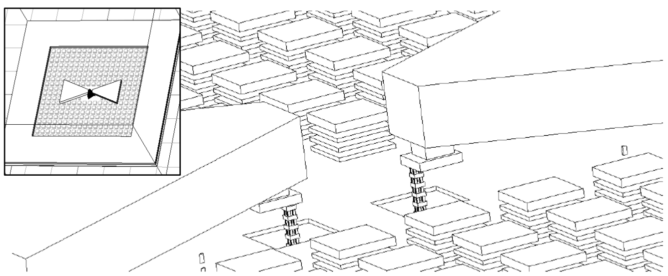

Fig. 2. A drawing of the complete model of the antenna used for simulations.

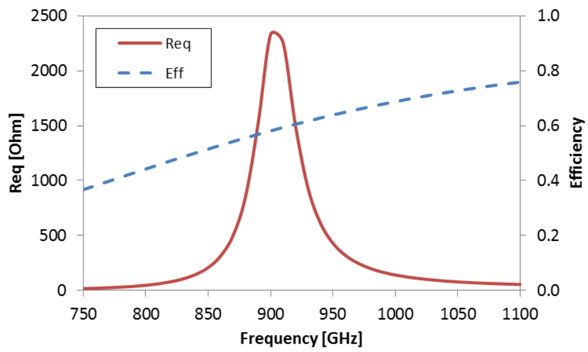

Fig. 3. Response and efficiency of antenna coupled to detector using the equivalent resistance factor.

To convert this figure to a typically comparable quantity, it is possible to consider that voltage responsivity is obtained multipliying R_{eq} by ideal current responsivity [2], which in optimal bias conditions can reach several Ampere/Watt, and therefore several kVolt/Watt are achievable.

Moreover, as expected due to the shielding of the substrate with the ground plane, stable directivity and far-field patterns are obtained without any surface waves. In particular, effective area obtained from directivity at 900 GHz suggests feasible pixel pitch of 200μm for the focal-plane arrangement.

IV. CONCLUSIONS

An antenna for a 900 GHz FET detector has been designed maximizing efficiency and response while obeying to the CMOS process manufacturing rules and constraints.

Simulations results show that high responsivities in the kV/W range are achievable thanks to 58% radiation efficiency and no surface waves. Arrangement in a pixel grid of 200 μm is feasible for the implementation of imaging arrays, also considering that the lower metal level is available for connections and processing electronics.

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