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Very Low Temperature Epitaxy of Group-IV Semiconductors for Use in FinFET, Stacked Nanowires and Monolithic 3D Integration

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As CMOS scaling proceeds with sub-10 nm nodes, new architectures and materials are implemented to continue increasing performances at constant footprint. Strained and stacked channels and 3D-integrated devices have for instance been introduced for this purpose. A common requirement for these new technologies is a strict limitation in thermal budgets to preserve the integrity of devices already present on the chips. We present our latest developments on low-temperature epitaxial growth processes, ranging from channel to source/drain applications for a variety of devices and describe options to address the upcoming challenges.

CMOS components have been miniaturized for more than three decades to continuously improve chips performances at lower energy consumption and cost. Transistors characteristic dimensions have reached a few tens of nm and can no longer be downscaled easily. Alternative materials and technologies are therefore required to keep on increasing computing and data transfer capabilities. The move to non-planar architectures such as FinFETs has been a successful example of disruptive change in the manufacturing of logic devices.1–2 In addition to benefits regarding electrostatic control of carriers in the channel, it has been a turning point for taking advantage of the vertical dimension. Tall fins with high aspect ratio are now considered to maximize drive currents and Surrounded-Gate Transistors (SGT) or Gate-All-Around (GAA) devices are being investigated as an ultimate extension of FinFETs.3 From the materials side, complementary to Si, SiGe and Ge are evaluated as high mobility channel materials4–7 and Source/Drain (S/D) stressor layers are employed to enhance channel mobility and reduce S/D contact resistance.5,6–10 Working with these geometries and materials sets different requirements for the epitaxial growth steps in device fabrication. Accurate controls over dimensions and thermal budgets are of prime importance to avoid variability and reliability issues. It is for instance imperative to avoid the relaxation and reflow of strained channels, significant materials intermixing and uncontrolled dopants diffusion. The situation becomes even more challenging when considering 3D-stacked devices or chips as thermal budget constraints can cumulate when front-end-of-line transistors and metal interconnects are already present. In this paper, we will review our efforts toward a reduction in thermal budget during epitaxial growth processes necessary for the integration of high mobility group-IV materials in advanced technologies. Our activities cover epi processes from channel formation and passivation to source/drain applications for different kinds of devices.

Electrolysis for Channel and Source/Drain Materials

All the epitaxially grown layers discussed in this work were grown either in an ASM Epsilon 3200 single wafer reactor or in an ASM Intrepid Reduced-Pressure Chemical Vapor Deposition (RP-CVD) production cluster. The cluster includes two epi reactors and an integrated pre-epi clean module (Previum). The Previum module enables the low temperature removal of a thin oxide layer present on wafers starting surface, which is mandatory for most of low thermal budget epi processes. The epi reactors are equipped with conventional and high order Si and Ge precursors for lower temperature processes.5 The choice of precursors will be discussed in the relevant sections of the paper. P and n-type dopants are provided to the growth chemistry through the use of diborane (B2H6), arsine (AsH3) and phosphine (PH3). Finally, for Selective Epitaxial Growth (SEG), we use HCl and Cl2, Cl2 being the preferred option for low temperature processes.11

Tall Si0.7Ge0.3 fins with high aspect ratio for higher drive currents.—Reducing the width of the fins prior to wrapping them with the gate stack enhances the electrostatic control of carriers via gate bias. However, decreasing their active area obviously limits the maximum achievable drive current. This is the motivation for preparing tall SiGe fins with large height/width (h/w) ratios. Etching dense and tall fins is challenging as they might wiggle and collapse,12 which in turn sets limits for the aspect ratio and the critical dimension between fins (pitch, p). For Si1–x,Ge x fins grown on Si(001) or Si1–y,Gey(001) Strain-Relaxed Buffers (SRB), Si1–x,Ge x relaxation should be avoided to keep defectivity under control and preserve the longitudinal strain along the channel.13 In reference 13, the authors have studied the relaxation behavior of 20 nm wide and 30 nm high Ge fins patterned from Ge blanket layers grown on a Si12,Ge8 SRB. The pitch (distance between two fins) was 45 nm. Here, we extended the study to taller Si0.7Ge0.3 fins patterned on Si and tried to determine the maximum fin height usable without risking longitudinal strain relaxation.

Relaxation behaviors of blanket Si0.7Ge0.3.—Figure 1 summarizes a relaxation study performed on Si0.7Ge0.3 layers grown on Si(001). In order to identify the highest Si0.7Ge0.3 fin height enabling the formation of strained channels, the degree of strain relaxation of different blanket epi layers grown at 600°C with Dichlorosilane (DCS) and GeH4 in the Epsilon reactor (conditions providing a SiGe growth rate equal to 4.5 nm/min) was evaluated. Results generated by fitting X-Ray Diffraction (XRD) Reciprocal Space Maps (RSM), are summarized on the graph displayed in Figure 1a. Blanket Si0.7Ge0.3 with a thickness up to at least 150 nm can be grown in a metastable strained state on Si(001). However, when applying the thermal budgets required for the processing of state-of-the-art FinFET to the blanket materials (STI densification and activation spike anneals), all the probed layers (50 nm thick or more) start relaxing by the formation of misfit dislocations. However, the situation might be different for fin patterned wafers as the thermal steps are typically applied after fin patterning during which elastic relaxation is expected to occur.13 We have also

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Figure 1. (a) Degree of strain relaxation extracted from XRD-RSM acquired in the vicinity of the asymmetric (224) Bragg reflection on as-grown and annealed Si$_{0.7}$Ge$_{0.3}$ layers of different thicknesses grown on Si(001) at wafers center. Error bars correspond to a relaxation of $\pm 5\%$. The post epi anneals were done in 300 mm production furnaces with the following conditions. Long anneals were performed at 700°C for 30 min in N$_2$ ambient. The temperature ramp rate was 10°C/min. “Spike” anneals were executed in He and took advantage of a different technology. The reactor was kept at the target temperature of 1000°C prior to loading the wafer in the close vicinity of the reactor walls, from which it is separated by a very thin layer of gas (here He), allowing for a very efficient and extremely fast energy transfer. (b) XRD-RSM acquired in the direction parallel to the 20 nm wide fins around the (113) Si Bragg reflection, at different steps in a 50 nm Si$_{0.7}$Ge$_{0.3}$ fin fabrication process, at the center of the wafer. (c), (d) 2D plots of scattered light intensity (haze maps) originating from the surface of two 200 nm thick Si$_{0.7}$Ge$_{0.3}$ layers grown on Si and corresponding thickness profiles extracted from 6-points HR-XRD radius scans, with a $-8^\circ$C relative edge temperature offsets applied in the case of (d).

observed that peculiar relaxation mechanisms occur at wafers edges. In the case of Si$_{0.7}$Ge$_{0.3}$ grown on 300 mm Si(001) wafers, more than 200 nm thick SiGe layers could be grown relaxation-free at the center of the wafer. However, relaxation was systematically initiated at wafers edges. SP3 haze maps acquired on two 200 nm thick Si$_{0.7}$Ge$_{0.3}$ layers grown on Si and corresponding thickness profiles extracted by HR-XRD are shown in Figure 1c and Figure 1d. Details about the haze measurement technique can be found in Ref. 14. Light areas, mostly observed on outer rings at wafers periphery, correlate with regions where high haze signals were recorded. These regions match with areas layers an onset of SiGe relaxation was confirmed with XRD-RSM (not shown here). The only difference between the two presented wafers is that a $-8^\circ$C relative edge temperature offset (colder edge during epi) has been applied when processing the wafer shown in Figure 1d. As expected, the thickness profile was varied from edge-thick to center-thick. Correspondingly, the importance of the high haze area decreased, i.e. a lower fraction of the wafer surface was covered by partly relaxed SiGe. In the case of Figure 1d, relaxation at wafer edge cannot be attributed to an increase in SiGe thickness toward the edge. However, it shows that relaxation can to some extent be delayed by decreasing the thermal budget applied to wafer edges, indicating that great care should be devoted to the control of epi layers structural properties in the vicinity of wafers edges in order to avoid variability in devices properties across the wafers.

Strain in 50 nm Si$_{0.7}$Ge$_{0.3}$ fins.—Considering the preliminary results from blanket studies, we have worked on the fabrication of 50 nm high Si$_{0.7}$Ge$_{0.3}$ fins and confirmed that they could remain longitudinally strained after fin etch. Figure 1b shows a summary of the evolution of strain in the direction parallel to the Si$_{0.7}$Ge$_{0.3}$ fins during processing. The 50 nm as-grown blanket Si$_{0.7}$Ge$_{0.3}$ layer is fully biaxially strained with respect to the underlying substrate. Indeed, the Si and
SiGe diffraction spots are vertically aligned at $H = 1$, demonstrating that the SiGe epilayer has the same in-plane lattice parameter as the underlying substrate. After fin etch, Shallow Trench Isolation (STI) filling between fins and fins reveal (STI recess), the SiGe spot is found close to its initial position, indicating that most of the initial 1.10% compressive strain is preserved. An accurate fitting and analysis of the XRD-RSM data shown in Figure 1b allows to extract a compressive longitudinal strain of 1.03% after fin reveal. The reported values are in good agreement with the ~1.13% compressive strain expected for Si$_{0.7}$Ge$_{0.3}$ grown on Si.\(^2\) Note that no high thermal budget has been applied between these two steps. As a conclusion, thick SiGe epilayers needed for the fabrication of tall fins should be grown with a controlled and limited thermal budget to ensure the formation of metastable strained layers and avoid relaxation during epi. After fin etch, free sidewalls allow for some elastic deformation\(^1\) which helps avoid plastic relaxation, making 50 nm Si$_{0.7}$Ge$_{0.3}$ a viable option for device processing.

**SiGe/Si or SiGe/Ge multi-stacks for GAA preparation.**—In the GAA geometry, horizontally-stacked Si, SiGe or Ge nanowire or nanosheet channels are formed by selective etching of sacrificial SiGe layers, epitaxially grown in SiGe/Si, Si$_{1-x}$Ge$_x$/Si$_{1-y}$Ge$_y$ ($x > y$) or SiGe/Ge multi-stacks, respectively. For Si- and SiGe-channel GAA devices, strained multi-layers can be grown with conventional precursors (SiH$_4$ or DCS in combination with GeH$_4$) at conventional temperatures of 600–700°C.\(^6\) The obtained compositional gradients are sufficiently steep to allow efficient wire release by selective SiGe or Si removal.\(^4\),\(^7\),\(^1\)\(^5\) As already shown in Ref. 16, the use of SiGe/Si multi layers enables the growth of metastable stacks with larger equivalent SiGe critical thicknesses compared to blanket SiGe. In this work, we observe that SiGe/Si multi-stacks, generate lower wafer bow and warp than their single-layer counterparts, confirming improved mechanical stability (Figure 2). This allows to maintain a very low surface roughness ($< 1$ nm RMS, not shown here). With this approach, multi-stacks can be grown without relaxation, allowing the fabrication of GAA devices including up to 7 stacked nanowires or more.\(^1\)\(^7\) However, one should take into account difficulties for patterning dense SiGe/Si fins with high h/w ratios and for uniformly releasing the different channels. Indeed, adding Si spacers increases the required patterned fin height (doubled if $t_{SiGe} = t_{Si}$) for a given SiGe active section, thereby strongly complexifying fin patterning steps with additional risks for damages to materials and pattern collapse.\(^1\)\(^2\) In other words, fins with very high h/w ratios are required to compete with equivalent single-layer fins. In the case of Ge GAA, the epitaxial growth of Ge-rich SiGe/Ge on SiGe Strain Relaxed Buffers (SRB) is more challenging.\(^6\) Extremely low process temperatures ($< 400°C$) are required to avoid strain relaxation. These layers necessitate the use of higher order precursors (Si$_2$H$_6$ and Ge$_2$H$_6$), since conventional precursors become ineffective.\(^6\)

![Figure 2](145.94.116.75). (a) Schematic cross-section of the SiGe/Si multi-stacks used for Si GAA devices and cross-section SEM of a stack including 15 [10 nm Si$_{0.7}$Ge$_{0.3}$/10 nm Si] periods. (b) Measured wafer bow and warp as a function of SiGe nominal thickness (e.g. 50 nm Si$_{0.7}$Ge$_{0.3}$ corresponds to a multi-stack with 5 [10 nm Si$_{0.7}$Ge$_{0.3}$/10 nm Si] periods). (c) Degree of strain relaxation extracted from XRD-RSM acquired around the (113) Bragg reflection for Si$_{0.7}$Ge$_{0.3}$ layers as a function of Si$_{0.7}$Ge$_{0.3}$ nominal thicknesses. Error bars correspond to a degree of relaxation of $\pm 5\%$. Downloaded on 2019-10-08 to IP 145.94.116.75 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).
Si passivation for Ge-rich channels.—The epitaxial growth of ultra-thin Si layers on (strained) Ge fins or nanowires has been thoroughly discussed in Ref. 18. In this work, SiH₂ and Si₅H₁₀ were used as Si precursors to enable the epitaxy of very thin Si films to passivate Ge channels at temperatures as low as 330°C. It was found that the strain due to the lattice mismatch between the Si passivation layer and the Ge fin is the driving force for unwanted Ge surface reflow during Si deposition. The reflow is strongly affected by H-passivation during Si-capping and can be avoided by carefully selecting process conditions and keeping the epi thermal budget as low as possible.

Low temperature epitaxy of p-type S/D materials for SiGe and Ge fin FETs and GAA.—The downscaling of transistors systematically leads to a reduction in the S/D contact area. As a result, the contact resistance becomes a key contributor to device parasitics⁶,⁹,¹⁰ and device performance might be limited by the metal-semiconductor contact. For this reason, minimizing the contact resistivity at metal-S/D level is mandatory. Contact resistivity values of ≤ 1 × 10⁻⁹ Ω·cm² are typically considered as targets for advanced technology nodes. To meet this objective, the right materials, matching interfaces from band structure perspective, should be grown selectively in S/D areas with thermal budgets compatible with existing devices. Required active doping levels are usually extremely high (> 1 × 10¹⁹ cm⁻³) and far above the dopants solubility limits. This motivates the use of far-from-thermodynamic-equilibrium processes. In addition, S/D epi materials are often used as channel stressors to boost carrier mobility. The later aspect must also be taken into account when defining S/D for a given technology. In the next section we focus on p-type S/D. For reference, results on the SEG of highly-doped Si:P have been presented in Ref. 9.

Low temperature SiGe epitaxy and etch.—Decreasing epi or etch temperature typically results in a decrease in growth or etching rate, respectively, until the processes become ineffective (no growth, no etch). Conventional epi precursors typically provide decent growth rates of a few nm/min down to temperatures of ~ 500°C (SiH₄) and ~ 350°C (GeH₄).⁶ From the etch side, HCl can be used down to ~400°C for the etch of pure Ge but to etch Si or SiGe, the process temperature needs to be strongly increased, up to ~ 600°C, as soon as the Si content exceeds 50%.²¹ Higher order silanes and germanes enable important reductions in SiGe growth temperatures.⁶ In addition, Cl₂ allows dramatic reductions of the vapor etching temperature, e.g. down to ~ 350°C for Siₓ₅Ge₀₇.¹¹ We considered different combinations of precursors and etchants as described in the following paragraphs.

p-type SiGe.—Highly B-doped Siₓ₅Ge₀₇ (with 40% ≤ x ≤ 70%) materials are often regarded as the best option for the epitaxy of S/D for pMOS Si devices.²²–²⁵ In addition to acting as a natural stressor for Si channels, an additional benefit of using SiGe as S/D material is the capability to selectively deposit layers with very high active B concentrations (~ 1 × 10²¹ cm⁻³), using conventional precursors at temperatures of 500°C or higher, as illustrated in Figure 3a. The situation differs for so-called high-mobility channel devices, where the Si channel is replaced by compressively strained Ge in case of pMOS. There, SiGe S/D layers do not apply the right stress and, for pure Ge (or SiGe with >70% Ge), the low B solubility makes it extremely challenging to reach a high active doping concentration. Moreover, for Ge pMOS and 3D stacking of Si, SiGe or Ge based devices, the epi thermal budget should be reduced. For these reasons, alternative process conditions are being explored. We consider the use of disilane (Si₂H₆) and digermane (Ge₂H₆) for the epitaxy of highly-doped SiGe at reduced temperatures (< 450°C). Initial results obtained from Si₀₅Ge₀₇:B epi layers grown at 400°C have yielded an active B concentration of 5 × 10²⁰ cm⁻³, which still needs to be increased in order to compete with conventional processes. In addition, these low temperature processes have the drawback of being non-selective, resulting in the unwanted deposition of amorphous or polycrystalline SiGe on STI-oxide and nitride spacers. This makes it mandatory to work with cyclic schemes including low temperature growth and selective etching of amorphous/polycrystalline SiGe versus crystalline SiGe using Cl₂. Figure 3b displays top-view SEM images acquired on (80 × 80 μm²) measurement pads and 100 nm Si fin test structures surrounded by STI, after the cyclic deposition-etch of Si₀₅Ge₀₇:B at 400°C. Different deposition time/etch time ratios were used. We observed that selective depositions could be achieved for deposition/etch time ratios lower than 5. For reference, a deposition/etch time ratio of 5 provided a net growth rate of ~ 1.4 nm per cycle on wafers used for the 3D sequential stacking of planar devices. Obviously, the growth and etch rates per cycle depend on the considered mask (percentage of area covered by silicon oxide and nitride) and device geometry, so these timings are to be adjusted for every application. More optimizations are obviously needed to develop processes fully selective toward nitride spacers used for advanced devices and to further increase active doping. Nevertheless, low temperature SiGe doped processes provide new options for the epitaxy of advanced S/D.

![Figure 3](image-url)

Figure 3. (a) Highest active B concentrations obtained in Si, SiGe and Ge SEG S/D epi layers grown with conventional precursors (DCS, SiH₄, GeH₄, HCl) as measured by Micro Hall Effect measurements (MHE). To extract active doping values, a Hall Scattering Factor of 1 is assumed. (b) Top-view SEM images acquired on test structures after the cyclic deposition-etch of Si₀₅Ge₀₇:B using Si₂H₆, Ge₂H₆ and Cl₂ at 400°C with different dep/etch ratios between 10 and 2.
Ga as an alternative p-type dopant for SiGe S/D.—The solubility of boron in Ge is more than a factor 10 lower than that of boron in Si, as listed in Table I. As a result, achieving high B-doping in Ge-rich SiGe is a challenge. For this reason, Ga is considered as a promising alternative dopant, due to the higher solubility of Ga in Ge. Ga can also be used for SiGe, eventually as a co-dopant in addition to B. Experimental evidences of contact resistivity improvements using Ga have already been provided in Ref. 27, where record-breaking low contact resistivity values below $10^{-4}$ Ω·cm² have been demonstrated with Ga-implanted SiGe layers. However, the reported processing scheme requires an unwanted high thermal budget (laser anneal) for dopants activation and does not allow conformal doping profiles on patterned structures. Therefore, the selective epitaxial growth of in-situ doped Ge:Ga and SiGe:Ga or SiGe:B:Ga is highly desired to ensure a full compatibility with advanced FinFET and Gate-All-Around devices, both in terms of selectivity, conformality, process complexity and thermal budget. Achieving high p-type doping of SiGe with Ga has some challenges. Indeed, the low Ga solubility in Si leads to a severe risk for Ga precipitation and agglomeration. Moreover, unwanted carbon incorporation can be an issue, as all commercially available Ga process gases contain alkyl groups (CH₃, etc.). We have explored the R-P-CVD of Ga-doped SiGe and [B + Ga] co-doped SiGe/Ge layers. Dopants incorporation and distribution in the semiconductor matrix were investigated and correlated with the electrical properties of the layers.

**Table I. Atomic radius and maximum solubilities of several dopants in Si and Ge.**

<table>
<thead>
<tr>
<th>Specie</th>
<th>Atomic radius (pm)</th>
<th>Max. solub. in Si (cm⁻³)</th>
<th>Max. solub. in Ge (cm⁻³)</th>
</tr>
</thead>
<tbody>
<tr>
<td>B</td>
<td>87</td>
<td>$8 \times 10^{20}$</td>
<td>$2 \times 10^{18}$</td>
</tr>
<tr>
<td>Si</td>
<td>111</td>
<td>Atomic density: $5.0 \times 10^{22}$</td>
<td></td>
</tr>
<tr>
<td>Al</td>
<td>118</td>
<td>$2 \times 10^{19} \sim 8 \times 10^{20}$</td>
<td>$4 \times 10^{20}$</td>
</tr>
<tr>
<td>Ge</td>
<td>125</td>
<td>Atomic density: $4.4 \times 10^{22}$</td>
<td></td>
</tr>
<tr>
<td>Ga</td>
<td>136</td>
<td>$4 \times 10^{19} \sim 1 \times 10^{20}$</td>
<td>$5 \times 10^{20}$</td>
</tr>
<tr>
<td>Sn</td>
<td>145</td>
<td>$7 \times 10^{19}$</td>
<td>$4 \times 10^{20}$</td>
</tr>
</tbody>
</table>

Highly-doped Ge:B grown at low growth temperature using Ge₂H₆.—Growing Ge:B with B₂H₆ and Ge₂H₆ instead of Ge₂H₄ allows maintaining decent growth rates of a few nm/min at reduced temperatures ($<350°C$). At low growth temperatures, dopants adsorbed on the growing surfaces see their diffusion length and desorption rate reduced. As a consequence, dopants incorporation and activation are enhanced, as previously reported for Ge:P. In order to assess the electrical properties of our Ge:B epi layers, we have combined SIMS, micro 4-points probe (m4pp) and Micro Hall Effect (MHE) measurements. Figure 5a summarizes these results on a 300 mm Si wafer. We could demonstrate contact resistivities as low as $2.9 \times 10^{-3}$ Ω·cm². This value should be compared with the contact resistivity of $6.1 \times 10^{-3}$ Ω·cm² obtained with a similar layer grown without Ga. This is a clear demonstration that Ga-doping helps in reaching contact resistivity targets for future technology nodes, although the limits of the evaluated approaches are not yet known.
data do not show any saturation and an active doping concentration as high as $3 \times 10^{20}$ cm$^{-3}$ could be obtained. However, mobility values keep on reducing with increasing B content. On the other hand, m4pp data shows an apparent saturation in active doping concentration, which implies that assumed mobility values (available in literature for $[B]_{\text{active}}$ up to $\sim 1 \times 10^{20}$ cm$^{-3}$) are not correct (overestimated) for these highly-doped layers. Finally, by using a Ge:B process providing an active B concentration of $2.2 \times 10^{20}$ cm$^{-3}$, a low Ti/p+Ge contact resistivity of $5.5 \times 10^{-9}$ $\Omega$.cm$^2$ has been obtained without any post-epi treatment. Due to the non-selective nature of the process, we expect similar properties on patterned structures as loading effects should be absent or very weak.

As Ge:B growth with Ge$_2$H$_6$ is not selective, a cyclic deposition-etch routine needs to be used for selective S/D deposition schemes. Because of the low processing temperature, Cl$_2$ is suggested as etchant. The desired epi layer thickness and process selectivity were tuned by optimizing individual steps and the number of deposition/etch cycles. Although tuning the uniformity of both epitaxy and etch steps was not a straightforward task, very decent thickness and resistivity profiles have been achieved with a 1-standard-deviation uniformity of 0.9% for a $\sim 105$ nm thick Ge:B layer grown on blanket Ge/Si (Figure 5b). These optimized conditions resulted in an average layer resistivity of $\rho_{\text{Ge:B}} = 0.43$ $\Omega$.cm. The impact of B-doping on layers’ structural properties was evaluated with Triple-Axis XRD (TA-XRD) measurements for Ge:B layers grown on undoped Ge VS (Figure 5c). The peak located at $\sim 5450$ arcsec is assigned to the slightly tensile strained Ge VS and the peak at higher angles is assigned to Ge:B. The position of the Ge:B peak shifts toward higher angles with increasing B contents, due to an increase in tensile strain in the layer. Finally, Ge:B processes were applied to fin device structures. An example SEM image is provided in Figure 5d, where the full selectivity of the process versus STI-oxide and nitride spacers is confirmed. It also indicates that the S/D material quality obtained on 20 nm fins is sufficiently high as the selective etching does not result in any observable etch pits nor roughness.

**GeSn:B selective epitaxial growth for S/D.**—Adding SnCl$_4$ to the GeH$_4$+B$_2$H$_6$ growth chemistry allows the selective epitaxial growth (without the need for cyclic selective etching) of GeSn:B with active B concentrations up to $3.2 \times 10^{20}$ cm$^{-3}$. The active doping can be further increased up to $5 \times 10^{20}$ cm$^{-3}$ for $\delta$-doped GeSn. Due to the presence of Sn, one can expect the achievement of low contact resistivities and the transfer of compressive strain to Ge channels (see Table 1). However, due to the low Sn solubility in Ge, there is a risk for Sn precipitation and clustering, similar to what was observed for Ga-doping. This is especially important for the epitaxy of GeSn on patterned wafers where loading effects can enhance this risk. After an optimization of growth conditions $r_{\text{c}}$ values as low as $3.6 \times 10^{-9}$ $\Omega$.cm$^2$ were extracted from MR-CTLM measurements on Ti/Ge$_{0.99}$Sn$_{0.01}$:B stacks. Again, this low $r_{\text{c}}$ value was obtained without post-growth thermal treatments to increase active dopant concentration. We have also worked on the implementation of Ge$_{0.99}$Sn$_{0.01}$:B S/D on advanced Ge GAA devices and could demonstrate very good process conformality and selectivity. More details about these aspects are discussed in Ref. 41.
Figure 5. (a) Summary plot of SIMS, m4pp and MHE data generated from a series of Ge:B layers grown at 320°C with different B2H6 flows. (b) Thickness and resistivity profiles for optimized CDE processes along a wafer diameter, evaluated using step height (using specific test structures) and m4pp measurements. (c) TA-XRD scan acquired on Ge:B layers with B contents varying from $2.8 \times 10^{20}$ to $2.7 \times 10^{21}$ cm$^{-3}$ and grown on a Ge VS. The Ge VS peak is observed at $\sim -5450$ arcsec (0.2% tensile-strained Ge) and Ge:B peaks at higher angles. All peaks are referenced to the Si substrate peak at 0 arcsec. (d) Tilted-view SEM of a Ge:B grown by CDE on relaxed Ge fins with gate patterning.

Conclusions

In this contribution, we have presented some of our latest developments on the low-temperature epitaxial growth of group-IV semiconductors. Working on new devices and chips architectures imply new constraints for the growth processes. Epi thermal budgets should in general be reduced, especially when working with high-mobility channel materials, where relaxation needs to be avoided and strain preserved. We have seen that 50 nm tall strained Si$_{0.7}$Ge$_{0.3}$ fins can be prepared using standards Si and Ge precursors. Blanket Si$_{0.7}$Ge$_{0.3}$ layers are metastable and do not sustain the high thermal budgets required for state-of-the-art fin processing. For this reason, care has to be taken to ensure that fully-strained layers reach fin patterning, after which transverse elastic relaxation helps maintaining longitudinal strain in the fins. Si$_{0.7}$Ge$_{0.3}$/Si multi-stacks, as used for GAA, improve fins mechanical stability but complicate subsequent fin etch steps. Therefore, compromises are to be found to fabricate tall and strained SiGe fins devices. Additional challenges arise when considering source/drain processes. The low temperature deposition processes should remain selective and provide very high doping levels. We consider different approaches to meet these objectives. Higher order precursors are used for the growth of Ge and SiGe materials at very reduced temperatures of $\leq 400^\circ$C. If interesting electrical properties can be obtained, these processes are typically non-selective, which makes their implementation in devices difficult. B-doped GeSn alloys are an interesting alternative to Ge source/drain, as the deposition is intrinsically selective and high growth rates are obtained at low temperature with conventional GeH$_4$. Finally, we also consider alternative dopants such as Ga to circumvent limitations due to the low solubility of B in Ge.

We demonstrate that adding Ga dopants in source/drain layers enables a reduction in contact resistivities. Results obtained with Ti/p+ Ge$_{0.99}$Sn$_{0.01}$:B and Si$_{0.5}$Ge$_{0.5}$:B:Ga materials yielded $\rho_c$ values as low as $3.6 \times 10^{-9}$ $\Omega$.cm$^2$ and $2.9 \times 10^{-9}$ $\Omega$.cm$^2$, respectively, for layers grown conformally and without post-growth thermal treatments.

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