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Zero Sequence Currents Externally Circulating between the Back to Back Modular Multilevel Converters in Parallel AC-DC Distribution Links

Aditya Shekhar, Thiago Batista Soeiro, Laura Ramírez-Elizondo and Pavol Bauer

***Abstract*—During the operation of a three line ac link in parallel with a ac-dc-ac link system that employs Back-to-Back (B2B) Medium Voltage Modular Multilevel Converters (MMC), a path for the low frequency zero sequence currents is shown to exist. Apart from causing additional losses, these currents can result in limitations on power capacity. A detailed analysis on the influence of cell capacitance, arm inductance and link conductor length on the circulating zero sequence currents and the means to mitigate them through a simulated control strategy is investigated. The simulations show that the dc link employing B2B-MMC can successfully operate in parallel with ac link without transformer isolation by controlling the zero sequence currents.**

***Index Terms*—AC/DC converter, circulating current control, common dc and ac buses, common mode current, parallel connected, zero-sequence circulating current.**

I. Introduction

There is an increasing application of flexible dc links for restructuring medium voltage distribution grids [1], [2]. Due to this interest in using dc distribution for existing ac grid reinforcement and power capacity enhancement, parallel ac-dc link architecture as illustrated in Fig. 1 is becoming common [3]–[10].

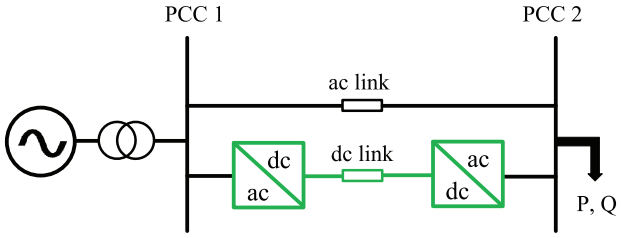

Fig. 1: Illustration of parallel ac-dc link in a distribution network.

As the role of dc in distribution grids widens, the use of Power Electronics for Utility Interface (PEUI) will also increase. For example, the ac/dc converters need to steer active power between the ac and dc links and support the reactive power demands for the grid at each side. To do this efficiently modular multilevel converters (MMC) can be an interesting possibility [11]–[16]. Moreover, an isolating transformer may not be employed at the Point of Common Coupling (PCC) of the parallel ac-dc path [17]–[19]. At medium voltage level, such as at 10 kV, the parallel ac-dc link length between two voltage buses can be short, in the range of about 20 km. As a consequence of these requirements, challenges that arise during operation of the PEUI are highlighted in this study.

Specifically, this paper focuses on the problem on Zero Sequence Currents (ZSC) that externally circulate between the B2B MMCs and the ac link via the path provided by the dc link conductors. Although the system architecture constitutes of three wires in the ac link side, the dc-link creates a path for the zero sequence. Due to short link length, the inductance separating these MMCs is relatively small and consequently, the system is similar to parallel connected ac/dc converters sharing a common ac and dc side. The problem of ZSC in such systems with Voltage-Sourced-Converters (VSC) sharing a common ac and dc side is explored in [20]–[23]. This can lead to additional conduction losses, impact the operational range and in worse cases, cause failure in system components [24]. The cell voltage control can have influence on the ZSC. The main contributions of this paper are as follows:

- Describe the problem of ZSC externally circulating between B2B MMCs in parallel ac and dc links (Section II).
- Mitigate the ZSC using the zero sequence current controller at one side of the ac-dc link system (Section III).
- Analyze the sensitivity of these ZSC with different link lengths and submodule capacitance (Section IV-A).
- Quantify the harmonic component in various system parameters to determine the effectiveness of the developed control strategy (Section IV-B).

The importance of this study is mainly to caution that ZSC may exist even in B2B converter power routing systems. This possibility should not be overlooked even when the PCC1 and PCC2 are located at buses that are a few kilometers apart.

II. Existence of Zero Sequence Current Path between Parallel AC-DC Links

The equivalent circuit of a dc link with B2B MMCs in parallel with an ac link is shown in Fig. 2.

The MMCs are connected to the PCC1 and PCC2 via inductance L_{f}. Each arm of the MMC is abstracted as a inductance L_{arm} in series with a variable voltage source consisting of N

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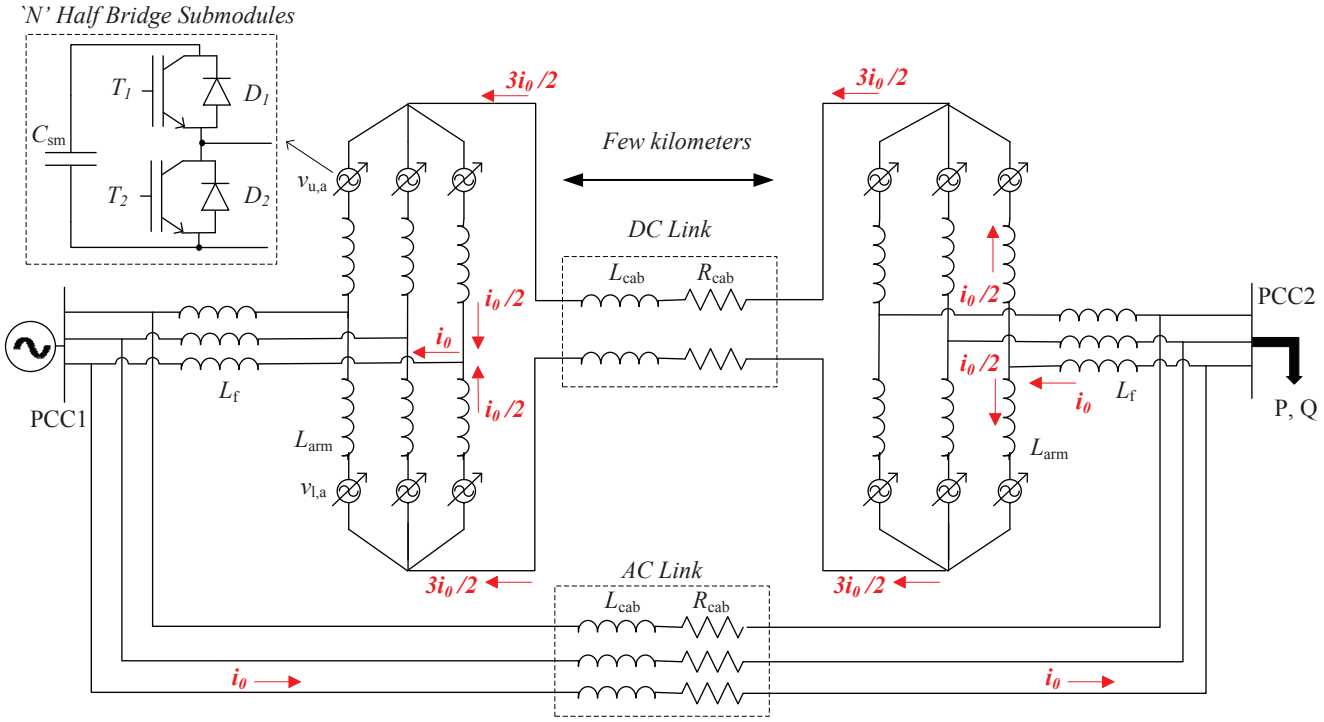


Fig. 2: Path of zero sequence current flow in modular multilevel converter based parallel AC-DC distribution links.

number of half bridge submodules. The submodule can either insert or bypass a capacitance C_{sm} using two IGBT switches T_1 and T_2 with antiparallel diodes D_1 and D_2 respectively. The conductors of both ac and dc links can be modelled as having a resistance R_{cab} and inductance L_{cab} that vary with the link length. For ac link phase current i_a, i_b and i_c, the zero sequence current component i_0 is given by (1).

$$i_0 = \frac{i_a + i_b + i_c}{3} \tag{1}$$

The path of i_0 through the parallel ac-dc link system is shown in Fig. 2. For each phase of the ac link, i_0 splits into half for each arm of the MMC phase leg and returns via the dc link. The equivalent circuit for the zero sequence currents externally circulating between the dc link of the B2B MMC and the parallel ac link is shown in Fig. 3.

The various system parameters used in this work are presented in Table I. The ac and dc link each deliver 50 % power demand at PCC2. In order to simplify the interpretation of results, it is assumed that L_{arm} is designed such that the filter inductance L_f is zero.

The third harmonic current equal to $\frac{3i_0}{2}$ flows through each dc link conductor as shown in Fig. 4a. The ZSC of the ac link given by (1) is depicted in the secondary y-axis of Fig. 4a. The direction and magnitude of these ac and dc link ZSC are consistent with equivalent circuit depicted in Fig 3. The ZSC of MMC ac output currents at PCC1 and PCC2 are denoted by $i_{0,PCC1}$ and $i_{0,PCC2}$ shown in Fig. 4b.

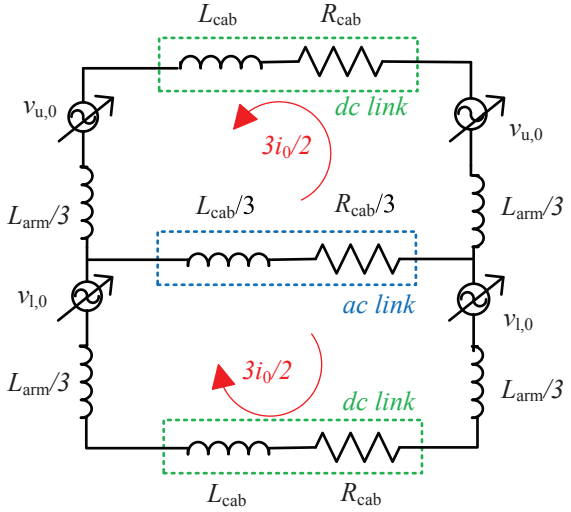


Fig. 3: Equivalent circuit for the ZSC externally circulating between the dc link of the B2B MMC and parallel ac link.

III. Zero Sequence Current Controller (ZSCC)

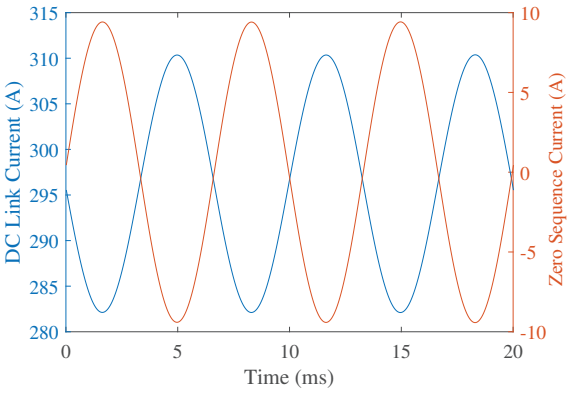
A. RSS-Side MMC Control Schematic

The controller schematic of RSS-side MMC is shown in Fig. 5. The control structure of Output Current Controller (OCC), Circulating Current Controller (CCC) and Direct Voltage Control (DVC) is developed based on the theory presented in [25].

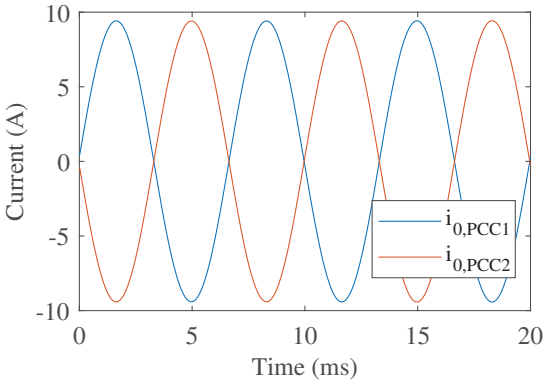
The OCC generates the reference output voltage $v^*_{s,\alpha\beta}$ based on the error between the actual output ac current ($i_{s,\alpha\beta}$) and the

TABLE I: System parameters used for the simulation results.

Converter Capacity	10 MVA, pf=0.9
AC Grid Voltage (Line to line, rms)	10 kV
Submodule Capacitance C_{sm}	3.3-10 mF
Arm Inductance L_{arm}	2-5 mH
Total Power Demand at PCC2	10 MVA, pf=0.9
Number of Submodules (N)	9
DC Link Voltage	17 kV
Link Conductor Resistance	65 mΩ/km
Link Conductor Inductance	0.554 mH/km



(a)



(b)

Fig. 4: Waveform for zero sequence circulating currents in the (a) dc and ac link (b) SSS and RSS side converters with link length of 5 km for C_{sm}=3.3 mH and L_{arm}=3 mH.

reference current ($i^*_{\text{s},\alpha\beta}$) corresponding to the required active and reactive power set-points. The bandwidth (BW) of the Proportional-Resonant (PR) OCC is $\alpha_{\text{P,occ}} = 2000$ rad/s so that the proportional gain $k_{\text{p,occ}} = \alpha_{\text{P,occ}} * L_{\text{arm}}/2$. The BW of the resonant integrator $\alpha_{\text{R,occ}} = 50$ rad/s so that the integral gain is given by $k_{\text{i,occ}} = 2\alpha_{\text{R,occ}} k_{\text{p,occ}}$. The BW of the voltage feed-forward $\alpha_{\text{vff}} = 1000$ rad/s.

The internally circulating arm current i_{c} (this current is different from the externally circulating ZSC in B2B MMC with shared ac and dc link) is controlled using CCC to the dc component corresponding to one-third of the dc link current (i_{d}) delivering the required active power share. The P-gain $k_{\text{p,ccc}} = 10$ with resonator gains $k_{\text{i,ccc}}$ corresponding to

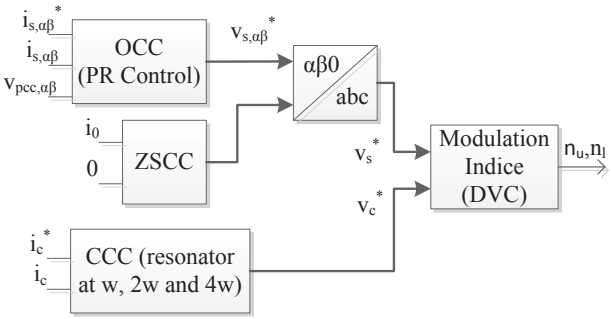


Fig. 5: Controller block diagram for the RSS-side MMC with ZSCC.

$\alpha_{\text{i,ccc}} = 200$ rad/s for frequencies w, $2w$ and $4w$, where w is the fundamental grid frequency in rad/s.

Based on the generated reference voltages, the insertion indices for the upper and lower arms (n_{u} and n_{l} respectively) are calculated using Direct Voltage Control (DVC). The SSS-side MMC has identical bandwidths for OCC, CCC and DVC and is used to voltage control of the dc link. In this paper, the RSS-side MMC control structure is modified by adding a ZSCC in the OCC and a 4^{th}-harmonic resonator in the CCC (i.e. at 4w) as shown in Fig. 5. The simulated response of the system with and without these adaptations is discussed in subsequent sections.

B. Output Current ZSCC

Fig. 6 shows the control structure based on the theory in [24] for the ZSC suppression.

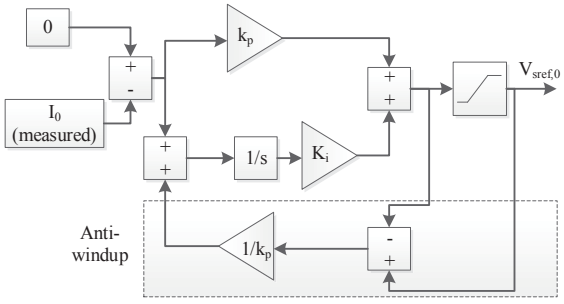


Fig. 6: ZSCC PI-Control Structure with anti-windup.

The proportional-integral (PI) controller gains k_{p} and k_{i} are tuned based on the link length dependent inductance. The anti-windup loop is added to avoid high currents drawn by the converters due to the non-linearity introduced by the saturation block. The waveform for the dc link current and the zero sequence current in the ac link is shown in Fig. 7, with ZSCC enabled at $t_0 = 0$.

It can be observed that i_0 nearly reduces to zero and the dc link current settles to nearly a constant value corresponding to the active power demand from the converter.

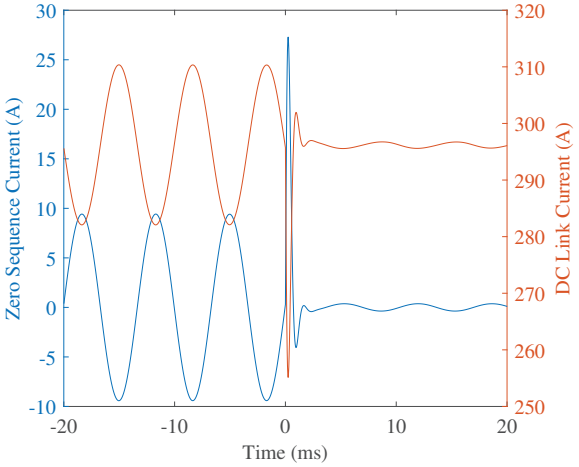


Fig. 7: Zero Sequence and dc link current waveforms with ZSCC triggered at $t_0 = 0$.

C. Circulating Current Control with ZSCC

The internal circulating current of a given phase ($i_{c,a}$) is defined based on the upper ($i_{u,a}$) and lower ($i_{l,a}$) phase arm of the MMC as (2).

$$i_{c,a} = \frac{i_{u,a} + i_{l,a}}{2} \tag{2}$$

It is discussed in [25] that the dc component of $i_{c,a}$ is one third the dc link current during steady state. The parasitic component in sum-capacitor voltages translate to a 2nd harmonic ripple in the internally circulating current, which is removed using a Proportional-Resonant (PR) controller sensitive to twice the fundamental frequency.

However, when the output current ZSCC was activated, a fourth harmonic ripple was observed in the $i_{c,a}$ at steady state for $t > t_0$ as shown in Fig. 8. $i_{c,a,4h}$ circulates between the arms of the MMC and does not appear in the output ac current of the dc link current, causing additional conduction losses. Therefore, a resonator tuned for four times the fundamental frequency was added to the internal circulating current control to eliminate $i_{c,a,4h}$, as can be observed in Fig. 8.

IV. Quantification of Zero Sequence Currents

The ZSC result in reduction of system efficiency due to conduction losses in the ac and dc link conductors. A sensitivity analysis of the ZSC problem with various parallel ac-dc system parameters must be performed at the design stage.

A. Sensitivity to System Parameters

The system is simulated for varying link lengths for different submodule capacitance C_{sm} of 3.3 mF, 5 mF and 10 mF. The peak of the zero sequence current ($i_{ac0,peak}$) in the ac link when no ZSCC is employed is depicted in Fig. 9.

It is evident that increasing the C_{sm} can limit the externally circulating ZSC in the parallel ac-dc link, particularly for short link lengths. On the other hand, this can increase the size and cost of the dc link MMCs as discussed in [15].

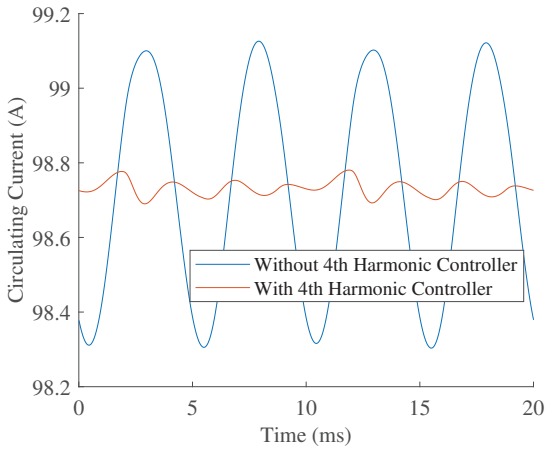


Fig. 8: Effect of ZSCC on the internally ciculating currents in the MMC.

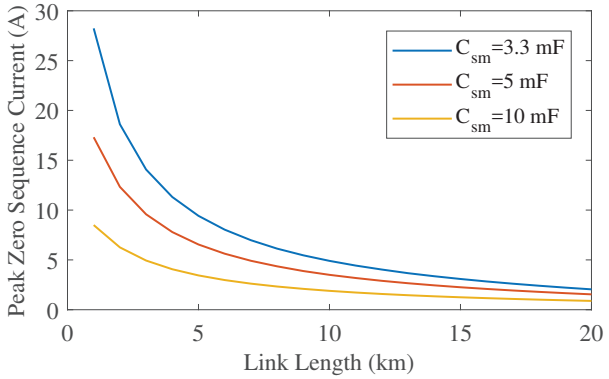


Fig. 9: Peak zero sequence current with respect to link length for different MMC submodule capacitances with L_{arm}=3 mH.

With increasing link length, the ZSC decreases due to a corresponding increase in the link conductor inductance. A similar reduction in ZSC can be expected if arm inductance is increased. However, an increase in L_{arm} would not only increase the cost, size and losses in the MMC, but also reduces the PQ-capability of the converter [26]. Therefore, mitigating the impact of ZSC using control techniques is important and shall be explored in Section III.

B. Harmonic Analysis of System Waveforms

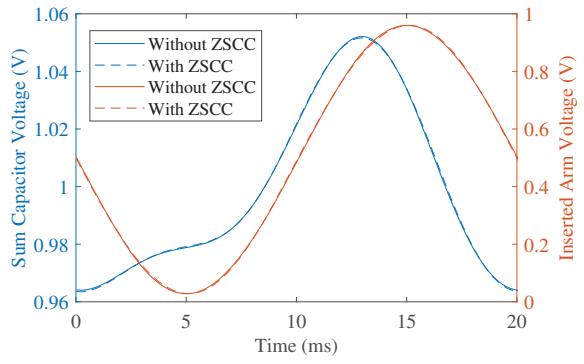
In order to numerically trace the path of ZSC depicted in Fig. 3, the waveforms of arm current (i_u) and inserted arm voltage (v_u) are analysed. The relation between the sum capacitor voltages on an upper phase arm of the MMC ($V^{\Sigma}_{cu,a}$), the insertion indice (n_{ua}), the arm current (i_{ua}) and the inserted arm voltage (v_{ua}) is given by (3) and (4) as described in [25].

$$V^{\Sigma}_{cu,a} = \left(\frac{N}{C_{sm}}\right) \int n_{ua} i_{ua} \tag{3}$$

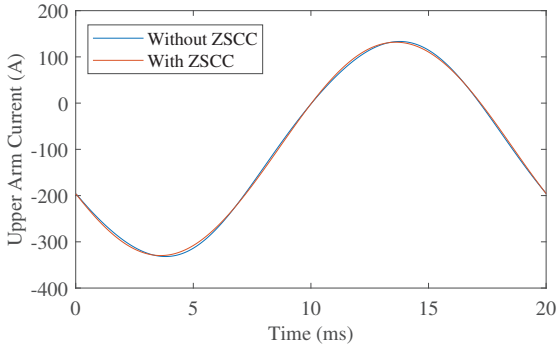
$$v_{ua} = n_{ua} V^{\Sigma}_{cu,a} \tag{4}$$

Fig. 10 shows the MMC arm waveforms with and without ZSCC under full load condition with $N = 9$, $C_{sm} = 3.3$ mF

and $L_{\text{arm}} = 3\,\text{mH}$ for a 5 km link. It can be observed that for these values, the impact of i_0 is not significant, and therefore, the converter losses may not change considerably. On the other hand, the i_0 with a peak of about 10 A will flow through the link conductors, leading to additional conduction losses if left unchecked.



(a)



(b)

Fig. 10: Converter arm parameter wave-forms with and without ZSCC for (a) Sum capacitor voltage and arm voltage (b) Arm Current.

It can Let t_0 represent the time instant at which the zero sequence current controller (described in Section III) is enabled. The Fast Fourier Transform (FFT) is performed on 10 cycles of the waveforms for i_{ua}, $V^{\Sigma}_{\text{cu,a}}$ and n_{ua} at steady-state for $t < t_0$ and $t > t_0$. The third harmonic (3h) component as a percentage of fundamental (50 Hz) for different submodule capacitance and link length is given in Table II.

The variation in $i_{\text{ua,3h}}$ is in accordance to the trend observed in Section IV-A with different l and C_{sm} for $t < t_0$ and significantly reduces, close to 0 due to control action for $t > t_0$. This can be inferred from the consequent change in $n_{\text{ua,3h}}$ from 0 at $t < t_0$ to a higher value at $t > t_0$. The related influence of $i_{\text{ua,3h}}$ and $n_{\text{ua,3h}}$ can be observed in $v^{\Sigma}_{\text{ua,3h}}$. Note that even though $v^{\Sigma}_{\text{ua,3h}}$ varies with both l and C_{sm} for $t < t_0$, the dependence of l is negligible for $t > t_0$, indicating good performance of the control designed.

V. Conclusions

It is shown that externally circulating zero sequence currents exist in parallel ac-dc link systems employing back to back MMCs and argued that particularly for medium voltage distribution links of short distances (up to 20 km), this problem cannot be ignored. The results indicate that these ZSC manifest as third harmonic ripple in the submodule capacitance. Sensitivity analysis is performed for varying link length and submodule capacitance to highlight that there is a trade-off between the installation cost and system losses.

The main contribution of this paper is to show that the problem of ZSC in parallel ac-dc link systems employing back to back MMCs can be mitigated by adding a combination of zero sequence current controller for output ac current and fourth harmonic suppression control of internal circulating currents in the MMC. This strategy can potentially reduce the conduction losses occurring in the ac and dc link conductors as well as the B2B MMC arms. However, the consequence of ZSCC on the operational boundaries of the MMC is important for dc link voltage rating because it conflicts with the requirements for 3$^{\text{rd}}$-harmonic injection technique for PQ-range extension.

TABLE II: Third harmonic components arm current ($i_{\text{ua,3h}}$) and sum capacitor voltage ($v^{\Sigma}_{\text{ua,3h}}$) with varying link length (l) and submodule capacitance (C_{sm}) before and after $t = t_0$.

l	C_{sm}	$i_{\text{ua,3h}}$		$v^{\Sigma}_{\text{ua,3h}}$		$n_{\text{ua,3h}}$	
km	mF	% of fundamental amplitude					
		$t < t_0$	$t > t_0$	$t < t_0$	$t > t_0$	$t < t_0$	$t > t_0$
1	3.3	5.86	0.14	2.16	0.72	0	1.07
	5	3.76	0.13	1.38	0.5	0	0.76
2	3.3	4.1	0.21	1.29	0.68	0	1.07
	5	2.72	0.14	0.86	0.47	0	0.76
5	3.3	2	0.09	0.34	0.7	0	1.07
	5	1.39	0.07	0.25	0.48	0	0.76
10	3.3	0.98	0.04	0.34	0.71	0	1.05
	5	0.71	0.03	0.21	0.48	0	0.76

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