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Due to their very nature, Spin Waves (SWs) created in the same waveguide, but with different frequencies, can coexist while selectively interacting with their own species only. The absence of inter-frequency interferences isolates input data sets encoded in SWs with different frequencies and creates the premises for simultaneous data parallel SW based processing without hardware replication or delay overhead. In this paper we leverage this SW property by introducing a novel computation paradigm, which allows for the parallel processing of n-bit input data vectors on the same basic SW based logic gate. Subsequently, to demonstrate the proposed concept, we present 8-bit parallel 3-input Majority gate implementation and validate it by means of Object Oriented MicroMagnetic Framework (OOMMF) simulations. To evaluate the potential benefit of our proposal we compare the 8-bit data parallel gate with equivalent scalar SW gate based implementation. Our evaluation indicates that 8-bit data 3-input Majority gate implementation requires 4.16x less area than the scalar SW gate based equivalent counterpart while preserving the same delay and energy consumption figures.

I. INTRODUCTION

The information technology revolution our society experienced during the past decade resulted in the generation of huge amounts of raw data, which precessing requires efficient computing platforms[1]. So far, CMOS downscaling was able to meet these requirements, however, due to different technological issues: (i) reliability wall[4], (ii) leakage wall[2,3], and (iii) cost wall[2,4], CMOS downscaling turns out to be more in more difficult, which indicates the close end of Moore's law. In view of this, different technologies, e.g., tunneling FET, Graphene pn-Junction, spintronics, and memristor, have been considered as CMOS alternatives to meet the data processing market requirements[5].

Among those Spin-Wave (SW) based computing seems be one of the most promising avenues due to its[5]: (i) Ultra-low power consumption (it doesn't involve any charge movements), (ii) acceptable delay, (iii) scalability to nm wavelength range, and (iv) intrinsic data parallelism (multiple frequencies can independently and simultaneously coexist in the same waveguide).

In view of SW great potential, various logic gates based on SW interactions have been reported, e.g.,[6–16]. The first SW logic gate experimentally realized was a current controlled Macha-Zender interferometer based NOT gate[6]. Subsequently, by using a similar approach, XNOR, NAND and NOR logic gates were designed[7–9]. Two parallel re-configurable nanochannel magnonic devices were used to design voltage-controlled XNOR and NAND gates[11] and by placing two magnon transistors in the arms of a Mach-Zehnder interferometer, an XOR gate was designed[10]. While the previous gates make use of SW amplitude information encoding SW phase information encoding has been also considered[12] and different logic gates including buffer, inverter, (N)AND, (N)OR, XOR and Majority gates were proposed[12]. Moreover, cross structures were used to build (N)OR gate[13]. Additionally, two phase encoding based Majority gates were physically realized[1415].

While the previously mentioned proposals disregard (iv), which potentially opens a data parallel computation avenue unfeasible for CMOS and in general for any charge moving based technology, in has been suggested in[16] that one 3-input Majority gate can simultaneously process 3 input data sets encoded in SW with different frequencies. The presented structure contains bent regions, which are not preferred in SW designs, and makes use of magnonic crystals as input and output filters, which induces substantial delay overhead.

In this paper we revisit the multi-frequency SWs support for data parallelism, discuss it in its general form, and propose a generic n-frequency data parallel in-line gate structure. Subsequently, we present XOR and Majority SW gates capable to simultaneously process in the same waveguide 8 input data sets encoded in 8 different frequencies. The main contributions of this work can be summarized as follows:

- Design of multi-frequency byte-wide in-line Spin Wave logic gate: 8-bit 3-input Majority gate is implemented using the multi-frequency in-line structure.
- Validation of the proposed structure: The byte-wide Majority gate is validated by means of OOMMF simulations.
- Comparison of the design with the conventional approach: The proposed byte-wide 3-input Majority gate requires 4.16x less area than the conventional approach with similar latency and energy consumption.

The rest of the paper is organized as follows. Section II provides basic background of SWs physics and SW based computing. Section III describes the proposed data parallel gate and Section IV provides inside on the simulation setup, and parameters. In Section V we evaluate 8-bit instance of the proposed design, compare it with conventional scalar logic gate based counterpart, and discuss scalability aspects. Section VI concludes the paper.

II. SW BASED COMPUTING BACKGROUND

The electron spins tend to align themselves along the applied magnetic field direction to decrease the total energy to the lowest level, when applying an external magnetic field to a ferromagnetic material[17]. If an, e.g., Magnetoelectric (ME) cell, antenna, based excitation method is utilized to deflect the electron spin, a Spin Wave (SW) is created by exchange and dipole interactions. This results in a precessional spin movement[17], which can be described by the Landau-Lifshitz-Gilbert (LLG) equation[18]:

$$\frac{d\vec{m}}{dt} = -|\gamma|\mu_0 \left(\vec{m} \times \vec{H}_{eff}\right) + \alpha \left(\vec{m} \times \frac{d\vec{m}}{dt}\right), \tag{1}$$

where α is the damping factor, γ the gyromagnetic ratio, μ_0 the vacuum permeability, and m the magnetization. Also, H_{eff} is the effective field and it is equal to $H_{eff} = H_{ext} +$

$H_{ex} + H_{demag} + H_{ani}$ where H_{ext} is the external field, H_{ex} the exchange field, H_{demag} the demagnetizing field, and H_{ani} the magneto-crystalline anisotropy.

An excited SW is characterized by its f, determined by the time a complete spin precession takes, wavelength λ, the shortest distance between two spins exhibiting the same spinning behaviour, wave-number k $\left(k = \frac{2*\pi}{\lambda}\right)$, amplitude A, and phase ϕ. Such SWs can simultaneously propagate through the same waveguide, while carrying information potentially encoded in amplitude, phase, frequency or combination of those, and their mutual interaction is governed by the superposition and interference principles. As such, two SWs having the same A, λ, and f will constructively or destructively interfere if their phase difference is 0 or π, respectively. Moreover, the majority decision governs the interference process when more than two waves with the same A, f, and λ coexist in the waveguide. Specifically, if the number of SWs that have $\phi = 0$ (logic "0") is greater than the number of SWs that have $\phi = \pi$ (logic "1"), then the interference result is logic 0 and 1 otherwise, which provides a natural support for the direct evaluation of Majority functions. Consequently, the behaviour of a 3-input Majority gate, which CMOS implementation requires 18 transistors, can be mimicked by the interference in the same waveguide of 3 SWs[12]. In addition, SWs carrying amplitude and/or phase encoded information but with different fs can simultaneously propagate in the same waveguide while only interfering with their own species (waves having the same frequency), which provides natural supports for data parallel computing. We note that, in the most general case, SW with distinct A, f, ϕ, and λ generated in the same waveguide will interfere and generate SWs results that can provide support for yet to be unveil computation paradigms, but in this paper we only concentrate on the interaction of SW with the same amplitude and frequency.

Different SW types, i.e., exchange spin wave, exchange-dipole spin wave, magnetostatic surface spin wave, forward volume magnetostatic spin-waves, backward volume magnetostatic spin-waves, can be excited depending on the SW propagation direction versus the magnetization and effective magnetic field directions[17]. While each type has certain attractive characteristics, as seen from the circuit design point of view Forward Volume Magnetostatic spin-waves (FVMSWs) appear to be the most interesting because the in-plane spin-wave propagation is isotropic. As a result, the same wave-number is generated in all directions, which creates circuit design opportunities not achievable for the other SW types.

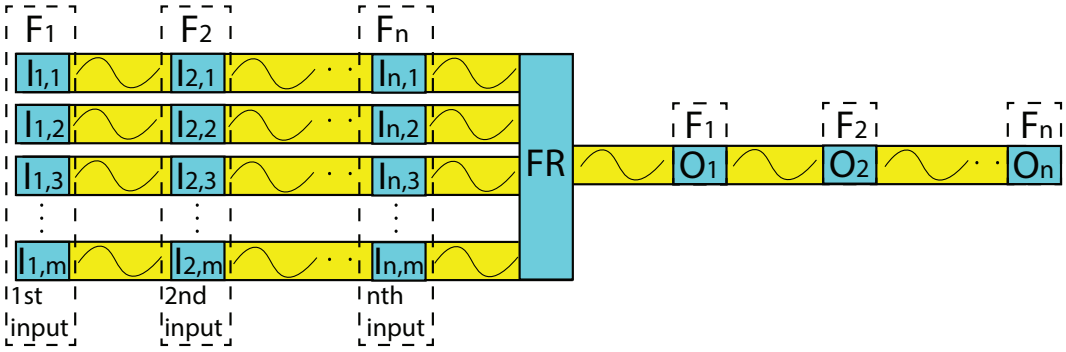

FIG. 1. Multi-Frequency Spin Wave Logic Gate

III. n-BIT DATA PARALLEL SW LOGIC GATE

The proposed m-input n-bit data parallel SW logic gate structure is depicted in Figure 1. It operates on a set of n m-bit values, while each set element is being encoded in it own frequency, $f_i, \{i = 1, 2, \ldots, n\}$. As graphically indicated in the Figure, SW excitation elements, e.g., ME cells, placed along the m input waveguides are utilized to transform the input values at $I_{1,1}$, $I_{1,2}$, $I_{1,3}$, $\ldots$, $I_{m,n}$ into SWs, which subsequently propagate towards the Functional Region (FR) without interfering with each-other. Only when the $m \times n$ waves reach the FR SWs within each group $\{I_{1,1}, I_{1,2}, I_{1,3}, \ldots, I_{m,i}\}_{i=1,n}$ start to interact, which results in n output SWs that can be read by transducers placed at O_1, O_2, $\ldots$, O_n or passed to potential following SW gates. As the proposed structure enables independent propagation and interaction of multiple frequency SWs it allows for parallel processing of multiple input sets within the same structure. This, potentially results in delay and area savings when compared to a conventional evaluation based on serialization or hardware replication, respectively.

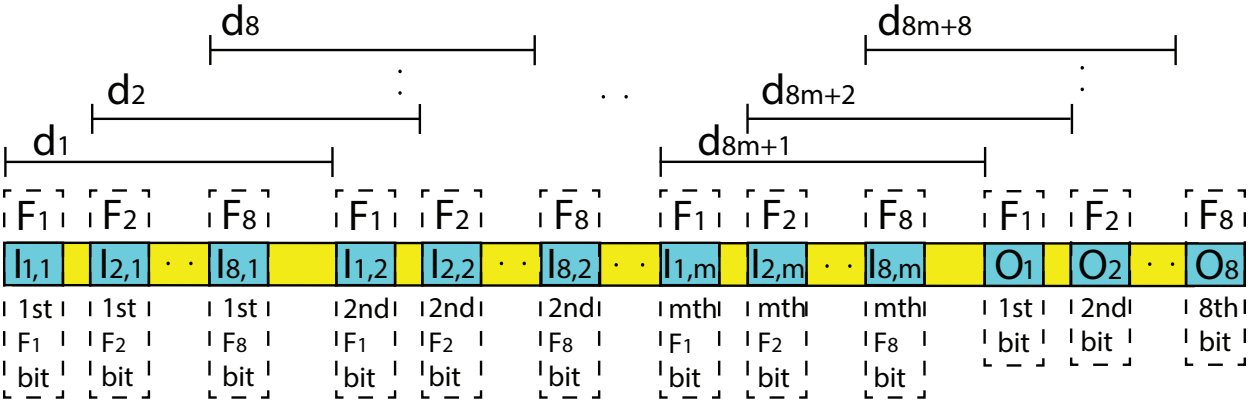

FIG. 2. Byte-based In-line Spin Wave Logic Gate Structure

While the structure is generic, its implementation by following the topology depicted in Figure 1 relies on waveguide stacking on top of each other and have bent regions, which are impeding proper SW propagation. To this end, a more appropriate realization is the one waveguide only in-line structure depicted in Figure 2 for the particular case of an 8-input 8-bit data parallel gate. As indicated in the Figure the voltage- or current-encoded logic values ($I_{1,i}$, $I_{2,i}$, ..., $I_{8,i}$) applied to ME cells or other transducers are used to excite $f_i, \{i = 1, 2, \ldots, 8\}$ SWs within the same waveguide, which eventually interact and generate an 8-bit output.

To ensure correct gate functionality, SWs with the same frequency must be excited with the same amplitude and wavelength. In addition, the distance between the SW excitation location and the interference points have to be properly adjusted as they play a key role in the gate behaviour. For example, if the desired result of SWs interference is constructive if they have the same phase and destructive if they are out of phase, then the distances between similar frequency sources must be $n \times \lambda_i, i = (1, 2, 3, \ldots, 8)$, i.e, $d_1 = n\lambda_1$, $d_2 = n\lambda_2$, $\ldots d_8 = n\lambda_8$ (where $n = 1, 2, 3, \ldots$). In contrast, if the opposite behaviour is required, the distances between similar frequency sources must be $\frac{n}{2}\lambda_i$, i.e., $d_1 = \frac{n}{2}\lambda_1$, $d_2 = \frac{n}{2}\lambda_2$, ..., $d_8 = \frac{n}{2}\lambda_8$ (where $n = 1, 3, 5, \ldots$).

Due to the very SW nature the gate can provide direct or complemented output values by properly adjusting the position, i.e., the transducer location, at which each output is read. For example, if the non-inverted output is required the transducers sould be located at $n\lambda_i, i = (1, 2, 3, \ldots, 8), n = (1, 2, 3, \ldots)$ from the last f_i SW source, i.e, $d_{n+9} = n\lambda_1$, $d_{n+10} = n\lambda_2$, ... $d_{n+16} = n\lambda_8$. When the inverted version is of interest the output should be detected at a distance $\frac{n}{2}$ λ_i from the last f_i SW source, i.e., $d_{n+9} = \frac{n}{2}\lambda_1$, $d_{n+10} = \frac{n}{2}\lambda_2$, ... $d_{n+16} = \frac{n}{2}\lambda_8$ (where $n = 1, 3, 5, \ldots$). The two strategies can be combined in case that the direct function is required for some input sets and the inverted for the rest.

IV. EXPERIMENTAL SETUP

This section provides inside on the simulation platform and parameters, we utilized to validate our proposal.

A. Simulation Platform

To validate the proposed structure and get inside on its functionality, the Object Oriented MicroMagnetic Framework (OOMMF)[19], which predicts the magnetization dynamics by numerically solving the LLG equation, was utilized. OOMMF inputs consists of Tckl/Tk scripts describing the gate structure and for a better visualization, we Matlab post-processed the OOMMF simulation results.

B. Simulation Parameters

During the experiments we made use of a $Fe_{60}Co_{20}B_{20}$ waveguide with Perpendicular Magnetic Anisotropy (PMA), with has an anisotropy field $H_{anisotropy} > M_s$, which implies that no external magnetic field is required. The waveguide thickness and width were set to 1 nm and 50 nm, respectively. To evaluate the gate structures, the following parameters values were utilized during the simulations: perpendicular anisotropy constant $k_{ani} = 8.3177 \times 10^5$ J/m^3, magnetic saturation $M_s = 1.1 \times 10^6$ A/m, damping constant $\alpha = 0.004$, and exchange stiffness $A_{exch} = 18.5$ pJ/m[20]. As we evaluated 8-bit data parallel gates we made use of SWs with 10 GHz, 20 GHz, 30 GHz, 40 GHz, 50 GHz, 60 GHz, 70 GHz, and 80 GHz frequencies. Based on the FVMSW dispersion relation and the wavenumber $k = \frac{2\pi}{\lambda}$, the distances between the same frequency sources were determined as follows: $d_1 = 166$ nm, $d_2 = 100$ nm, $d_3 = 117$ nm, $d_4 = 165$ nm, $d_5 = 174$ nm, $d_6 = 130$ nm, $d_7 = 168$ nm, and $d_8 = 176$ nm. In addition, the minimum distances between two consecutive sources has been set to 1 nm.

V. SIMULATION RESULTS AND DISCUSSION

This section discusses OOMMF simulation results for the Byte-based Majority gate. Subsequently, we compare the data parallel design with conventional SW gate based implementation and, finally, discuss scalability related issues and the effect of waveguide width scaling.

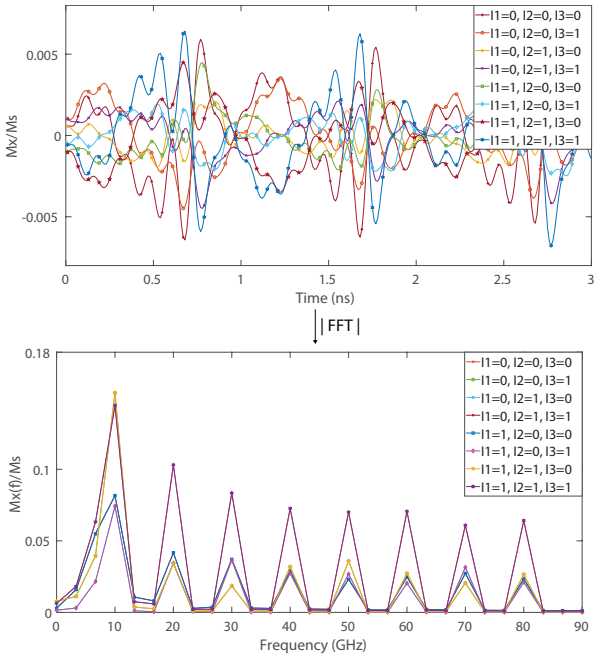

FIG. 3. Byte-Based Majority Gate Response in Time and Frequency

A. Simulation Results for 3-input Majority Gate

Figure 3 presents OOMMF simulation results for the byte-based 3-input Majority gate. Also in this case the 8 output values can be extracted by taking the spin wave FFT amplitude absolute value and different frequency SWs do not affect each other as there are no frequency peaks at other frequencies than the excitation frequencies. As it can be observed in Figure 4, SWs with different frequencies propagate through the waveguide, and only SWs with similar frequency are interfering constructively and destructively depending on their phases. At the first output detector, which corresponds to a frequency 10 GHz, the result of the 3 inputs at this frequency is obtained as it is clear in Figure 4 a). When $I_1 = I_2 = I_3 = 0$, the waves interfere constructively resulting in a phase 0 SW, i.e., a logic 0. When only of the inputs is 1 while the others are 0 the waves interfere constructively and destructively, which also results in a phase 0 SW. However, when two or more inputs are 1 the gate output is a phase π SW, i.e., a logic 1. This holds true of all the 8 output detectors embedded in the gates.

B. Comparison and Discussion

To get inside on the potential implications of our proposal we compare byte-based 3-input Majority gate with counterpart implementation obtained by the instantiation of 8

normal (scalar) Majority gate, in terms of area, delay, and energy consumption. We assume that excitation/detection cell are 10 nm × 50 nm in all cases and that they are the main contributors to circuit delay and energy consumption. This means that the two implementation styles exhibits similar delay and energy consumption as they use the same number of sources and detectors. In terms of area, the conventional approach consumes 0.116 μm^2 real estate to implement Majority gate as 8 Majority gates are required to evaluate the 8-bit 3-inputs Majority gate. In contrast, the 8-bit data parallel gate requires only 0.0279 μm^2 to implement Majority gate as all the SW inputs are excited in the same waveguide. That indicates that the byte parallel approach requires 4.16x less area for the Majority gate implementation.

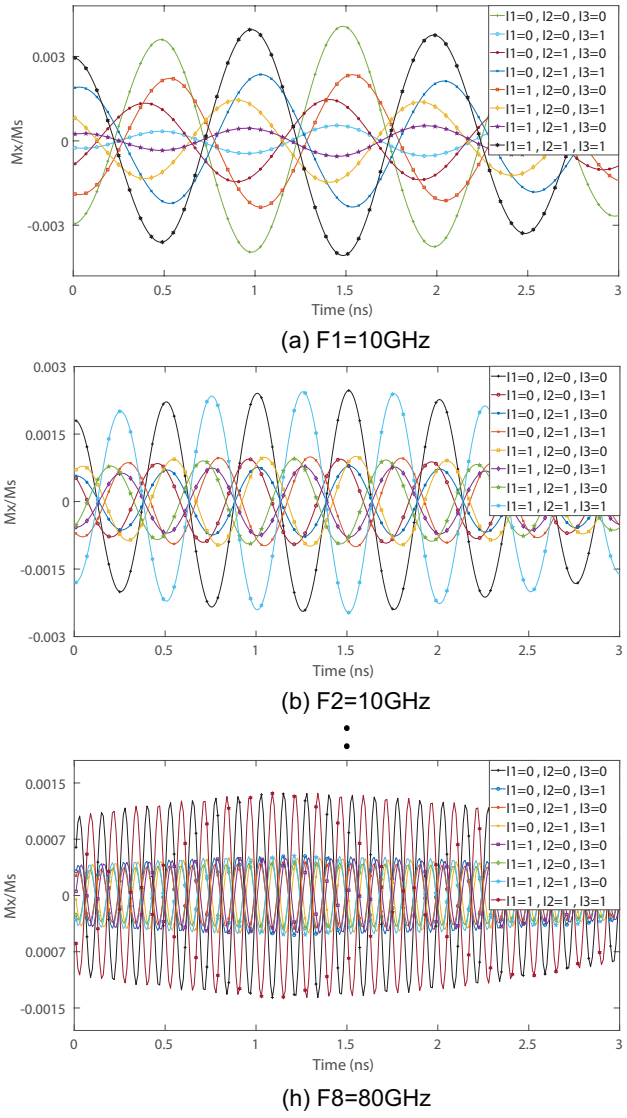

FIG. 4. MAJ Gate Outputs: a) f_1=10GHz, b) f_2=20GHz, ..., h) f_8=80GHz

Scalability While the proposed structure is generic and in principle functions correctly for a high number of inputs. However, due to the damping effect, SWs might have to be excited at different intensity levels if large number of inputs are required, such that the I_n energy $< I_{n-1}$ energy $< .. < I_1$ energy to guarantee the correct functionality of the structure. This variation in input energy can be used just if incorrect behaviour of the logic gate is noticed. Also, the source itself might be programmed to generate these different levels without a need for the input variation.

Waveguide Width Variation To examine the waveguide with effect on gate functionality we scaled it up to 500 nm. We noticed that the width scaling doesn't affect the functionality of the proposed structure, no crosstalk effects were present, and that the logic gates are still functioning correctly. In addition, as the width increases the ferromagnetic resonance frequency decreases, and by implication the first used frequency can assume a lower value.

VI. CONCLUSIONS

In this paper, we introduced a novel data parallel multi-frequency Spin Wave computation paradigm the associated generic in-line gate structure, which builds upon the selective interference of SWs with different frequencies coexisting in the same waveguide. To validate and evaluate the impact of our proposal, we implemented byte-wide 3-input Majority gates operating on 8 different frequency SWs, validated them by means of OOMMF simulations, and compared their area, delay, and energy consumption with conventional SW gate implementation counterparts. Our evaluation indicated that the byte-wide approach provided a 4.16x area reduction for the implementation of an 8-bit 3-input Majority gate without inducing any delay and power overhead.

REFERENCES

[1]R. L. Villars, C. W. Olofson, and M. Eastwood, "Big data What it is and why you should care," IDC, 2011.

[2]D. Mamaluy and X. Gao, "The Fundamental Downscaling Limit of Field Effect Transistors," Applied Physics Letters, vol. 106, no. 19, p. 193503, 2015.

[3]B. Hoefflinger, Chips 2020: A Guide to the Future of Nanoelectronics. Springer Science and Business Media, 2012.

[4]N. Z. Haron and S. Hamdioui, "Why is CMOS Scaling Coming to an End?" in Design and Test Workshop, 2008. IDT 2008. 3rd International. IEEE, 2008, pp. 98–103.

[5]D. E. Nikonov and I. A. Young, "Overview of Beyond-CMOS Devices and a Uniform Methodology for their Benchmarking," Proceedings of the IEEE, vol. 101, no. 12, pp. 2498–2533, Dec 2013.

[6]M. P. Kostylev, A. A. Serga, T. Schneider, B. Leven, and B. Hillebrands, "Spin-Wave Logical Gates," Applied Physics Letters, vol. 87, no. 15, p. 153501, 2005.

[7]T. Schneider, A. A. Serga, B. Leven, B. Hillebrands, R. L. Stamps, and M. P. Kostylev, "Realization of Spin-Wave Logic Gates," Applied Physics Letters, vol. 92, no. 2, p. 022505, 2008.

[8]K.S. Lee and S.K. Kim, "Conceptual Design of spin-wave Logic Gates Based on a Machzehnder-Type spin-wave Interferometer for Universal Logic Functions," Journal of Applied Physics, vol. 104, no. 5, p. 053909, 2008.

[9]I. A. Ustinova, A. A. Nikitin, A. B. Ustinov, B. A. Kalinikos, and E. Lhderanta, "Logic Gates Based on Multiferroic Microwave Interferometers," in 2017 11th International Workshop on the Electromagnetic Compatibility of Integrated Circuits (EMCCompo), July 2017, pp. 104– 107.

[10]A. V. Chumak, A. A. Serga, and B. Hillebrands, "Magnon Transistor for All-Magnon Data Processing," Nature Communication, volume 5, pp. 4700, 2014.

[11]B. Rana and Y. Otani, "Voltage-Controlled Reconfigurable Spin-Wave Nanochannels and Logic Devices," Physical Review Applied, vol. 9, p. 014033, Jan 2018.

[12]A. Khitun and K. L. Wang, "Non-Volatile Magnonic Logic Circuits Engineering," Journal of Applied Physics, vol. 110, no. 3, p. 034306, 2011.

[13]K. Nanayakkara, A. Anferov, A. P. Jacob, S. J. Allen, and A. Kozhanov, "Cross Junction spin-wave Logic Architecture," IEEE Transactions on Magnetics, vol. 50, no. 11, pp. 1–4, Nov 2014.

[14]T. Fischer, M. Kewenig, D. A. Bozhko, A. A. Serga, I. I. Syvorotka, F. Ciubotaru, C. Adelmann, B. Hillebrands, and A. V. Chumak, "Experimental prototype of a spin-wave majority gate", Applied Physics Letter, Vol. 110, February 2017, pp. 152401-1-4.

[15]F. Ciubotaru, G. Talmelli, T. Devolder, O. Zografos, M. Heyns, C. Adelmann, and I. P. Radu, "First experimental demonstration of a scalable linear majority gate based on spin waves", IEEE International Electron Devices Meeting (IEDM), January 2019, pp.

36.1.1-36.1.4.

[16]A. Khitun, "Multi-frequency magnonic logic circuits for parallel data processing," Journal of Applied Physics, vol. 111, no. 5, pp. 054307, 2012.

[17]A. V. Chumak, A. A. Serga, and B. Hillebrands, "Magnonic Crystals for Data Processing," Journal of Physics D: Applied Physics, vol. 50, no. 24, p. 244001, 2017.

[18]L. Landau and E. Lifshitz., "On the Theory of the Dispersion of Magnetic Permeability in Ferromagnetic Bodies," Physikalische Zeitschrift der Sowjetunion, pp. 101– 114, 1935.

[19]M. J. Donahue and D. G. Porter, "OOMMF User's Guide, version 1.0," Interagency Report NISTIR 6376, Sept 1999.

[20]T. Devolder, J.-V. Kim, F. Garcia-Sanchez, J. Swerts, W. Kim, S. Couet, G. Kar, and A. Furnemont, "Time-Resolved Spin-Torque Switching in MgO-Based Perpendicularly Magnetized Tunnel Junctions," Physics Review B, vol. 93, p. 024420, Jan 2016.