Device-Aware Test for Emerging Memories: Enabling Your Test Program for DPPB Level

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Device-Aware Test for Emerging Memories: Enabling Your Test Program for DPPB Level

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***Abstract*—This paper introduces a new test approach: device-aware test (DAT) for emerging memory technologies such as MRAM, RRAM, and PCM. The DAT approach enables accurate models of device defects to obtain realistic fault models, which are used to develop high-quality and optimized test solutions. This is demonstrated by an application of DAT to pinhole defects in STT-MRAMs and forming defects in RRAMs.**

I. Introduction

Memory testing has gone through a long evolution process. Before 1980, memory chips were tested using functional and ad-hoc tests where the concept of fault models was not applicable. This resulted in a low defect coverage and/or very long test time, in the order of $\mathcal{O}\left(n^2\right)$ with n representing the number of addresses. In the 1980s, several fault models such as stuck-at faults and address decoder faults were introduced [1]. This led to the development of march tests which allowed the fault coverage to be provable. As a result, the test time was reduced significantly to the order of $\mathcal{O}\left(n\right)$. In the 1990s, experimental results revealed that a number of faults could not simply be covered by the known fault models [2]. This paved the way for introducing new fault models, e.g. write disturb faults, or coupling faults. These faults were derived based on circuit simulations with resistive defects. This approach assumes that a defect in a device (e.g., transistor) can be modeled as a linear resistor. Recent work (supported by silicon data) on STT-MRAM and RRAM devices has shown that a linear resistor is inaccurate for modeling the defective behavior of these devices [3,4], and it is even misleading in the sense that it can result in fault models that have nothing to do with the actual fault behavior of the devices. Such devices have unique defect mechanism, and are by nature non-linear. This indicates the importance of developing new approaches for fault modeling and test of emerging memories.

The *device-aware test* (DAT) approach [5] is a possible solution. A key difference of DAT from the conventional one is that device defects are modeled physically instead of lumping all defect effects into a parallel or series resistor. This is achieved by incorporating the defect effects into the technology parameters of the device and thereafter into its electrical parameters. In other words, it creates a parameterized SPICE-based model for the detective device, which enables accurate fault simulation; the defect strength is changed by sweeping the model parameters which are of interest for the defect. Next we will briefly introduce DAT and subsequently apply it to one defect in STT-MRAMs and one in RRAMs.

II. Device-Aware Test

Fig. 1 shows the three-step DAT flow.

1) Device-aware defect modeling: First, a defect needs to be physically analyzed and characterized to understand its forming mechanism, location, occurrence rate, and the key technology parameters that are impacted. Thereafter, the effects of the defect are quantitatively incorporated into these technology parameters. Second, the defect-induced changes in the technology parameters are mapped into the device's electrical parameters. This allows us to convert the defect-free device model into a parameterized defective model. Third, the obtained model can be further calibrated by fitting to silicon data if available.

2) Device-aware fault modeling: First, a complete fault space which describes all possible faults in emerging memories is defined and classified. To this end, the conventional *fault primitive* (FP) notation: $\langle S/F/R \rangle$ [6] is inherited and expanded. S denotes the operation sequence that sensitizes a fault, while R describes the readout result if the last operation in S is a read. F denotes the value in the faulty cell after S is applied. Apart from logic '0' and '1', F can also be 'U' (undefined), 'L' (extreme low) and 'H' (extreme high) states due to defects, as indicated by silicon data shown in [5]. Based on the extended FP definition, all memory faults can be defined and classified into two categories: *easy-to-detect* (EtD) faults and *hard-to-detect* (HtD) faults [5]. EtD faults are those which can be detected by applying normal write and read operations, i.e., March tests, while HtD faults refer to those which cannot be guaranteed by March tests in their detection. Second, a systematic fault analysis based on circuit simulations for each targeted defect is conducted; this is to derive realistic faults that can be sensitized by such a defect within the pre-defined fault space.

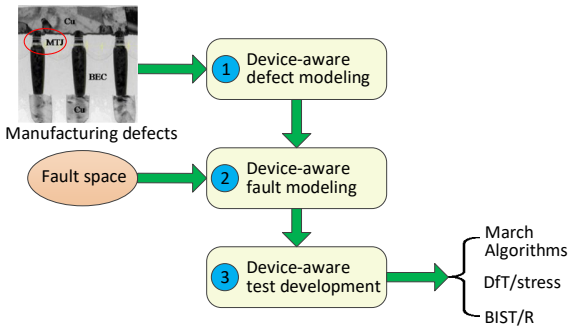

Fig. 1. Device-aware test flow.

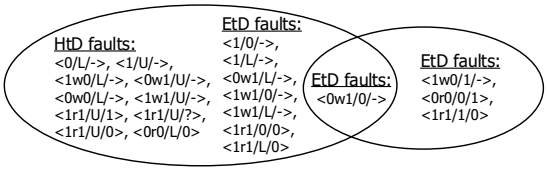

Fig. 2. DAT (left) vs. conventional approach (right) for pinhole defects.

3) Device-aware test development: The accurate and realistic faults obtained from the previous step are used to develop test solutions for DPPB level. Specifically, EtD faults can simply be detected by March tests. HtD faults, however, need special Design-for-Testability (DfT) or stress tests. The clear mapping between physical defects and fault models enables us to not only reduce test escapes and time but also speed up yield learning [5,7].

III. DAT for Pinhole Defects in STT-MRAMs

Pinhole defects are a key type of manufacturing defects [7]; they form in the MgO tunnel barrier of *magnetic tunnel junction* (MTJ) during the multi-layer deposition process [8,9].

1) Device-aware defect modeling: We identified in [8] that *resistance-area* (RA) product and *tunneling magneto-resistance* (TMR) are the two key technology parameters that are mainly impacted by the defect. Therefore, we incorporated the effects of pinhole defects into these two technology parameters and subsequently into the electrical parameters of the MTJ device. By fitting to experimental data and model optimization, we derived a pinhole-parameterized MTJ compact model [8].

2) Device-aware fault modeling: The above DAT-based pinhole model was used to derive accurate and realistic faults using SPICE-based circuit simulations with Cadence Spectre. Fig. 2 compares the fault modeling results of the DAT and traditional resistive approaches; the results are given using the FP notations and the names of these FPs can be found in [5]. It can be seen that 17 unique faults including both EtD and HtD faults, were sensitized using the the DAT approach; an example of HtD faults is *state fault* S1FU=$\langle$1/U/-$\rangle$ meaning that the MTJ device is initialized to state '1' but it ends up at state 'U'. These faults were not observed with the conventional resistive model. This indicates that test solutions developed with resistive models may lead to test escapes. Moreover, the resistive model sensitized three EtD faults which were not observed using the DAT-based defect model, meaning a waste of test time and resources. Only one EtD fault: W1TF0=$\langle$0w1/0/-$\rangle$ is covered by both models.

3) Device-aware test development: EtD faults and HtD faults require different test solutions. March tests including the element $\Updownarrow$(w1,r1) can guarantee the detection of all sensitized EtD faults using the DAT approach as shown in Fig. 2. However, HtD faults require dedicated DfT or stress tests to detect them. For instance, a hammering write '1' stress test can be used to intentionally enlarge the pinhole size and transform his faulty behavior from HtD faults to EtD ones, making its testing with just a March test feasible [8].

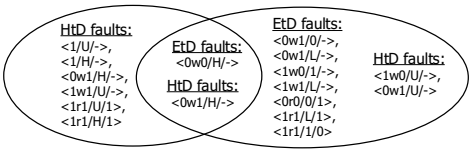

Fig. 3. DAT (left) vs. conventional approach (right) for forming defects.

IV. DAT for Forming Defects in RRAMs

Forming defects take place during the *conductive filament* (CF) forming step of RRAM manufacturing process [5].

1) Device-aware defect modeling: To physically model the defect, its impact is first incorporated into three key technology parameters of RRAM device: CF top width ϕ_{T}, CF length l_{CF}, and CF length variation Δl_{CF}; these three updated parameters are mapped into the device's electrical parameters determining the resistance and switching behavior of an RRAM device. After fitting to measurement data, an optimized defective RRAM device for forming defects can be derived [5].

2) Device-aware fault modeling: Fig. 3 shows the results of fault analysis. Clearly, the DAT approach can sensitize faults which can not be found using the traditional fault modeling approach based on linear resistor injection.

3) Device-aware test development: Testing EtD faults for this defect can be done easily with a March element $\Updownarrow$(w0,w0,r0). For HtD faults, a DfT scheme is needed. For instance, reducing write time or voltage is useful to defect faults related to the 'U' faulty state [10].

V. Conclusion

This paper has shown the concept of Device-Aware-Test (DAT) and its superiority in being able to model unmodeled faults by the traditional fault modeling approach. DAT has the capability to win the war against unmodeled faults not only in non-linear devices such as RRAM, PCM, STT-MRAM, but also in devices such as FinFET especially when it comes to small technology nodes. Not to mention the potential of DAT in speeding up diagnosis and yield learning, reducing the overall test cost and yield loss.

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