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Zhang, Boyao; Carisey, Yorick; Damian, A.; Poelma, Rene; Zhang, Guo Qi; van Zeijl, Henk

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3D Interconnect technology based on low temperature copper nanoparticle sintering

B. Zhang, Y.C.P. Carisey, A. Damian, R.H. Poelma and G.Q. Zhang

Department of Microelectronics, Delft University of Technology, Delft, 2628CT, the Netherlands

H.W. van Zeijl

Else Kooi Lab, Delft University of Technology, Delft, 2628CT, the Netherlands

Abstract - **We explore a methodology for patterned copper nanoparticle paste for 3D interconnect applications in wafer to wafer (W2W) bonding. A novel fine pitch thermal compression bonding process (sintering) with coated copper nanoparticle paste was developed. Most of the particle size is between 10-30 nm. Lithographically defined stencil printing using photoresist and lift-off was used to apply and pattern the paste. Variations in sintering process parameters, such as: pressure, geometry and ambient atmosphere, were studied. Compared to Sn-Ag-Cu (SAC) microsolder bumps, we achieved better interconnect resistivity after sintering at 260 ℃ for 10 min, in a 700 mBar hydrogen forming gas (H_2/N_2) environment. The electrical resistivity was 7.84 ± 1.45 $\mu\Omega\cdot cm$, which is about 4.6 times that of bulk copper. In addition, metallic nanoparticle interconnect porosity can influence the electrical properties of the interconnect. Consequently, we investigated the porosity effect on conductivity using finite element simulation. A linear relationship between the equivalent conductivity and particle overlapping ratio was found.**

Keywords: Interconnect; 3D packaging; copper nanoparticle paste; low-temperature sintering

I. INTRODUCTION

The need for more functionalization, miniaturization and lower energy consumption drives the ongoing semiconductor industry. Interconnect material that can be fabricated in accurate nanoscale, with advanced properties, is essential [1-3]. Heterogeneous integration including chip to wafer (C2W), wafer to wafer (W2W) and package on package stacking (PoP), requires interconnect structures with ultra-fine accuracy, profound electrical property and better reliability. Current bonding technology, including wire bonding and flip-chip technology, are facing challenges as requirements in feature size, reliability and electrical property have raised [4-10].

To overcome the drawbacks mentioned in previous technologies, metallic nanoparticles have become a promising candidate for 3D heterogeneous integration. Among various of metallic nanoparticles, Cu nanoparticle paste is emerging as a promising candidate in 3D interconnect applications [11]. First, bulk copper can be formed after sintering, which will have similar reflow temperature as melting temperature of bulk copper (1085 ℃). In typical flip-chip technology, which usually use Sn-Ag-Cu (SAC) alloy microsolder bumps, with a reflow temperature of 220-250 ℃. However, copper nanoparticle paste, with particle size 40 nm in average, does not reflow after the first sintering process since the nanoparticle fuse together [10]. In addition, creep failure inside solder joints due to secondary intermetallic compounds formation, can be avoided by pure Cu nanoparticle paste. However, one drawback of Cu nanoparticles, is the oxidization in air. In this paper, we use Cu nanoparticle with an organic coating to protect Cu from oxidation. Furthermore, these core-shell structured Cu nanoparticles are dispersed in viscous solution, which enables them to be patterned as interconnect structures [12].

As feature sizes within chips are decreasing, it is difficult and expensive to achieve fine pitch (<50 μm) interconnect structure, due to processing limitations [13]. In this paper, a novel methodology based on low temperature thermal compression (sintering) using copper nanoparticle paste is developed for W2W 3D interconnect. Lithographic defined stencil printing method was developed to obtain pattern Cu nanoparticle paste below 10 μm. A novel fine pitch thermal compression bonding process (sintering) with coated copper nanoparticle paste was developed. Variations in sintering process parameters, such as: pressure, geometry and ambient atmosphere, were studied. As a result of that, lower electrical resistivity than typical SAC, was achieved after sintering at 260 ℃ for 10 min, in a 700 mBar forming gas environment. Considering of the fact that sintered nanoparticles have porous structure, which will influence the electrical property of interconnect, finite element simulation is used in to investigate the porosity effect on resistivity/conductivity.

II. COPPER NANOPARTICLE PASTE INTERCONNECT PROCESSING AND CHARACTERIZATION

When the copper particle size reduces towards nanoscale, surface energy will increase. This will suppress the local melting point of the particle the bulk material melting temperature [14]. This scale effect makes copper nanoparticles a strong candidate for 3D integration application. The copper nanoparticle paste used in this study is commercially available [12]. These copper nanoparticles are coated with an organic protective layer to prevent oxidation.

A. Mask design and process for photolithography patterning and wafer bonding

We employed photolithography defined stencil printing method for wafer-level processing. Photoresist is applied and patterned using front-end wafer-level processing. Then copper paste is applied and finally photoresist lift-off process is used to obtain patterned structures for electrical and mechanical tests. The process flow is illustrated in Figure. 1.

For the first step, a 300 nm low-stress silicon nitride (SiN_x) was deposited on the silicon substrate by using low-pressure-chemical-vapour-deposition (LPCVD). Then a 1.4 μm thick photoresist (EVG 120) was spin coated on the top. Then the photoresist was exposed and developed with a designed mask.

A patterned surface structure was obtained as shown in Figure 1(a). Next, a small amount of Cu nanoparticle paste was applied, as delivered from Lockheed Martin. As shown in Figure 1(b), silicone squeegee, from KOENEN Technologies, was selected to manually distribute Cu nanoparticle paste over the patterned wafers surfaces. The shore hardness was 65°.

As shown in Figure 1(c), test wafers with Cu nanoparticle paste were followed by drying at 50 ℃ for 5 min using a hot plate. After that, a water ultrasonic bath with a beaker filled with N-Methyl-2-pyrrolidone (NMP) was used for photoresist layer removal at room temperature. The last step was completed by DI waster rinse and drying, as shown in Figure 1(d).

In Figure 2, there are different microstructures that were designed to test the pattern accuracy of this Cu nanoparticle paste. It can be seen that Cu nanoparticle paste has that ability to reach fine pitch accuracy, even below 5 μm. As an initial research work, manual distribution is acceptable. However, for high volume industry production, other distribution methods that can be applied in mass production is essential to ensure accuracy and consistency.
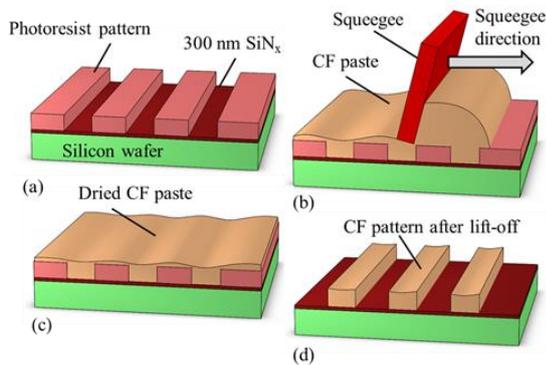

Figure 1. Schematic patterned test wafer process flow: (a) photoresist pattern on top of SiNx layer; (b) Cu nanoparticle paste distribution by squeegee; (c) Cu nanoparticle paste was dried using hot plate; (d) photoresist removal by ultrasonic bath in NMP.
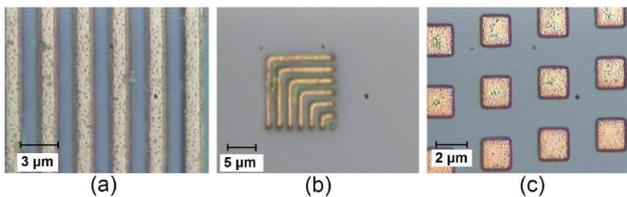

Figure 2. Patterened microstructrure on wafer level. (a), (b), (c) are different microstructures designed to test the Cu nanoparticle paste pattern accuracy.

After Cu nanoparticle paste was spread and dried on bottom wafer, top and bottom wafers were treated differently as shown in Figure 2. For the top wafer, SiN_x and silicon oxide layers were partially etched to give access to probe pads for electrical property measurement, as shown in Figure 3(c). Then, both wafers were deposited and patterned with 300 nm thin layer of copper with the same mask, by using conventional litho/etch processing, as shown in Figure 3(a). Then only bottom wafer was distributed and patterned with Cu nanoparticle paste, using the method described in previous

section, as shown in Figure 3(b). After pasted was dried, both top and bottom wafer were transferred to bonding machines for sintering, as shown in Figure 3(c). In order to study the ambient atmosphere effect on sintering result, three different atmosphere and four sintering methods were used, including N_2, hydrogen forming gas and vacuum sintering w/o N_2 flow. Based on Andreis results, 260 ℃ was chosen to be the ultimate sintering temperature [15]. The process were as follow:

1. 200 mBar N_2 enviornment was created by Heraus Vaccum oven for wafer bonding. The heating rate was about 10 ℃/min and wafers were annealed at 260 ℃ for 10 min. The cooling rate was 1 ℃/min.
2. In Aixtron Black Magic PECVD system, a controlled forming gas environment with 700 mBar was given. The hydrogen forming gas is a mix gas with a 10:1 concentration of H_2 and N_2. The rest of bonding parameters were the same as in N_2 environment.
3. AML wafer bonder could provide a high vacuum environment (~ 10^{-4} mBar) with controlled heating. Wafers were sintered at 200 °C (due to temperature limit of machine) at 30 ℃/min heating rate and annealed for 10 min. In one circumstance, a small N_2 flow was provide to avoid any possible oxygen inside the oven. The cooling rate was 1 - 2 ℃/min, depending on w/o N_2 flush.

To give access for electrical measuring probe, top wafer was removed by 30% KOH solution at 80 ℃, as shown in Figure 3(d). The KOH etch stopped at SiN_x layer of bottom wafer. Some mechanical force was applied to break the thin SiN_x layer on top wafer.
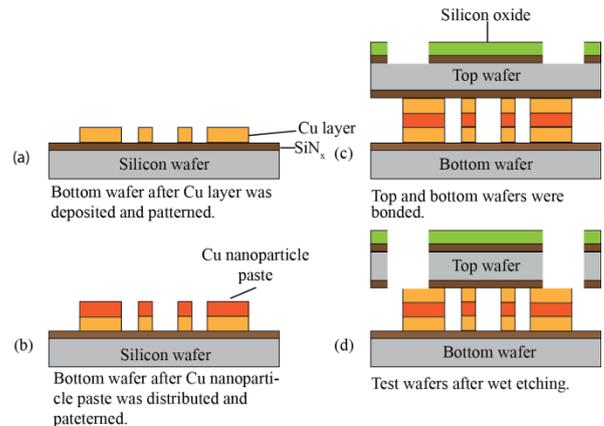

Figure 3. Process flow of wafer bonding procedure.

B. *Electrical resistivity measurement*

Electrical resistivity is one of the most important properties for 3D interconnect materials. Greek cross Van der Pauw (VDP) structures were designed within test wafers to measure the resistivity of Cu nanoparticle paste [16, 17]. The schematic structure of Greek cross VDP is shown in Figure 4. Forced current is applied through area 3 and 4. Then consequent voltage can be measured from area 1 and 2. A corresponding microstructure of Greek VDP was obtained in test wafers after Cu nanoparticle paste stencil printing, as shown in Figure 5.
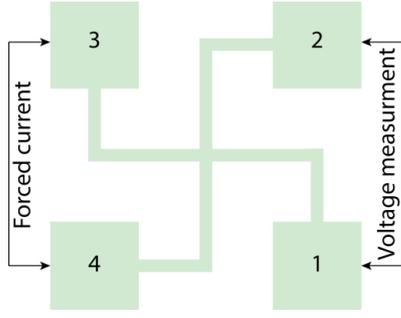
Figure 4. Schematic Greek cross VDP structure for sintered Cu nanoparticle paste resistivity measurement. The Forced current will be applied through area 3 and 4. Then consequent voltage could be measured through area 1 and 2.
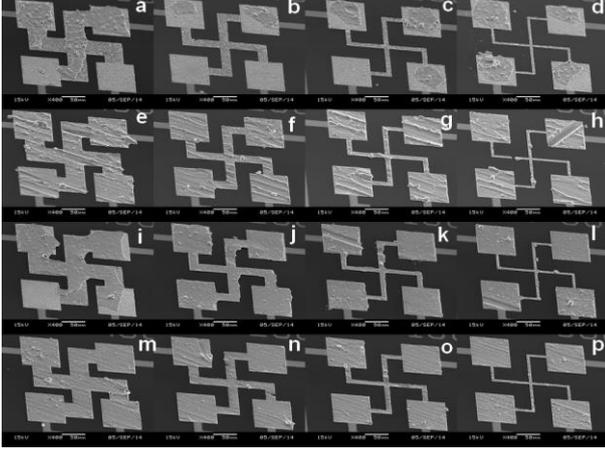

Figure 5. A various of Greek cross VDP structures on test wafers after Cu nanoparticle paste stencil printing.

A four point probe needles setup was used to perform I –V curve measurement. The forced current range was ± 10 mA. Sintered Cu nanoparticle paste thickness t was measured before bonding using a Dektak profile meter. The thicknesses of Cu nanoparticle paste can be controlled using the thickness of the photoresist. We processed three wafers with different photoresist thickness, and we obtained 1.5 μm, 2 μm and 3 μm. From Equation (1), sheet resistance can be derived by using Greek cross VDP methodology [16].

$$R_{sh} = \frac{\pi}{\ln 2} \frac{V_{34}}{I_{12}} \qquad (1)$$

The bulk resistivity of the sintered Cu nanoparticle paste is obtained by multiplying the sheet resistance by the film thickness,

$$\rho_{Cu\,NP} = R_{sh}\,t \,. \qquad (2)$$

Resistivity measurements in different ambient atmospheres were performed to study the influence of oxidation, see Figure 6. Samples sintered under vacuum atmosphere. For vacuum sintering, samples with a small flow of N_2 , the resistivity of it was measured as 52.68 ± 24.92 μΩ·cm. For the samples sintered in vacuum oven, without a flow of N_2, the resistivity is 75.90 ± 23.63 μΩ·cm without N_2 flush. Hydrogen forming gas ambient sintering atmosphere

resulted in the lowest resistivity of sintered Cu nanoparticle paste , which was 7.84 ± 1.45 μΩ·cm. In N_2 environment, the resistivity was 63.44 ± 22.12 μΩ·cm. Sintered Cu nanoparticle paste in hydrogen forming gas atmosphere showed the lowest resistivity, which is better than values reported previously in literature. Hydrogen forming gas, provides a reducing environment for Cu nanoparticle oxides during sintering, hence improving conductivity. For the higher resistivity obtained in vacuum atmosphere, both with and without N_2 flow, it is possible that vacuum pumping enable some surfactants in paste to evaporate. As a result of that, Cu nanoparticles were partially oxidized in a medium vacuum environment.
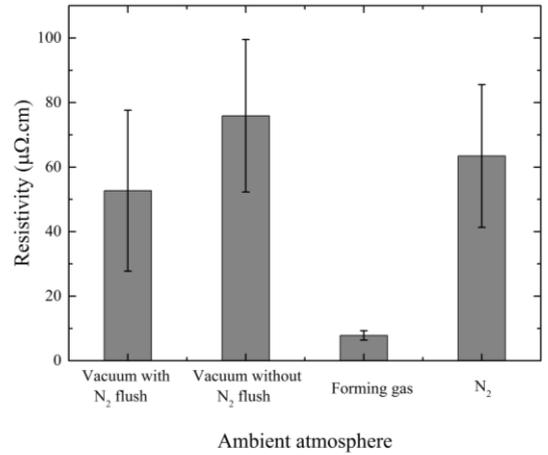

Figure 6. Sintered Cu nanoparticle paste resistivity with different ambient atmosphere

III. Finite Element Modelling of Porosity Effects on Electrical Resistivity

Our electrical resistivity measurements show that the value of sintered Cu nanoparticle paste was higher than that of bulk Cu. Considering the composition and structure of sintered Cu nanoparticle paste, porosity, organic shell residuals and oxidation during sintering probably decrease the conductivity of fused materials. To quantitatively understand the porosity effect on the electrical resistivity, a finite element modelling approach was used. A body centred cubic (BCC) structure was employed to capture the particle packing density in the sintered material. The BCC structure allows for the definition of a simple cubic unit cell and easy variation of the density. To characterize the effective resistivity of the unit cell, we apply a current on one side of the cell while grounding the other side. Solving the model, results in a voltage gradient over the unit cell, which is used to calculate the effective resistivity, see Figure 7. The copper atomic density is 1.530×10^{15} atom·cm^{-3} and the lattice parameter of BCC unit cell is 361.5 Å. In this study, we assumed that the neck formation happened between copper particles in the BCC unit cells.

The variation of porosity was simulated by adjusting the overlapping distance between each particle. A given overlapping distance δ between two particles indicates an interface area A_s and contact radius x, as shown in Figure 8. The particle radius is R, so the geometrical relation can be presented as in equation (3).

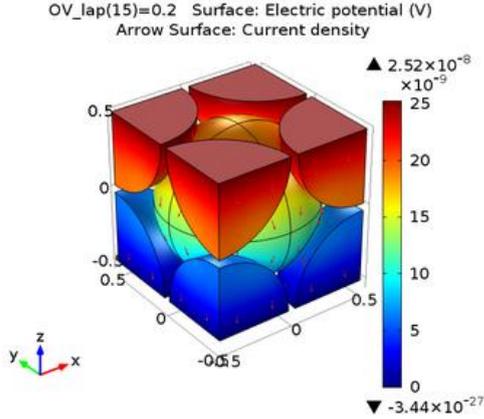$$x^2 + \left(R - \frac{\delta}{2}\right)^2 = R^2 \qquad (3)$$

Figure 7. Representative porous Cu nanoparticle arrange in BCC structure. The overlapping distance between each particle was 0.2 of the particle radius.
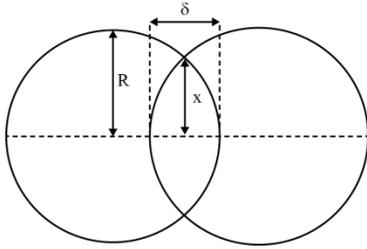

Figure 8. Schematic description of particle overlapping parameters.

To small δ, a simple model of resistance in series was used. The whole resistance Ω can be simplified as below, assumed that $\delta \ll R$ and $x \ll R$:

$$\Omega = \Omega_{particle} + \Omega_{contact} \approx \rho\frac{1}{\pi x} \qquad (4)$$

Then the resistivity can be derived as following:

$$\rho_{eq} = \Omega\frac{A}{L} \approx \Omega\, L \approx 2\Omega R \approx \frac{2\rho}{\pi}\frac{R}{x} \qquad (5)$$

$$\sigma_{eq} \approx \frac{\pi}{2\rho}\frac{x}{R} \qquad (6)$$

Where ρ_{eq} is equivalent resistivity and σ_{eq} is equivalent conductivity. It can be seen that equivalent conductivity σ_{eq} is linearly dependent with x/R.

As shown in Figure 9(b), unit cell equivalent conductivity, σ_{eq}, presents good linear relation with x/R, which agrees with

Equation (6). The slope of linear fit, in the range of 0% to 60% relative radius, is $9.00 \times 10^7\, S \cdot m^{-1}$. Hence the corresponding resistivity is 1.74 µΩ·cm. This is close to the resistivity of bulk copper, 1.68 µΩ·cm.
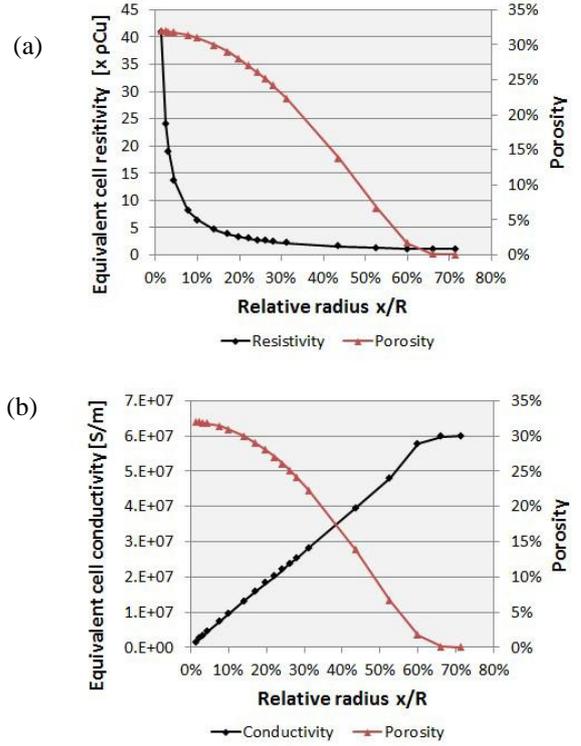

Figure 9. Simulation results of (a) equivalent electrical resistivity, (b) equivalent electrical conductivity with different relative radius (overlapping between particles).

IV. CONCLUSION AND OUTLOOK

In summary, a novel lithographic defined stencil printing method as developed to pattern Cu nanoparticle paste. The metallic nanoparticle paste has a low sintering temperature of 260 ℃. The paste was used to fabricate 3D interconnect structures for wafer to wafer bonding. A low electrical resistivity at 7.84 ± 1.45 µΩ·cm is obtained after sintering at 260 ℃ for 10 min, in 700 mBar forming gas environment. The result indicates that reducing sintering environment can improve electrical properties. The effects of porosity of sintered Cu nanoparticle paste on electrical conductivity was investigated by finite element simulation. The nanoparticles were placed in a simple BCC structure unit cell. This model was used to evaluate the equivalent unit cell conductivity under different particle packing density. The simulation of copper nanoparticle porosity presented a linear relation between the overlapping ratio and electrical conductivity. It suggests that this BCC unit cell can be used as a representative model to study porosity effect on electrical resistivity.

In future work, we will investigate automated distribution/spreading methods of copper nanoparticle paste, that have higher accuracy and repeatability. In addition, simulations with more complex and realistic models will be studied, as well as the effects of the sintering process on the material properties.

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