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A Fully Integrated Bluetooth Low-Energy Transmitter in 28 nm CMOS With 36% System Efficiency at 3 dBm

Masoud Babaie, *Student Member, IEEE*, Feng-Wei Kuo, Huan-Neng Ron Chen, Lan-Chou Cho, Chewn-Pu Jou, Fu-Lung Hsueh, Mina Shahmohammadi, *Student Member, IEEE*, and Robert Bogdan Staszewski, *Fellow, IEEE*

***Abstract*—We propose a new transmitter architecture for ultra-low power radios in which the most energy-hungry RF circuits operate at a supply just above a threshold voltage of CMOS transistors. An all-digital PLL employs a digitally controlled oscillator with switching current sources to reduce supply voltage and power without sacrificing its startup margin. It also reduces 1/f noise and supply pushing, thus allowing the ADPLL, after settling, to reduce its sampling rate or shut it off entirely during a direct DCO data modulation. The switching power amplifier integrates its matching network while operating in class-E/F_2 to maximally enhance its efficiency at low voltage. The transmitter is realized in 28 nm digital CMOS and satisfies all metal density and other manufacturing rules. It consumes 3.6 mW/5.5 mW while delivering 0 dBm/3 dBm RF power in Bluetooth Low-Energy mode.**

***Index Terms*—All-digital PLL, Bluetooth Low-Energy, class-E/F_2 power amplifier, Internet of Things (IoT), low-power transmitter, low-voltage oscillator, switching current-source oscillator.**

I. Introduction

ULTRA-LOW-POWER (ULP) radios underpin short-range communications for wireless Internet of Things (IoT) [1]–[12]. Yet, the IoT system lifetime still tends to be severely limited by a transmitter power consumption and available battery technology. Fig. 1 shows a system lifetime for various battery choices as a function of current consumption. State-of-the-art Bluetooth Low Energy (BLE) radios [1]–[3] consume $\sim$7 mW and thus can *continuously* operate no more than 40 hours on a single SR44 battery, which has comparable dimensions to the radio module. This triggers inconvenient battery replacements at least every few months, which limits their marketing attractiveness. The lifetime could be easily extended with larger batteries but that comes at a price of increased weight and size and it is clearly against the vision of IoT miniaturization.

Energy harvesting from the surrounding environment can enable and further spur the IoT applications by significantly extending their lifetime. Solar cells offer the highest harvested power per area, as can be gathered from Fig. 2 [10], [13]. However, they provide much lower voltages (0.25–0.75 V) than the nominal deep-nanoscale CMOS supply of $\sim$1 V. Hence, boost converters are typically used to bring the supply level up to the required $\sim$1V. As evident from Table I, the relatively poor efficiency ($\leq 80\%$) of state-of-the-art boost converters wastes the harvested energy, thus worsening the system-level efficiency, in addition to increasing the hardware complexity coupled with issues of switching ripples. Consequently, it would be highly desirable for the ULP radios to operate *directly* from the harvested voltage.

In this paper, several new system and circuit techniques are exploited to enhance the ULP transmitter efficiency: First, the most energy-hungry circuitry, such as a digitally controlled oscillator (DCO) and an output stage of a power amplifier (PA), can operate directly at the low voltage of harvesters. Second, a new switching current-source oscillator reduces power and supply voltage without compromising the robustness of its start-up. Third, thanks to the low wander of the DCO, digital power consumption of the rest of all-digital PLL (ADPLL) is saved by scaling the rate of a sampling clock to the point of its complete stillness. Last, a fully integrated differential class-E/F_2 switching PA is utilized to optimize high power added efficiency (PAE) at low output power of 0–3 dBm.

The paper is organized as follows. Section II introduces a new RF oscillator topology that is suitable for ultra-low voltage/power applications. The tradeoffs between the output power, matching network insertion loss, drain and power-added efficiency of the class-E/F_2 PA are investigated in Section III. The ADPLL-based TX architecture is discussed in Section IV. Section V experimentally verifies our approach.

II. Switching Current-Source DCO

RF system designers shall be able to better optimize a power budget of various IoT radio blocks by understanding

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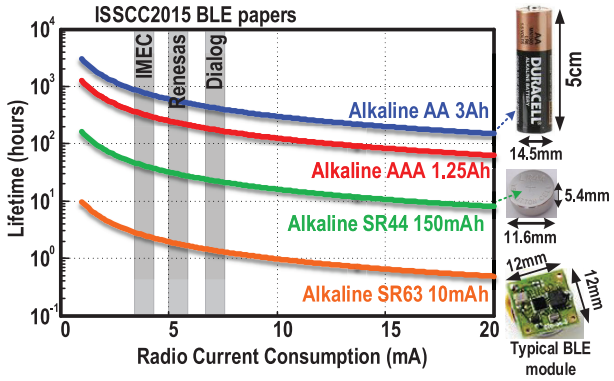

Fig. 1. BLE system lifetime versus radio current consumption for various battery types.

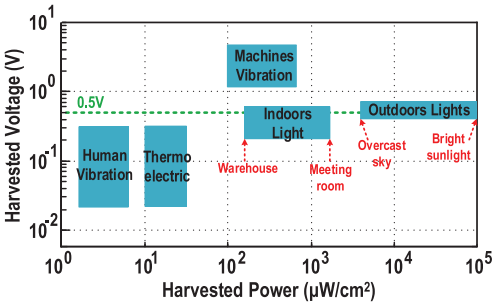

Fig. 2. Delivered voltage and power density for various harvester types.

TABLE I
PERFORMANCE SUMMARY OF STATE-OF-THE-ART BOOST CONVERTERS

	[14] ISSCC'12	[15] ISSCC'14	[16] ISSCC'15
Technology	N/A	65nm CMOS	0.18μm CMOS
Input voltage range	0.1–2.9 V	0.15–0.5 V	0.45–3 V
Output voltage range	3 V	0.5–0.6 V	3.3 V
Efficiency @V_{in}=0.5V	$\leq$ 80%	$\leq$ 72.5%	$\leq$ 78.5%

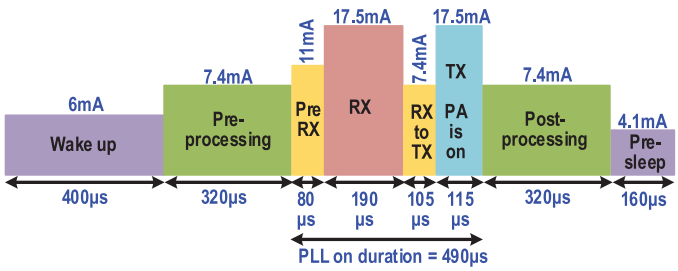

Fig. 3. Power consumption breakdown of a Texas Instruments CC2541 BLE device during a single connection event.

the characteristics of a BLE transient power profile. Fig. 3 illustrates such an example of a commercial CC2541 IC from Texas Instruments during a single connection event [17] and could be used as our rough guide. We infer that the frequency synthesizer activity is at least 3x longer than that of a PA. Furthermore, the PLL power consumption is generally known to be merely 3–4x lower than that of the PA at the maximum BLE output power of 1 mW. This ratio gets even lower as the TX output power reduces. By considering both scenarios, the energy consumption of the frequency synthesizer could even be larger than that of the PA. Consequently, RF oscillators, as one of the BLE transceiver's most power-hungry circuitry, must be very power efficient and preferably operate directly at the energy harvester output [18].

A. Oscillator Power Consumption Tradeoffs

Phase noise (PN) and figure of merit (FoM) of any RF oscillator at an offset frequency $\Delta\omega$ from its resonating frequency $\omega_0 = 2\pi f_0$ can be expressed by

$$\mathcal{L}(\Delta\omega) = 10\log_{10}\left(\frac{KT}{2Q_t^2\alpha_I\alpha_V P_{DC}}\cdot F\cdot\left(\frac{\omega_0}{\Delta\omega}\right)^2\right)$$

and

$$\text{FoM} = 10\log_{10}\left(\frac{10^3 KT}{2Q_t^2\alpha_I\alpha_V}\cdot F\right) \tag{1}$$

where K is the Boltzmann's constant, T is the absolute temperature, Q_t is the LC-tank quality factor; α_I is the current efficiency, defined as a ratio of the fundamental current harmonic I_{ω_0} over the oscillator DC current I_{DC}; and α_V is the voltage efficiency, defined as a ratio of the single-ended oscillation amplitude, $V_{osc}/2$, over the supply voltage V_{DD} [21]–[25]. F is the oscillator's effective noise factor and estimated by

$$F = \frac{R_{in}}{2KT}\cdot\sum_i\frac{1}{2\pi}\int_0^{2\pi}\overline{i_{n,i}^2(\phi)}\cdot\Gamma_i^2(\phi)d\phi \tag{2}$$

where $\phi = \omega_0 t$, $\overline{i_{n,i}^2(\phi)}$ is the white current noise power density of the ith noise source, Γ_i is its relevant ISF function from the corresponding ith device noise [26]. Finally, R_{in} is an equivalent differential input parallel resistance of the tank's losses. The oscillator I_{DC} may be estimated by one of the following equations:

$$I_{DC} = \frac{I_{\omega_0}}{\alpha_I}\xrightarrow{I_{\omega_0}=\frac{V_{osc}}{R_{in}}} I_{DC} = \frac{V_{osc}}{R_{in}}\cdot\frac{1}{\alpha_I}\xrightarrow{V_{osc}=2\alpha_V V_{DD}}$$

$$I_{DC} = \frac{2V_{DD}}{R_{in}}\cdot\frac{\alpha_V}{\alpha_I}. \tag{3}$$

As a result, the RF oscillator's P_{DC} is derived by

$$P_{DC} = \frac{2V_{DD}^2}{R_{in}}\cdot\frac{\alpha_V}{\alpha_I}. \tag{4}$$

By considering the BLE blocking profile in [19], the oscillator's PN shall be better than -105 dBc/Hz at $\Delta f = 3$ MHz offset from a $f_0 = 2.45$ GHz carrier [6], [9]. Hence, the PN requirements are quite trivial for IoT applications[1] and can be easily met by LC oscillators as long as Barkhausen start-up criteria are satisfied over process, voltage and temperature (PVT) variations.[2] Consequently, maximally reducing the oscillator's power consumption, P_{DC}, at a low V_{DD} is the ultimate goal in

[1]For a traditional LC oscillator with $\alpha_I = 1.2$, $\alpha_V = 0.4$, $F = 2.4$, and by assuming $Q_t = 10$, and $V_{DD} = 1$ V, BLE PN requirements is satisfied with just $P_{DC} \geq 2\mu$W, which corresponds to $R_{in} \leq 300$ kΩ. Obviously, realizing such a large R_{in} is not feasible in CMOS technology.

[2]Ring oscillators can also satisfy such a relaxed PN requirement. However, they consume much higher power than LC oscillators at $f_0 \geq 1$ GHz, [20].

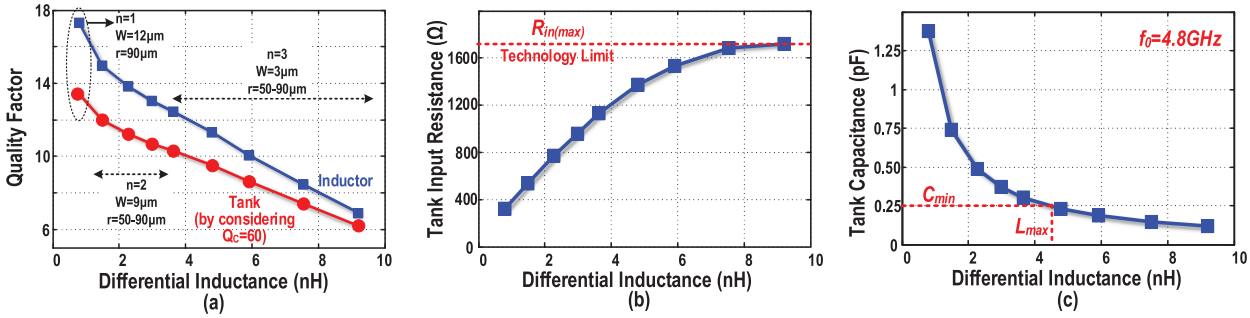

Fig. 4. Dependency of various inductor parameters in 28 nm LP CMOS across inductance value: (a) inductor and tank Q-factor; (b) equivalent differential input resistance of the tank; and (c) required tank capacitance at 4.8 GHz resonance. Note that at this point the inductors are without dummy metal fills.

IoT applications. Eq. (4) indicates that the minimum achievable P_{DC} can be expressed in terms of a set of *optimization* parameters, such as R_{in}, and a set of *topology*-dependent parameters, such as minimum V_{DD}, α_V and α_I.

Lower P_{DC} is typically achieved by scaling up $R_{in} = L_p\omega_0 Q_t$ simply via a large multi-turn inductor, as in [27]. For example, while maintaining a constant Q_t, doubling L_p would theoretically double R_{in}, which would reduce P_{DC} by half but with a 3 dB PN degradation. However, at some point, that tradeoff stops due to a dramatic drop in the inductor's self-resonant frequency and Q-factor. Fig. 4(a) shows the simulated Q-factor of several multi-turn inductors in TSMC 28 nm CMOS versus their inductance. As the inductor enlarges, the magnetic and capacitive coupling to the low-resistivity substrate increases, such that the tank Q-factor drops almost linearly with L_p. As evident from Fig. 4(b), this constraint sets an upper limit on R_{in}, which is chiefly a function of the technology node. Parasitic capacitance of inductor windings, gm-devices, switchable capacitors and oscillator routings determines a minimum floor of the tank's capacitance, which appears to be $\sim$250 fF at $f_0 = 4.8$ GHz. It puts another restriction on L_p and $R_{in(max)}$ to $\sim$4.5 nH and $\sim$1.3 $k\Omega$ and sets a lower limit on P_{DC} of each oscillator structure. Under this condition, the tank's Q-factor drops to ≤ 9. This explains the poor FoM of RF oscillators in modern BLE transceivers [1]–[3].

The topology-dependent parameters also play an important role in trying to reduce P_{DC}. Eq. (4) favors structures that offer higher α_I or can sustain oscillation with smaller V_{DD} and α_V. On the other hand, $\alpha_V \cdot \alpha_I$ should be maximized to avoid any penalty on FoM [22], [28], as evident from (1). Consequently, to efficiently reduce P_{DC} without disproportionately worsening the FoM, it is desired to employ structures with a higher α_I and a lower minimum V_{DD}. To get a better insight, Fig. 5 shows such effects for the traditional cross-coupled NMOS-only (OSC_N) and complementary push-pull (OSC_{NP}) structures [30], [31]. Due to the less stacking of transistors, the $V_{DD,min}$ of OSC_N can go 40% lower than in OSC_{NP}. However, α_I of OSC_{NP} is doubled due to the switching of tank current direction every half period. Its oscillation swing, and thus α_V, is also 50% smaller. Hence, OSC_{NP} offers $\sim 3\times$ lower α_V/α_I. However, both structures demonstrate similar $\alpha_V \cdot \alpha_I$ product [32]. Consequently, each of them has its own set of advantages and drawbacks such that their minimum achievable P_{DC} and FoM are almost identical, as shown in Table II. Note that applying a tail filtering technique to a class-B oscillator increases its α_V [22], [33], which is in line with the FoM optimization but against the P_{DC} reduction, as evident from (1) and (4). Furthermore, while maintaining the same R_{in}, a class-F_3 operation does not reduce P_{DC} of traditional oscillators, since its minimum V_{DD}, α_V and α_I are identical to OSC_N [24].

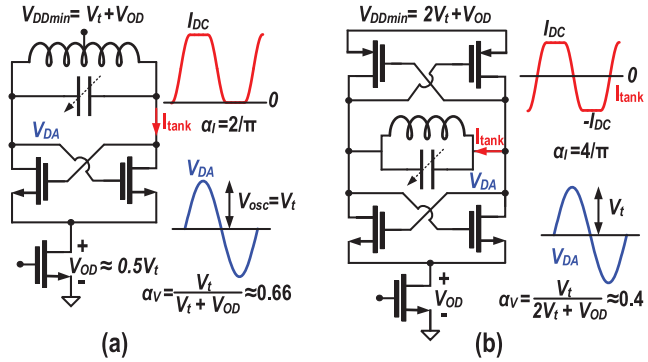

Fig. 5. $V_{DD,min}$, α_I and α_V parameters for: (a) cross-coupled NMOS; and (b) complementary push-pull oscillators.

A push-pull class-C oscillator appears as an excellent choice for ULP applications due to its largest α_I and smallest α_V [34], as per Table II. However, it needs an additional complex biasing circuitry (e.g., an opamp) to guarantee the proper oscillator start-up and to keep the transistors in saturation during the on-state. There are also strong mutual tradeoffs between the biasing circuit's P_{DC}, oscillator's amplitude stability and PN, much intensified in ULP applications where the tank capacitance tends to be smaller [35]. As a consequence, the biasing circuitry can end up consuming comparable power as the ULP oscillator itself. On the other hand, V_{DD} of class-D oscillators can go below a threshold voltage, V_t. However, due to hard switching of core transistors, its α_V and α_I are respectively higher and lower than other structures [36], as shown in Table II. According to (4), this trend is against the P_{DC} reduction. Consequently, the current oscillator structures have issues with reaching simultaneous ultra-low power *and* voltage operation.

In this work, we propose to convert the fixed current-source of the traditional low-voltage NMOS topology into a structure with alternating current sources such that the tank current direction can change every half-period. Consequently,

TABLE II
MINIMUM P_{DC} FOR DIFFERENT RF OSCILLATOR TOPOLOGIES

Topology	$V_{DD,min}$†	α_V‡	α_I*	P_{DCmin}	$\alpha_V.\alpha_I$
OSC_N	$V_t+V_{OD}\approx1.5V_t$	0.66	$2/\pi$	$4.66\,V_t^2/R_{in}$	0.42
OSC_{NP}	$2V_t+V_{OD}\approx2.5V_t$	0.4	$4/\pi$	$3.92\,V_t^2/R_{in}$	0.51
OSC_{NP} with tail filter	$2V_t+V_{OD}\approx2.5V_t$	0.63	$4/\pi$	$6.2\,V_t^2/R_{in}$	0.8
Class-C_{NP}	$2V_t+V_{OD}\approx2.5V_t$	0.25	2	$0.15mW+1.56\,V_t^2/R_{in}$	0.5
Class-D	$\approx V_t$	1.635	0.5	$6.54\,V_t^2/R_{in}$	0.82
Class-F_3	$V_t+V_{OD}\approx1.5V_t$	0.66	$2/\pi$	$4.66\,V_t^2/R_{in}$	0.42
This work	$V_t+V_{OD}\approx1.5V_t$	0.33	$4/\pi$	$1.2\,V_t^2/R_{in}$	0.42

† by considering $V_{OD}=0.5V_t$ for the current source,
‡ at the minimum V_{DD},
* ideal value.

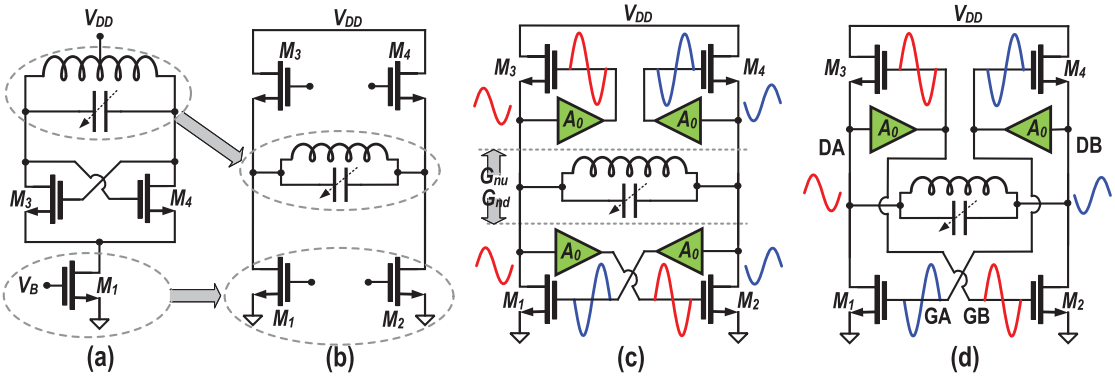

Fig. 6. Evolution towards the switching current-source oscillator.

the benefits of low supply of the OSC_N topology and higher α_I of OSC_{NP} structure are combined to reduce power consumption further than practically possible in the traditional oscillators.

B. Switching Current-Source Oscillator

Fig. 6 shows an evolution towards the switching current-source oscillator. The OSC_N topology is chosen as a starting point due to its low-V_{DD} capability. To reduce P_{DC} further, it is desired to switch the direction of the LC-tank current in each half period, which will double α_I. Consequently, we propose to split the fixed current source M_1 in Fig. 6(a) into two switchable "current sources" M_1 and M_2, as suggested in Fig. 6(b). This allows for the tank to be disconnected from the V_{DD} feed and be moved in-between the upper and lower NMOS transistor pairs to give rise to an H-bridge configuration. In the next step, the passive voltage gain blocks, A_0, are added to the NMOS gates, as shown in Fig. 6(c). Both upper and lower NMOS pairs should each individually demonstrate *synchronized* positive feedback to realize the switching of the tank current direction. The "master" positive feedback enforces the differential-mode operation and is realized by the lower-pair transistors configured in a conventional cross-coupled manner. Since the lower pair is *voltage-biased*, its negative conductance seen by the tank may be estimated as $G_{nd}=-0.25\cdot A_0[g_{m1}(\phi)+g_{m2}(\phi)]$.

On the upper side, the differential-mode oscillation of the tank is *reinforced* by the $M_{3,4}$ devices which realize the second positive feedback.[3] The negative conductance seen by the tank into the upper pair can be calculated as $G_{nu}=-0.25\cdot(A_0-1)[g_{m3}(\phi)+g_{m4}(\phi)]$, which clearly indicates that the voltage gain block is necessary and A_0 must be safely larger than 1 to be able to present a negative conductance to the tank, thus enabling the H-bridge switching. By merging the redundant voltage gain blocks,[4] the proposed switching current-source oscillator is arrived at in Fig. 6(d).

Figs. 7–8 illustrate the proposed oscillator schematic and simulated waveforms indicating various operational regions of M_{1-4} transistors. The two-port resonator consists of a step-up 1:2 transformer and tuning capacitors, $C_{1,2}$, at its primary and secondary windings. The current-source transistors $M_{1,2}$ set the oscillator's DC current. Along with M_{3-4}, they play a vital role of switching the tank current direction. As can be gathered from Fig. 8, G_B oscillation voltage is high within the first half-period. Hence, only M_2 and M_3 are on and the current flows from the left to right side of the tank. However, M_1 and M_4 are turned on for the second half-period and the tank's current direction is reversed, thus doubling α_I to $4/\pi$.

V_{DD} of the proposed oscillator can be as low as $V_{OD1}+V_{OD3}\approx V_t$, which is extremely small given the capability of switching the tank current direction. Note that the oscillation

[3]It should be noted that the "master/slave" view is mainly valid from a small-signal standpoint. Both are equally important when considering the large-signal switching operation.

[4]The tank with an implicit voltage gain can be realized by using a capacitive divider, autotransformer or step-up transformer. The transformer-based tank is chosen in this work due to its simplicity.

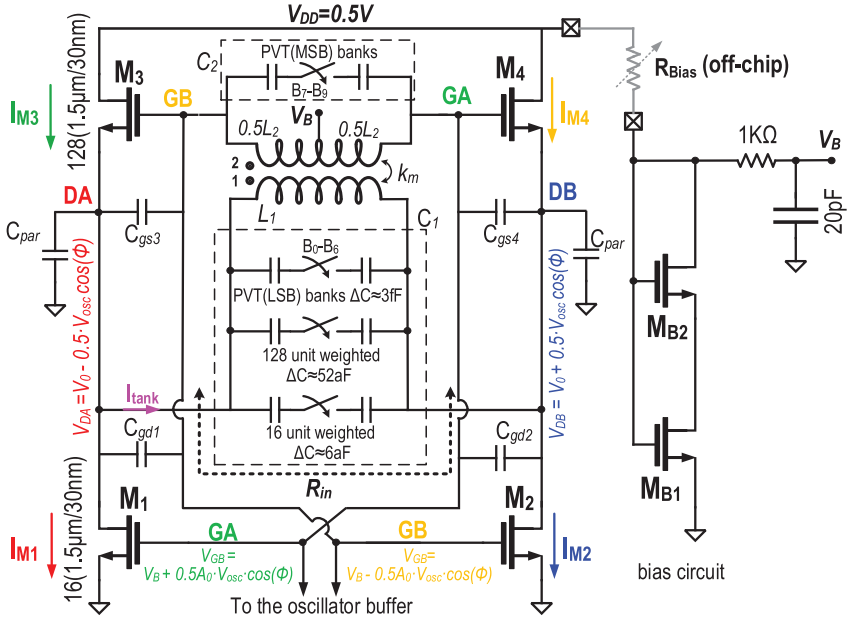

Fig. 7. Schematic of the proposed switching current-source oscillator.

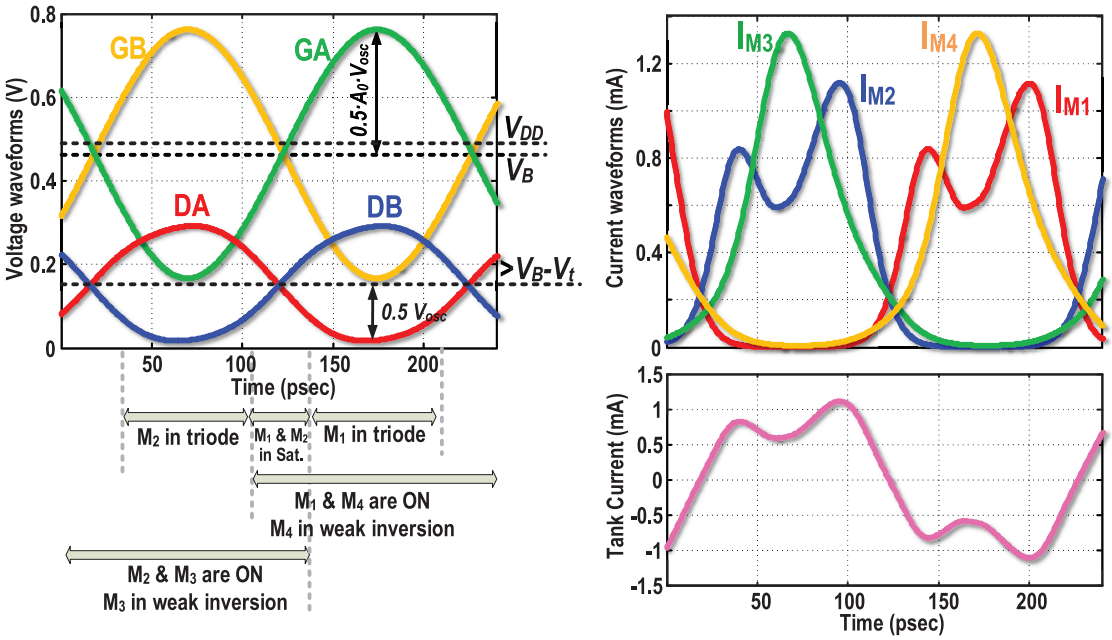

Fig. 8. Simulated waveforms and various operational regions of M_{1-4} transistors across the oscillation period.

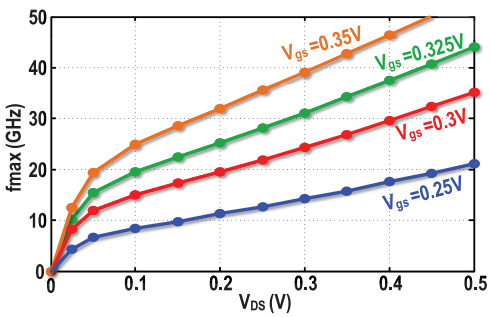

Fig. 9. f_{max} of low-V_t 28 nm transistor versus V_{DS} for different V_{GS}.

swing cannot exceed $V_{OD1,2}$ at DA/DB nodes and is chosen 150 mV to satisfy the PN requirements with a margin. However, it is the bias voltage $V_B \approx V_{OD1} + V_{gs3}$ that limits the minimum supply. Hence, $M_{3,4}$ should work in weak-inversion keeping $V_{gs3} < V_t$ to achieve lower $V_{DD,min}$. However, the transistor's cut-off frequency f_{max} drops dramatically in the subthreshold operation. Note that f_{max} should be at least 3–4× higher than the operating frequency $f_0 = 4.8$ GHz to guarantee the oscillator start-up over PVT variations. This constraint limits $V_{gs3} \approx 0.3$ V for $V_{OD3} \approx 150$ mV, as inspected from Fig. 9. Consequently, even by considering the tougher V_B requirement,

the proposed structure can operate at V_{DD} as low as 0.5 V, on par with OSC_N.

Such low V_{DD} and swing could easily lead to start-up problems in the traditional oscillators. This could certainly increase power consumption, P_{buf}, of the following buffer, which would require more gain to provide a rail-to-rail swing to output a clock to a following ÷2 divider. Fortunately, the transformer gain enhances the oscillation swing at $\mathrm{M}_{1,2}$ gates to even beyond V_{DD}, thus guaranteeing the oscillator start-up and reduction of P_{buf}. Consequently, the oscillator buffer is connected to the secondary winding.

As evident from Fig. 8, $\mathrm{M}_{3,4}$ transistors operate in a class-C manner as in a Colpitts oscillator, meaning that they deliver somewhat narrow-and-tall current pulses. However, their conduction angle is quite wide, $\sim\pi$, due to the low overdrive voltage in the subthreshold operation. On the other hand, $\mathrm{M}_{1,2}$ operate in a class-B manner like cross-coupled oscillators, meaning that they deliver square-shape current pulses. Hence, the shapes of drain currents are quite different for the lower and upper pairs. However, their fundamental components demonstrate the same amplitude and phase to realize the constructive oscillation voltage across the tank. The higher drain harmonics obviously show different characteristics. However, they are filtered out by the tank's selectivity characteristic. Note that the current through a transistor of the upper pair will have two paths to ground: through the corresponding transistor of the lower pair and through the single-ended capacitors. Consequently, the single-ended capacitors sink the higher current harmonics of $\mathrm{M}_{3,4}$ transistors.

C. Thermal Noise Upconversion in the Proposed Oscillator

To calculate a closed-form PN equation, the proposed oscillator model is simplified in Fig. 10. At the resonant frequency, the transformer-based tank can be modeled by an equivalent LC-tank of elements L_{eq}, C_{eq} and R_{in}.[5] On the other hand, M_{1-4} transistors, together with the passive voltage gain of the transformer, are decomposed into two nonlinear time-variant conductances. The first one is always negative to compensate for the circuit losses:[6] $G_n(\phi) = G_{nd}(\phi) + G_{nu}(\phi) = -0.25\,[A_0(g_{m1}(\phi) + g_{m2}(\phi)) + (A_0 - 1)\cdot(g_{m3}(\phi) + g_{m4}(\phi))]$. The second one is always positive, $G_{ds}(\phi) = 0.25\sum g_{ds,1:4}(\phi)$, modeling the equivalent channel conductance of M_{1-4}. The noise sources of M_{1-4} are uncorrelated and always find a path through the tank and via C_{par} to ground. To get a better insight, the equivalent noise due to channel conductance, $\overline{i^2_{n,Gds}}(\phi) = 4KTG_{ds}(\phi)$, and due to transconductance gain, $\overline{i^2_{n,Gm}}(\phi) = KT(\gamma_1(g_{m1}(\phi) + g_{m2}(\phi)) + \gamma_4(g_{m3}(\phi) + g_{m4}(\phi)))$, of M_{1-4} are modeled separately here.

It is well known that the relevant impulse sensitivity function of noise sources associated with a sinusoidal waveform oscillator, $V_{osc}\cdot\cos\phi$, may be estimated by $\Gamma = \sin(\phi)$ [26], [30]. By exploiting (2), the effective noise factor due to resistive losses of the oscillator becomes

$$\begin{aligned} F_{loss} &= \frac{R_{in}}{2KT}\cdot\frac{1}{2\pi}\int_0^{2\pi} 4KT\left(\frac{1}{R_{in}} + G_{ds}(\phi)\right)\cdot\sin^2(\phi)\cdot d\phi \\ &= \frac{1}{2\pi}\int_0^{2\pi} 2\sin^2(\phi)\cdot d\phi + R_{in}\left(\frac{1}{2\pi}\int_0^{2\pi} G_{ds}(\phi)\cdot d\phi\right. \\ &\quad \left. - \frac{1}{2\pi}\int_0^{2\pi} G_{ds}(\phi)\cdot\cos(2\phi)\cdot d\phi\right) \rightarrow \\ F_{loss} &= 1 + R_{in}\left(G_{DS}[0] - G_{DS}[2]\right) \\ &= 1 + R_{in}G_{DSEF} = 1 + \frac{R_{in}}{2}\left(G_{DS1EF} + G_{DS4EF}\right). \end{aligned} \tag{5}$$

where $G_{DS}[k]$ describes the k_{th} Fourier coefficient of the instantaneous $G_{ds}(\phi)$. To get better insight, different components of the above equation are graphically illustrated in Fig. 11(a)–(c). The literature interprets $R_{in}G_{DSEF}$ term in (5) as the tank loading effect.[7] In our design, M_1 and M_2 alternatively enter the triode region for part of the oscillation period and exhibit a large channel conductance. As shown in Fig. 11(a), simulated $0.5R_{in}G_{DS1EF}$ can be as large as 0.6 for the lower pair transistors. However, $\mathrm{M}_{3,4}$ work only in saturation and demonstrate small channel conductance for their entire on-state operation, as evident from Fig. 11(a). Hence, the simulated value of $0.5R_{in}G_{DS4EF}$ is as low as $\sim$0.17. Note that both NMOS and PMOS pairs of the OSC_{NP} structure simultaneously enter the triode region for part of the oscillation period and load the tank from both sides. In the proposed structure, however, only one side of the tank is connected to the AC ground when either $\mathrm{M}_1/\mathrm{M}_2$ is in triode while the other side sees high impedance. Hence, this structure at least preserves the charge of differential capacitors over the entire oscillation period. Consequently, compared to the traditional oscillators, the tank loading effect is somewhat reduced here.

To sustain the oscillation, the average power dissipated in the oscillator's resistive loss, $R_{in} + 1/G_{ds}(\phi)$, must equal the average power delivered by the negative resistance, $G_n(\phi)$, of the active devices. As proved in [37], this energy conservation requirement results in

$$\begin{aligned} G_{NEF} = G_{NDEF} + G_{NUEF} &= -\left(\frac{1}{R_{in}} + G_{DSEF}\right) \rightarrow \frac{A_0}{4} \\ &\quad \times (G_{M1EF} + G_{M2EF}) + \frac{(A_0 - 1)}{4} \\ &\quad \times (G_{M3EF} + G_{M4EF}) = \frac{1 + R_{in}G_{DSEF}}{R_{in}}. \end{aligned} \tag{6}$$

As with OSC_{NP} [31], [37], both upper and lower feedback mechanisms should exhibit almost identical, i.e., $\sim$50%, contribution to the compensation of oscillator losses. Consequently,

$$\begin{aligned} G_{M1EF} + G_{M2EF} &= \frac{2}{A_0}\cdot\frac{1 + R_{in}G_{DSEF}}{R_{in}}, \text{ and,} \\ G_{M3EF} + G_{M4EF} &= \frac{2}{A_0 - 1}\cdot\frac{1 + R_{in}G_{DSEF}}{R_{in}} \end{aligned} \tag{7}$$

[5]The interested reader is directed to [41] for accurate closed-form equations of L_{eq}, C_{eq} and R_{in}.

[6]Calculated following the method in [37].

[7]The interested reader is directed to Appendix A for accurate closed-form equations of G_{DS1EF} and G_{DS4EF}.

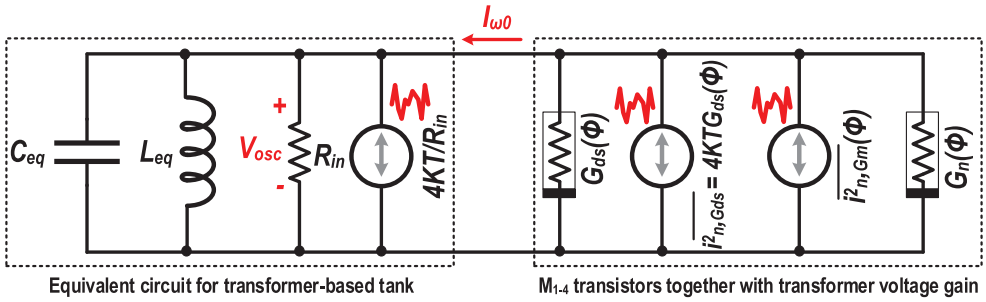

Fig. 10. Generic noise circuit model of the proposed oscillator.

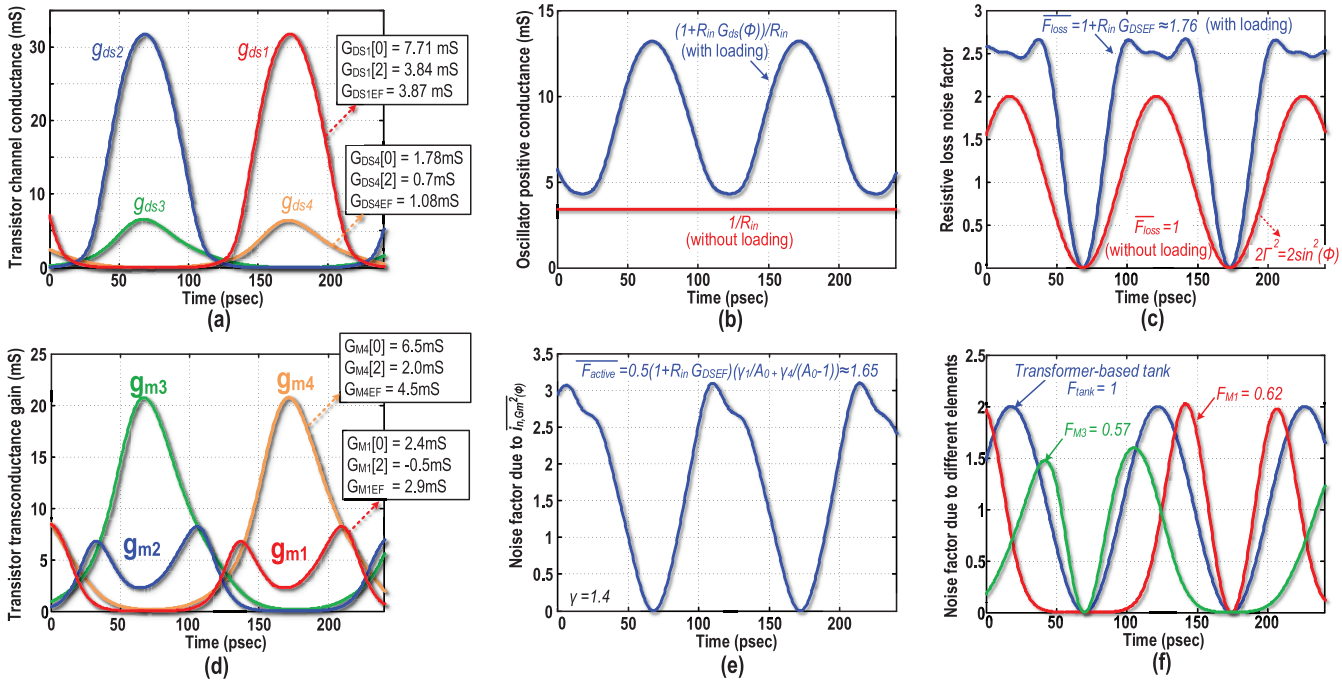

Fig. 11. Circuit-to-phase-noise conversion across the oscillation period in the switching current-source oscillator. Simulated (a) channel conductance of M_{1-4}; (b) conductance due to resistive losses; (c) noise factor due to losses; (d) transconductance of M_{1-4}; (e) effective noise factor due to $\overline{i^2_{n,Gm}}(\phi)$; (f) effective noise factors due to different oscillator's components.

By exploiting (2), the effective noise factor due to transconductance gain is calculated as

$$F_{active} = \frac{R_{in}}{2KT} \cdot \frac{1}{2\pi} \int_0^{2\pi} \overline{i^2_{Gm}(\phi)} \cdot \sin^2(\phi) \cdot d\phi$$
$$= R_{in} \left(\frac{1}{2\pi} \int_0^{2\pi} \frac{1}{4} \sum_{i=1}^{4} \gamma_i g_{m,i}(\phi) d\phi \right.$$
$$\left. - \frac{1}{2\pi} \int_0^{2\pi} \frac{1}{4} \sum_{i=1}^{4} \gamma_i g_{m,i}(\phi) \cdot \cos(2\phi) d\phi \right) \rightarrow$$
$$F_{active} = \frac{R_{in}}{4} \left[\gamma_1 \left(G_{M1EF} + G_{M2EF} \right) \right.$$
$$\left. + \gamma_4 \left(G_{M3EF} + G_{M4EF} \right) \right] \quad (8)$$

To get better insight, different components of above equation are graphically illustrated in Fig. 11(d)–(e). By merging (7) into (8), we have

$$F_{active} = (1 + R_{in} G_{DSEF}) \cdot \left(\frac{\gamma_1}{2A_0} + \frac{\gamma_4}{2(A_0 - 1)} \right) \quad (9)$$

As discussed in conjunction with Fig. 6(c), the transformer's passive voltage gain, A_0, covers a significant part of the required loop gain of the lower positive feedback. Hence, the lower-pair transistors have to compensate only $1/(2A_0)$ of the circuit losses. For the upper positive feedback however, A_0 covers a smaller part of the required loop gain. Consequently, the upper transistors should work harder and compensate $1/(2(A_0 - 1))$ of the oscillator loss. Consequently, as (9) indicates, the G_M noise contribution by the lower pair is smaller. However, its effect on F_{loss} is larger such that both pairs demonstrate more or less the same contribution to the oscillator PN [see Fig. 11(f)]. Finally, the total oscillator effective noise factor is

$$F = F_{loss} + F_{active}$$
$$= (1 + R_{in} G_{DSEF}) \cdot \left(1 + \frac{\gamma_1}{2A_0} + \frac{\gamma_4}{2(A_0 - 1)} \right). \quad (10)$$

By considering $\gamma_1 = \gamma_4 = 1.4$ and $A_0 = 2.15$, the noise factor of the proposed oscillator is ~5.3 dB, which is just 1.5 dB

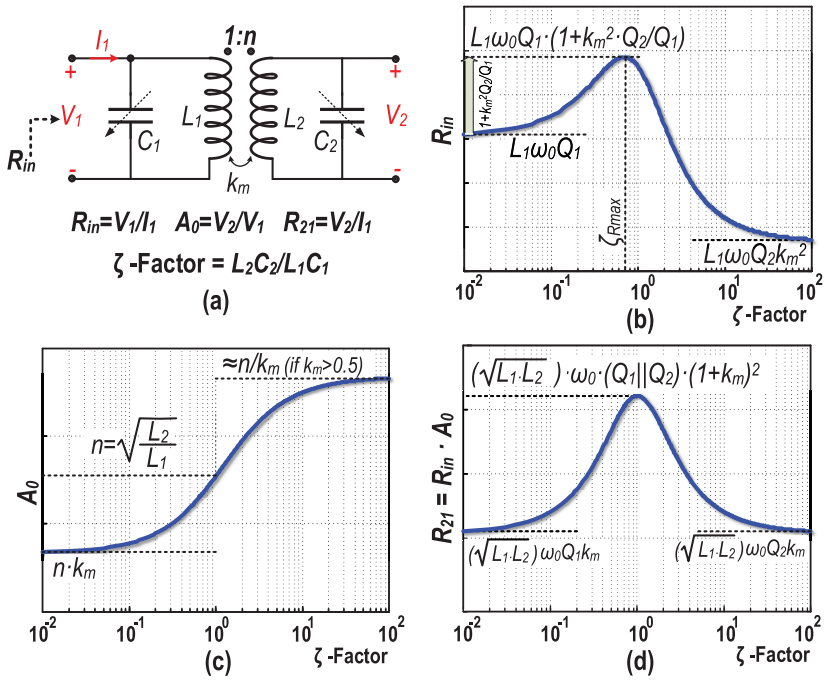

Fig. 12. Transformer-based tank: (a) schematic; (b) input parallel resistance; (c) voltage gain; and (d) R_{21} versus ζ-factor.

higher than the ideal value of $(1+\gamma)$ despite the aforementioned practical issues of designing ultra-low voltage and power oscillators. The phase noise and FoM of the proposed oscillator can be calculated by replacing (10) in (1).

D. 1/f Noise Upconversion in the Proposed Oscillator

Several techniques have been exploited to lower the oscillator's 1/f noise upconversion. First, dynamically switching the bias-setting devices $\mathrm{M}_{1,2}$ will reduce their flicker noise, as also demonstrated in [38]. It also lessens the DC component of their effective ISF [26]. Second, as suggested in [39] and [40], 1/f noise upconversion can be alleviated by realizing an auxiliary resonance at $2\omega_0$ such that the 2nd-harmonic current flows into an equivalent resistance of the tank in order to avoid disturbing the waveform's rise and fall symmetry. Since common-mode signals, e.g., the 2nd harmonic of the drain current, cannot see the tuning capacitance at the transformer's secondary [21], the auxiliary $2\omega_0$ resonance can be realized without die area penalty by adjusting the single-ended capacitance at the transformer's primary [39]. The last source of 1/f noise is $\mathrm{M_{B1}}$ in the biasing circuitry. By utilizing long-channel devices in $\mathrm{M_{B1/B2}}$ biasing, their power consumption becomes negligible. Furthermore, their large WL area generates less 1/f noise. Consequently, based on aforementioned techniques, a lower $1/\mathrm{f}^3$ PN corner is expected than in the traditional oscillators.

E. Optimizing Transformer-Based Tank

The transformer-based tank's input equivalent resistance, R_{in}, and voltage gain, A_0, should be maximized for the best

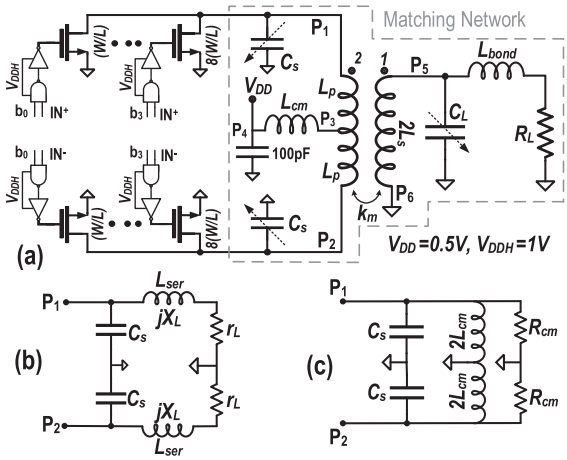

Fig. 13. (a) Schematic of the proposed class-E/F$_2$ PA. Equivalent circuit PA's matching network for (b) differential and (c) common-mode excitations.

system efficiency. They are a strong function of $\zeta{=}L_2C_2/L_1C_1$ [18], [41], as shown in Fig. 12. R_{in} may be estimated by

$$R_{in} = L_1\omega_0 Q_1 \cdot \frac{\left(1-\left(\frac{\omega_0}{\omega_s}\right)^2\left(1-k_m^2\right)\right)\zeta}{-\left(\frac{\omega_0}{\omega_s}\right)^4\left(1+\frac{Q_1}{Q_2}\right)+\left(\frac{\omega_0}{\omega_s}\right)^2\left(1+\frac{Q_1}{Q_2}\zeta\right)} \tag{11}$$

where $\omega_s^2 = 1/L_2C_2$, and Q_1 and Q_2 are respectively the Q-factors of the transformer's primary and secondary windings. It can be shown that R_{in} reaches its maximum when

$$\zeta_{Rmax} = \frac{Q_2}{Q_1}\cdot\left(\frac{Q_2}{Q_1+Q_2}\cdot k_m^2 + \frac{Q_1}{Q_1+Q_2}\right). \tag{12}$$

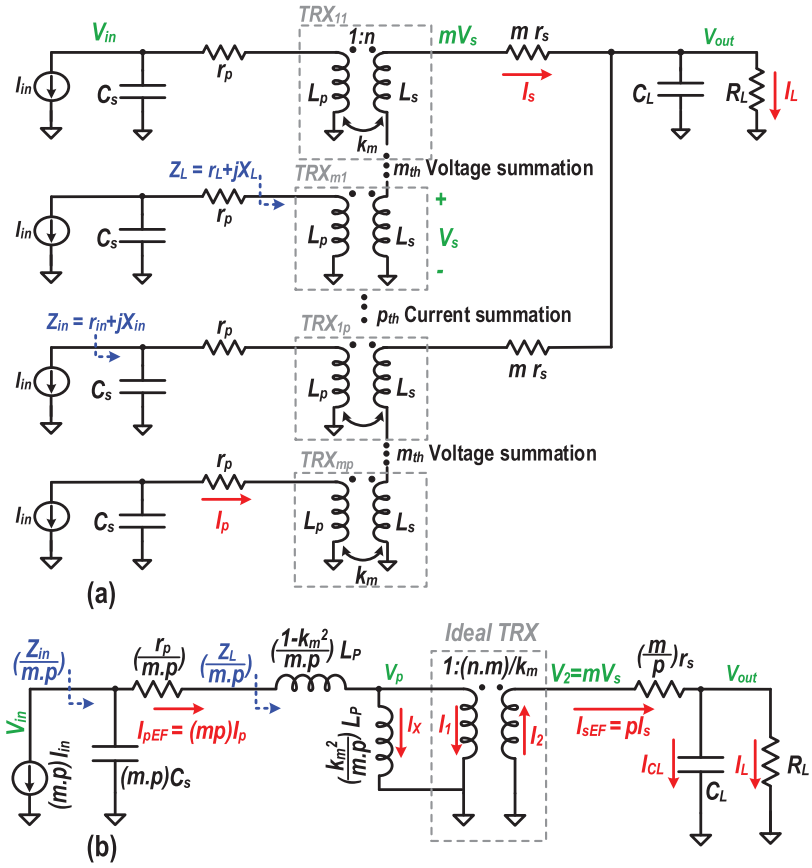

Fig. 14. (a) Transformer-based matching network with m-way voltage and p-way current summation; and (b) its equivalent circuit model.

Note that the tank Q-factor is maximized at different $\zeta = Q_2/Q_1$ [24]. The maximum R_{in} is obtained by inserting (12) into (11):

$$R_{inmax} = L_1\omega_0 Q_1 \cdot \left(1 + k_m^2 \cdot \frac{Q_2}{Q_1}\right). \tag{13}$$

Consequently, the transformer's coupling factor k_m enhances R_{in} by a factor of $\sim (1 + k_m^2)$ at ζ_{Rmax}. For this reason, the switched-capacitor banks are distributed between the transformer's primary and secondary to roughly satisfy (12). For $k_m \geq 0.5$, the voltage gain of the transformer-based tank may be estimated by

$$A_0 = \frac{2k_m n}{1 - \zeta + \sqrt{1 + \zeta^2 + \zeta(4k_m^2 - 2)}}. \tag{14}$$

As shown in Fig. 12(c), A_0 increases with larger ζ. Note that larger R_{in} and A_0 are desired to reduce P_{DC} and P_{buf}, respectively. To consider both scenarios, trans-impedance $R_{21} = R_{in} \cdot A_0$ term is defined and depicted in Fig. 12(d). R_{21} reaches its maximum at $\zeta = 1$ for $Q_1 \approx Q_2$, which is reasonable for monolithic transformers. We also define the maximum of R_{21} as the transformer FoM $= (Q_1 \| Q_2) \cdot (1 + k_m)^2 \cdot \sqrt{L_1 L_2} \cdot \omega_0$. Consequently, the transformer dimensions and winding spacing are chosen to maximize this term.

III. Class-E/F$_2$ Switched-Mode Power Amplifier

The second most energy-hungry block in a BLE transceiver is the PA.[8] Designing a fully integrated PA optimized for low output power ($P_{out} < 3$ dBm) with high power-added efficiency (PAE $> 40\%$) is very challenging, especially when the spurious harmonic level must be below -41 dBm to fulfill the FCC 15.247 regulation. To deliver such a low P_{out} with the highest PAE to the $R_L = 50\ \Omega$ load, the equivalent resistance r_L seen by PA switching transistors must be *scaled up* by the PA's output matching network.

A single-ended (SE) class-D PA generates the lowest P_{out} among various flavors of switched-mode PAs when considering the same V_{DD} and r_L. Hence, the impedance transformation ratio, ITR $= r_L/R_L$, and therefore insertion loss of its matching network, can be theoretically the lowest, making the class-D PA an attractive choice for fully integrated BLE transmitters, as also gathered from [1]–[3]. However, the 2nd-harmonic emission of SE class-D PAs is quite poor and thus an additional feedback structure is needed to adjust the PA's conduction angle to $\sim\pi$ in order to suppress even-order harmonics [1]–[3]. However, that circuitry worsens the system power consumption, die area and complexity. Furthermore, a loaded Q-factor of a class-D series LC matching network $Q_L = L_s\omega_0/R_L$ is quite low ($\sim$1 for L_s as large as 3.5 nH). Hence, its filtering function would not be capable to suppress the 3rd harmonic to

[8]PA is the most power-hungry block in a BLE radio, but it is the second in energy consumption due to its shorter operational cycles–see Fig. 3.

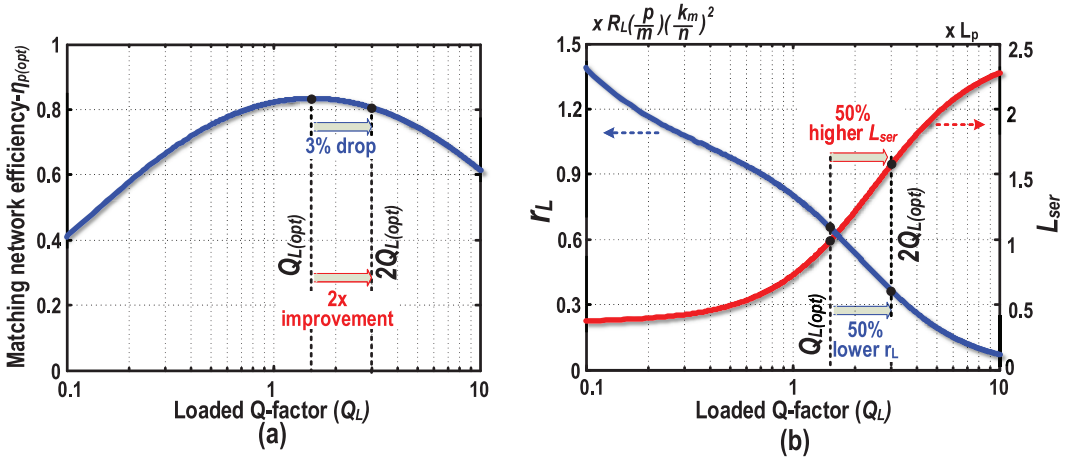

Fig. 15. (a) Maximum possible efficiency, $\eta_{p(opt)}$; and (b) real and imaginary parts of the equivalent impedance, Z_L, seen at the transformer's primary winding versus Q_L while satisfying (16). Conditions: $Q_p = 11$, $Q_s = 17$, $k_m = 0.8$, $n = 2$ and $f_0 = 2.45$ GHz.

≤ -41 dBm. As a consequence, an additional on-chip [2], [3] or off-chip [1] low-pass filter is required. This approach dramatically increases the matching network insertion loss and area such that the original benefits of SE class-D PAs are lost and the BLE system efficiency is limited to $\leq 20\%$ in state-of-the-art publications [1]–[3].

In this work, a fully integrated differential class-E/F$_2$ PA [Fig. 13(a)] is exploited to address the aforementioned issues. Its characteristics and its matching network will be optimized in the following subsections.

A. Efficiency and Selectivity Tradeoff in Transformer-Based Matching Network

Fig. 14 illustrates a general schematic of a transformer-based matching network of a switched-mode PA, which performs simultaneously m-series (i.e., voltage) and p-parallel (i.e., current) combining [42], [43]. As proven in Appendix B, the matching network efficiency η_p can be calculated as shown in (15) at the bottom of the page.

η_p is a strong function of the effective inductance seen by the load, mL_s/p, and C_L. Hence, for the sake of simplicity, ξ is defined as $p/(mL_sC_L\omega_0^2)$. We also define $Q_L = R_LC_L\omega_0$ as the loaded Q-factor of the secondary side of the matching network. The η_p reaches its local maximum when

$$\frac{\partial \eta_p}{\partial C_L} = 0 \rightarrow \xi_{opt} = \frac{p}{mL_{s(opt)}C_L\omega_0^2} = 1 + \frac{1}{Q_s^2} + k_m^2\left(\frac{Q_p}{Q_s}\right). \tag{16}$$

By exploiting the Q_L definition above and replacing $L_{s(opt)}$ from (16) into L_s in (15), and carrying out lengthy algebra, the local maximum of η_p may be estimated by (17), shown at the bottom of the page.

Fig. 15(a) shows the maximum possible passive efficiency $\eta_{p(opt)}$ versus Q_L. As can be seen, there exists a global optimum Q_L that maximizes the transformer-based matching network efficiency at a given frequency. The η_p reaches its global maximum when

$$\frac{\partial \eta_{p(opt)}}{\partial Q_L} = 0 \rightarrow Q_{L(opt)} = \sqrt{\frac{Q_s^2}{1 + k_m^2 Q_p Q_s}} \xrightarrow{k_m^2 Q_p Q_s \gg 1} Q_{L(opt)} \approx \frac{1}{k_m}\sqrt{\frac{Q_s}{Q_p}}. \tag{18}$$

As a result, the global optimum load capacitance, $C_{L(opt)}$, may be estimated by $\sqrt{Q_s/Q_p}/(k_mR_L\omega_0)$. Note that both (16) and (18) are more general and accurate than in [42]. Using the optimum ξ and Q_L, the maximum η_p will be given by

$$\eta_{p(max)} = \frac{1}{1 + \frac{2}{k_m^2 Q_p Q_s}\left(1 + \sqrt{1 + k_m^2 Q_p Q_s}\right)} \tag{19}$$

which is the same result as in [42]. As gathered form Fig. 15(a), there is a strong tradeoff between the frequency selectivity and efficiency of the transformer-based matching network for $Q_L \geq Q_{L(opt)}$. Fortunately, the $\partial\eta_p/\partial Q_L$ slope is small around $Q_L = Q_{L(opt)}$. Combined with the fact that the effective matching network's Q improves almost linearly with Q_L, it is therefore

$$\eta_p = \frac{R_L}{R_L + \frac{m}{p}\frac{L_s\omega_0}{Q_s}|1 + jR_LC_L\omega_0|^2 + \frac{m}{p}\frac{L_s\omega_0}{k_m^2Q_p}|\frac{1}{Q_s} + \frac{pR_L}{mL_s\omega_0} - R_LC_L\omega_0 + j(1 + \frac{R_LC_L\omega_0}{Q_s})|^2} \tag{15}$$

$$\eta_{p(opt)} = \frac{1}{1 + \frac{1+Q_L^2}{\xi_{opt}Q_sQ_L} + \frac{1}{\xi_{opt}k_m^2Q_pQ_L}\cdot\left(\left(\frac{1}{Q_s} + Q_L(\xi_{opt} - 1)\right)^2 + \left(1 + \frac{Q_L}{Q_s}\right)^2\right)} \tag{17}$$

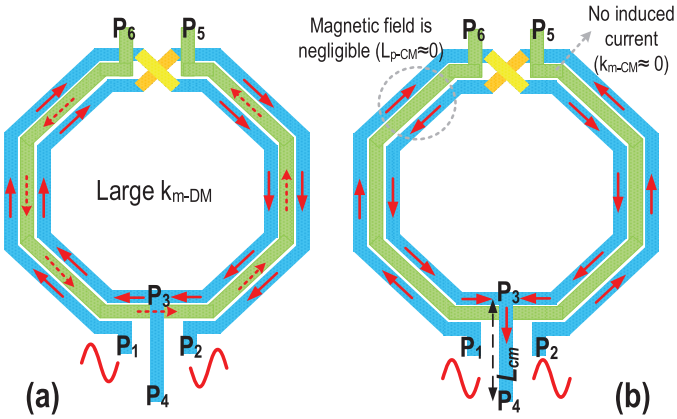

Fig. 16. Behavior of a 2:1 step-down transformer in: (a) differential-mode and (b) common-mode excitations.

TABLE III
DESIGN SETS FOR DIFFERENT FLAVORS OF CLASS-E/F PA

Tuning	K_C	K_L	K_P
E	0.184	1.152	0.577
E/F$_2$	0.337	1.609	0.381
E/F$_3$	0.209	0.961	0.657
E/F$_{2,3}$	0.323	0.832	0.747
E/F$_4$	0.218	1.173	0.533
E/F$_{2,4}$	0.361	1.667	0.350

desired to use $Q_L = 2Q_{L(opt)}$ ($C_L = 2C_{L(opt)}$) to double the frequency selectivity for the price of a negligible, i.e., $\leq 5\%$, efficiency drop.

B. Impedance Transformation

The matching network should also realize the required load resistance, r_L, and series inductance, L_{ser}, for proper zero-voltage and zero-slope switching (ZVS and ZdVS) operation of the class-E/F PA. As shown in Appendix B, r_L may be estimated by

$$r_L \approx R_L \cdot \frac{p}{m}\left(\frac{k_m}{n}\right)^2 \cdot \frac{Q_s + Q_L/\xi}{2\xi Q_L + Q_s + Q_L^2 Q_s(\xi-1)^2}. \quad (20)$$

To deliver the relatively low $P_{out} \leq 3$ dBm to the antenna, realizing a larger r_L is desired. Unfortunately, as can be gathered from (20), the voltage summation ($m > 1$) and imperfect magnetic coupling k_m exhibit reverse effect of reducing r_L. The p-way current combining enhances r_L but at the price of $(p-1)$ extra transformers and thus a dramatic increase in the PA die area [43], [44]. Hence, the parallel combining is not considered in this work. Eq. (20) further indicates that a step-down transformer (1: n) with a small turns ratio ($n < 1$) could be used to enhance r_L. However, the Q-factor of transformer windings, and thus its efficiency, drops dramatically as n reduces. Consequently, the turns ratio of 1:1/2 was chosen in consideration of both the r_L enhancement and η_p optimization scenarios. P_{out} is further reduced by using $V_{DD} = 0.5$ V (i.e., roughly half the nominal supply) for the drains of switching transistors with the side effect of $\sim$6 dB lower power gain for PA's transistors. However, the power gain of 28 nm NMOS devices is high enough at a relatively low frequency of 2.4 GHz such that the 6 dB power gain penalty has a negligible effect on the total system efficiency. Furthermore, the drain voltage peak of the switching transistors is ≤ 1.5 V, thus alleviating reliability issues due to a gate-oxide breakdown [21], [45].

As shown in Appendix B, the equivalent series inductance, L_{ser}, seen from the transformer's primary is

$$L_{ser} = L_p\left[(1-k_m^2) + k_m^2 \cdot \frac{2\xi Q_L + Q_L^2 Q_s \xi(\xi-1)}{2\xi Q_L + Q_s + Q_L^2 Q_s(\xi-1)^2}\right]. \quad (21)$$

Note that switched-mode PAs typically need a large L_{ser} to satisfy the ZVS/ZdVS criteria, which leads to a large inductor with a reduced Q-factor. As can be gathered from (21) and Fig. 15(b), L_{ser} increases with a larger Q_L for $\xi \geq 1$. More interestingly, L_{ser} can even be larger than the primary inductance, L_p, for $Q_L \geq Q_{L(opt)}$, which helps to reduce both matching network dimensions and insertion loss. Unfortunately, r_L reduces with C_L and thus the peak efficiency occurs at a higher output power. Consequently, it is again desired to choose $C_L \approx 2C_{L(opt)}$ by considering the tradeoff between r_L and L_{ser} enhancement factors.

C. Class-E/F$_2$ Operation

Fig. 13(b) illustrates an equivalent circuit of the PA matching network in the differential mode at the fundamental frequency ω_0. At all higher odd harmonics, L_{ser} presents high impedance and thus the only load seen by the switch is its parallel capacitance C_s, just the way it is in the traditional class-E PAs.

As illustrated in Fig. 16, the step-down 2:1 transformer acts differently to the common-mode (CM) and differential-mode (DM) input signals. When the transformer's primary is excited by a CM signal [Fig. 16(b)], the magnetic flux within the primary's two turns cancels itself out [46]. Consequently, the transformer's L_p is negligible and no current is induced at the transformer's secondary ($k_{m-CM} \approx 0$). Hence, R_L, L_s and C_L cannot be seen by even harmonics of drain current.

Furthermore, the CM inductance, $2L_{cm}$, seen by the switching transistors is mainly determined by the dimension of the trace between the transformer's center-tap and decoupling capacitors at the V_{DD} node. Together with C_s, $2L_{cm}$ realizes a CM resonance, ω_{cm}. Note that P_{out} of the class-E PA can be reduced by $\sim$2 dB at the same r_L and V_{DD} by means of an additional open circuit acting as the switches' effective load at $\sim 2\omega_0$ (i.e., class-E/F$_2$ operation [47]), as supported in the power factor, K_p, column in Table III. Consequently, this PA needs smaller ITR for $P_{out} < 3$ dBm, which results in a lower insertion loss for its matching network and thus higher system efficiency. However, in practice, limited value of an equivalent parallel resistance of the CM resonance, R_{cm}, leads to a power loss at the second harmonic and thus a penalty on the PA's efficiency if ω_{cm} is set at precisely $2\omega_0$. Consequently, in this design, we adjust the CM resonance slightly lower (i.e., at $\sim 1.8\omega_0$) to benefit from the lower K_p of semi class-E/F$_2$ operation, while avoiding the additional power loss at even harmonics.

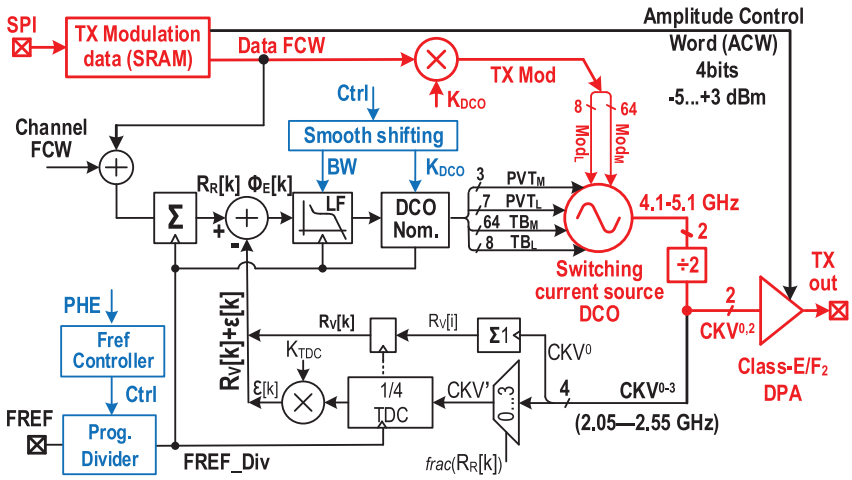

Fig. 17. Block diagram of the 2.4 GHz ULP Bluetooth Low-Energy transmitter.

Table III summarizes the design sets of class-E/F$_X$ PAs for satisfying the ZVS/ZdVS criteria. The design procedure starts by calculating r_L for a given V_{DD} and P_{out} from $r_L = \eta_p \cdot m \cdot p \cdot K_P \cdot (V_{DD} - V_{Dsat})^2 / P_{out}$, where V_{Dsat} represents the transistor's average V_{DS} in the on-state. As explained in [44], V_{Dsat} is a strong function of the switch size, technology and topology-dependent parameters, and it is set to $\sim$0.12 V to maximize the PAE of the proposed PA. The shunt capacitance, C_s, and series inductance, L_{ser}, may be estimated by exploiting K_c and K_L definitions: $C_s = K_C/(r_L \cdot \omega_0)$ and $L_{ser} = K_L \cdot r_L/\omega_0$. Now, the transformer geometry should be designed to realize the required r_L and L_{ser} by (20)–(21) while optimizing the matching network efficiency via (16)–(19). In this work, the circuit variables are as follows: $r_L \approx 29\ \Omega$, $C_s \approx 750\ fF$, $L_s \approx 440\ pH$, $C_L \approx 3.5\ pF$.

IV. All-Digital Phase-Locked Loop and Transmitter Architecture

Fig. 17 shows a block diagram of the proposed ultra-low-power (ULP) all-digital PLL (ADPLL), whose architecture is adapted from a high-performance cellular 4G ADPLL disclosed in [48]. Due to the relaxed PN requirements of BLE, the DCO $\Sigma\Delta$ dithering [49] was removed thanks to the fine switchable capacitance of the tracking bank varactors producing a fine step size of 4 kHz. The DCO features two separate tracking banks (TB): 1) phase-error correction, and 2) direct FM modulation. Each bank is segmented with LSB (i.e., 1x $\equiv$ 4 kHz) and MSB (i.e., 8x) unit-weights. Each TB range is 4 kHz $\times$ $(8 + 8 \times 64) = 2.08$ MHz.

The DCO clock is divided by two to generate four phases of a variable carrier clock, CKV$^{0-3}$, in the Bluetooth frequency range of f_V = 2402–2478 MHz. Two of its phases, CKV^{0,2}, are fed as differential clock signals to the digital PA (DPA) in Fig. 13(a). The four CKV$^{0-3}$ phases are routed to the phase detection circuitry, which selects the phase whose rising clock edge is *expected* to be the closest to the rising clock edge of a frequency reference (FREF) clock. This prediction is based on two MSB bits of a fractional part of reference phase, $R_R[k]$,

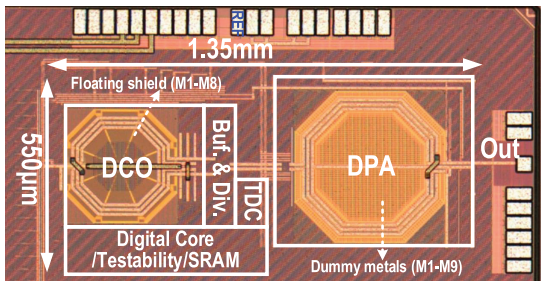

Fig. 18. Die micrograph of the proposed ULP transmitter.

which is an accumulated frequency command word (FCW). By means of this prediction, the selected TDC input clock CKV' spans a quarter of the original required TDC range, i.e., $T_V/4$, where T_V is the CKV clock period. This way, the long string of 417 ps/12 ps $>$ 35 TDC inverters is shortened by 4x, improving INL linearity and power consumption by the same amount.

The TDC output, after decoding, is normalized to T_V by the Δ_{TDC}/T_V multiplier and the quadrant estimation, normalized to $T_V/4$, is added to produce the phase error ϕ_E. The DCO tuning word is updated based on ϕ_E. The $\phi_E[k]$ is fed to the type-II loop filter (LF) with 4th-order IIR. The LF is dynamically switched during frequency acquisition to minimize the settling time while keeping phase noise (PN) at optimum. The built-in DCO gain, K_{DCO}, and TDC gain, K_{TDC}, calibrations are autonomously performed to ensure the wideband FM response.

The following architectural innovations allow the ADPLL to support ULP operation (highlighted in blue): The effective sampling rate of the phase detector and its related DCO update is dynamically controlled by scaling-down the FREF clock and simultaneously adjusting the LF coefficients in order to keep the same bandwidth and LF transfer-function characteristics. During the ADPLL settling, the full FREF rate is used, but afterwards its rate could get substantially reduced (e.g., 8x), or completely shut down, thus saving power consumption of the digital circuitry. The resulting in-band PN degradation is tolerable due to low PN of the DCO. In fact, freezing FREF would incur sufficiently low-frequency drift during the BLE

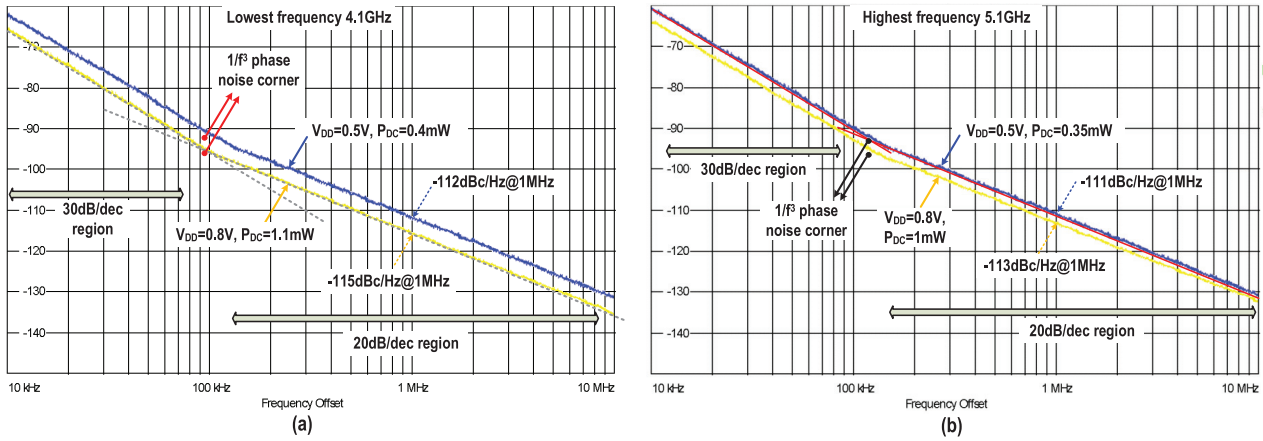

Fig. 19. Measured phase noise of the proposed oscillator at (a) the lowest and (b) the highest frequency.

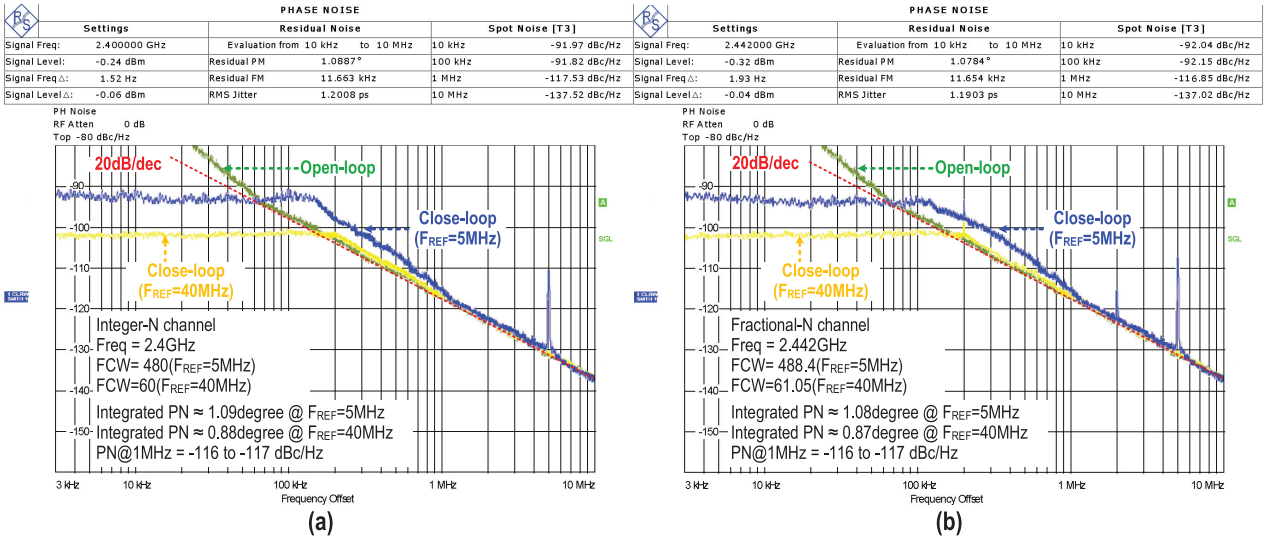

Fig. 20. Measured transmitter PN in open-loop and different close-loop configurations for (a) integer-N and (b) fractional-N channels.

376 μs packets, while keeping in operation the bare minimum of circuitry highlighted in red.

V. Experimental Results

Fig. 18 shows the die photo of the ULP TX in TSMC 1P9M 28 nm CMOS. Both DCO and PA transformers' windings are realized with top ultra-thick metal. However, they include a lot of dummy metal pieces on *all* metal layers (M1–M9) to satisfy very strict minimum metal density manufacturing rule of advanced ($\leq$ 28 nm) technology nodes [48].

Fig. 19 displays the phase noise of the proposed oscillator at the lowest and highest tuning frequencies for $V_{DD} =$ 0.5 V and 0.8 V, while $R_{in} \approx 310\ \Omega$. The measured PN is -111 dBc/Hz at 1 MHz offset from 5.1 GHz carrier while consuming $\sim$0.35 mW at 0.5 V. As justified in Section II-D, the $1/f^3$ PN corner of the oscillator is extremely low (i.e., $\leq$ 100 kHz) across the tuning range (TR) of 22% (i.e., from 4.1 to 5.1 GHz). Its average FoM is 189 dBc and varies $\pm$1 dB across the TR.

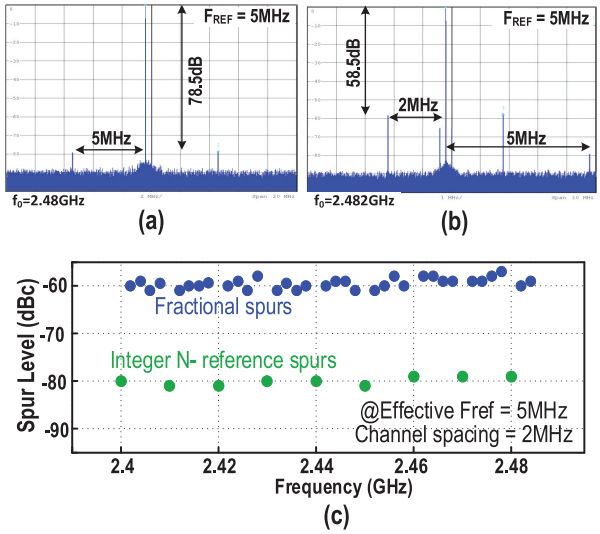

Fig. 21. Measured ADPLL spectrum for (a) integer-N and (b) fractional-N channels; (c) ADPLL fractional, reference and open-loop spurs versus BLE channels.

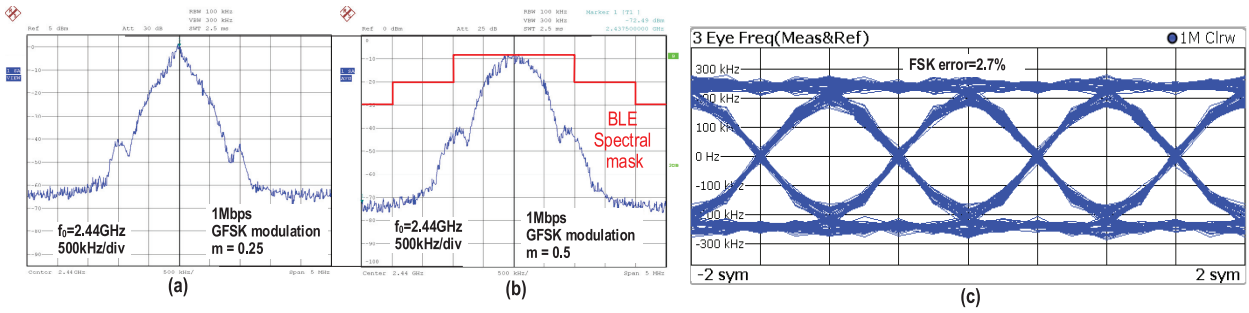

Fig. 22. Bluetooth GFSK modulation spectrum for modulation index of (a) $\mathrm{m} = 0.25$, (b) $\mathrm{m} = 0.5$, and (c) burst-mode modulation accuracy.

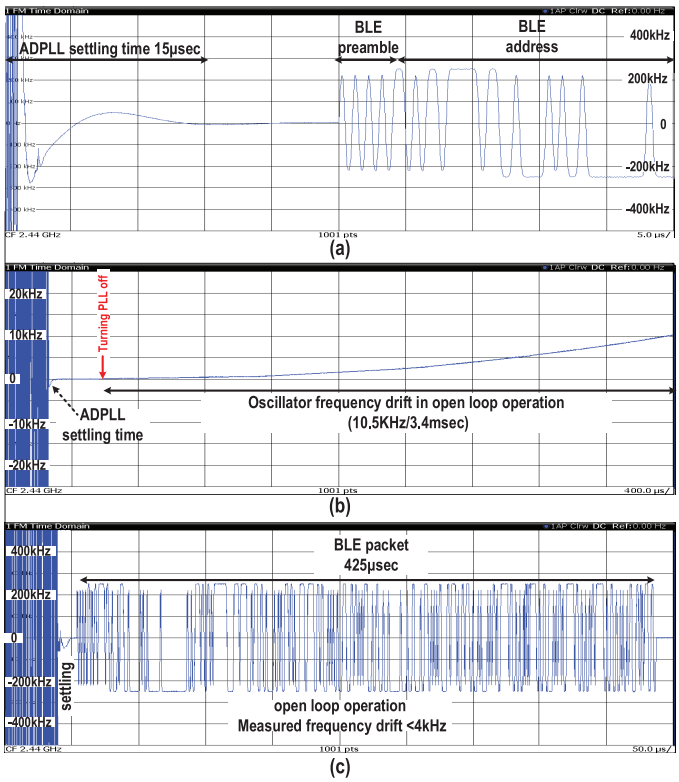

Fig. 23. (a) ADPLL settling; (b) oscillator frequency drift, and (c) demodulated TX frequency for 425 μs BLE packet in the open-loop operation.

For the supply frequency pushing measurements, the oscillator's V_{DD} supply is swept within 0.4–0.6 V while the off-chip bias resistor R_{Bias} (see Fig. 7) is removed and V_B is directly connected to an external reference voltage.[9] Contrary to the OSC_{NP} structure, V_{DD} perturbations here cannot directly modulate V_{gs} and thus the oscillator's DC current and nonlinear C_{gs} of M_{1-4} devices. Consequently, the worst-case supply frequency pushing is very low, 10–12 MHz/V across TR, thus making the oscillator suitable for direct connection to solar cells and integration with a PA.

Fig. 20 plots the measured phase noise at different configurations for both integer-N and fractional-N BLE channels. When used as an LO at *undivided* 40 MHz FREF, the ADPLL consumes 1.4 mW with an integrated PN of 0.87° (yellow line in Fig. 20). It exhibits in-band PN of -101 dBc/Hz, which corresponds to an average TDC resolution of $\sim$12 ps. Thanks to the low wander of the DCO, digital power consumption of the rest of ADPLL can be saved by scaling the rate of sampling clock to 5 MHz. However, the in-band PN increases by $10\log_{10}(40/5) = 9$ dB to -92 dBc/Hz with an integrated PN of 1.08° (blue line in Fig. 20).

Fig. 21 shows a representative spectrum of the ADPLL at integer-N and fractional-N channels and summarizes the worst-case spur for each BLE channel. The reference spur is -80 dBc and the worst-case fractional spur is -60 dBc. The open-loop spurs are not visible above the -90 dBc noise floor of our equipment.

Fig. 22 shows the TX spectra for 1 Mb/s GFSK modulation at different modulation indexes and its burst modulation quality. All spectral mask requirements are fulfilled, while the FSK error is 2.7%.

To achieve simultaneous fast locking and power savings, the loop bandwidth is dynamically controlled via a gearshift technique [49]. During frequency acquisition, the loop operates in type-I, with a wide bandwidth of 2 MHz. It is then switched to type-II, 4th-order IIR filter with a 500 kHz bandwidth when it enters the tracking mode. Finally, the loop bandwidth is reduced to 200 kHz to optimize the ADPLL integrated jitter. The measured lock-in time is less than 15 μs for f_{REF} of 40 MHz as shown in Fig. 23(a). Thanks to the low flicker noise, frequency pushing and pulling of the DCO, its frequency drift is extremely small, as demonstrated Fig. 23(b). Consequently, the rest of ADPLL can be shut-down during the modulation to improve the power efficiency of the BLE transmitter. The maximum difference between 0/1-symbol frequency at the start of the BLE packet and 0/1 frequencies within the packet payload should be less than $\pm$ 50 kHz. This specification is properly satisfied with over an order-of-magnitude margin even while in the open loop operation, as shown in Fig. 23(b) and (c).

The PA output level is digitally adjustable between -5 to $+3$ dBm and reaches peak PAE of 41%, which includes the power consumption of two stages of PA drivers [see Fig. 24(a)]. The measured TX harmonic emissions are shown in Fig. 24(b). Due to the differential operation, proper 2nd-harmonic termination and trading negligible efficiency loss for higher loaded Q-factor of PA's matching network, 2nd and 3rd harmonics remain well below the -41 dBm regulatory limit. The proposed TX

[9]Since V_B biasing does not consume any DC current, the current consumption of its internal biasing circuit is extremely low; therefore, realizing an on-chip V_B voltage reference with a good PSRR would be quite straightforward.

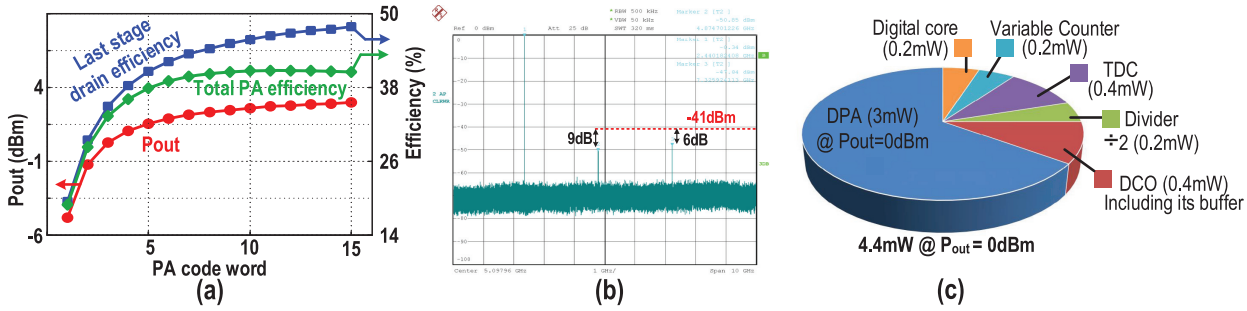

Fig. 24. (a) PA characteristics; (b) TX harmonic emissions; and (c) TX power breakdown at $P_{out} = 0$ dBm.

TABLE IV
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART

	This work			ISSCC'15 IMEC [1]	JSSC'15 Dialog [2]	ISSCC'15 Renesas [3]	ISSCC'12 Toumaz [4]	ESSCIRC'14 Frontier [5]	TMTT2013 [6]	CC2640 TI [7]	
CMOS technology	28nm			40nm	55nm	40nm	130nm	65nm	130nm	N/A	
OSC PN @1MHz (dBc/Hz)	-116 to -117			-110	-111.5	N/A	-107	-108.2	-110	-109	
OSC FoM (dB)	188-189			183	179	N/A	N/A	N/A	185	N/A	
OSC tuning range	2.05-2.55GHz (22%)			25%	20%	N/A	N/A	N/A	N/A	N/A	
PLL in-band PN (dBc/Hz)	-92 @ FREF=5MHz -101@ FREF=40MHz			-90	N/A	N/A	-87	-87.5	-100	N/A	
Integrated PN (degree)	1.08 @ FREF=5MHz 0.87 @ FREF=40MHz			1.5	N/A	N/A	N/A	N/A	N/A	N/A	
PLL FoM* (dB)	-238.65			-236	N/A	N/A	N/A	N/A	N/A	N/A	
PLL settling time(μs)	15			15	15	N/A	N/A	N/A	N/A	N/A	
Reference/Fractional spurs (dBc)	-80 / -60			-70 / -38	N/A	N/A	N/A	N/A	-75/-37	N/A	
TX Modulation error	2.70%			5%	N/A	N/A	7.30%	7%	N/A	N/A	
Output power (dBm)	-5 to +3			-2/1	-20 to 0	0	-30 to +5	-10 to -3	1.6	-21 to +5	
Total PA efficiency	41%			25%	30%	<30%	N/A	<25%	26.80%	N/A	
On-chip matching network	Yes			No	Yes	Yes	No	No	Yes	No	
Strongest harmonic emission	HD3/-47dBm			HD2/-49dBm	HD3/-52dBm	HD3/-48dBm	N/A	N/A	HD3/-32dBm	-46dBm	
Supply voltage (V)	0.5 / 1			1	0.9-3.3	1.1	1	1.1	1	1.8-3.8	
TX power consumption (mW)	@P_{OUT}	0dBm	3dBm	-2dBm	0dBm	0dBm	0dBm	-3dBm	1.6dBm	0dBm	5dBm
	open-loop	3.6	5.5	4.2	10.1†	7.7†	8.9†	5.1†	5.9	18.3	27.3
	close-loop	4.4	6.3								
TX efficiency (P_{OUT}/P_{DC})	open-loop	28%	36%	15%	10%	13%	12%	10%	25%	5.5%	11.5%
	close-loop	23%	32%								
TX active area (mm^2)	0.65			0.6†	0.6‡	0.6‡	1‡	0.6‡	0.6‡	N/A	

* FoM $= 10\log_{10}[\sigma^2_{\text{jitter}} \cdot (P_{DC,PLL}/1\text{mW})]$.
† including DC-DC converters.
‡ graphically estimated.

consumes 3.6/5.5 mW during the open-loop 1 Mb/s GFSK BLE modulation at 0/3 dBm output, resulting in $\eta_{TX} = 28/36\%$ total TX efficiency. The power consumption would increase by 0.8 mW with TDC, variable counter and digital circuitry turned on when the ADPLL is clocked at 40 MHz FREF. Thus, even in the closed loop, with $\eta_{TX} = 23/32\%$ at 0/3 dBm, it is still more power efficient than the prior record [6] (also [50] but at 13.5 dBm output). The TX power breakdown is also illustrated in Fig. 24(c). Table IV summarizes the performance and compares it with leading ULP transmitters. The proposed ULP TX achieves the lowest power consumption and phase noise.

VI. CONCLUSION

We have proposed an ultra-low power (ULP) Bluetooth Low Energy (BLE) transmitter that demonstrates the best-ever reported system efficiency and phase purity, while abiding by the strict 28 nm CMOS technology manufacturing rules. A new switching current-source oscillator combines advantages of low supply voltage of the conventional NMOS cross-coupled oscillator with high current efficiency of the complementary push-pull oscillator to reduce the oscillator supply voltage and dissipated power further than practically possible in the traditional oscillators. Due to the low wander of DCO, digital power consumption of ADPLL can be significantly saved by scaling down the rate of sampling clock after settling or even shutting it down entirely during direct DCO data modulation. A fully integrated differential class-E/F_2 switching PA is utilized to improve system efficiency at low output power of 0–3 dBm while fulfilling all in-band and out-of-band emission masks. Its required matching network was realized by exploiting different behaviors of a 2:1 step-down transformer in differential and common-mode excitations. Furthermore, for both the proposed oscillator and power amplifier, accurate key analytical equations are derived to provide useful design insights.

APPENDIX A

Consider the switching current-source oscillator of Fig. 7. Since M_{3-4} transistors work only in weak inversion and saturation during their on-state, short-channel modulation effects should be considered in the G_{DS4EF} calculation in (5). It is

well known that $g_{ds4}(\phi) = \lambda \cdot I_{M4}(\phi)$, where I_{M4} and λ are, respectively, the drain current and channel-length modulation coefficient of M_4. As a result, G_{DS4EF} is estimated as

$$\begin{aligned} G_{DS4EF} &= G_{DS4}[0] - G_{DS4}[2] \\ &= \frac{1}{2\pi}\int_0^{2\pi} g_{ds4}(\phi)\cdot(1-\cos 2\phi)\,d\phi \\ &= \frac{\lambda \cdot I_{DC}}{2}\cdot\left(1-\frac{I_{M4,H2}}{I_{DC}}\right) \end{aligned} \tag{A.1}$$

where $I_{M4,H2}$ is the 2nd harmonic of I_{M4}. By considering $\lambda = 4.8\ \mathrm{V}^{-1}$, $I_{M4,H2}/I_{DC} = 0.33$, and $I_{DC} = 750\ \mu$A, the calculated G_{DS4EF} becomes 1.2 mS, which agrees fairly well with the simulation results in Fig. 11(a).

On the other hand, since M_1 works in saturation only for a short part of the oscillation cycle and its channel conductance, g_{ds1}, is much larger in the triode region, a square-law behavior in the G_{DS1EF} calculation in (5) seems a good assumption. As a result, g_{ds1} may be estimated by

$$g_{ds1}(\phi) = \begin{cases} K_1[(V_B - V_t - V_0) & -\theta_0 \le \phi \le \theta_0 \\ \quad +0.5V_{osc}\,(1+A_0)\cos\phi] & \\ 0 & -\pi \le \phi \le -\theta_0, \\ & \text{and } \theta_0 \le \phi \le \pi \end{cases} \tag{A.2}$$

where $K_1 = \mu_n C_{ox} W_1/L_1$, and V_0 is the DC voltage at DA and DB. θ_0 is the triode angle calculated as

$$\theta_0 = \cos^{-1}\left(\frac{V_0 + V_t - V_B}{0.5V_{osc}\,(1+A_0)}\right). \tag{A.3}$$

By exploiting the G_{DS1EF} definition and carrying out a lengthy algebra, we obtain

$$\begin{aligned} G_{DS1EF} = \frac{K_1}{2\pi}\Big[&2\,(V_B - V_0 - V_t)\cdot(\theta_0 - \sin(\theta_0)\cos(\theta_0)) \\ &+\frac{2}{3}V_{osc}\,(1+A_0)\sin^3(\theta_0)\Big]. \end{aligned} \tag{A.4}$$

By replacing the oscillator's circuit parameters ($V_B = 0.45$ V, $V_t = 0.485$ V, $V_0 = 0.15$ V, $V_{osc} = 0.3$ V, $A_0 = 2.15$, and $K_1 = 0.125A/V$) in (A.3) and (A.4), the calculated G_{DS1EF} is equal to 3.81 mS, which is in good agreement with the simulations [see Fig. 11(a)].

APPENDIX B

Consider the transformer-based matching network shown in Fig. 14(b). The current through the secondary and primary windings of the ideal transformer can be respectively calculated by

$$\begin{aligned} I_{sEF} = pI_s = I_L\,(1 + jR_LC_L\omega_0)\,, \text{and} \\ I_1 = \frac{mn}{k_m}I_{sEF} = I_L\frac{mn}{k_m}\,(1+jR_LC_L\omega_0)\,. \end{aligned} \tag{B.1}$$

Furthermore, the voltage across the magnetizing inductance, $L_p k_m^2/(mp)$, is given by

$$\begin{aligned} V_p &= I_L\frac{k_m}{mn}\left(R_L + \frac{mr_s}{p}(1+jR_LC_L\omega_0)\right) \xrightarrow{r_s = L_s\omega_0/Q_s} \\ V_p &= I_L\frac{k_m L_s\omega_0}{np}\left(\frac{pR_L}{mL_s\omega_0} + \frac{1}{Q_s} + j\frac{R_LC_L\omega_0}{Q_s}\right). \end{aligned} \tag{B.2}$$

Consequently, the current through the leakage inductance, $L_p(1-k_m^2)/(mp)$, is calculated by

$$\begin{aligned} I_{pEF} &= I_1 + \frac{mpV_p}{jk_m^2L_p\omega_0} \\ &= I_L\frac{mn}{jk_m}\left(\left(\frac{pR_L}{mL_s\omega_0} + \frac{1}{Q_s} - R_LC_L\omega_0\right)\right. \\ &\quad \left. +j\left(1+\frac{R_LC_L\omega_0}{Q_s}\right)\right). \end{aligned} \tag{B.3}$$

As a result, the total power dissipated in the transformers' secondary and primary is respectively estimated:

$$\begin{aligned} P_{rs} &= \frac{mr_s}{p}|I_{sEF}|^2 \xrightarrow{r_s = L_s\omega_0/Q_s \text{ and } (B.1)} \\ P_{rs} &= I_L^2\frac{m}{p}\frac{L_s\omega_0}{Q_s}|1+jR_LC_L\omega_0|^2, \end{aligned} \tag{B.4}$$

and

$$\begin{aligned} P_{rp} &= \frac{r_p}{mp}\,|I_{pEF}|^2 \xrightarrow{r_p = L_p\omega_0/Q_p \text{ and } (B.3)} \\ P_{rp} &= I_L^2\frac{m}{p}\frac{L_s\omega_0}{k_m^2Q_p}\left|\left(\frac{1}{Q_s} + \frac{pR_L}{mL_s\omega_0} - R_LC_L\omega_0\right)\right. \\ &\quad \left. +j\left(1+\frac{R_LC_L\omega_0}{Q_s}\right)\right|^2. \end{aligned} \tag{B.5}$$

The matching network efficiency, η_p, is the ratio of power delivered to the load, P_L, over total power: $\eta_p = P_L/(P_L + P_{rp} + P_{rs})$. By exploiting (B.4) and (B.5), (15) is obtained.

On the other hand, the load Z_L seen from the input ports of the matching network (see Fig. 14) can be calculated by

$$\begin{aligned} Z_L = j(1-k_m^2)L_p\omega_0 + \frac{mpV_p}{I_{pEF}} \rightarrow Z_L = jL_p\omega_0 \\ \times\left[(1-k_m^2)+k_m^2\frac{(1+\xi Q_LQ_s)+jQ_L}{(1+Q_LQ_s(\xi-1))+j(Q_L+Q_s)}\right]. \end{aligned} \tag{B.6}$$

As a result, the equivalent series inductance and load resistance seen from the transformer's primary can be respectively estimated by

$$\begin{aligned} L_{ser} = \frac{Im\{Z_L\}}{\omega_0} = L_p\left[(1-k_m^2)\right. \\ \left. +k_m^2\frac{1+2\xi Q_LQ_s+Q_L^2+Q_L^2Q_s^2\xi(\xi-1)}{1+2\xi Q_LQ_s+Q_L^2+Q_s^2+Q_L^2Q_s^2(\xi-1)^2}\right] \end{aligned} \tag{B.7}$$

and

$$r_L = Re\{Z_L\} = k_m^2 L_p \omega_0 Q_L \cdot \frac{\frac{Q_s}{Q_L}(1+Q_L^2+\xi Q_L Q_s)}{1+2\xi Q_L Q_s+Q_L^2+Q_s^2+Q_L^2 Q_s^2(\xi-1)^2}. \quad \text{(B.8)}$$

By exploiting Q_L and ξ definitions, we have

$$r_L = R_L \cdot \frac{p}{m}\left(\frac{k_m}{n}\right)^2 \cdot \frac{\frac{Q_s}{\xi Q_L}(1+Q_L^2+\xi Q_L Q_s)}{1+2\xi Q_L Q_s+Q_L^2+Q_s^2+Q_L^2 Q_s^2(\xi-1)^2}. \quad \text{(B.9)}$$

By considering $Q_s \gg 1$ and $Q_s^2 \gg Q_L^2$, (B.9) and (B.7) are immediately simplified to (20) and (21).

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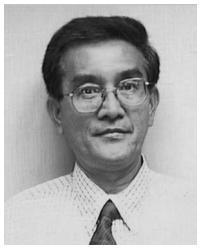

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