# Monolithic 3D Wafer Level Integration
# Applied for Smart LED Wafer Level Packaging

Kolahdouz Esfahani, Zahra

**DOI**
10.4233/uuid:ca460c12-bf40-4f40-9240-d6c8aa5c37ca

**Publication date**
2017

**Document Version**
Final published version

**Citation (APA)**
Kolahdouz Esfahani, Z. (2017). *Monolithic 3D Wafer Level Integration: Applied for Smart LED Wafer Level Packaging*. [Dissertation (TU Delft), Delft University of Technology]. https://doi.org/10.4233/uuid:ca460c12-bf40-4f40-9240-d6c8aa5c37ca

**Important note**
To cite this publication, please use the final published version (if applicable).
Please check the document version above.

# Monolithic 3D Wafer Level Integration

## Applied for

## Smart LED Wafer Level Packaging

Zahra Kolahdouz Esfahani

# Monolithic 3D Wafer Level Integration

## Applied for

## Smart LED Wafer Level Packaging

**Proefschrift**

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus prof.ir. K.C.A.M. Luyben;
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op

donderdag 19 januari 2017 om 10:00 uur

door

**Zahra KOLAHDOUZ ESFAHANI**

Master of Science in Electrical Engineering,
University of Tehran, Iran
geboren te Tehran, Iran

This dissertation has been approved by the
promotor: Prof. dr. G. Q. Zhang
copromotor: Dr. ir. H. van Zeijl

Composition of the doctoral committee:

| | |
|---|---|
| Rector Magnificus, | chairman |
| Prof. dr. G. Q. Zhang, | Delft University of Technology |
| Dr. ir. H. van Zeijl, | Delft University of Technology |
| Independent members: | |
| Prof. dr. P. M. Sarro, | Delft University of Technology |
| Prof. dr. P. French, | Delft University of Technology |
| Prof. dr. U. Staufer, | Delft University of Technology |
| Prof. dr. H. P. Urbach, | Delft University of Technology |
| Prof. dr. S. Wei, | Tsinghua University, Beijing, China |



Zahra Kolahdouz Esfahani,
Monolithic 3D Wafer Level Integration Applied for Smart LED Wafer Level Packaging,
Ph.D. Thesis (with summary in Dutch),
Delft University of Technology.

*Keywords*: System-in-Package, 3D wafer-level integration, LED, high aspect ratio lithography, multi-step imaging, smart silicon interposer, side-wall photodiode, blue/UV selective photodetector, sensor readout, BiCMOS process, wafer-level optic, multidisciplinary simulation, optical simulation.

*Printed by*: Ipskamp drukkers, The Netherlands

*Front & back*: Front side shows wafer-level integration of 3D silicon-based smart interposer for LED System-in-Package (SiP), Back side shows a glowworm as a natural lighting SiP (photo from www.deviantart.com).


ISBN/EAN: 978-94-028-0513-0

An electronic version of this dissertation is available at http://repository.tudelft.nl/.

# Table of Contents

# Chapter 1

# Introduction

Have you ever noticed the wonderful world of insects? There are well over 1 million different known species of insects in the world, and some experts estimate that there might be as many as 10 million. Different species with different ecosystems, body structures, and ways of life.

Let's consider insects as different kinds of systems packaged in various bodies. Systems which can be divided into widespread categories considering the functionality, existing environments, body structures, etc. Insects have segmented bodies supported by exoskeletons, the hard outer covering made mostly of chitin. The segments of the body are organized into three **distinctive but interconnected units**, or tagmata: a head, a thorax, and an abdomen. The head supports a pair of sensory antennae, a pair of compound eyes, and, if existing, one to three simple eyes (or ocelli) and three sets of variously modified appendages that form the mouthparts. The thorax has six segmented legs – one pair each for the prothorax, mesothorax and the metathorax segments making up the thorax – and, none, two or four wings. The abdomen comprises eleven segments, however in a few species of insects, these segments may be fused together or shrunk. The abdomen also contains most of the digestive, respiratory, excretory and reproductive internal structures. Significant deviation and many adaptations have happened in the body parts of insects, especially wings, legs, antenna, and mouthparts [1].

Going to electronics area, there is a similar world of systems in packages**.** According to International Technology Roadmap for Semiconductors (ITRS) [2]**, System in Package (SiP)** is a combination of multiple active electronic components of different functionalities, assembled in a single unit that provides multiple functions associated with a system or a sub-system. A SiP

may optionally contain passives, MEMS, optical components, and other packages and devices; again, **distinctive but interconnected units.**

1

Package in place of body of system should provide four major functions: powering, signal distribution, mechanical protection and thermal management. Package as an outer shell, like what a chitin out covering does for an insect, is the interface of a system to outer domain holding the input and output paths. Different functionalities and operation environments lead to different kinds of packaging material and technologies.

## 1.1 System in Package (SiP)

System integration can be done at different levels. One is combining various functionalities in an IC, which is called System-on-Chip (SoC). An alternative is integrating different dies in a single package, entitled System-in-Package (SiP). In contrast to connecting different functional ICs and components on a board, the new integration methods offer higher efficiency and lower costs. System integrators are the major players for further innovation in electronic industry [3].

By rather fast development in consumer electronics industry, the SiP technology is receiving more attentions and efforts. It is known as one of the key technology to improve functionality density, in parallel to lowering the cost per function. That encourages the effective use of three dimensions rather than two in packaging and interconnect trends [4].

The main general drives for 3D integrations are [5], [6]:

- Lower form factor: it reduces system volume, weight, and footprint.
- Improved performance: first of all, integration density is increased. This reduces interconnect length leading to higher transmission speed and lower power consumption.
- Integration of different heterogeneous technologies: due to 2D SoC limitations for integrating different technologies, 3D platform is used to first make discrete dices, and then to combine them either on a substrate or 3D stacking. This has adaptability to a wide variety of microsystem applications.
- Low cost batch production: 3D integration decreases processing costs for mixed technologies.
- New application demands.

The 3D integration technologies can be grouped into 3 main classes, namely 3D on-chip integration, 3D IC-stacking, and 3D-packaging [6]. It should be clarified that if the

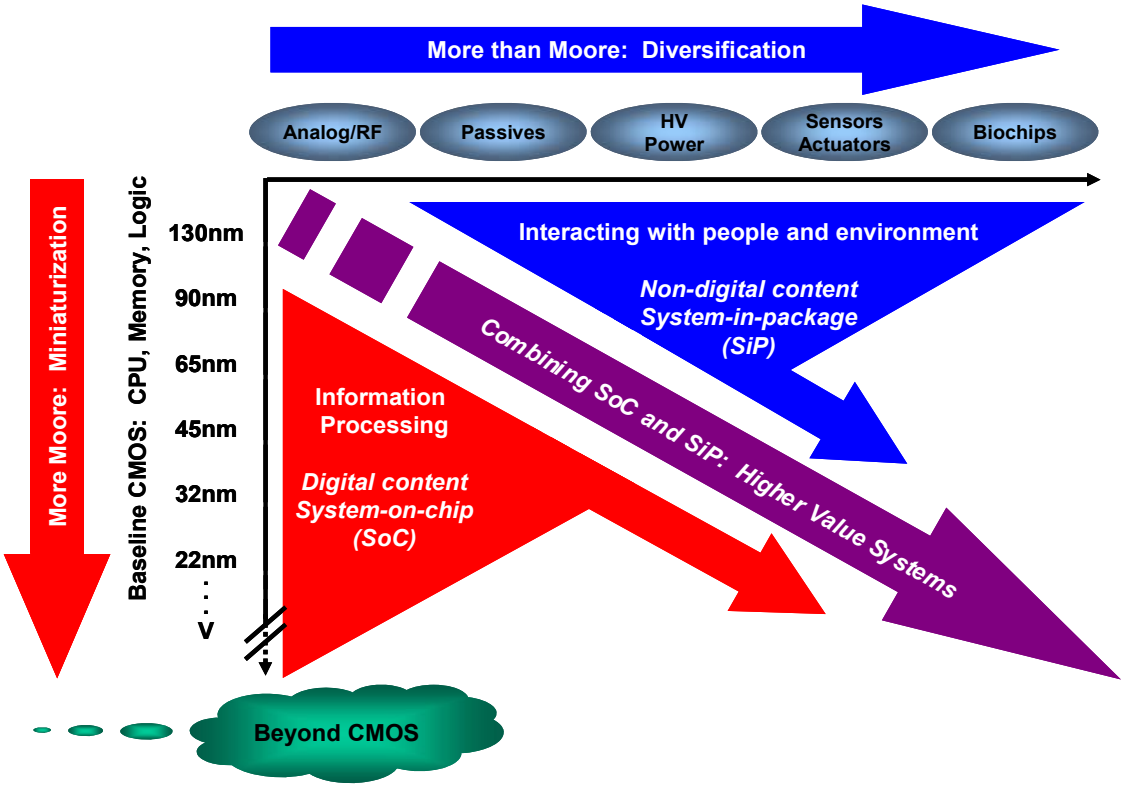



*Figure 1-1: The combined need for digital and non-digital functionalities in an integrated system is translated as a dual trend in the International Technology Roadmap for Semiconductors: miniaturization of the digital functions ("More Moore") and functional diversification ("More-than-Moore") [7].*

interconnections are made through Si vias (TSV), the technology is categorized as 3D IC-stacking, and if the interconnections are made outside of the die, then it has been categorized as 3D-packaging. Simultaneously, having all these together we have a complete 3D system package, one can call "System-in-Package."

Today, there are increasing industrial demands for smaller size, higher speed, lower power dissipation, better reliability, and more functionality. There is a dual trend for new systems. For digital electronics, there is a trend for continuous miniaturization and its related benefits in terms of performances which is labeled "More Moore". For analog circuits and systems, it is integration of diverse functionality, which is entitled "More-than-Moore". This combined needs for digital and non-digital functionalities in a product is depicted in Figure 1-1 [7].

While "More Moore" may be considered as the brain of a smart compact system, "More-than-Moore" refers to its skills to interact with the outside world and the users.

To cope with this dual trend, we should consider the challenges with both parts. First, in "More Moore" stream, it is important to figure out how to best use existing infrastructure available in IC industry, especially wafer level processing.

Next, in "More-than-Moore direction", we need advanced SiP, but the challenges are:

1) how to master the complexity and the different types of interconnects with the focus on the electronic domain;
2) how to combine different technologies often work in different domains for heterogeneous integration.

For both topics, the key is how to assemble and connect, or in another word having a reliable mechanical and electrical interconnect. In many technologies, the mechanical and electrical interconnect are coupled (solder bumps, cu-cu bonding etc.). In technologies like wire bonding, mechanical and electrical interconnect are de-coupled and can be optimized separately.

### 1.1.1 SiP Concerns and Requirements

There are many concerns and challenges for SiP related to its diversity and 3D IC integration such as [8], [9]:

- Non-defined technology standards and industry parameters for optimal technology selection
- Lack of design guidelines, tools, and rules
- Lack of test methods and equipment
- Challenges for mixing chips with different speeds and sizes
- Equipment accuracy for alignments
- Wafer thinning and thin wafer handling during processes
- Thermal management issues
- Challenges with vertical interconnects (like TSV): design tools, high cost, lacking/expensive high-volume production tools, etc.

These all indicate the importance of research efforts considering various aspects of the SiP related to the materials, technologies, design, fabrication, and reliability issues. In literature, detailed classifications could be found addressing the 'levels of integration' such as wafer-stack, chip-stack, and package/module-stack [10]. Interconnects technology have been addressed by Al-Sarawi [11].

The reliability factors for SiP products are the same as other areas but the relative importance

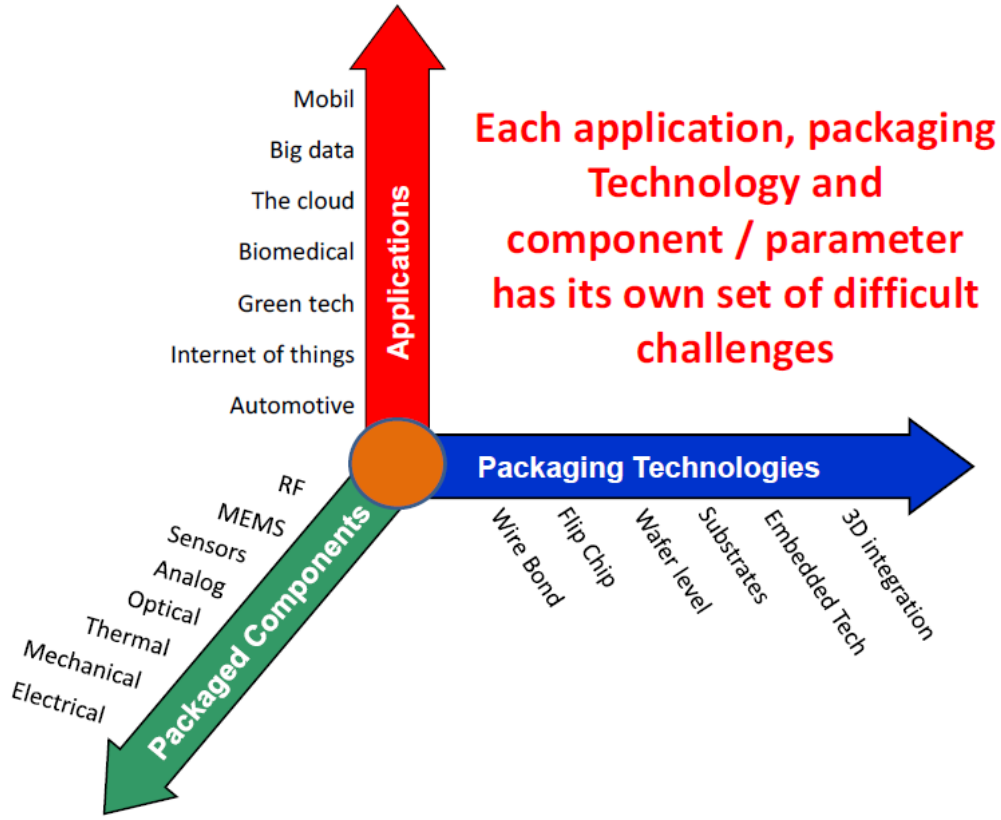



*Figure 1-2: Complex SiP contains various types of elements through heterogeneous integration [7].*

changes. They have higher thermal cycle count and mechanical stress, and wider range of storage and usage environments due to the use pattern of consumer electronics. Meeting the reliability requirements of future SiP components and systems will require tools and procedures that are not yet available. They should cover from failure mechanisms and standards to lifetime, reliability models, and characterization [2]. The factors that may affect the reliability concerns can be listed as follows: complexity, miniaturization, power, material selection, end use conditions, and interconnect [2], [12]–[14].

### 1.1.2 Heterogeneous Integration and Wafer Level Packaging

Heterogeneous integration comprises high level assembly of different separately manufactured components. It can enhance functionality and improve the operating characteristics. As SiP includes different elements (as shown in Figure 1-2), heterogeneous integration concerns should be addressed as well.

Wafer-Level Packaging is defined as a technology which all the packaging process are

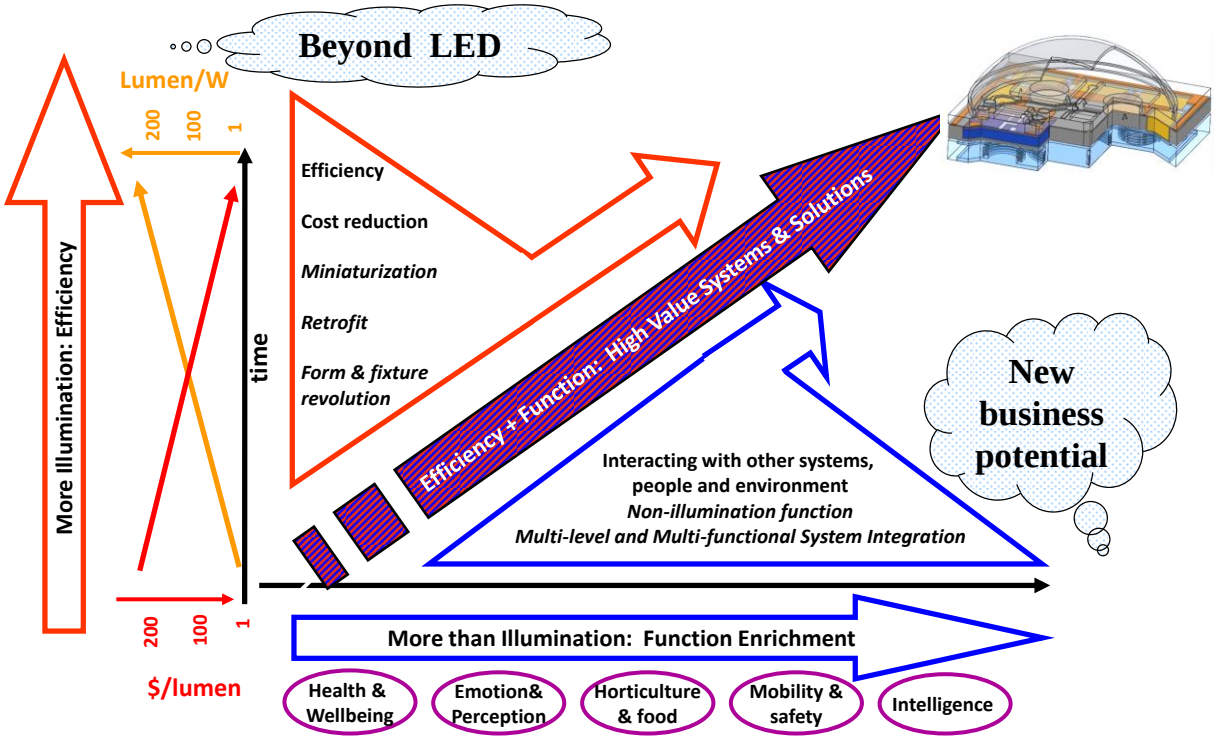



*Figure 1-3: New industrial / technology landscape of lighting.*

performed at the wafer level. It is one of the best potential options among different packaging technologies, because of lower costs, higher scale, superior yields, and higher accuracy. It can achieve highest density integration for hybrid applications. However, there are still some challenges for high accuracy domains [2], [6].

There are two major concerns in wafer-level 3D integration: final reliability and yield after stacking multiple wafers [15]. Wiring between the subsystems, known as "wiring crisis", is the main limitation for performance, multi- functionality, and reliability of 3D systems. It is one of the critical performance bottlenecks for current and future IC generations. So, the key technologies for 3D systems are wiring and wafer bonding, in another word *interconnection*. The quality of interconnection directly addresses the 2 concerns.

## 1.2 Motivation for LED Wafer Level Packaging

The similar trends of Figure 1-1 can also be observed in lighting landscape, as depicted in Figure 1-3. The vertical axis demonstrates the much more illumination trend, pointing to continuing of Haitz's law, in which Ronald Haitz predicted that every decade, the cost per lumen falls by a factor of 10, and the amount of light generated per LED package increases by a factor

of 20, for a given wavelength (color) of light. This is considered the LED counterpart to Moore's law [16]. Besides, there is another trend for much more than miniaturization, lumen/$, and lumen/Watt. It includes the increasing demands for multi-functionality, -discipline, -technology, -variability, -material, -interface, -process, -scale, -damage/failure mode, and -testing targets.

This trend introduces more attention not only in technology area but also for covering multi-application/market, -million investment, -innovation/complexity, -talent, -supply chain, -business models, -infrastructure, and -competition [17].

Taking part into this tremendous developing industry and market demands, wafer level packaging can be considered as a key processing point. At present, most LED components are made with single chip packaging technology. The main manufacturing processes follow conventional chip-based IC packaging. So, there is a need for LEDs to migrate to wafer level packaging to use the same benefits as IC's [18]. Nevertheless, there are different boundary conditions to adopt wafer level packaging of LEDs. For instance, there is limited usability of wafer level packaging processes on the LED device wafer directly [19]. But hybrid integration of LED chips on a Si interposer can reduce the cost, and moreover, eases the integration of various functional devices. Using Si devices and capabilities makes it possible to design and fabricate a smart lighting module as a SiP for broad applications especially in the Internet of Things (IoT) area. As IoT promises application diversification, the spotlight is now turned to advanced packages in order to answer market demands [20].

## 1.3 Thesis Objectives

In this work, we are going to introduce a methodology for monolithic wafer-level integration of 2D and 3D systems. It can be employed to fabricate a smart silicon-based interposer for broad range of applications such as MEMS/NEMS, communication and lighting modules. Such interposers can offer various benefits by also integrating some active components, circuits, and systems. One of the best fit application area is a smart solid-state lighting (SSL) unit.

LEDs are believed to dominate all lighting applications in near future. As mentioned before, integration and packaging are two of the critical issues that resolving them enables efficient and reliable solutions for lighting requirements. Wafer level packaging is a promising method to have a lower cost, higher scale, and superior yield.

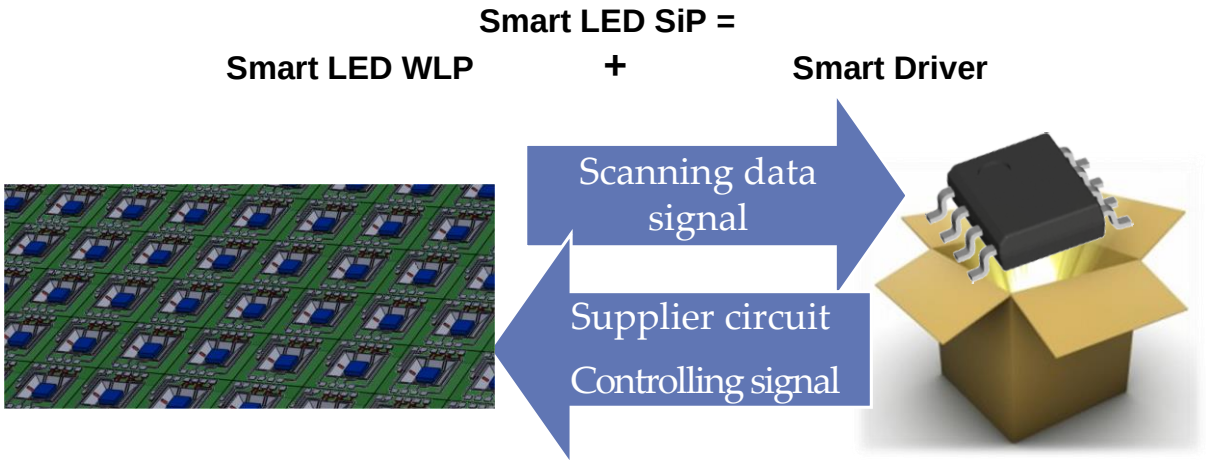



*Figure 1-4: A smart LED system comprising a smart LED WLP and a smart driver.*

In this dissertation, a new integration approach of a smart unit of LED lighting is introduced: LED SiP. It comprises a *smart LED wafer level package (WLP)* and a *smart driver*. This concept is depicted in Figure 1-4. Smart LED WLP is used as a Si based interposer for LED chips. Firstly, it integrates the wafer level optics, related interconnections, monitoring devices and powering circuits. LED chip would be later mounted. In addition, to make the package smart and leverage semiconductor process, as much controlling functions as possible can be integrated into the silicon interposer. Smart driver is the brain of the total system. It works both as a driver circuit to supply power and a controller. By getting real time sensing data of the package, it can have a better control over electrical and thermal management and so on. Also, wireless communication and remote control functions can be included. Due to rather large nature of LED chips, the final Si utilization yield of the interposer cannot get that high, but a simple low cost processing can compensate total cost of the package.

Main effort of this dissertation is on the smart WLP part. The final smart WLP is a high lumen output lighting module. It includes high current blue LEDs and different sensors in a reflector cavity. In this Si interposer with a high topography, lithography defined wiring is used as a reliable interconnect solution. Additionally, control circuit of the LED output light are integrated on the same die to reduce costs of any required external circuitry. In more details, the interposer monolithically integrates on-chip reflector cavity, sensors, remote phosphor layer, litho-defined wiring, power switching transistors, digital sensor readout circuit, and analog light feedback circuit into one smart LED wafer-level package.

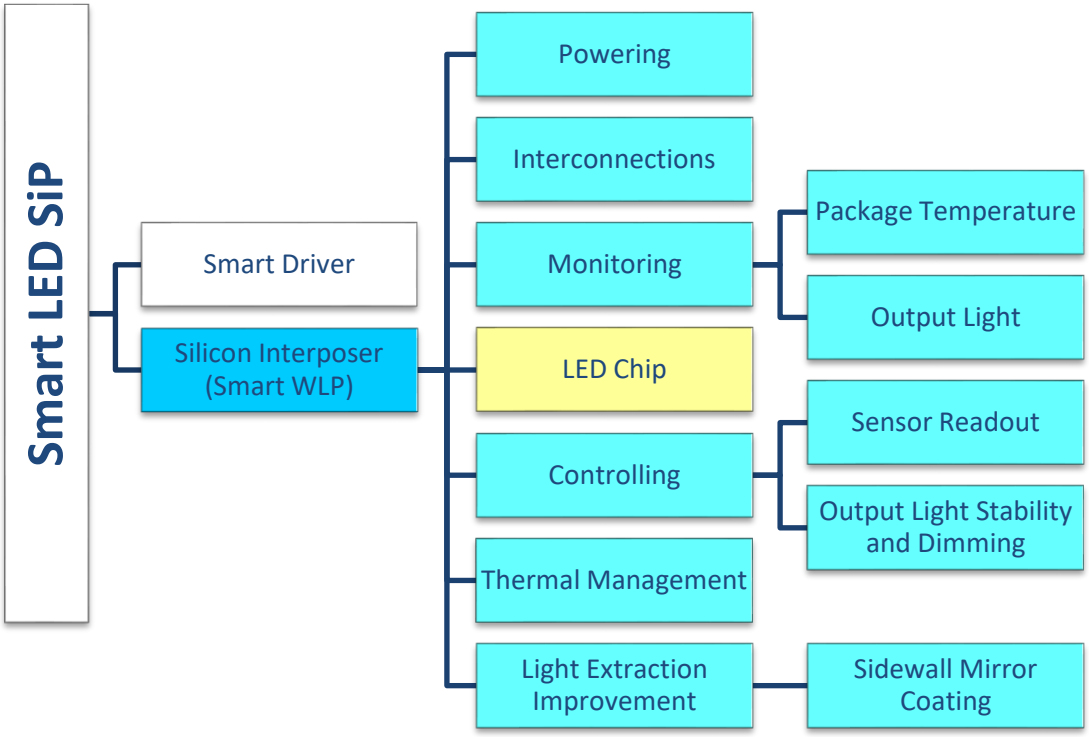



*Figure 1-5: Different functions in a smart LED SiP (scope of this dissertation is shown in color).*

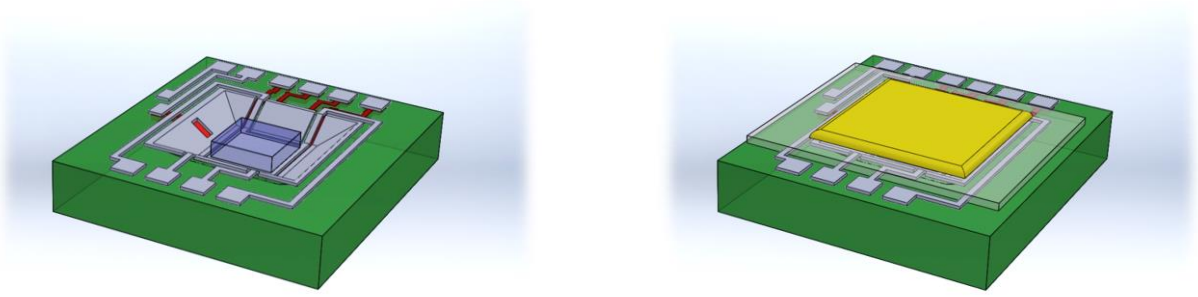
Different functions and operation levels of this system is presented in Figure 1-5. The advantages of such a LED SiP are:

- Capability of wafer-level optics
- Capability of wafer-level phosphor remote coating for stable color uniformity
- Higher brightness efficiency: on chip reflector cup (cavity with mirror coating) reflects the side light and improves light extraction efficiency up to 15%.
- Better thermal management: high thermal conductivity of Si substrate
- Lifetime improvement: self-monitoring system
- High reliability: better interconnect reliability, closed-loop feedback circuit for stability and aging compensation

The 3D system integration processing comprises different steps. The final 3D package containing an active reflector cup and one LED chip is schematically shown in Figure 1-6.

## 1.4 Thesis Outline

This thesis is composed of two parts. In the first part, the principles, design and implementation of a monolithically integrated 2D LED SiP are covered. At first, the required low cost processing scheme is explained. It is followed by description of different components



*(a)* *(b)*

*Figure 1-6: Unit cell of a 3D LED WLP; (a) LED chip is mounted on an active reflector cup including sidewall light sensor, bottom temperature sensor and high aspect ratio litho defined wiring lines, and (b) placement of remote phosphor plate on top of the cup.*

for using in monitoring and controlling blocks in 2D system. This part ends with demonstration of some measurement and simulation results. In the second part, challenges, design and implementation of 3D system are discussed and demonstrated. Primarily, a high aspect ratio (HAR) lithography approach is developed, which is a significant key for 3D processing. Next, the implementation of 3D package is described.

The first part starts from Chapter 2 by a short introduction of BiCMOS5/7 process and the design concept for smart LED package. A cost effective 5-7 mask (1-2 metal layers) BiCMOS process is proposed for integration in LED WLP. This simple BiCMOS process allows on-chip integration of different Si based sensors, functioning blocks and circuits to be used for an advanced lighting system. To utilize this process for IC fabrication, a complete framework from modeling to measurement is suggested.

In Chapter 3, a Si based multi-functional WLP for phosphor-based white LED systems is discussed. The system is designed and manufactured using 7-mask BiCMOS process. This package integrates 4 high-power blue light LED dies with temperature sensors, and blue selective light sensors for monitoring the system performance. Sensors are part of the smart monitoring unit. An interdigitated power transistor and a 4-bit flash analog to digital converter were also integrated and described, which are integrated with sensors' readout and extra controlling functions.

In Chapter 4, the blue selective photodiode is elaborated, which is used for output blue light

evaluation in previous system. It is composed of a Si stripe-shaped photodiode. This chapter presents how this detector shows a high selectivity to blue light with noticeable responsivity comparing to similar reported devices. The maximum responsivity at 480nm is matched with the target blue LED illumination. It also covers the physical simulation of the device and principles.

In Chapter 5, a monolithic light feedback control circuit is proposed. It is an opamp-based feedback circuit combined with a high-power transistor and the blue-selective photodiode, which controls the output light based on real-time sensor data. The new system guarantees a stable and reliable output light under different working conditions. Besides, integrating this module offers that the output light can be controlled linearly by a reference input voltage.

The second part elaborates on how to move our 2D SiP to a 3D package. In this case, a KOH etched cavity in Si interposer makes a high topography that brings up new challenges. It acts as a precision cavity with aluminum coating in place of sidewall mirror. The main challenge is the lithography process steps over a few hundred micrometer topography.

In Chapter 6, we are going to describe a high aspect ratio (HAR) lithography approach that can be used both for the 3D SiP and, in general, for litho-defined lateral wire bonding. Litho-defined wire bonding uses conventional CMOS interconnect toolset and processes in combination with multi-level lithography aiming for “wire bond like” interconnect structures and HAR interconnect. It also enables advanced heterogeneous integration of different components with less reliability issues and problems. This method consists of placing and attaching the chips on supporting substrate, passivation layer deposition, metal deposition and patterning through advanced HAR lithography. At the end, different simulation and experimental results are reported.

In Chapter 7, the final 3D LED SiP is described covering the design concepts, process flow, challenges, and some measurement results. It uses cavity not only as a precision LED site and for its sidewall mirrors, but also as an *active* reflector cup. It is active since the cavity bottom contains local temperature sensors and the sidewalls carry the output light detector in addition to the HAR interconnects. This is for the first time that an active device (the photodiode) is fabricated on sidewall of a silicon cavity. Other controlling circuit described in 2D package is also integrated on Si top surface.

Finally, Chapter 8 concludes this dissertation and presents suggestions for future developments.

## 1.5 References

[1] Wikipedia, “Insects.”

[2] W. Chen, W. Bottoms, K. Pressel, and J. Wolf, “The next step in assembly and packaging: System level integration in the package (SiP),” *ITRS White Pap.*, pp. 1–127, 2008.

[3] ITRS, “International Technology Roadmap for Semiconductors 2.0: Executive Report,” 2015.

[4] T. Tekin, “System-in-package technologies for photonics,” in *SPIE*, 2010, vol. 7605, pp. 760506-760506–12.

[5] M. Wolf and P. Ramm, “Technologies for 3D wafer level heterogeneous integration,” in *Design, Test, Integration and Packaging of MEMS/MOEMS, 2008. MEMS/MOEMS 2008. Symposium on*, 2008, pp. 123–126.

[6] D. D. Lu and C. P. Wong, *Materials for advanced packaging*. 2009.

[7] W. Arden, M. Brillouët, P. Cogez, and M. Graef, “More-than-Moore white paper,” *ITRS White Pap.*, 2010.

[8] J. Lau and X. Zheng, “Failure analyses of 3D Sip (system-in-package) and WLP (wafer-level package) by finite element methods,” *IEEE Proc. 16th IPFA*, 2009.

[9] T. Tekin, “Review of Packaging of Optoelectronic ,” *IEEE J. Sel. Top. QUANTUM Electron.*, vol. 17, no. 3, pp. 704–719, 2011.

[10] K. Morihiro, “The dawn of 3D packaging as system-in-package (SIP),” *IEICE Trans. Electron.*, 2001.

[11] S. Al-Sarawi and D. Abbott, “A review of 3-D packaging technology,” *Manuf. Technol.*, vol. 21, no. 1, pp. 2–14, 1998.

[12] D. Lu and C. P. Wong, *Materials for Advanced Packaging*. Boston, MA: Springer US, 2009.

[13] C. Uchibori and X. Zhang, “Effects of chip-package interaction on mechanical reliability of Cu interconnects for 65nm technology node and beyond,” in *Interconnect Technology*, 2006, no. Vcc, pp. 196–198.

[14] L. Mercado, C. Goldberg, and S. Kuo, “Analysis of flip-chip packaging challenges on copper/low-k interconnects,” *IEEE Trans. DEVICE Mater. Reliab.*, vol. 3, no. 4, pp. 111–118, 2003.

[15] C.-T. Ko, K.-N. Chen, W.-C. Lo, C.-A. Cheng, W.-C. Huang, Z.-C. Hsiao, H.-C. Fu, and

Y.-H. Chen, “Wafer-level 3D integration using hybrid bonding,” in *2010 IEEE International 3D Systems Integration Conference (3DIC)*, 2010, pp. 1–4.

[16] “Haitz’s law,” *Nat. Photonics*, vol. 1, no. 1, p. 23, Jan. 2007.

[17] W. D. van Driel and X. J. Fan, Eds., *Solid State Lighting Reliability*. New York, NY: Springer New York, 2013.

[18] S. W. R. Lee, R. Zhang, K. Chen, and J. C. C. Lo, “Emerging trend for LED wafer level packaging,” *Front. Optoelectron.*, vol. 5, pp. 119–125, 2012.

[19] M. Hornung, “LED Wafer Level Packaging – Motivation, Challenges and Solutions to Meet Future Cost Targets,” *SUSS Rep. 02/2012*, 2012.

[20] A. Ivankovic, T. Buisson, S. Kumar, A. Pizzagalli, and R. Beica (YOLE Developpement), “YOLE Report: Status of Advanced Packaging Industry,” 2015.

# Part I:

# Monolithically Integrated Smart Silicon Interposer Utilized for 2D LED SiP

# Chapter 2

# Introduction to BiCMOS5/7 Process and Design Concept for Smart LED Package[1]

In this chapter, a cost effective 5-7 mask BiCMOS process, proposed for integration in LED WLP, is demonstrated. This straightforward BiCMOS process allows on-chip integration of different silicon-based sensors, functional blocks and circuits to be used for advanced lighting systems. To utilize this process for IC fabrication, a complete framework from modeling to measurement is suggested. This approach is also useful for heterogeneous integration in applications with rather large area and low cost requirements.

## 2.1 Introduction

Currently, the advanced ICs are quite complex. Transistor count is the most common measure of IC complexity. Today, modern CPUs have over 7 billion transistors integrated in a chip and each device must perform a specific function [1]. The extremely high demands on the processing are pushing the equipment suppliers to deliver machines that not only can produce ICs with high yield, but also with the lowest cost. While the cost per transistor is reduced in advanced IC technology, in contrast, the cost per area is increasing rapidly. Consequently, using

[1] The BiCMOS5 process was firstly designed and developed in Dimes Technology Center in 2010 by Dr. Henk van Zeijl. The models and frameworks in this chapter are developed in cooperation with MSc student Teng Ma [3].

advanced and high cost processing for large area applications is not practical.

The CMOS and MEMS technologies provide a broad technology portfolio with many applications for solid-state lighting (SSL). However, for LED wafer level packaging (WLP), due to large nature of each LED die (mm range), high Si throughput is not possible. To reduce the fabrication cost, process should be at the lowest cost. So, to make WLP reasonable for SSL, a reliable fabrication process is required which should be simple, robust, flexible, and low cost. Moreover, it should be able to fulfil the requirements to build active electronics and sensors. In Dimes Technology Center[2], a BiCMOS process with only 5 to 7 mask steps (BiCMOS5/7), comprising 1-2 metal layers, was developed which shows a possible direction towards building basic electronics by using unconventional metallization steps [2]. Nevertheless, it had never been employed for IC design. In this chapter, we introduce the concept and a framework for IC design based on BiCMOS5/7. This approach can open new areas for heterogeneous integration in broad range of applications such as smart interposers and lab on chips.

This chapter is organized as follows: in Section 2.2, we are going to present the general idea of BiCMOS5/7 process and the main process steps. In Section 2.3, layout of BiCMOS test die including its main devices is described. Section 2.4, suggests an IC design framework based on BiCMOS5/7 from device modeling to wafer level implementation and measurements. In Section 2.5, we talk about using BiCMOS for smart LED wafer level packaging. Finally, it will end by a short conclusion of the chapter.

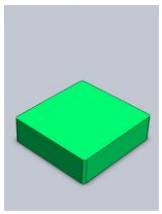
## 2.2 Methodology

The BICMOS5 process was firstly designed by Dr. ir. Henk van Zeijl for education purposes [3]. However, its rather low cost and simple nature motivated us to use it as a base process for monolithically integration of different devices in LED WLP. The main characteristics of the process are: simple technology in terms of layout and process steps, while at the same time three main devices are being fabricated; NPN bipolar transistor, NMOS, and PMOS [2]. Table 2-1 lists core of the process consists of 5 mask steps. A brief process overview is given in Figure 2-1. More detailed outline of the process is summarized in Table 2-2. The three main devices are illustrated in Figure 2-2.

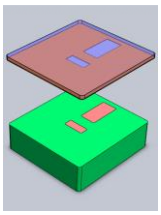
[2] The Dimes Technology Center affiliation is changed to Else Kooi Lab, EKL, from April 2015.

*Table 2-1: Core process mask steps of the BICMOS5/7 process (the grey shaded ones are added for BiCOMS7).*

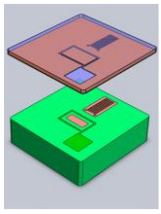
| Mask name | Main purpose |
|---|---|
| NW | – N-type area for the PMOS transistor (N-well) and for the collector of the bipolar transistor |
| SN | – N-type source-drain for the NMOS transistor and for the emitter of the bipolar transistor.<br>– Low resistance collector contact<br>– N-type guard ring |
| SP | – P-type source-drain for the PMOS transistor and for the base of the bipolar transistor<br>– P-type guard ring |
| CO | – Contact openings |
| IC | – Interconnect and gate material |
| VIA | – VIA openings |
| IC2 | – Second interconnect layer |



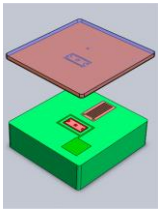
***(a) Start material: p-type silicon.***



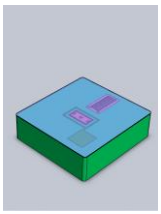
***(b) Mask 1 is used for patterning the phosphor implant and deep diffusion of n-well and n-type collector.***



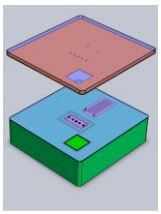
***(c) Mask 2 is used for patterning the shallow boron implant for p-type source/drain and p-type base.***



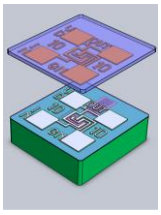
***(d) Mask 3 is used for patterning the shallow arsenic implant for n-type source/drain and n-type emitter.***



***(e) The wafer is annealed and the surface is thermally oxidized (100 nm $SiO_2$).***



***(f) Mask 4 is used for contact opening and wet chemical etching.***



***(g) Mask 5 is used for interconnect metal. AlSi (1%) is deposited using PVD and patterned and etched with dry etching process.***

*Figure 2-1: Process overview of the core steps in the BICMOS5 process.*

*Table 2-2: Outline of BiCMOS5 Process*

| Process | Mask Name | Process Description |
|---|---|---|
| Substrate | | Silicon, $10^{16}cm^{-3}$ boron doped |
| Oxidation | | 20 nm thermal oxidation of silicon |
| N-well implantation | NW | Low dose high energy phosphorus implantation |
| N-well drive-in | | 1100 °C, 4 hours diffusion to form the NPN collector and the N-well for the PMOS |
| Shallow N implantation | SN | High dose low energy arsenic implantation to form the NPN emitter and the NMOS source and drain |
| Shallow P implantation | SP | Medium dose medium energy boron implantation to form the NPN base and the PMOS source and drain. |
| Gate oxidation | | 1000 °C anneal and dry oxidation to activate the dopants and form the gate oxide of 100 nm. |
| Contact opening etch | CO | Wet etch thermal silicon dioxide |
| Metal deposition | | AlSi (1%) sputtering to deposit the gate electrode and interconnect metal |
| Metal pattern etch | IC | Wet or dry etch the metal pattern |
| Alloying | | Alloying by annealing at 400 °C in forming gas |

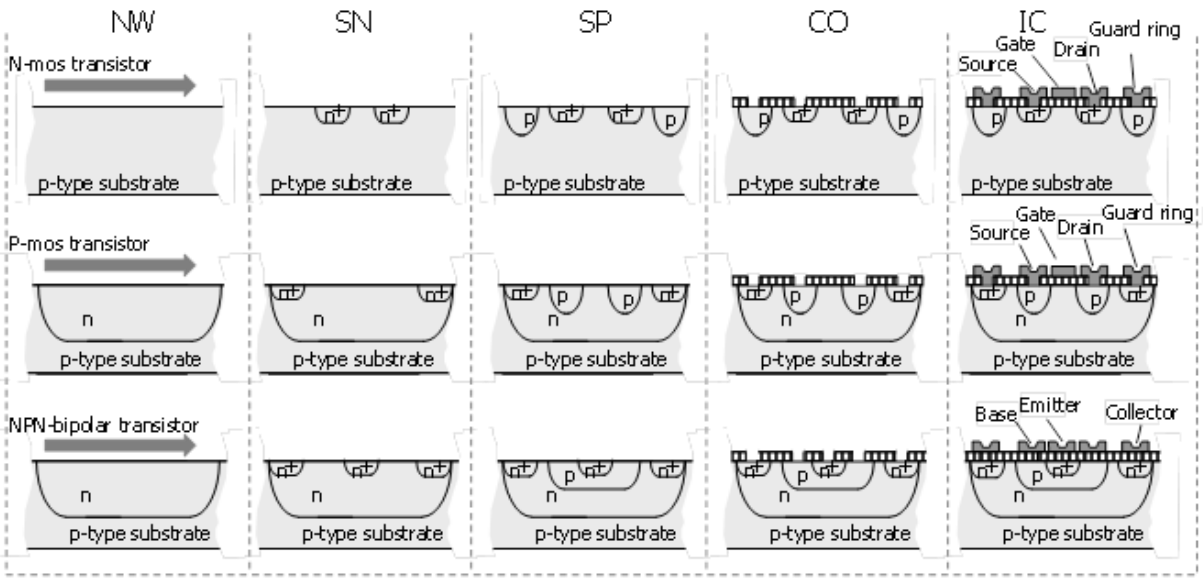



*Figure 2-2: Formation of three main devices: NMOS, PMOS, and NPN bipolar transistors during 5 mask steps of BiCMOS5.*

*Table 2-3: Additional process steps of the BICMOS5 process.*

| Mask name | Main purpose |
|---|---|
| BN | Buried N layer to reduce the collector resistance of the NPN transistor. This process requires an epitaxial silicon deposition process after the BN process. |
| PP | The dopant concentration of the P-type source drain implant is limited because this implantation is also used for the NPN-base implant. To reduce the PMOS source drain resistance, a higher dopant concentration is applied. |
| $V_T$ adjust | To adjust the threshold of the MOS devices, a blanket boron implantation is applied |

The core process requires tight tolerances on the P-type substrate doping; $1\times10^{16}$ $cm^{-3}$. The available P-type wafers at DIMES TC has much wider specifications (2-5 Ω·cm) which corresponds $7–3\times10^{15}$ $cm^{-3}$. We can make it in two ways: epitaxy and extra implantation (to adjust the threshold voltage of the MOSFETs). As epitaxy is a complicated and expensive process, an alternative would be to add a blanket high energy/ multi-energy boron implant and anneal to obtain the required dopant concentration. Also, the threshold voltage ($V_T$) adjust implantation, can be tuned. The dose and parameters of both methods can be tuned based on resistivity measurements of substrate wafers. However, using epitaxial layer is recommended for more reliable results.

Obviously, with only 5 masking layers; three diffusions, one contact opening and one metallization, the device performance is not ideally optimized. Additional process steps can be added to improve the PMOS and the NPN transistors. Those process steps are listed in Table 2-3.

At the end, the electrical characterization is performed and the difference in the relevant transistor parameters are studied in relation to the process variations. The $V_T$ adjust is usually implanted on 3 quadrants on the wafer with 3 different implantation dose, see Figure 2-3.

For BiCMOS7 just two more mask steps are added, for opening VIA's and patterning second interconnect layer. They are shown in grey shaded rows of Table 2-1. The corresponding additional process steps, summarized in Table 2-4, are added before final alloying.

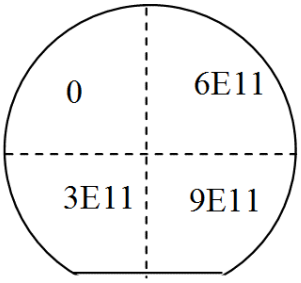



*Figure 2-3: Dose variations (in $cm^{-2}$) of the boron implantation for $V_T$ adjust. The implantation energy is 25 keV.*

*Table 2-4: Additional process steps of the BICMOS7 process.*

| Process | Mask Name | Process Description |
|---|---|---|
| Isolation layer deposition | | $SiO_2$ deposition @ 400°C with CVD |
| VIA etch | VIA | Dry etch CVD silicon dioxide |
| Metal deposition | | AlSi (1%) sputtering to deposit the second interconnect metal |
| Metal pattern etch | IC2 | Wet or dry etch the metal pattern |

## 2.3 Layout of BiCMOS Test Die

The test devices to be characterized are designed in a 6×6$mm^2$ test die. The die layout is given in Figure 2-4(a). The test chip contains different devices and test structures designed to measure the variation and parameters of process steps and characterize the transistors, resistors, etc. The devices are organized in groups called cells (see Figure 2-4(b)). Each cell is indicated with a red rectangle and a number in the die. The most relevant cells are marked and will be discussed in the following. The regular pattern of the contact pads makes it easy to do automated measurements with a probe station.

Figure 2-5 gives the layout of a set of NMOS test transistors with gate width of 20 µm. They are from cell number 2 and 3 in Figure 2-4(b). The lithographically defined gate length is indicated near the transistor. Due to the out-diffusion of the source/drain dopants, the effective gate length is much smaller. There are two columns of identical sets of test transistors for redundancy purposes. For each test structure or test device, the functions of the terminals are indicated in the interconnect pattern.

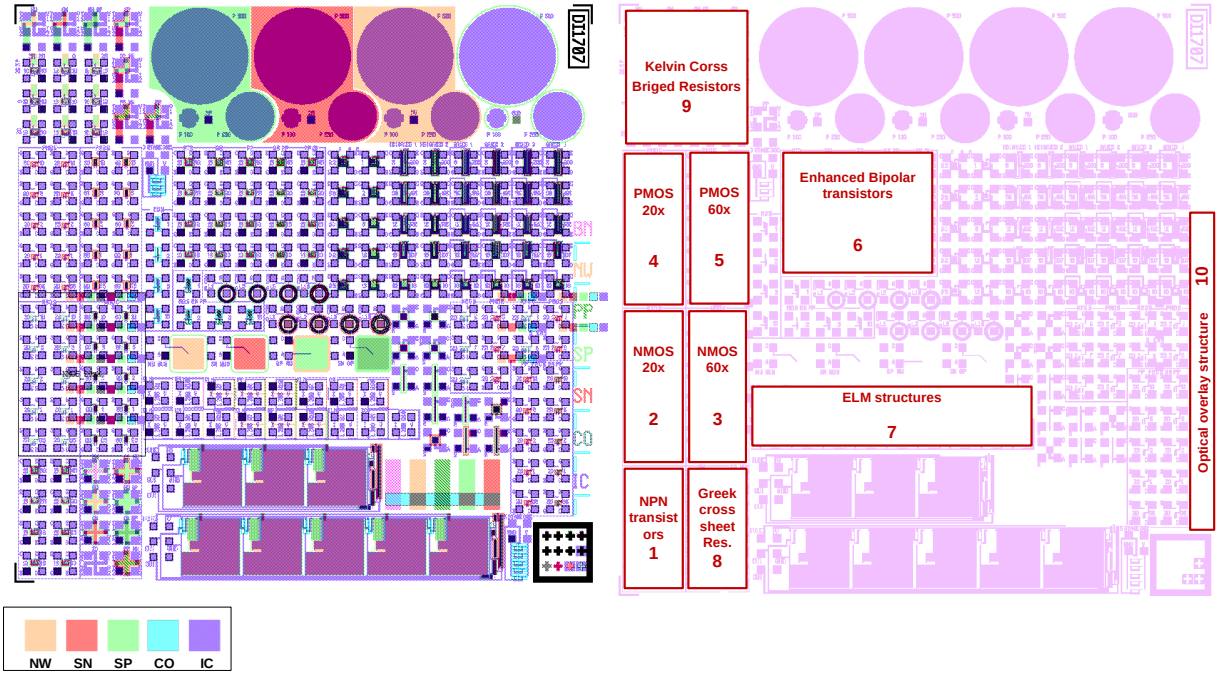



*Figure 2-4: BiCMOS5 test structures: (a) die layout, and (b) different cells.*

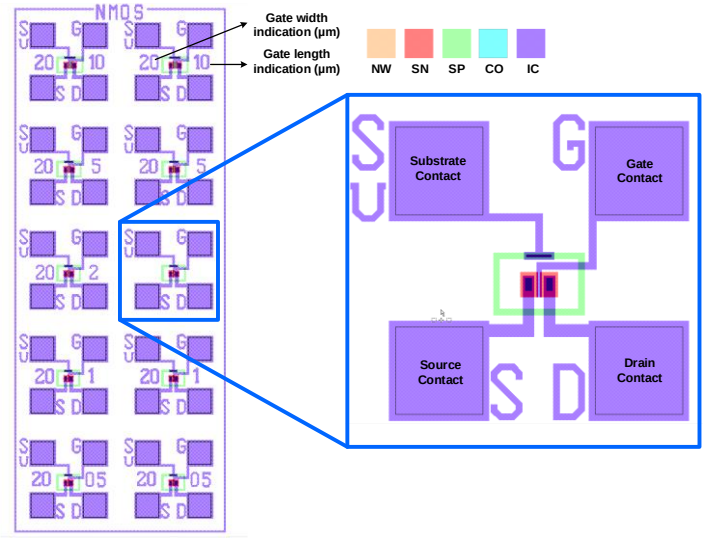



*Figure 2-5: Layout of a set of NMOS transistors with gate width of 20 µm for test purposes.*

The same test structures are included for PMOS transistors in cell number 4 and 5 in Figure 2-4(b).

Figure 2-6 gives the layout of a set of NPN bipolar test transistors with different area from cell number 1 in Figure 2-4(b). The emitter area is indicated near the transistor.

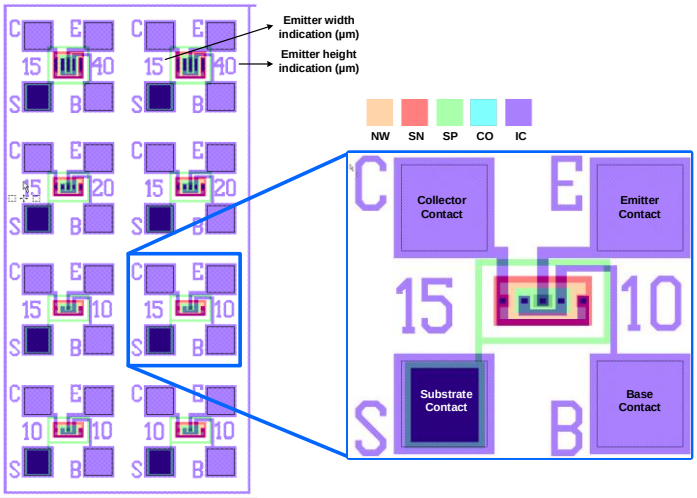



*Figure 2-6: Layout of set of NPN bipolar transistors with different emitter areas for test purposes.*

There are also some process control test structures such as: electrical linewidth measurement (ELM) structures (cell number 7), Greek cross sheet resistance structures (cell number 8), cross bridge Kelvin resistors (cell number 9), and optical overlay test structures (cell number 10).

The sheet resistance is measured using the Greek cross structures. These structures make it possible to measure the sheet resistance of the different layers on the processing wafer [4]. The contact resistance is a measure for the resistance between two layers, for instance between interconnect and doped areas. A contact resistance exists due to a bandgap difference between two contacting materials. It can be measured by using a cross bridge Kelvin resistor [5].

## 2.4 Design Framework Based on BICMOS 5/7

BICMOS5 process was firstly developed in Dimes Technology Center in 2010. However, it had never been employed for IC design. The five-mask process basically meets the fabrication requirements for single components and small circuits. For the very large scale integrated circuit (VLSI) designs, more metal layers are needed. For extra metal, two additional masks are required (for patterning and etching the vias between the metals, and the second metal interconnects).

For IC design panel, making reliable device models is critical. They are later imported in circuit design tool as a reference design library. The model types are different for various simulation tools. $BSIM_3V_3$, as one of the most used MOSFET model in H-Spice simulator, is chosen for our modeling. For physical verification of the design, we should also develop design

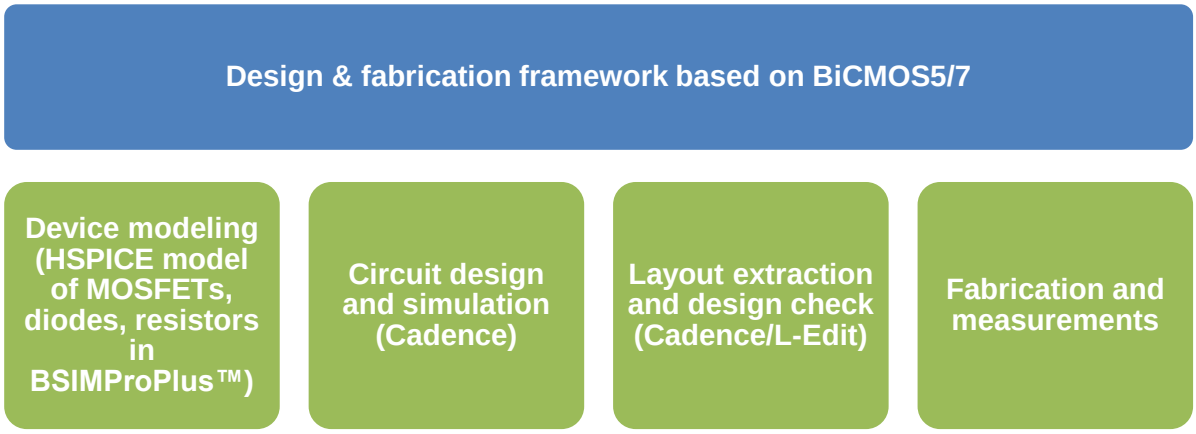





*Figure 2-7: Design and fabrication framework for BiCMOS process.*

rule check (DRC) and layout versus schematic (LVS) check based on our process features and limitations.

The models and design check regulations should be built up before starting the final design. In this section, a complete framework is proposed[3].

Figure 2-7 shows the proposed design framework for BICMOS process. It mainly consists of four phases:

- Firstly, full characterization of the devices is done and HSPICE models for MOSFETs, diodes, and passive components are extracted using BSIMProPlus™ tool.
- Secondly, the complete model is introduced into Cadence CAD tool for circuit design and simulation.
- Thirdly, the correspond circuit layouts are sketched by applying DRC and LVS check. These checking files should be compiled based on the process criteria and design requirements. The complete layout can be transferred into L-Edit tool in order to finalize the ".tdb" mask file to produce the masks for fabrication process.
- Finally, the ICs are fabricated through BICMOS process in DIMES cleanroom 100. Then, measurement are done in both wafer/PCB-level. The feedbacks based on measurement results can be applied to the previous steps to revise/optimize the design.

The following subsections are going to describe each step in detail.

[3] Thanks for the efforts made by Xiaochen Zhang, Jianzhao Chen and Hua Dong from UESTC. They firstly proposed a preliminary design framework based on DIMES BICMOS process in 2013.

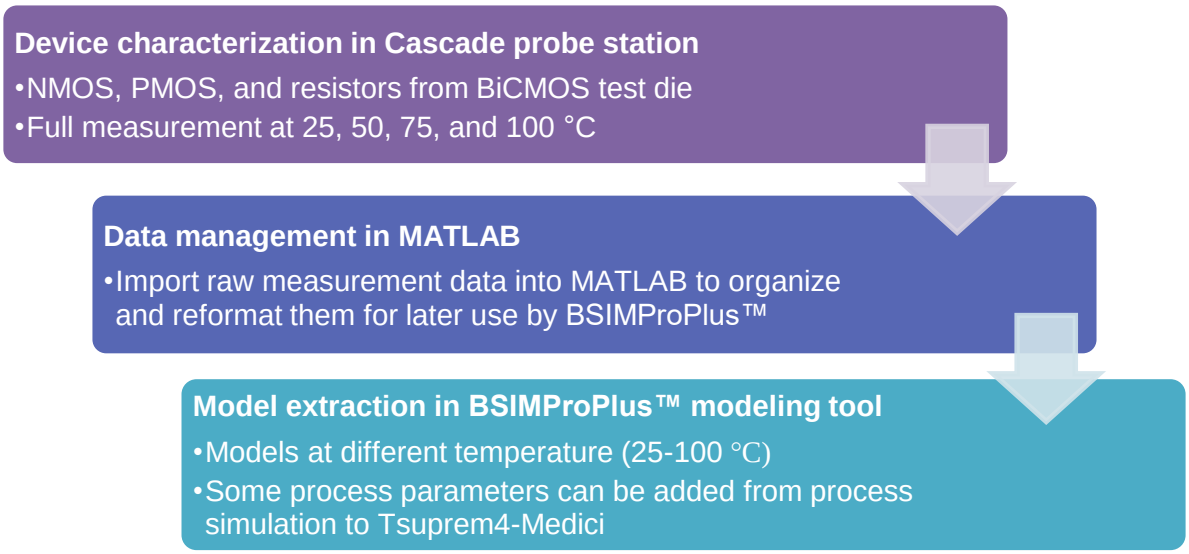



*Figure 2-8: Device modeling steps.*

### 2.4.1 Device Modeling

The steps are summarized in Figure 2-8. Initially, all the devices, such as NMOS, PMOS, and diodes incorporated in the BiCMOS test die are electrically characterized on the Cascade probe station. The current/voltage data are automatically recorded by a control system. For later investigation of temperature effect on our ICs, the devices are characterized at 25, 50, 75 and 100 °C. Since the BSIMProPlus™ modeling tool, can only handle certain format of data, the raw data should be organized in MATLAB. Finally, the formatted data can be loaded into BSIMProPlus™ for model extraction. With a proper extraction scheme, the output $BSIM_3V_3$ models have a small average error and good consistency with the measurement results. Some process parameters like junction depth can be determined by means of process simulation. In the design phase, these models can be directly used in circuit design tool.

### 2.4.2 Circuit Design and Simulation

To setup the library of components in Cadence, the models generated in the previous step are imported into Cadence CAD environment. In Cadence design environment, first the single components and later the circuits are designed and interconnected. In next step, the designed blocks are simulated by H-spice simulator within analog design environment (ADE). In order to study the package temperature effects on circuit performance, different temperature models from 25 to100 °C can be switched over during simulation. Based on simulation results, the design can

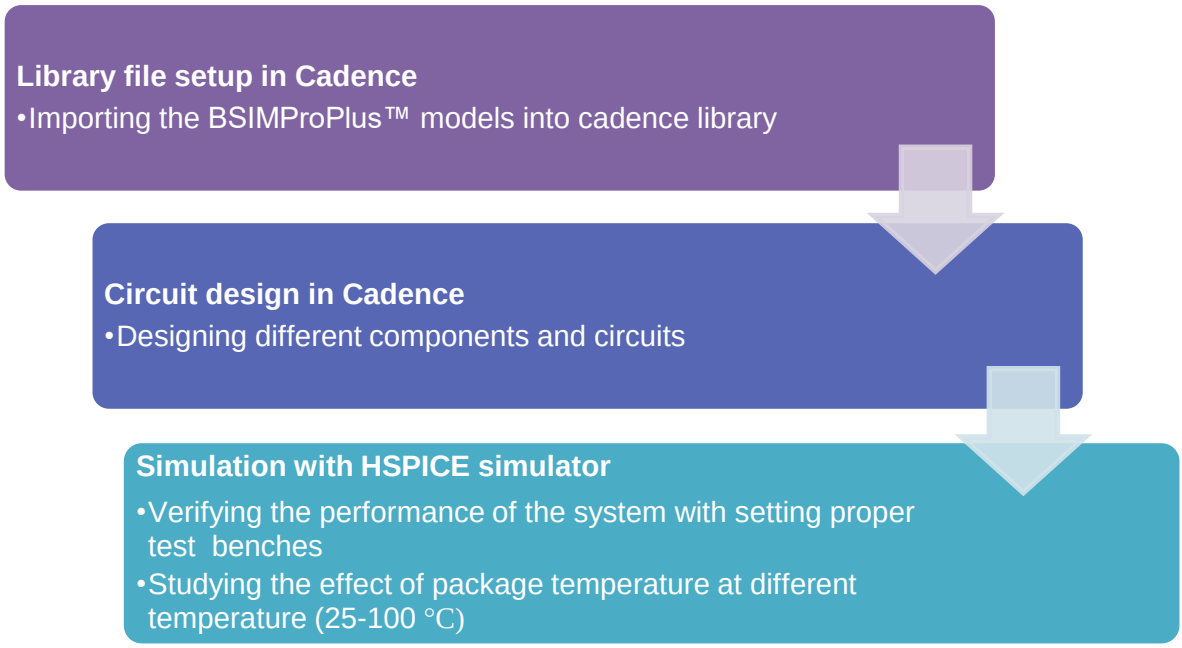



*Figure 2-9: Circuit design and simulation steps.*

be enhanced to optimize the performance under required conditions. The design flow is shown in Figure 2-9.

### 2.4.3 Layout Extraction and Design Check

First of all, the layers according to each mask step of BiCMOS process should be defined, each layer with its own name and functionality. Additionally, for preventing unwanted errors in the layout, we should think of some checking strategy. For layout inspection, a checking tool called “Calibre”, from Mentor Graphics Inc., is available in Cadence environment. There are two main physical verifications, which are design rule check (DRC) and layout versus schematic (LVS) check. The DRC ensures all the layout geometries such as line width, clearance, area, etc. are within the acceptable range for fabrication. The LVS check is to make sure that the drawn layout is exactly corresponding to the same circuit as the schematic design is. However, it is necessary to compile two rule files for the DRC and LVS, based on BiCMOS process conditions and design requirements in advance.

Following, the layout is sketched in a hierarchy mode, from low to high level. Besides, some sub-circuit blocks can be added as process control modules for quick test on the wafer level. Then, it is necessary to perform the rule checks (DRC and LVS) on the whole layout and modify it if needed. For some applications, it is also recommended to do post layout extraction and

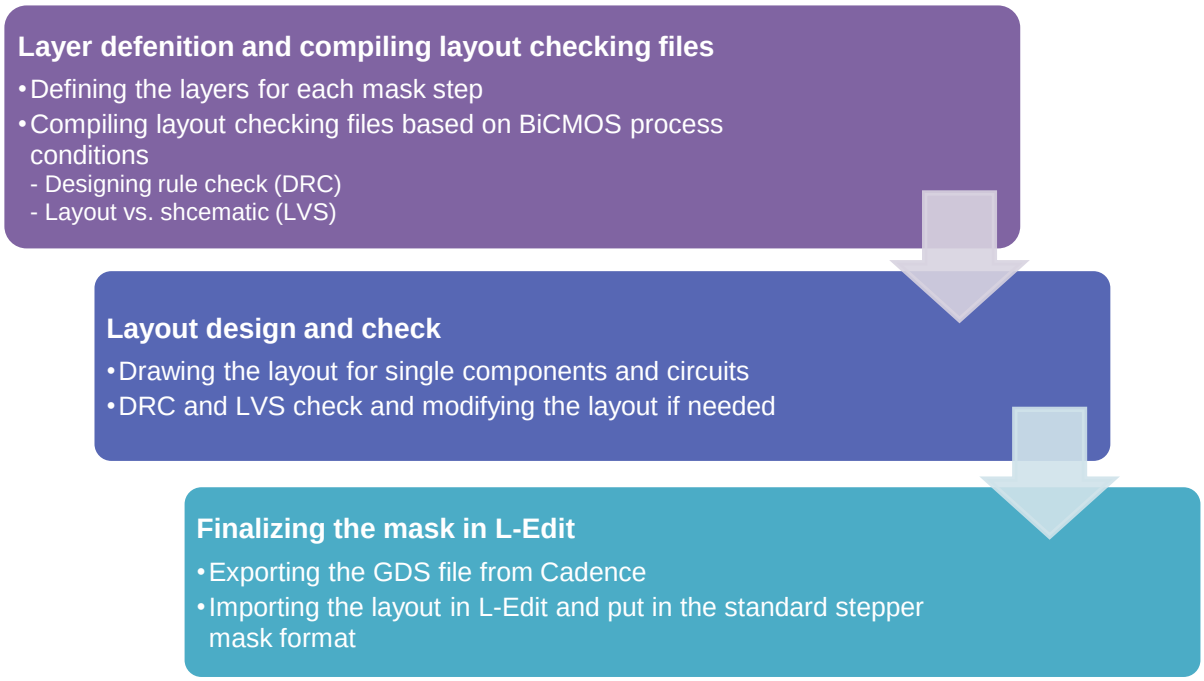



*Figure 2-10: Layout extraction steps.*

investigate the parasites and their influences on our target performance.

As a final step, the complete circuit layout is exported as a GDS file and imported into another layout edit tool called "L-Edit", to finalize the mask layout in stepper format. These steps are depicted in Figure 2-10.

### 2.4.4 Fabrication and Measurements

Based on the final die layout, the stepper chromic masks are printed. The process is done in EKL clean-room 100 on 4-inch wafers. For process evaluation and calibration in all the BiCMOS runs, at least 4 BiCMOS test dies are included in wafer layout (1 in each wafer quadrant). They are generally considered as process control modules (PCM). BiCMOS5 flowchart comprises almost 90 steps. For BiCMOS7, some extra steps are added for 2$^{nd}$ metal layer.

Small blocks, some sensors, and devices can be directly measured on probe station. For bigger circuits with larger number of I/O terminals and special measurements for some of the devices, tests should be done on printing circuit board (PCB). So, dies are diced and packaged. They will be later assembled on pre-designed PCBs. Figure 2-11 summarized the steps.

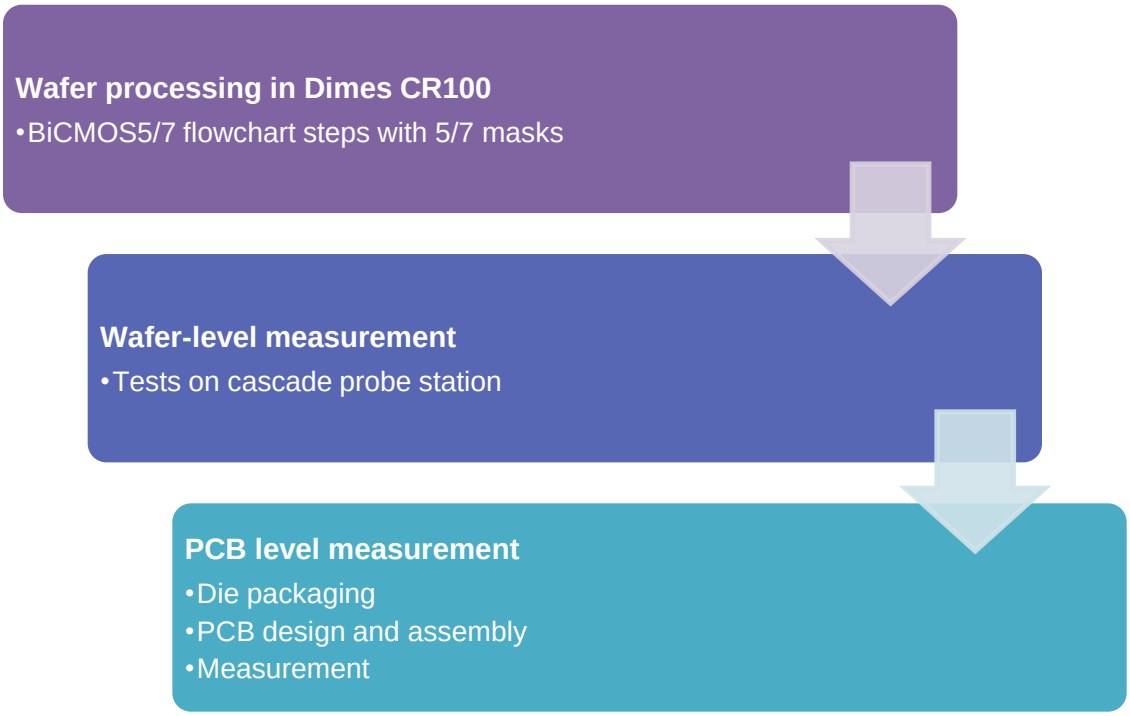



*Figure 2-11: Fabrication and measurements steps.*

## 2.5 Smart LED Package Runs (SMACK)

In different parts of this project, several BiCMOS runs were carried out. The optical part was designed in 4.5×10 $mm^2$ die size, for integrating 4 LED chips with corresponding sensors and circuits. It will be discussed in next chapters. For sensor readout system, an electrical part was also added and so the full die size became 10×10 $mm^2$.

To develop the previously discussed framework, device modeling was done for MOS transistors, resistors, and diodes. The IV measurements were performed for both NMOS and PMOS transistors with 3 different channel lengths (2, 5 and 10 μm) and 2 different channel widths (20 and 60 μm) to obtain a broad overview of device characteristics. The data is then organized to be imported into BSIMProPlus™ for model extraction.

The transfer ($I_{DS}$ $-V_{GS}$) and output characteristics ($I_{DS}$ − $V_{DS}$) of the transistors were measured. The source was grounded for both NMOS and PMOS. The biasing conditions for both NMOS and PMOS for IV characterizations are tabulated in Table 2-5 and Table 2-6.

*Table 2-5: NMOS biasing conditions for IV characterization.*

| I-V data | $V_{GS}$ (V) | $V_{DS}$ (V) | $V_{BS}$ (V) |
|---|---|---|---|
| $I_{DS}$ -$V_{GS}$ | $-7 \leq V_{GS} \leq 7$<br>Step= 0.2 V | $V_{DS}$ = 0.1 V (Linear mode)<br>$V_{DS}$ =7 V (Saturation mode) | $-7 \leq V_{BS} \leq 7$<br>Step =1 V |
| $I_{DS}$ –$V_{DS}$ | $1 \leq V_{GS} \leq 7$<br>Step= 1 V | $0 \leq V_{DS} \leq 7$<br>Step= 0.1 V | $V_{BS}$ = 0 V<br>$V_{BS}$ =-7 V |

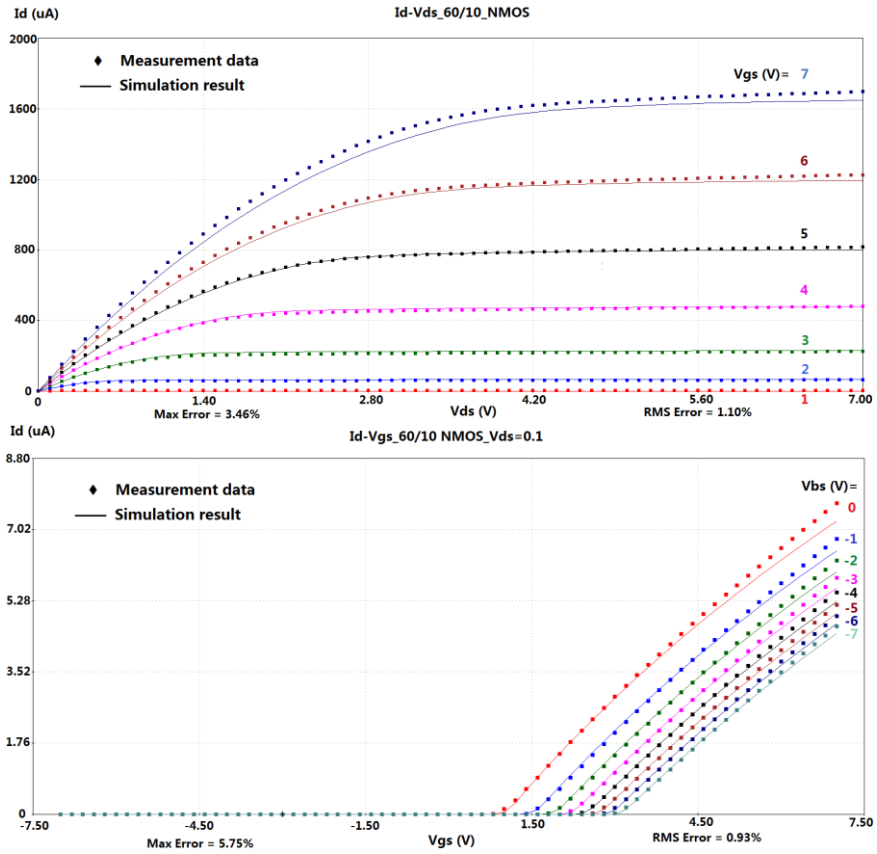
*Table 2-6: PMOS biasing conditions for IV characterization.*

| I-V data | $V_{GS}$ (V) | $V_{DS}$ (V) | $V_{BS}$ (V) |
|---|---|---|---|
| $I_{DS}$ -$V_{GS}$ | $-10 \leq V_{GS} \leq 5$<br>Step= 0.2 V | $V_{DS}$ = - 0.1 V (Linear mode)<br>$V_{DS}$ = -7 V (Saturation mode) | $0 \leq V_{BS} \leq 7$<br>Step =1 V |
| $I_{DS}$ –$V_{DS}$ | $-8 \leq V_{GS} \leq -2$<br>Step= 1 V | $-7 \leq V_{DS} \leq 0$<br>Step= 0.1 V | $V_{BS}$ = 0 V<br>$V_{BS}$ = 3 V |

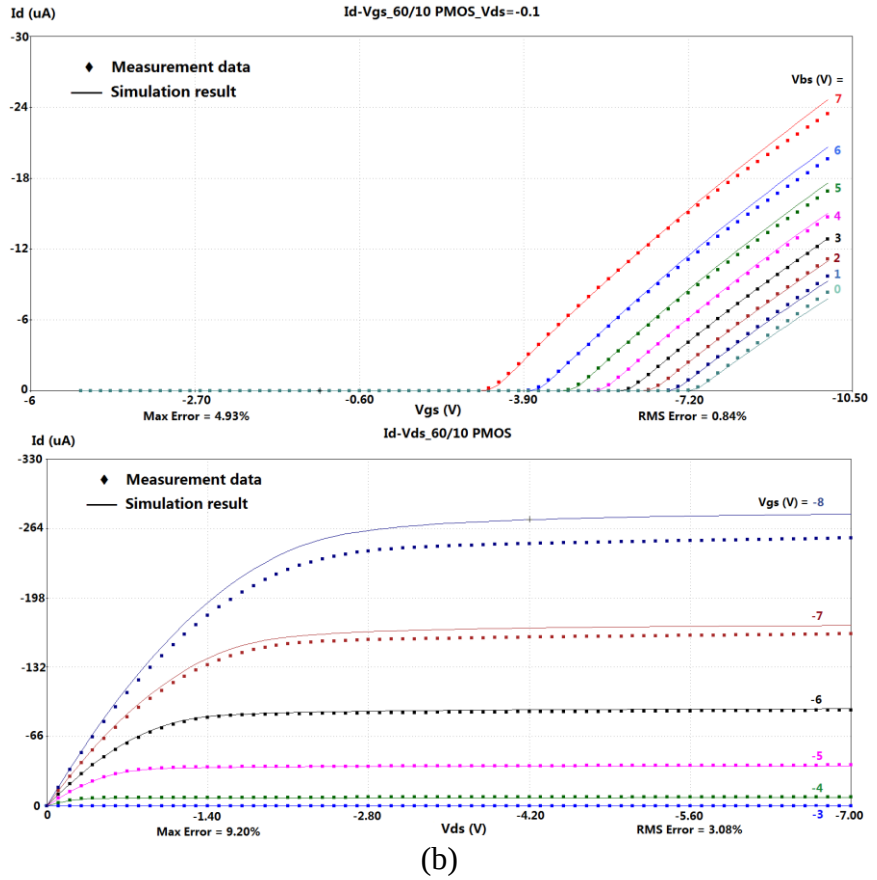
Furthermore, to investigate the temperature effects on the designed blocks, four models were extracted based on the data measured at 25, 50, 75, and 100 °C. Cascade probe station, Agilent 4155B parameter analyzer, and temperature controller were utilized as the main test equipment.

Due to the out-diffusion of the source/drain dopants, the transistors with gate length smaller than 1 μm do not work properly. The ones with gate length smaller than 2 μm have very serious channel length modulation effect.

$BSIM_3V_3$ is a scalable model that can cover a wide geometry range with one set of model parameters. To generate initial device models, the strategy here is to use global parameters as the extraction method. Based on the Tsuprem-4 and Medici simulation results and process data, some extraction parameters such as gate oxide thickness, substrate doping concentration and junction depth can be optimized. The optimized model shows a better accuracy and it can precisely reproduce the IV characteristics of actual devices. Figure 2-12(a-b) show the measurement and simulation results at 25 °C for W/L=60μm/10μm NMOS and PMOS, respectively. It shows a good agreement between the model and the actual measurement data. Also, the average error is acceptable for the target voltage range. The threshold voltage in the wafers with epi layer, using 3E11 $cm^{-2}$ $V_T$ adjust dose, is 1 V for NMOS and -3.5 V for PMOS.




(a)




(b)

*Figure 2-12: IV characteristics for device modeling of (a) NMOS and (b) PMOS at 25 °C.*

*Table 2-7: NPN biasing conditions for IV characterization of diodes.*

| I-V data | $V_B$ (V) | $V_E$ (V) | $V_C$ (V) | $V_S$ (V) |
|---|---|---|---|---|
| $I_E$ –$V_{BE}$ | 0 *V* | $-1 \leq V_E \leq 1$ Step =0.01 V | 0 *V* | 0 *V* |

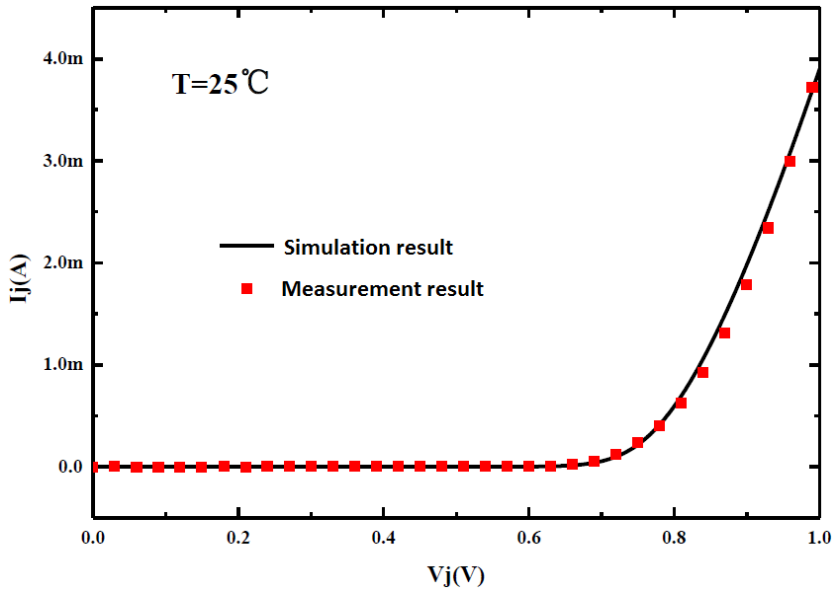



*Figure 2-13: Ij vs. Vj of base-emitter junction diode at 25°C.*

Base-emitter (BE) junction of a NPN bipolar junction transistor was used as a diode in our designs. The IV characterizations were performed at four different temperatures (25 – 100 °C) to obtain a wide overview of the device characteristics. The measurement data was converted into a specific format for BSIMProPlus™ and the model parameters were extracted. The biasing conditions are summarized in Table 2-7.

Figure 2-13 shows the comparison of simulation and measurement results at 25 °C for BE diode. The simulation results are well consistent with the measurement results.

As BiCMOS does not include a Poly-silicon layer, the resistors are implemented using shallow-N (SN). We mainly considered the out-diffusion effect, and voltage and temperature coefficients during resistor modeling. Due to the lateral diffusion of dopants, the effective width of resistor is bigger than layout width. This error is not related to layout width but to the process. The effective width of resistor equals W+dw. Then resistance is

$$R = R_{\blacksquare} \frac{L}{W+dW}, \tag{2.1}$$

*Table 2-8: Temperature and voltage coefficients of 10 µm SN Resistor.*

| Length | TC1(ppm/°C) | TC2(ppm/°C) | VC1 (ppm/V) | VC2 (ppm/V) |
|---|---|---|---|---|
| 10 µm | 1559 | 0.464 | 646.17 | 27.82 |

where $R$ is the resistance value, $R_{\blacksquare}$ is the sheet resistance and $L$ is the length of SN resistor.



Linear data fitting method were used to characterize the relation of conductance with layout width. For 10 µm width, the lateral diffusion was determined as 0.62 µm.

Temperature and voltage coefficients were also extracted. The relation of resistance with temperature ($T$) is a complicated non-linear relationship. Quadratic polynomial data fitting method were used to describe this non-linear relationship. $T_{Factor}$ as the temperature effect coefficient for resistance value is considered

$$T_{Factor} = 1 + TC1 \times T + TC2 \times T^2, \tag{2.2}$$

where *TC1* and *TC2* are 1st and 2nd order coefficients that are extracted with data fitting. The change of the thickness of depletion region between $N^+$ dopant region (SN area) and P-sub with applied voltage ($V$) will impact the effective sectional area of resistor, i.e. the resistance will change with the applied voltage. By using quadratic polynomial data fitting method, we get the relation of resistance with applied voltage. ΔV- Factor as the voltage coefficient for resistance value is modeled,

$$\Delta V_{Factor} = 1 + VC1 \times V + VC2 \times V^2, \tag{2.3}$$

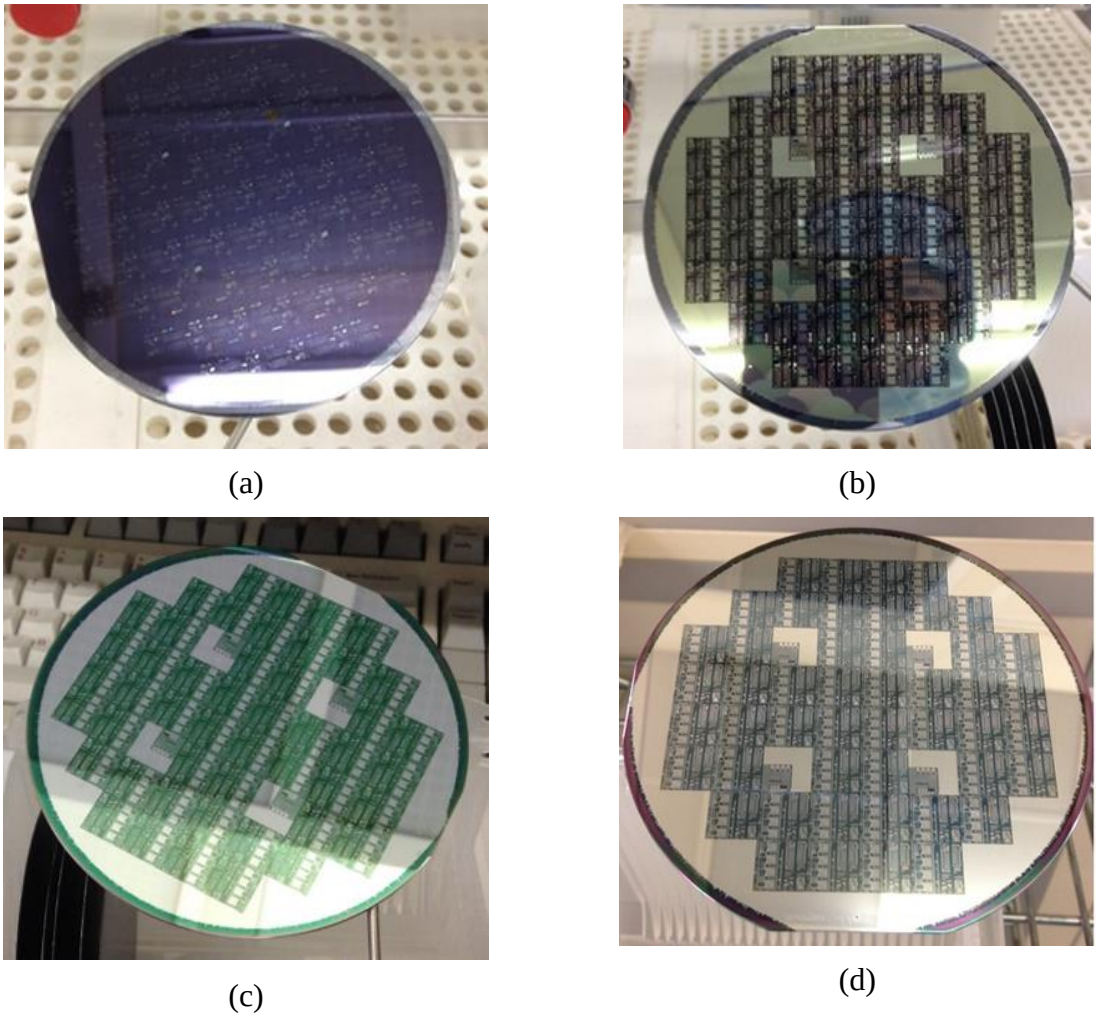
where *VC1* and *VC2* are 1st and 2nd order voltage coefficients that are extracted with data fitting. In summary, the temperature coefficient and voltage coefficient of a 10 µm SN resistor are shown in Table 2-8.

Considering the above coefficients, the sheet resistance is $R_{\blacksquare} = 52.21\ \Omega$.

The models were later used for IC design. The wafers were split into two branches for different $V_T$ adjust implantation parameters. Figure 2-14 shows a wafer in SMACK run through different BiCMOS7 steps. The details on achieved results will be presented in next chapters.

## 2.6 Conclusions

In this chapter, the BICMOS5/7 process was introduced. It is a simple process that by just using 5-7 mask steps can monolithically implement different devices such as MOSFETs, BJTs,



(a) (b)

(c) (d)

*Figure 2-14: SMACK wafers through BiCMOS7 process run, (a) after NW, SN, and SP implantation, (b) with first metal pattern, (c) after VIA patterning, and (d) the complete wafer with second metal patterns.*

diodes, and resistors. Due to large die size of LED chips, BiCMOS5/7 has a large potential to be utilized for WLP of smart LED systems. A design and fabrication framework based on BICMOS process was suggested. This framework covers the whole process from device modeling to system fabrication and measurements. It can be well applied for circuit design based on BiCMOS process. In addition, modeling of some of the devices used for smart LED package was discussed that will be later used in next chapters.

## 2.7 References

[1] "ISSCC Technology Trend," 2015.

[2] N. S. Lawand, H. van Zeijl, P. J. French, J. J. Briaire, and J. H. M. Frijns, "Titanium nitride (TiN) as a gate material in BiCMOS devices for biomedical implants," in *IEEE Sensors*, 2013, pp. 1–4.

[3] T. Ma, "Monolithic integration of light sensor readout system for multi-functional LED wafer-level packaging based on BICMOS process," TU Delft, 2014.

[4] S. Enderling, C. L. Brown, S. Smith, M. H. Dicks, J. T. M. Stevenson, M. Mitkova, and M. N. Kozicki, "Sheet resistance measurement of non-standard cleanroom materials using suspended Greek cross test structures," *IEEE Trans. Semicond. Manuf.*, vol. 19, no. 1, pp. 2–9, 2006.

[5] N. Stavitski, J. H. Klootwijk, H. W. van Zeijl, A. Y. Kovalgin, and R. A. M. Wolters, "Cross-Bridge Kelvin Resistor Structures for Reliable Measurement of Low Contact Resistances and Contact Interface Characterization," *IEEE Trans. Semicond. Manuf.*, vol. 22, no. 1, pp. 146–152, Feb. 2009.

# Chapter 3

# Silicon-Based Multi-Functional Wafer-Level-Package for LEDs[4]



Today, finding a low cost, efficient, functional and reliable solution for controlling smart lighting systems has become topic of many research groups and industry. In this chapter, design and fabrication of a multi-functional wafer level package (WLP) for phosphor-based white LED system using 7-mask BiCMOS process are discussed. This package integrates 4 high power blue LED dies with a temperature sensor and a blue selective light sensor for monitoring system performance. Each sensor has been designed, characterized and calibrated to be part of the smart monitoring unit. An interdigitated power transistor and a 4-bit flash analog-to-digital converter (ADC) were also monolithically integrated with sensors' readout and extra controlling functions.

## 3.1 Introduction

As LED technology is emerging dramatically in recent years, there are increasing demands for improving the luminous efficiency and lowering the cost for manufacturing industry. However, package reliability is still one of the main bottleneck for LED systems [1]. Specially for high power packages, high operating temperature can affect light intensity and color shifting over the time [2].

[4] This chapter was partially presented in China SSL 2014. The more completed version is submitted as: Z. Kolahdouz, T. Ma, , H. van Zeijl, H. Abdy, M. Kolahdouz and G. Q. Zhang, "Silicon-Based Multi-Functional Wafer Level Package for LEDs in 7-Mask BiCMOS Process," to Sensors and Actuators A.

Introducing high power light emitting diodes (LEDs) was a key step for development of new application areas in lighting such as: sustainable lighting, general interior and exterior illumination, backlighting for displays, smart lighting (e.g. data transportation), indicators and signs , non-visual applications (communication), and transportation equipment lighting [3]–[6].

Among different methods of producing white light for general illumination applications, the most common approach for high power white LED source is the dichromatic method (also entitled as phosphor-based white method). It is a combination of a short wavelength LED, such as blue or UV, and phosphoric wavelength shifter. In the phosphor coating, a portion of photons are converted to yellow and the rest travel without any change. The light output is seen as a white light by human eyes [7]–[9]. This method shows good color rendering, long lifetime and acceptable reliability over the time comparing to so called trichromatic approaches [3], [7]. This concept is elaborated in more details in Chapter 4.

In addition to general illumination, blue and UV LEDs are progressively applied in medical and sensing applications [10]. Improving the system reliability in general and mainly for more sensitive areas motivates industry to develop more advanced lighting modules. Functional blocks like system monitoring units and innovative color control technology provide the ability to control and adjust the light intensity and color temperature (CT). So, integration of more functions and packaging configurations are some of the critical keys for reliable and efficient solutions for the modern lighting demands. Previously, many integrations were done in PCB level [11], [12]. However, silicon-based wafer level packaging can be one of the best promising approach considering cost, efficiency, functionality, design flexibility and uppermost reliability [13], [14].

Another concern is large heat dissipation in such a high power package. Silicon wafer-level-package (WLP) can be a good solution for thermal management and a cost effective integration [14]–[16]. Using silicon-based infrastructures, IC technologies, and MEMS toolset and processes allows us to integrate different functional sub-blocks on the same die.

Many groups formerly reported integrations of temperature and optical sensors for the most important parameters of such packages in wafer level [16]–[20]. Though, using silicon substrate gives us the opportunity to integrate more functional module such as controlling unit and the whole readout circuits.

To address such issues, a new monolithic silicon-based package is introduced which is realized in the 7-mask BiCMOS process. BiCMOS7 process can potentially implement a smart LED driver platform for the cost less than 1-2 $/cm$^{-2}$ [20]. This process flow integrates monolithically the diodes, CMOS and BJT transistors all in just seven masks, which can simplify final package configuration. It is optimized for performance of different passive and active components. Final system will be a smart miniaturized LED WLP with two main functions: 1) system performance monitoring and 2) system controlling. The first function involves temperature sensors that monitor the package temperature. This data can be used for thermal management by controlling blocks or for further analysis. The monitoring function also includes blue selective photodiodes specially designed for the target LED wavelength that selectively detect the output blue light intensity. It provides very accurate brightness information of the mounted LED in the package. This photodiode is explained in depth in Chapter 4. The brightness information can be later used for a feedback control circuit to correct the intensity and color shifting of the output light [20]. The second function, system controlling, determines driving current of LEDs, which can be performed in either analog or digital ways. An analog control circuit is discussed in Chapter 5. A 4-bit flash ADC is also implemented for reading out sensor data. It can be used as a part of a digital control system. Next, a high current power switch is integrated for driving the LEDs. In this chapter the main blocks are discussed, which are the key elements for a full integrated smart silicon based LED platform.



Having different kinds of sensors in the same package with LED chips and readout circuits in a relatively low cost miniaturized module, can be an appropriate demonstrator for different applications such as biomedical diagnostic devices or other sensitive areas.

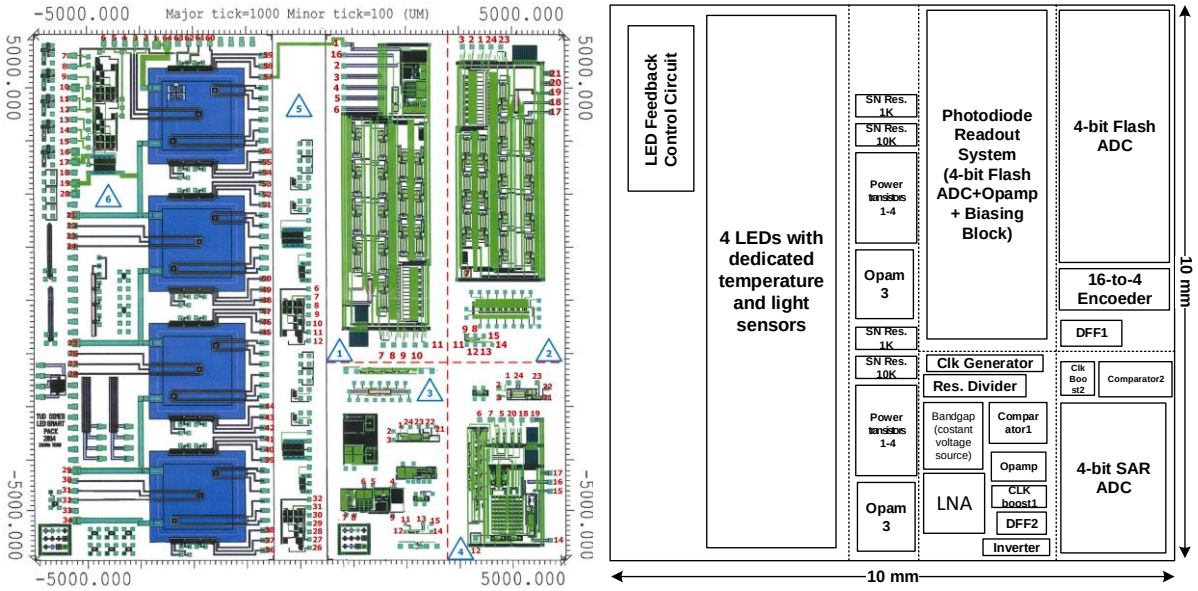
This chapter is organized as follows: in Section 3.2, design of the LED WLP is presented with explaining three main blocks: sensors, power transistor, and ADC. In Section 3.3 fabrication process is summarized with presenting the main steps of the 7-mask BiCMOS method. In Section 3.4, the implementation and measurement results are discussed. Finally, it will end by a short conclusion of this chapter.

## 3.2 Design of LED Wafer Level Package

The package is designed as a high lumen output package integrating 4 BXCD 45 mil x 45

*Table 3-1: Specification of the target LED.*

| | |
|---|---|
| **Dimension** | 1143×1143×150 μm$^3$ |
| **DC Forward current** | Max 700 mA |
| **Reverse voltage** | 5V |
| **Working temperature** | -40 – 100 °C |
| **Optical power (minimum)** | 340 mW |
| **Dominant wavelength** | 450-470 nm |

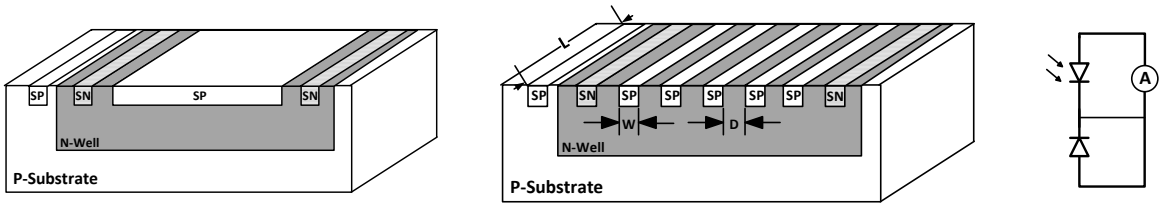



(a) (b)

*Figure 3-1: (a) Layout of the 2D LED WLP and (b) positions of different blocks.*

mil Bridgelux® Blue Power Die. The complete die size is 10×10 mm$^2$ including the test and main structures, but the main package is 6×10mm$^2$. The design is such that 4 LEDs can be turned on in series with any combinations of 1 to 4. The target LED in this study is a vertical blue power die from Bridgelux®. Some of its specifications can be found in Table 3-1. These LEDs are useful in a broad range of applications such as general illumination, automotive lighting, and LCD backlighting [21].

The whole design was manufactured using 2 μm 7-mask BiCMOS process. This process was introduced in Chapter 2. Moreover, the relative low area costs for IC processing enable 2D integration of IC's with large area devices such as LED chips, in our case 1.1×1.1 mm$^2$. Figure 3-1(a) shows the complete die layout which monolithically integrated different components for the multifunctional LED system. Figure 3-1(b) demonstrates location of different blocks.




(a) (b)

*Figure 3-2: Schematic of (a) the temperature sensor and (b) the striped-shape photodiode with its equivalent circuit.*

### 3.2.1 Temperature and Light Sensors

To monitor the system performance, temperature and light sensing elements were integrated. For temperature sensing, 12 PNP dual junctions are located at different positions under the LED dies. It consists of a $P^+$ in an N-well (SP area) on a P-substrate as shown in Figure 3-2(a). The lower N-P junction is short-circuited to eliminate the effect of surrounding charges and upper $P^+$-N junction is forward biased at constant current to evaluate the voltage as the temperature indicator.

For output light sensing, a blue selective photodiode was designed and fabricated which is schematically shown in Figure 3-2(b). These stripe-shaped dual junction photodiodes, with upper junction at 330 nm, demonstrated a very high selectivity to blue light. The maximum responsivity was achieved at 480nm which is matched with the blue LED's illumination [20].

### 3.2.2 Power Transistor

For switching LED driving current, NMOS power transistor with max 700 mA current was also integrated. For transistor, an interdigitated structure was used to improve area efficiency. As BiCMOS7 process has 2 µm minimum feature size for implantation, the transistor channel length is set to 2 µm. The source and drain, $N^+$ areas in the P-substrate called shallow-N (SN), were designed and manufactured as interdigitated finger-shaped structures in order to lower down the parasitic resistance in the channel and shrink the dimension. In this structure, four finger-shaped power transistors (W/L=1800µm/2µm) were connected in parallel in order to supply the required source current. It is schematically illustrated in Figure 3-3.

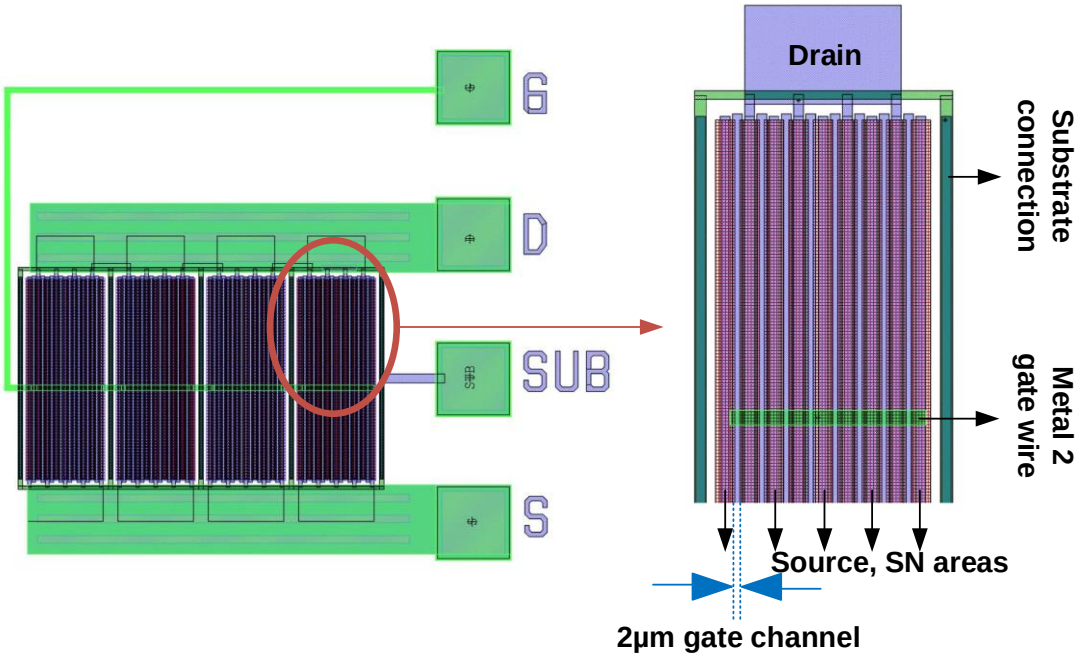


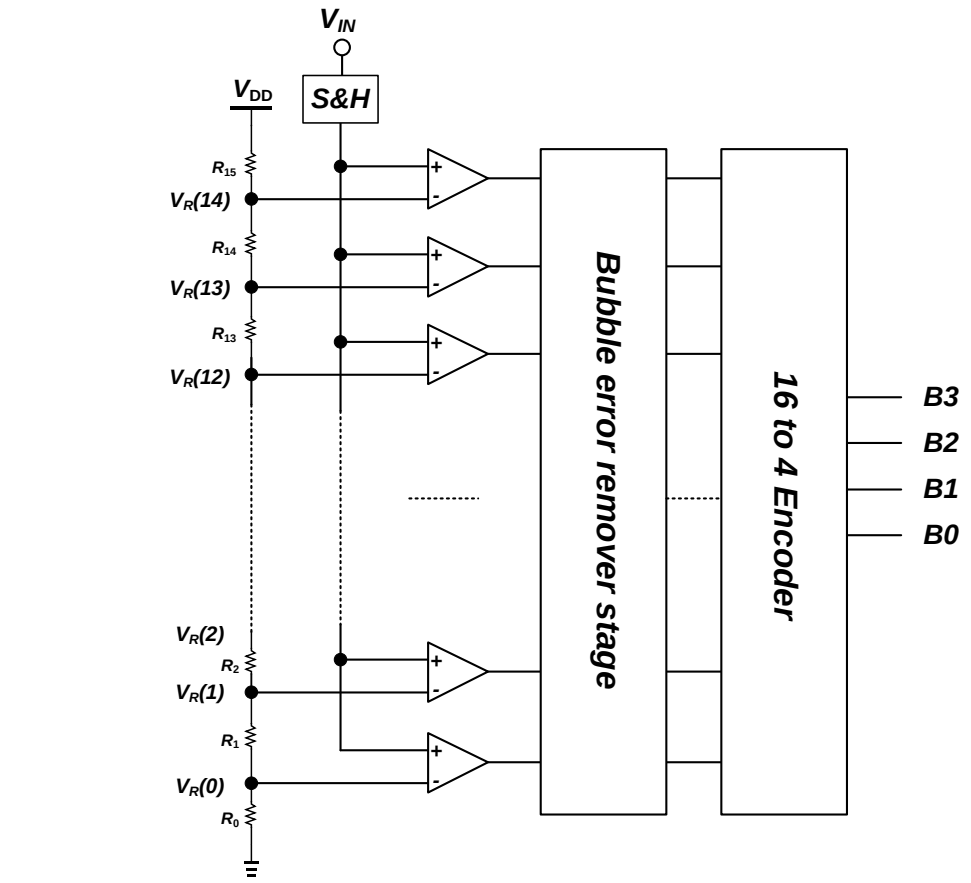

*Figure 3-3: Layout of the power transistor comprising 4 parallel interdigitated transistors each with five source/drain fingers (360 µm total width). The inset shows the magnified interdigit source and drain structure.*

### 3.2.3 Analog-to-Digital Converter

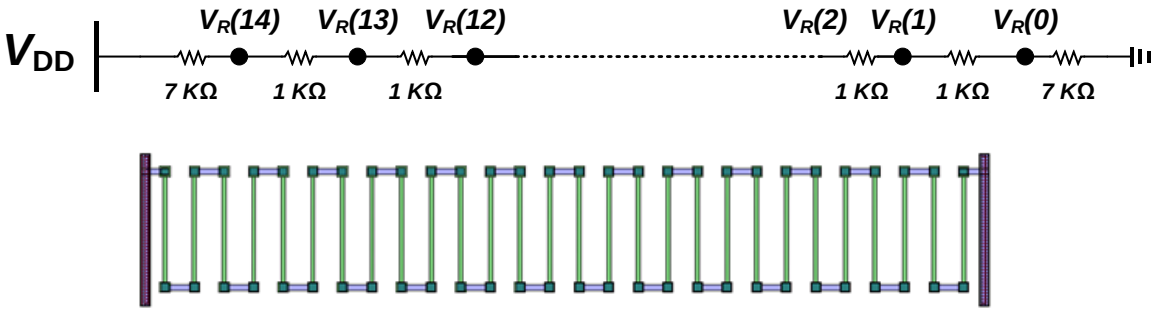
Having a complete BiCMOS run flow allows integration of some relevant logics for feedback and controlling units such as a 4-bit flash ADC combined with an operating amplifier for sensor readout circuit.

Flash ADC has various advantages like fast response, simple structure, and easy realization, which make it an ideal architecture for low bit ADC design. It is composed of four different parts as shown in Figure 3-4(a); reference voltage divider, comparator, bubble error remover, and thermometer encoder stages [22]. The supply voltage in our design is 7 V and the input range based on our light sensor output is 1.5-5.5 V.

For reference voltage divider, a resistor ladder is used. Normally, it is made with a polysilicon structure. However, in BiCMOS7, the poly is not used for process simplicity. The resistor is made by the ion implantation of N-type dopants (phosphorus) in the P-substrate, called SN resistors. The resistance value changes relatively with variations of temperature and biasing parameters. However, it is not critical since only the relative values are used to make the voltage




(a)




(b)

*Figure 3-4: (a) Block diagram of 4-bit flash ADC, and (b) schematic and layout of resistive voltage divider.*

levels. So, if the resistance value is changed, the voltage levels remain unchanged.

By measuring the Kelvin structure on the sample wafer, with similar parameters of the main process, the sheet resistance of SN is around 50 Ω/square. The over-diffusion width of dopants after implantation is 0.62 μm, according to the test of Electrical Line Width Measurement (ELM) structure. The voltage divider requires 15 ($2^n - 1, n = 4$) output nodes in a 4-bit Flash ADC.

Considering power consumption and driving capability, 1 kΩ resistor is an appropriate choice as the unit cell resistor between each two nodes. For 1 kΩ resistor and having 2 μm for width, the length of the SN resistor is calculated to be 52 μm. Figure 3-4(b) shows the layout for SN type voltage divider. Since the input signal range is 1.5-5.5 V, two resistors with 7 kΩ (7 × 1 kΩ unit) are used at two sides of the divider. So instead of using two extra reference voltages of 1.5 and 5.5 V, we can reuse the same 7 V power supply. The least significant bit (LSB), which indicates the voltage resolution, can be calculated as:

$$1\ LSB = \frac{V_{REFH} - V_{REFL}}{2^n} = 0.25\ V, \tag{3.1}$$

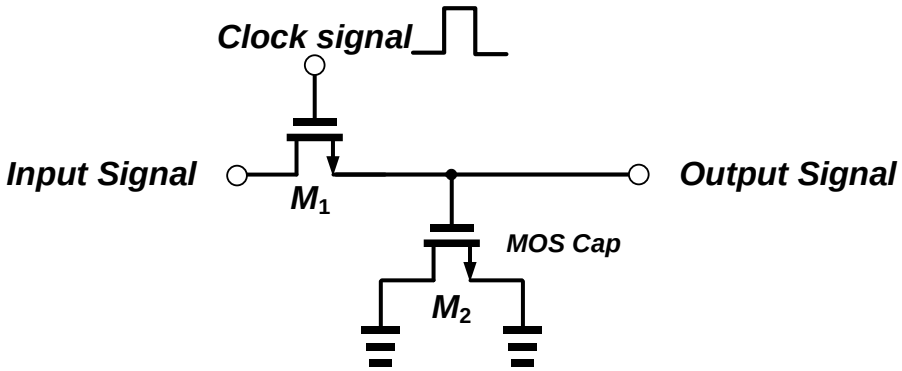


where $V_{REFH}$ and $V_{REFL}$ are 5.5 V and 1.5 V, respectively.

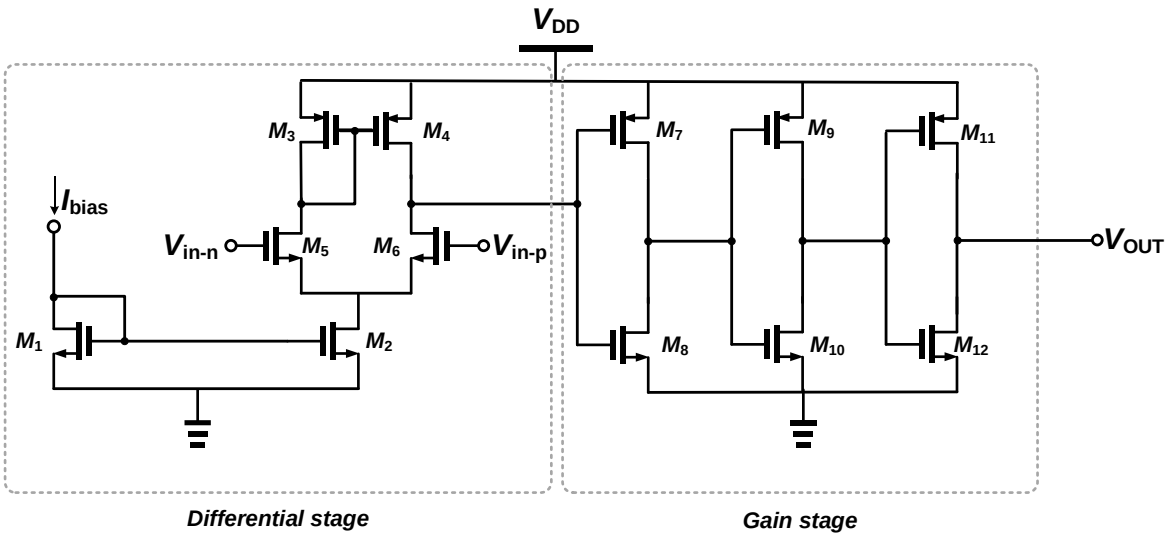
Sample and Hold module (S&H) is utilized between the input node and comparator stage (shown in Figure 3-5(a)). During ADC's operation, it initially tracks the time-varying input signal during the first half clock cycle through $M_1$ switch. In the second half clock cycle, it holds the last value on $M_2$ that is used as a MOS capacitor. This voltage is used by the comparator stage. In this way, the signal conflicts due to fast input variations can be effectively eliminated for reducing the possibility of functional failures.

The comparator can be considered as a key component in Flash ADC design. Its features directly affect the ADC performances such as maximum sampling rate, power consumption, input signal range, load capability, etc. However, it is a challenge to design a good comparator based on BICMOS7 process due to unideal transistor parameters and features (high and asymmetrical threshold voltages).

The 4-bit Flash ADC incorporates 15 separated comparators. As shown in Figure 3-5(b), each comparator consists of a differential stage and 3 sets of inverter as a gain stage. These inverters ensure that the final comparator output reaches the rail to rail values (0 and $V_{DD}$). Since comparator generally works in open loop mode, it does not require compensation for stability. The current flow through $M_2$ is the sum of the currents from $M_{3,5}$ and $M_{4,6}$, and this total current is determined by the biasing current through $M_1$. When Vin_p is larger than Vin_n, the current flows through $M_{4,6}$ will be more than that of $M_{3,5}$. Thus, voltage at the drain of $M_4$ will be reduced. Subsequently, at the output of inverter $M_{7,8}$, the voltage goes high. In order to improve the load capability of the comparator, two more inverters ($M_9$ – $M_{12}$) are added after the first




(a)




(b)

*Figure 3-5: (a) Sample and hold stage (S&H), and (b) comparator for the 4-bit Flash ADC.*

inverter. This results in a logic "1" at the final output. Similarly, if Vin_p is smaller than Vin_n, the drain voltage of $M_4$ will be increased, and make the final output "0".

To guarantee that the ADC works properly, offset voltage of comparator should always be less than half of LSB. For different input voltages, the offset voltage is different. Thus, it is necessary to characterize it carefully before determining the input range of the comparator. With the appropriate adjustment on the width/length ratio for each of the transistors, the simulated offset voltage in our target input range is less than 40 mV, which is well smaller than the LSB (i.e. 250 mV). Besides, to avoid the signal conflicts between input and output of the comparator, a flip-flop is connected to the output of the comparator. Depending on the clock cycle, it will periodically switch between open and close modes. For the sake of simplicity, this has not been

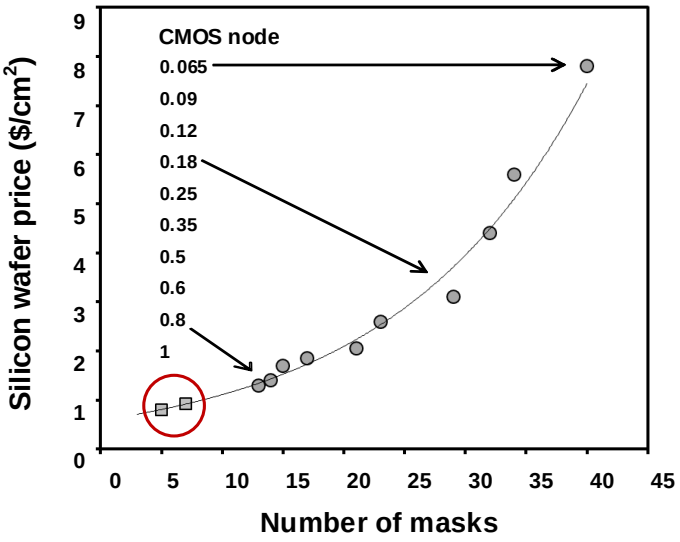



*Figure 3-6: Silicon wafer price for different number of masks used in IC processing. The red inset points out the BiCMOS5/7 nodes.*

shown in these figures.

To avoid bubble errors that might be caused by comparator meta-stability and noise, a bubble error remover stage, consists of a bunch of inverters and three-input NAND gates, is added to ADC.

In the final stage, a so-called thermometer code needs to be encoded into a 4-bit binary code. This work can be done by a simple 16-to-4 encoder, consists of NAND and NOR gates, implemented by CMOS transistors.

The whole system is simulated with a sample rate of 100 kHz. The simulation results show proper operation of the ADC. The simulated values of maximum integrated nonlinearity (INL) and differential nonlinearity (DNL) of the whole ADC are 0.037 and 0.24 LSB, which are lower than the nominal critical value of 0.5 LSB [22]. Thus, this design can be properly implemented for the light sensor readout system.

## 3.3 Fabrication Process

One of the main challenges in this application is low integration density for supporting LED bare dies. The dimension of a power LED bare die is usually in millimeter$^2$ scale which is quite large compared to the current IC transistor size. As shown in Figure 3-6, the continuous decrease of the feature size in CMOS planar technology results in boosting the number of masks and the silicon wafer price (cost/cm$^2$).

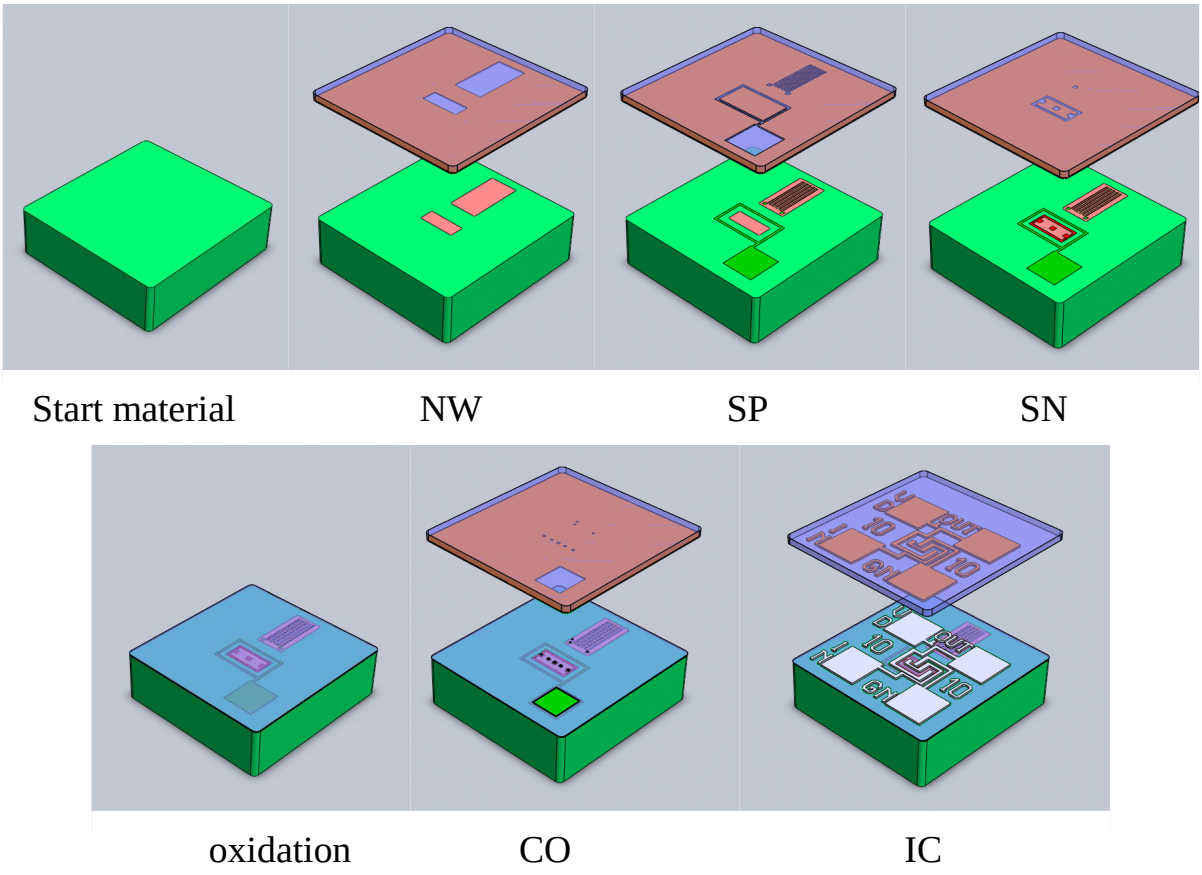



*Figure 3-7: Schematic of main steps in BiCMOS process up to metal 1.*

On the other hand, IC area is shrinking and so there are more dies fabricated on a single wafer which compensate the cost. Considering area limitation in solid state lighting, it seems that the fabrication of LED WLP is extremely cost ineffective by the advanced CMOS process. So, a low-cost CMOS planar technology is required as a promising option to subordinate the cost. Although BiCMOS5/7 has a limited performance, it is sufficient to be implemented for LED WLP and some simple IC designs. Figure 3-6 shows how BICMOS5/7 process can potentially implement a smart LED driver platform for the cost of even less than 1$/cm$^2$.

The BICMOS7 process is now explained by the structure of the transistors which is schematically shown in Figure 3-7. It started with a P-type wafer that was patterned for the N-type implantations: the N-wells of the NPN and PMOS transistors. This was done by a phosphor implantation and a deep diffusion. The second mask was used to create the P-type regions: the base of the NPN transistors, the source and drain of the PMOS transistors and the isolating rings around the NMOS transistors. They were doped using a shallow boron implant. The third mask

was for the highly doped N-regions: the emitter and (contact regions of) collector of the NPN transistor, the source and drain of the NMOS and the isolating ring around the PMOS. This was performed by a shallow arsenic implantation. After this step, the wafer was annealed/oxidized for 12 minutes at 1000 °C and the surface got an isolation layer of 100 nm of silicon dioxide (by thermal oxidation). This layer will act as an isolation layer between the first interconnect layer and the substrate as well as the gate material of the PMOS and NMOS transistors. This means that a trade-off has to be made for the thickness of this layer. A transistor has the best characteristics with a low gate oxide thickness, while the isolation layer at rest of the wafer must be preferably thick to minimize the parasitic effects. The fourth mask was used to make the contact openings in the isolation layer.

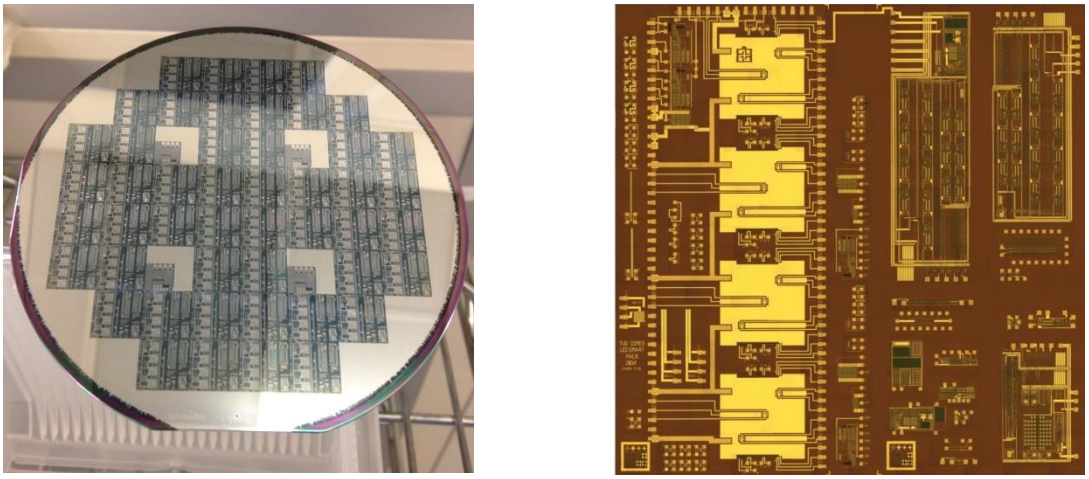


The fifth mask was utilized to pattern the first interconnect layer. This was the first metallization step for the contact openings and created wires by combining different components. Next, 200 nm chemical vapor deposition (CVD) oxide was deposited. The sixth mask was for patterning the vias between metal 1 and 2. Then, 2 µm Al (99%)-Si (1%) was sputtered as the second metal layer. The seventh and final mask was for patterning the second interconnect layer.

There are numbers of trade-offs in this design. The first is between the optimum gate layer thickness and the preferred isolation layer thickness. Another trade-off is the doping profiles of the N and the P regions which affect the sensor responsivity and transistor performances. Due to our simulations, the parameters were adjusted to best fit the application for blue LED spectra. However, there are many challenges for integration of all these devices in the same process. The CMOS transistors have non-standard threshold voltages, i.e. 1 V for NMOS and -3.5 V for PMOS. There are two issues concerning these over-high threshold voltages. In the conventional IC process technology, the threshold voltage is usually lower which enables a large headroom for the circuit design. The second problem is the asymmetric threshold voltages for NMOS and PMOS. This asymmetry affects the circuit balance and makes it challengeable to get the optimum design. These imperfect features seriously restrict the flexibility and feasibility in circuit design.

## 3.4 Implementation and Measurement Results

Different blocks and components were fully integrated in previously discussed BiCMOS



(a) (b)

*Figure 3-8: Monolithic integration of different blocks in LED package: (a) photo of full wafer, (b) 10×10 mm$^2$ die micrograph.*

process. Figure 3-8(a) shows the full wafer photo containing 48 complete packages and 4 process test dies. Figure 3-8(b) exhibits a full die micrograph after preparation. For each package, 4 LED chips were later mounted and wire bonded on predefined locations.

Figure 3-9 (a-b) show the layout of LED part and the package after the full process and mounting the LED dies. Temperature and light sensors are two main sensing elements in the package. Light sensors are located close to each LEDs to accurately evaluate the output light. Temperature is known as one of the key bottlenecks for monolithic integration of electronics in LED package because of its effects on the performance of both LEDs and other electronic components. So, three temperature sensors were located beneath each LED die for in-situ investigation.

The IV characteristic of the temperature sensors was extracted with external temperature controller. At constant forward driving current, the voltage drop over the upper PN junction can be considered as the linear function of temperature (so called one point technique [23])

$$T_j = \alpha + \beta V_{f_{|I_f}}, \tag{3.2}$$

where $\alpha$ and $\beta$ are calibration parameters obtained from measurements at two known temperatures and their corresponding voltages ($V_f$) at the same forward current $I_f$. In this case, we choose the forward voltage data recorded at $I_f$ = 20 μA. The calculated and measured results are summarized in Table 3-2. With the same approach, the temperature of the package for

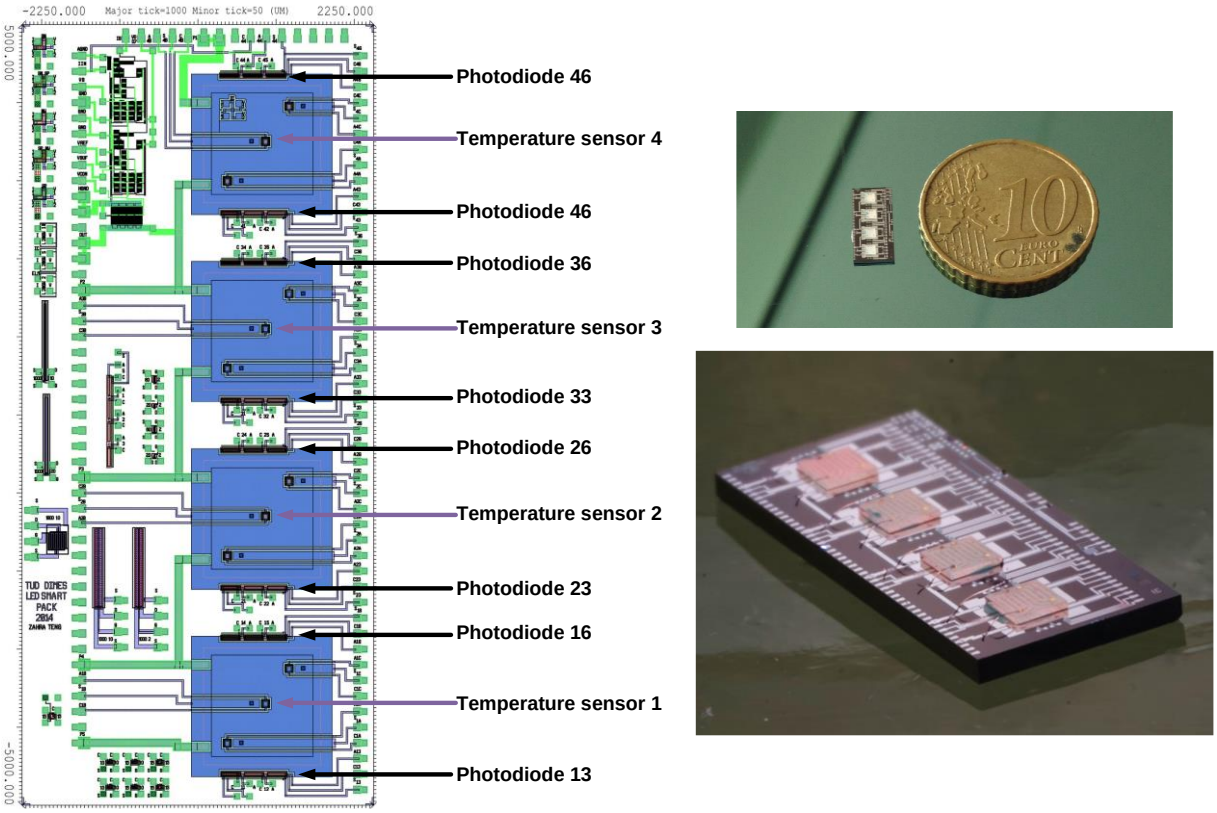



*Figure 3-9: (a) Layout of LED part and positions of LEDs and sensors. (b) Package with mounted LED dies and comparison of its size with 10 Cent coin.*

*Table 3-2: Measurement results of the temperature sensor.*

| $T_{Cal}$(°C/K) | $V_f$ (V) | $T_{meas}$(K) | ΔT |
|---|---|---|---|
| 70/343 | 3.803 | 345.07 | +2.07 |
| 90/363 | 3.855 | 366.36 | +3.36 |
| 110/383 | 3.903 | 386.01 | +3.01 |
| 130/403 | 3.945 | 403.03 | +0.038 |
| 150/423 | 3.985 | 421.32 | -1.68 |

different driving currents was monitored. Test was done on a metallic chuck which acted as the heat sink. The result is shown in Figure 3-10.

After turning light on, the temperature increased rapidly. For 500 mA source current, temperature jumps from 25°C to 57°C within one minute. Later, the temperature only increases 7 degrees in 2 hours. Moreover, the temperature changes at different currents were not the same at all. The temperature measured at 500 mA is twice larger than the one measured at 100 mA (see Figure 3-10).

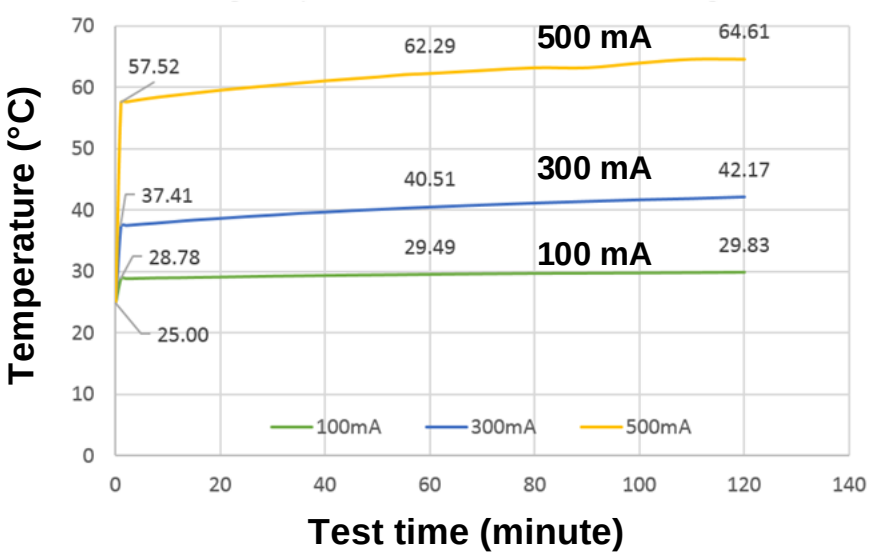
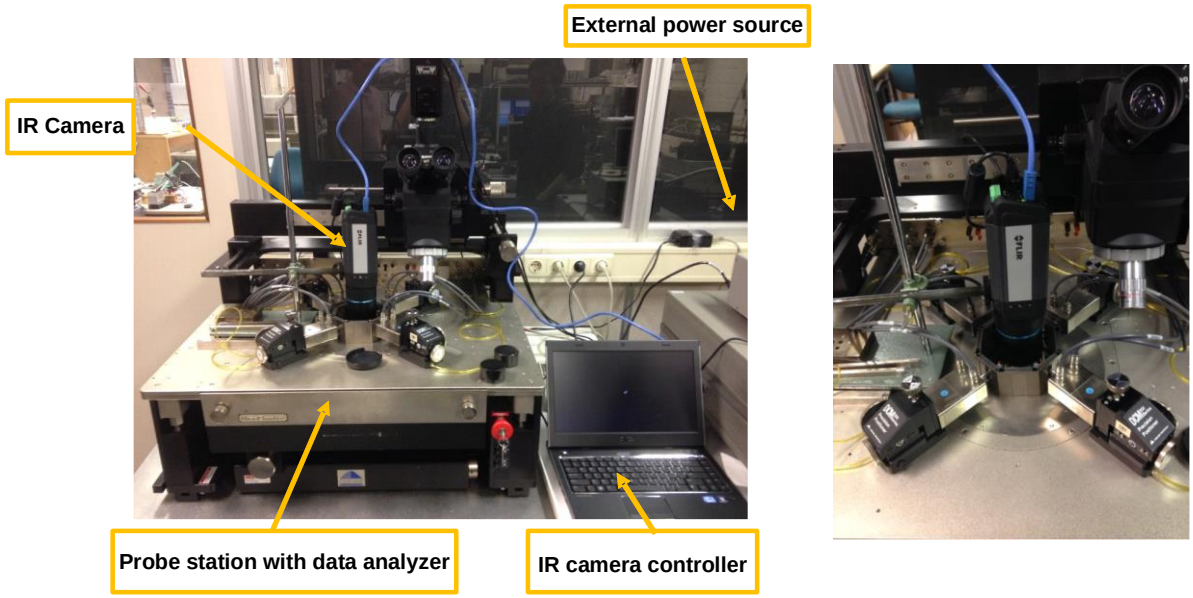



*Figure 3-10: Measured temperature of the package for different driving currents.*

*Table 3-3: Comparison between measurement results of the temperature sensor and IR image.*

| **Forward LED Current** | 100 mA | 300 mA | 500 mA |
|---|---|---|---|
| **Temp (from integrated sensor)** | 28.8 ℃ | 37.4 ℃ | 57.5 ℃ |
| **Temp (from IR image) @ SP#3** | 30.1 ℃ | 41.5 ℃ | 59.8 ℃ |

The temperature sensor results can be verified by thermal images. For this purpose, an infrared (IR) camera was placed above the previous package and the driving current was swept from 100 to 500 mA. Figure 3-11(a) displays the measurement setup and Figure 3-11(b) exhibits the temperature distribution over the package for 100-500 mA. It is worth mentioning that all LEDs were "on" in this image. Generally, the measurement results from temperature sensors are slightly smaller than the thermal camera readout and the average difference is around 2.5°C (see Table 3-3). This difference might be caused by the actual temperature difference between surface and backside of LED dies because of heat sink placement beneath the package. The thermal figures thus show the reliability of the measured value extracted from the temperature sensors. Another conclusion is that with a good heat sink, the temperature at the points far enough from LEDs, e.g. in Figure 3-11 9(b) sensing points (SP) 7, 8 and 9, is quite low. Therefore, monolithic integration of electronics and circuits on LED WLP might suffer less thermal effects.




(a)


(b)

*Figure 3-11: (a) IR camera setup, and (b) thermal image of the package with 4 blue LEDs at 100, 300 and 500 mA driving currents. Different sensing points (SP) #1-10 are pointed out in the micrograph.*

The second sensible parameter is the output light. The light intensity of LED was measured with the photodiodes at different driving currents. For each LED two sets of photodiodes were

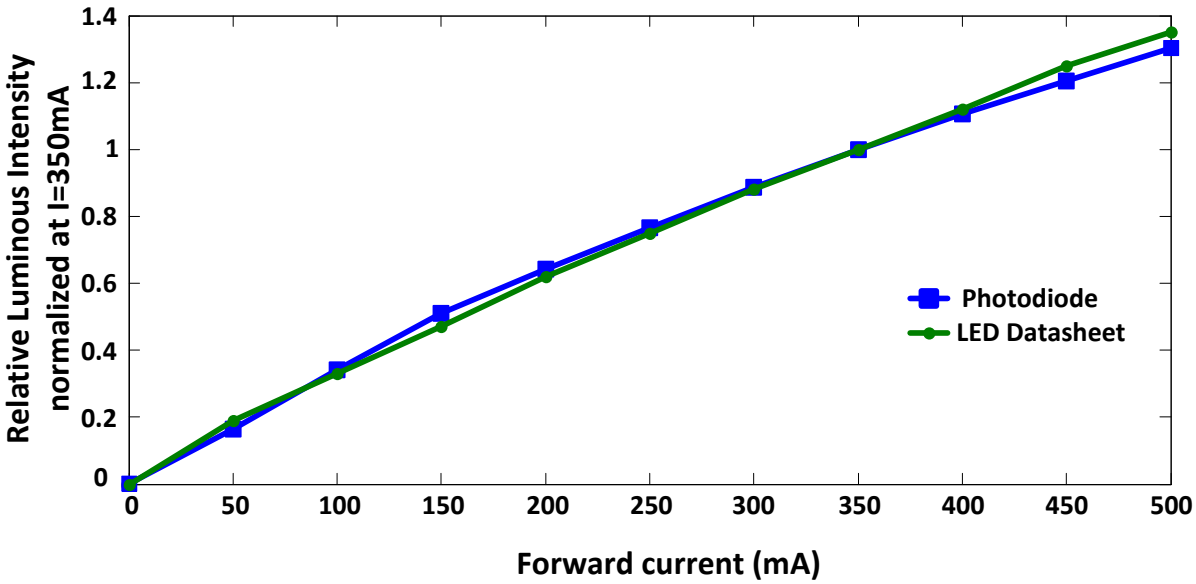


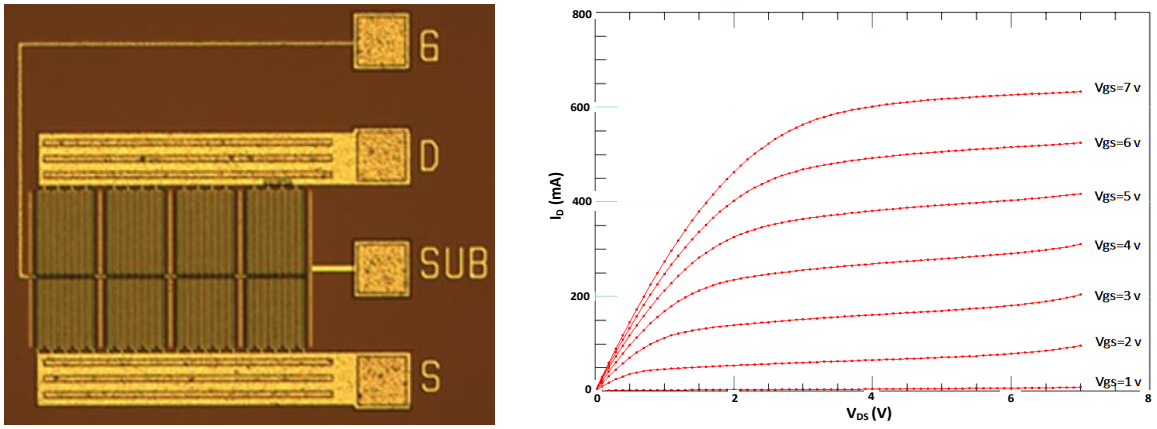

*Figure 3-12: Relative luminous intensity vs. LED forward current comparing the photodiode performance with the datasheet amounts.*

used to get output light measurement. When LED is "off", the reverse current value is 1 pA. Current measurement showed almost 6 orders of magnitude increase when the LED became on. By normalizing the output current and fitting to the LED datasheet, a remarkable consistency can be achieved (see Figure 3-12).

To investigate the effect of package temperature, the photodiode response was studied within 2 hours with constant input current of 350 mA. Relative luminous intensity decays 0.9%. This effect is caused by the temperature increase during the lighting.

The interdigit switching transistor micrograph is shown in Figure 3-13(a). Measured drain current ($I_D$) versus drain-source voltage ($V_{DS}$) of the power transistor is shown in Figure 3-13(b). The transistor can provide the nominal driving current for the LED dies and can be used for an in-situ controlling of the driving current.

The 4-bit flash ADC is designed and implemented in the light sensor readout system to convert the sensing signal into a 4-bit binary code at the output. When the input voltage is ramped from 1.5 to 5.5 V, ideally, a set of digital code will be displayed at the output which is varied from 0000 to 1111 with equal voltage interval (i.e. 1 LSB=0.25 V). Generally, both integration nonlinearity (INL) and differential nonlinearity (DNL) should be less than half of LSB. For doing the measurements, a constant voltage source of 7 V is used. ADC input signal is produced by a



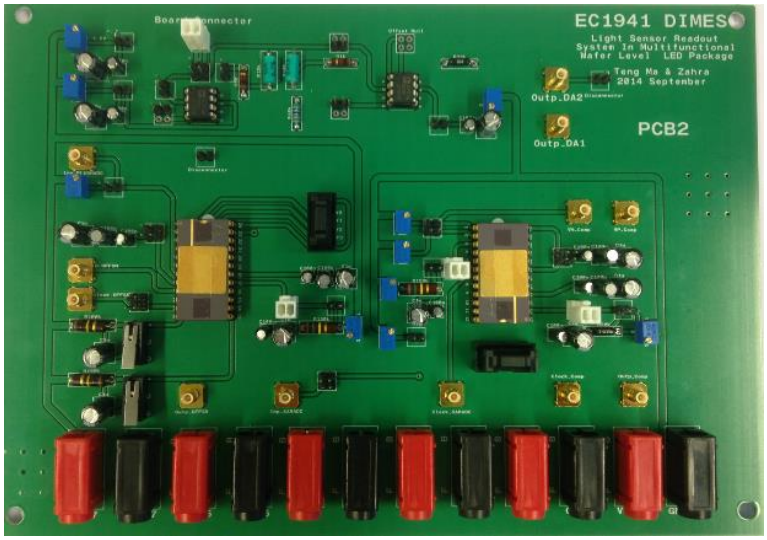

(a) (b)



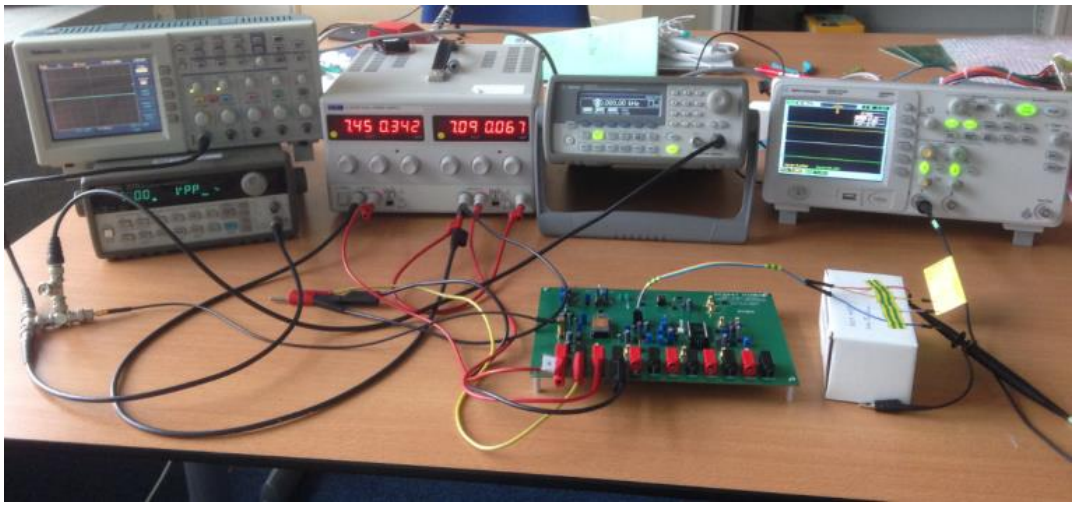
*Figure 3-13: Interdigit CMOS power transistor: (a) micrograph, and (b) $I_D$ versus $V_{DS}$ characteristic at different gate-source voltages ($V_{GS}$).*

trimmer to provide a tunable input voltage and bias current. Moreover, an external function generator makes the clock signal. The four digital output nodes are connected to an oscilloscope. The PCB with assembled component and test equipment setup are shown in Figure 3-14(a) and (b), respectively.

Input-output characteristic of the ADC from simulation and measurement results are shown in Figure 3-15(a). It shows that, the 4-bit flash ADC works properly. By increasing the input voltage from 1.5 V to 5.5 V, the ADC converts the input signal to a 4-bit binary code from 0000 to 1110 at the output. However, there is a missing code 1111 in the last output conversion level, when the input increases from 5.25 V to 5.5 V. This error does not exist in the simulation results. As the cause is traced back, the electrical characteristics of MOSFETs was slightly shifted due to the process variations during the fabrication, compared to the initial model used for simulation. The threshold voltage of PMOS was changed from -3.5 V to -3.3 V and from 1.0 V to 1.2 V for NMOS. This is validated by characterizing a set of separate MOSFETs after implementation. Consequently, the output current of transistors was not the same as previous extracted model. To verify the validity of our designs after fabrication, a new model was extracted based on the new measurement data, by updating the threshold voltages of the model. New simulation results show the same behavior as the measurement regarding the missing code.




(a)

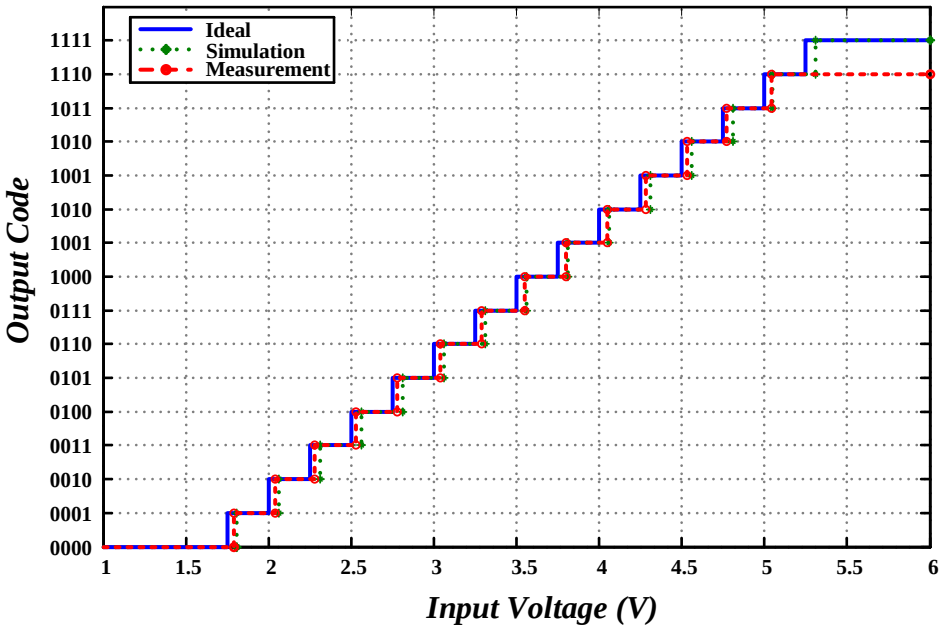


(b)

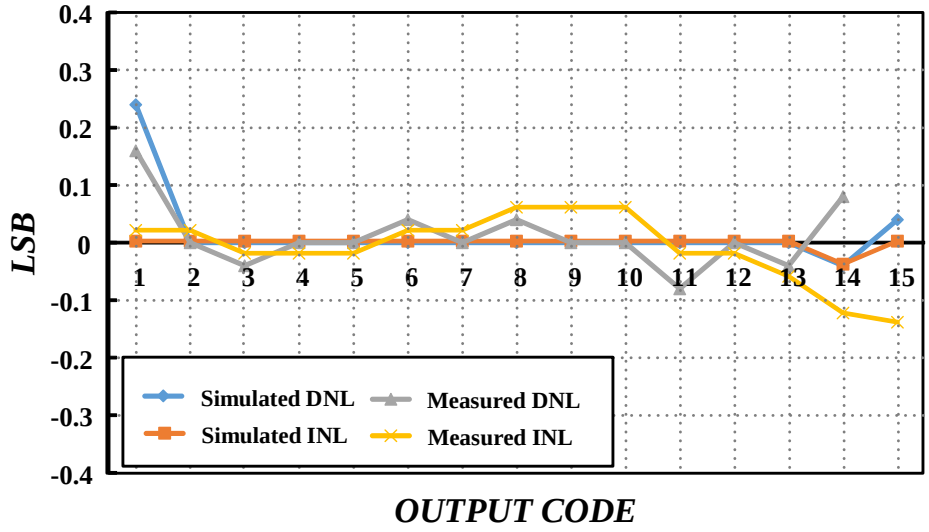
*Figure 3-14: (a) Designed PCB with assembled components and (b) measurement setup for 4-bit flash ADC.*

The shift in threshold voltage mainly affects the S&H module (shown in Figure 3-5(a)). In the initial model, output voltage of S&H follows the input signal for the whole range, which increases from 1.5 V to 5.5 V. However, in the new case, the output voltage does not follow the input near end of the range, thereby leading to the missing code at ADC output. This problem can be solved by using a T-gate instead of NMOS only switch. While the NMOS is turned off at high input voltages, the PMOS of a T-gate can conduct very well.

Figure 3-15(b) shows INL and DNL based on simulation and measurement results. The maximum measured INL and DNL are 0.16 and 0.14 LSB. They are well below the critical value of 0.5 LSB. This guarantees the correct functionality of the flash ADC.




(a)




(b)

*Figure 3-15: Simulation and measurement results of the 4-bit flash ADC: (a) output code versus input, and (b) DNL and IND normalized to LSB value.*

## 3.5 Conclusions

This chapter reports a successful integration of different functions appropriate for package of a phosphor-based white LED module and also any blue/UV LED. Silicon-based wafer level packaging through low cost 7-mask BiCMOS process, gives us the opportunity for integration of different passive and active components for a complete smart system. For sensing functions, thermal and optical sensors were implemented, characterized and calibrated. Blue selective

photodiode measurement showed notable consistency to the LED datasheet values. Temperature sensors integrated just beneath LED chips, measured the temperature in real time and the results were approved with IR photos. For controlling functions, 4-bit flash ADC for reading out sensing output light, and a power switch for driving the LED current were monolithically integrated. The ADC functionality was successfully tested with better than 0.16 LSB accuracy and the power transistor could provide more than 700 mA current. The whole design and measurement results were comprehensively discussed. The reported components can provide a notable platform for future work to have an analog or digital control system for any specific application. Furthermore, other technologies with large area demands, such as Lab-on-Chip that requires smart substrates, can benefit from the approach.

## 3.6 References

[1] M.-H. Chang, D. Das, P. V. Varde, and M. Pecht, "Light emitting diodes reliability review," *Microelectron. Reliab.*, Aug. 2011.

[2] S. Chhajed, Y. Xi, Y.-L. Li, T. Gessmann, and E. F. Schubert, "Influence of junction temperature on chromaticity and color-rendering properties of trichromatic white-light sources based on light-emitting diodes," *J. Appl. Phys.*, vol. 97, no. 5, p. 54506, 2005.

[3] J. Lau, R. Lee, M. Yuen, and P. Chan, "3D LED and IC wafer level packaging," *Microelectron. Int.*, vol. 27, no. 2, pp. 98–105, 2010.

[4] C. Wang, W. S. Lee, and N. Y. Kim, "A Novel Silicon-Based Packaging Platform for High-Efficiency LED Modules," *Adv. Mater. Res.*, vol. 314–316, pp. 359–363, Aug. 2011.

[5] G. Elger, B. Spinger, N. Bienen, and N. Benter, "LED Matrix light source for adaptive driving beam applications," *2013 IEEE 63rd Electron. Components Technol. Conf.*, pp. 535–540, May 2013.

[6] M. H. Chang, D. Das, P. V. Varde, and M. Pecht, "Light emitting diodes reliability review," *Microelectron. Reliab.*, vol. 52, no. 5, pp. 762–782, 2012.

[7] Y.-C. Lin, J. P. You, N. T. Tran, Y. He, and F. G. Shi, "Packaging of Phosphor Based High Power White LEDs: Effects of Phosphor Concentration and Packaging Configuration," *J. Electron. Packag.*, vol. 133, no. 1, p. 11009, 2011.

[8] H. Luo, J. K. Kim, E. F. Schubert, J. Cho, C. Sone, and Y. Park, "Analysis of high-power packages for phosphor-based white-light-emitting diodes," *Appl. Phys. Lett.*, vol. 86, pp. 1–3, 2005.

[9] J. K. Kim, H. Luo, E. F. Schubert, J. Cho, C. Sone, and Y. Park, "Strongly enhanced phosphor efficiency in GaInN white light-emitting diodes using remote phosphor configuration and diffuse reflector cup," *Japanese J. Appl. Physics, Part 2 Lett.*, vol. 44, no. 20–23, pp. 649–651, 2005.

[10] M. J. Kawa, "Medical applications use LEDs to light the way - Electronic Products," 2010. .

[11] S. Y. Ron Hui, S. N. Li, X. H. Tao, W. Chen, and W. M. Ng, "A novel passive offline LED driver with long lifetime," *IEEE Trans. Power Electron.*, vol. 25, no. 10, pp. 2665–2672, 2010.

[12] W. Chen, W. Bottoms, K. Pressel, and J. Wolf, "The next step in assembly and packaging: System level integration in the package (SiP)," *ITRS White Pap.*, pp. 1–127, 2008.

[13] R. Zhang, S. W. R. Lee, D. G. Xiao, and H. Chen, "LED Packaging using Silicon Substrate with Cavities for Phosphor Printing and Copper-filled TSVs for 3D Interconnection," in *Electronic Components and Technology Conference*, 2011, pp. 1616–1621.

[14] C. T. Tsou and Y.-S. Huang, "Silicon-Based Packaging Platform for Light-Emitting Diode," *IEEE Trans. Adv. Packag.*, vol. 29, no. 3, pp. 607–614, Aug. 2006.

[15] W. K. Jeung, S. H. Shin, S. Y. Hong, S. M. Choi, S. Yi, Y. B. Yoon, H. J. Kim, S. J. Lee, and K. Y. Park, "Silicon-Based, Multi-Chip LED Package," in *2007 Proceedings 57th Electronic Components and Technology Conference*, 2007, pp. 722–727.

[16] J. K. Kim and H. C. Lee, "A photo-sensor on thin polysilicon membrane embedded in wafer level package LED," in *Proceedings of the SPIE*, 2012, vol. 8431, pp. 8431–7.

[17] H. Ye, H. Van Zeijl, R. Sokolovskij, A. W. J. Gielen, and G. Q. Zhang, "Advanced LED package with temperature sensors and microfluidic cooling," in *Proceedings - Electronic Components and Technology Conference*, 2013, pp. 1920–1925.

[18] S. Junger, N. Verwaal, W. Tschekalinskij, and N. Weber, "Multispectral CMOS sensors with on-chip nanostructures for wavelength monitoring of LED devices," vol. 8641, p. 86411B, 2013.

[19] S. Chang and C. Tsou, "A novel silicon-based LED packaging module with an integrated temperature sensor," *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 4, no. 5, pp. 769–776, 2014.

[20] Z. Kolahdouz, A. Rostamian, M. Kolahdouz, T. Ma, H. Van, and K. Zhang, "Output blue light evaluation for phosphor based smart white LED wafer level packages," *Opt. Express*, vol. 24, no. 4, pp. 174–177, 2016.

[21] Bridgelux, *Bridgelux BXCD45 Product Data Sheet DS-C15 (10/22/2012)*, Revision C. Livermore: Bridgelux Inc., 2012.

[22] B. Razavi, *Principles of data conversion system design*. IEEE Press, 1995.

[23] M. M. Moslehi, "United States Patent," 5,436,494, 1995.

# Chapter 4

# Blue Light Evaluation for Phosphor-Based White LED WLP[5]



This chapter presents a blue light detector for evaluating the output light of phosphor based white LED package. It is composed of a silicon stripe-shaped photodiode designed and implemented in a 2 µm BiCMOS process. The final device shows a high selectivity to blue light. The maximum responsivity at 480 nm is matched with the target blue LED illumination. The designed structure has better responsivity compared to simple photodiode structure due to reducing the effect of dead layer formation close to the surface because of implantation. It has also a two-fold increase in the responsivity and quantum efficiency compared to previously similar published sensors.

## 4.1 Introduction

There are two major methods to produce white light in LED lighting systems. The first approach is to create white light by the proper mixture of three monochromatic sources, i.e. red, green and blue light (RGB method). These trichromatic LED-based white light sources provide

[5]This chapter was partially presented at ESSDERC 2014 as: Z. Kolahdouz et al., "Blue Selective Photodiodes for Optical Feedback in LED Wafer Level Packages," in ESSDERC, 2014, pp. 174–177. An extended version was published as: Z. Kolahdouz, A. Rostamian, M. Kolahdouz, T. Ma, H. Van, and G. Q. Zhang, "Output blue light evaluation for phosphor based smart white LED wafer level packages," Opt. Express, vol. 24, no. 4, pp. 174–177, 2016.

a good control over the light color temperature and luminous efficiency of radiation. However, this method is hardware intensive due to application of three RGB LEDs. Furthermore, these chips show different behaviors at high working temperature conditions and aging characteristics. The system also tends to render pastel colors unnaturally which results in poor color rendering index of RGB white light. Besides, the driving electric circuit for this method is complex to be used for white color production and makes it impractical for general illumination applications [1, 2].

The second approach, entitled the phosphor based white method, is to produce white light by a single short wavelength LED such as blue or UV, combined with a yellow phosphor coating. The blue or UV photons generated in the LED either travels through the phosphor layer without shift, or they are converted into yellow photons in the phosphor coating layer. The combination of the yellow light with the unabsorbed blue light appears as a white light in the human eyes. In some modules, remote phosphor layer is used in which phosphor is placed at a sufficiently large distance from the LED chip. It offers much better color rendering than RGB white, often similar to the fluorescent sources. Furthermore, phosphor converted white light is also much more efficient than RGB white. Because of its high efficiency and acceptable color rendering and lifetime, phosphor white is the most common approach of producing white light for general illumination [2, 3].

The exact shade or color temperature of dichromatic white light is determined by the dominant wavelength of the blue LED and the composition and thickness of phosphor coating. Manufacturers attempt to minimize the color variations by controlling the thickness and composition of the phosphor layer during manufacturing [2].

Despite all advantages these LEDs have, they are suffering from light intensity decay in stress tests. Their light intensity decays during a long operation time or at a high working temperature. Another drawback of phosphor based white method is color shifting due to degradation of the blue LED die and the yellow phosphor over time. It also happens when the device operates at a different current or operating temperature [1].

Some of the manufacturing companies have revealed the data for lifetime prediction of LED chips. As is shown in Figure 4-1 from ETAP company [4], the LED performance decays critically over the time which motivates us to develop a system monitoring unit. Although not

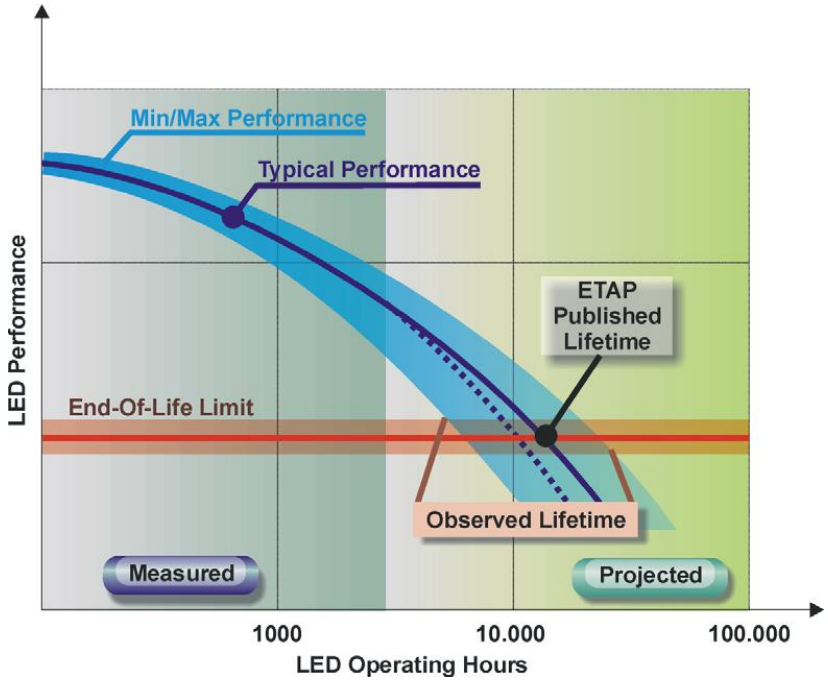



*Figure 4-1: Report of LED performance over operating hours from ETAP company [4].*



all the performance falloffs can be compensated, a smart integrated LED power control with light and temperature sensors can compensate for light intensity decay, monitor color shifting and protect for overtemperature problems.

Decay may refer both to phosphor and LED chip performance over the time. While phosphor working mechanism is related to the manufacturing process, we can compensate LED aging and adjust its light intensity by changing the driving current. There are two strategies to alter the current:

1- Feed a forward control based on the lifetime prediction: increasing current based on the correction values stored in a memory.

2- Using output light feedback: including blue light sensors and a control loop circuit.

A smart package with an output light feedback can compensate the brightness variation by changing the driving current. Light sensing can provide information both about light color and intensity. Employing a blue selective photodiode integrated in LED package can be a promising solution.

Silicon based wafer level packaging (WLP) is the technology of choice for broad range of applications. This technology is a key in terms of cost and thermal design. It can provide batch fabrication and component integration, as it is compatible with CMOS technology and thus, can include micro electromechanical systems (MEMS) components as well [5, 6]. Applying these

technologies, a smart LED package can be produced that resolves the brightness problems associated with LED intensity decay [7]. There are two categories of silicon-wafer-based wafer level packaging (WLP) LEDs; the surface-mount type, in which electrodes are formed on a silicon wafer and then the LED chip is attached to the wafer; and the cavity type, in which cavities are formed prior to the electrodes [7]. Generally, the cavity is fabricated using KOH wet etching with a (100) silicon wafer. The cavity acts both as a reflector and a holder for filling phosphor and resin.

In this chapter, we developed a photo sensor appropriate for the target wavelength (470 nm) and compatible to the cavity type WLP process and monolithic integration. Basic silicon photodetectors have generally a poor responsivity to blue and UV light, because these spectra absorbs very close to the surface while the active sensing regions of these devices are usually situated at a certain depth below the device surface [8]. Different structures for silicon photodiodes are used to tune wavelength selectivity. They are all based on wavelength-dependent absorption coefficient of light in silicon. The basic structure is a P-N-P dual-junction photodiode, the active region of the P-N photodiode is limited by a second N-P junction situated below the first one [9]. In [8], the detector doping profile of the photodiode is adjusted in a way to have a sharp and high potential barrier. It generates a strong built-in drift field in which photo-generated carriers are separated efficiently. This structure is intrinsically selective but fabricated in a dedicated sensor process, not compatible with CMOS standard processing. Another group proposed a stripe shaped photodiode, comprising shallow P layers implanted in a N-well [10]. The geometry was optimized for better UV/blue responsivity. These devices showed a promising selectivity for blue light. In our work, we used similar structure as in [10], but the size and features were changed to better fit the process and application requirements. All the structures are also simulated and the efficiencies of the devices have been thoroughly investigated before fabrication.

There are also some reports on novel works using different substrates or coating to enhance the responsivity to UV and blue spectra. In [11], TiO2 nano-crystalline film was prepared on SrTiO3 (001) substrate to form an N-N heterojunction active layer and final device shows a good responsivity in UV region. In another work [12] by employing conjugated polymer thin film blends, authors showed improving the ultraviolet response of silicon photodetectors for UV spectra. However, these methods are not applicable in standard BiCMOS process.

The photodiode is fabricated in a 5 mask BiCMOS process, used in a LED WLP which can selectively detect the output blue light intensity in a very accurate and efficient way which provides the brightness information of the mounted LED in the package.

This chapter is organized as follows: in Section 4.2, two photodiode structures including single anode and multi-stripe anode are described. Section 4.3 explains simulation results for both configurations. In Section 4.4, fabrication process and characterization results are deliberated. Section 4.5 investigates the photodiodes in wafer level system integration for blue LED packages. Finally, conclusion comes in Section 4.6.

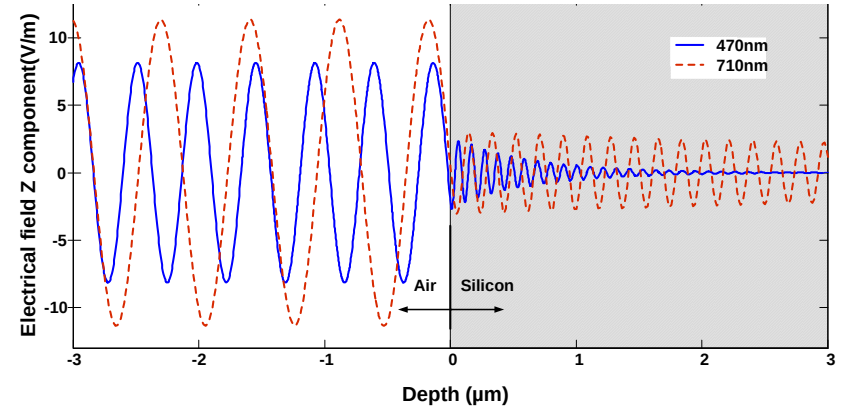
## 4.2 Photodiode Structure

In order to determine the best location to detect the blue light in silicon, light interaction was simulated using COMSOL Multiphysics. To check all physical aspects of the investigation, electromagnetic waves (Frequency domain) and semiconductor physic interfaces were coupled. The light illumination was simulated by solving the Helmholtz equations. This was achieved by analyzing the electromagnetic waves when it enters the device. The Fresnel equations were also employed to take multiple reflections of the propagating electromagnetic wave at each interface into account. The transverse mode of electromagnetic wave, which is a particular electromagnetic field pattern measured in a plane perpendicular to the propagation direction of the beam, was applied to solve the mentioned equations. The solution to these equations is the electric field which is needed for calculating the generation term. This electric field was used to calculate the Poynting vector, and hence the optical power. Finally, the generation term, which will be added to the final continuity equation, would be derived from the optical power as shown below:

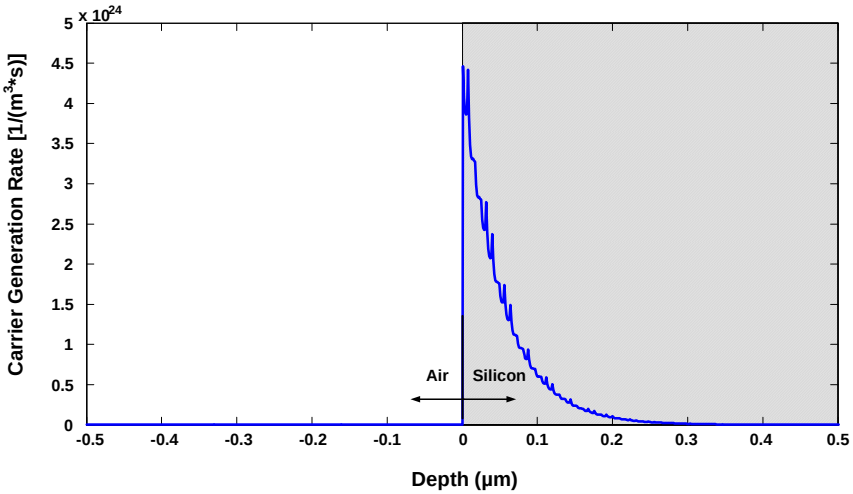
$$G = -\frac{\partial P_{op}}{\partial y} \times \frac{1}{hf}, \tag{4.1}$$

where $h$, $f$, $y$, and $P_{op}$ are respectively Plank's constant, frequency of the incident beam, depth and optical power. As the simulation results demonstrated, blue light ray optical power (470 nm) decays dramatically as it enters the silicon (Figure 4-2(a)).

Figure 4-2(b) displays carrier generation rate as a function of depth for 470 nm light in silicon interface. Hence it is shown that the best selective detection of the blue light occurs at the primary 300 nm from Si surface. Consequently, a photodiode with near surface P-N junction is required.



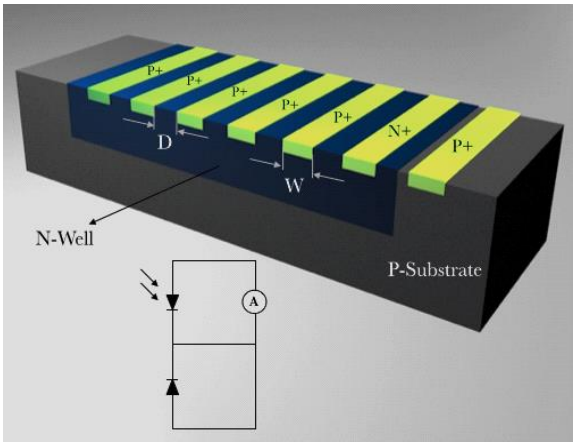

(a)



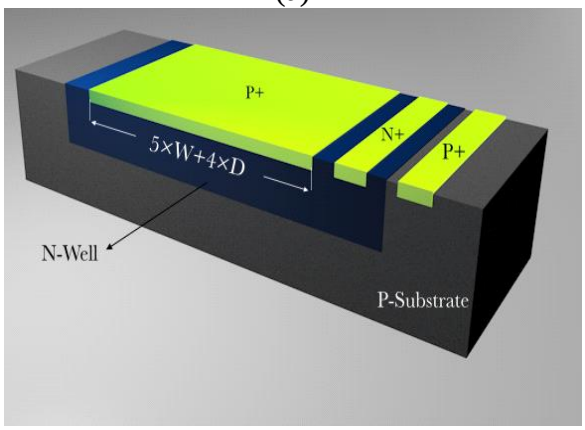

(b)

*Figure 4-2: (a) Electrical field for 470 and 710 nm light wavelengths, and (b) carrier generation rate as a function of depth for 470 nm light wavelength in silicon interface. Si interface is occurring at 0 μm for these plots.*

Two types of configurations for photodiode are considered; single anode and multi-stripe photodiodes. Figure 4-3(a) shows the schematic of the multi-stripe shaped photodiode and the equivalent circuit. This device is composed of stripe shaped $P^+$ regions, which are connected together as photodiode anode in an N-well (photodiode cathode). Biasing voltage is applied to the anode while the lower N-P junction is short-circuited in order to get only the photocurrent produced by the top shallow junction. $N^+$ and $P^+$ regions in the N-well and the P-substrate are for making low ohmic contacts. In the second photodiode, just a single anode but with rather large area is used (see Figure 4-3(b)). In this device, the anode geometry is simply a shallow $P^+$ region with width of 5W+4D, equal to sum of the width of all stripes (W) and the distances between them (D). The doping profiles for the $N^+$, $N^-$-well contact and $P^+$ substrate contact are the same as the multi-stripe shaped structure, but the anode is a wide $P^+$ region.




(a)




(b)

*Figure 4-3: Schematic of (a) the multi-stripe photodiode with its equivalent circuit and (b) the single anode photodiode.*

As illustrated in Figure 4-2, because the blue and UV spectrum is basically absorbed just beneath the surface, the dead layer formation due to high dose ion implantation decreases the responsivity significantly [13]. Due to a large number of defects in this region, electron-hole generated by target photons can recombine in the dead layer which is not desired and limit the sensitivity. This also creates an electric field which drifts more carriers towards the surface. Thus, by making multi-stripe shaped junction, we can minimize this problem. In this case, there is a shorter path for carriers to reach to the junction. Therefore, the dead layer in multi-striped structure in comparison to single anode structure is down scaled by W/(W+D) [10], which will improve the blue spectra responsivity. On the other hand, the effective depletion region area for photon absorption and carrier generation will increase in the multi-stripe shaped structure. This occurs due to the sides of the junctions in each $P^+$ region which are located very close to the surface.

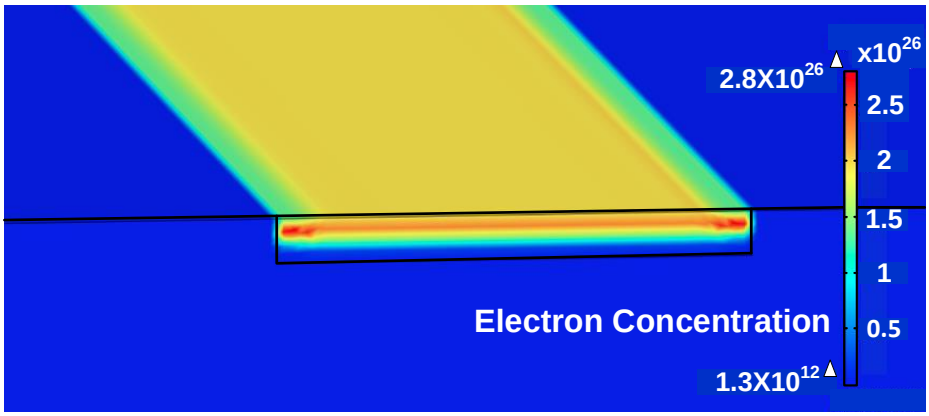



*Figure 4-4: Electron concentration in the $N^+$ region of the photodiode structure at 0 V bias condition.*

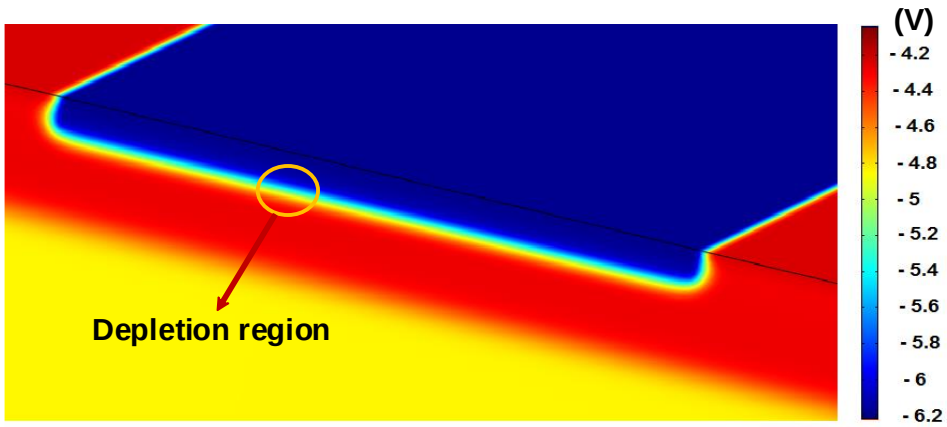



*Figure 4-5: Electric potential calculated from the vacuum level on a $P^+$ stripe to show where generation occurs in the depletion region.*

Although decreasing the junction length by converting single to multi shaped structure results in reduced photon absorption but on the other hand the dead layer recombination sites are decreased as well [10, 14].

For the multi-stripe shaped structure, the width of the stripes is 3 µm and the distance between two adjacent stripes is 5 µm. The stripes' length is 235 µm. According to these dimensions the shallow P-doped region for the single anode geometry is 35 µm.

## 4.3 Simulation and Discussion

Due to a large amount of surface defect generated during the doping process, Shockley-Read-Hall (SRH) recombination with a very high rate occurs at the surface which creates an electric field toward the substrate. The dead layer formation can be observed in electron concentration profile extracted from simulation as shown in Figure 4-4.

As discussed earlier, in order to improve selectivity and responsivity to blue rays, the active junction should be located in the top 300 nm inside the substrates. As shown in Figure 4-5, the junction depletion region, where generation occurs, happens mostly inside the N-well region and extends for about 150 nm. According to reports [13], a high level doping in ion implantation and boron redistribution during the annealing process, will cause dopant pileup in an interfacial layer between the top $SiO_2$ layer and Si. This layer acts as a sink for inactive dopant atoms in this region.

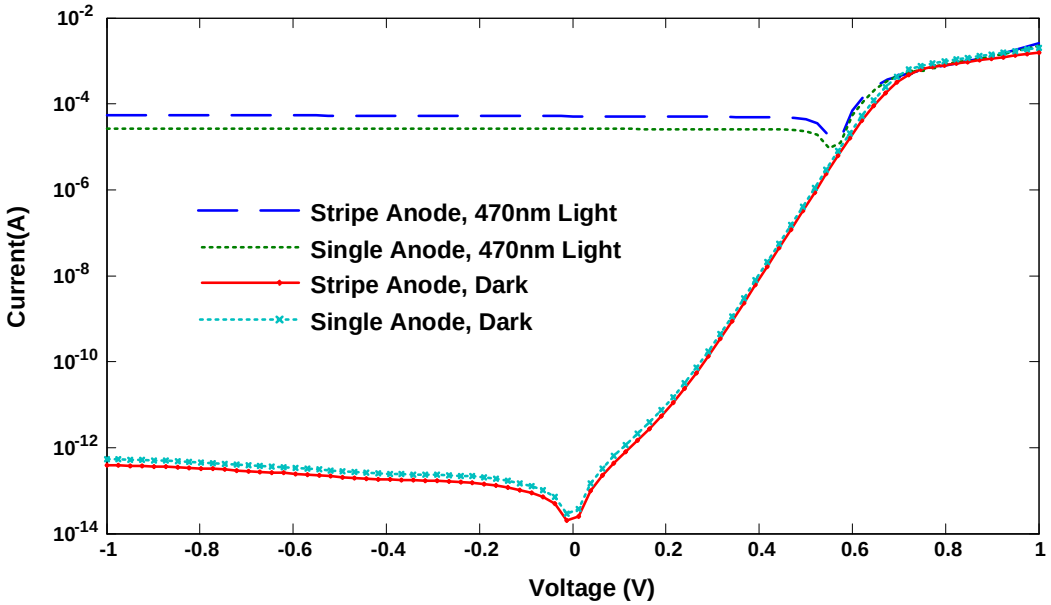
The anode current of the photodiode was simulated using the continuity equation consisting drift-diffusion, generation and recombination rates. Both single- and multi-stripe structures were analyzed without 470 nm radiation (see Figure 4-6(a)). The resulted I-V shows a bit higher current for the single-stripe structure compared to the multi-stripe structure under the dark condition due to the higher current cross-section area. However, multi-stripe device showed a 2.5 times improvement in the output current under illumination of 470 nm waves compared to the single anode one, which is a proof of concept for the significance of the dead layer and active depletion region. It is meaningfully matched with the improvement factor [10], we expected regarding to the designed parameter for D and W dimensions which is $(W+D)/W = 2.66$.

Figure 4-6(b) shows the responsivity curve for multi-stripe shaped samples extracted by sweeping the photons' wavelength in the simulation tool. It can be seen that using the real doping values and dimensions, the responsivity is very selective to 470 nm illumination. This can be explained by the fact that at higher wavelengths, the beam can travel a lot more inside the substrate and in order to absorb that range, one might need to increase the depletion width of the junction. But, at lower wavelengths, the junction must be located closer to the surface to have strong generation of carriers which consequently may recombine in the dead layer.

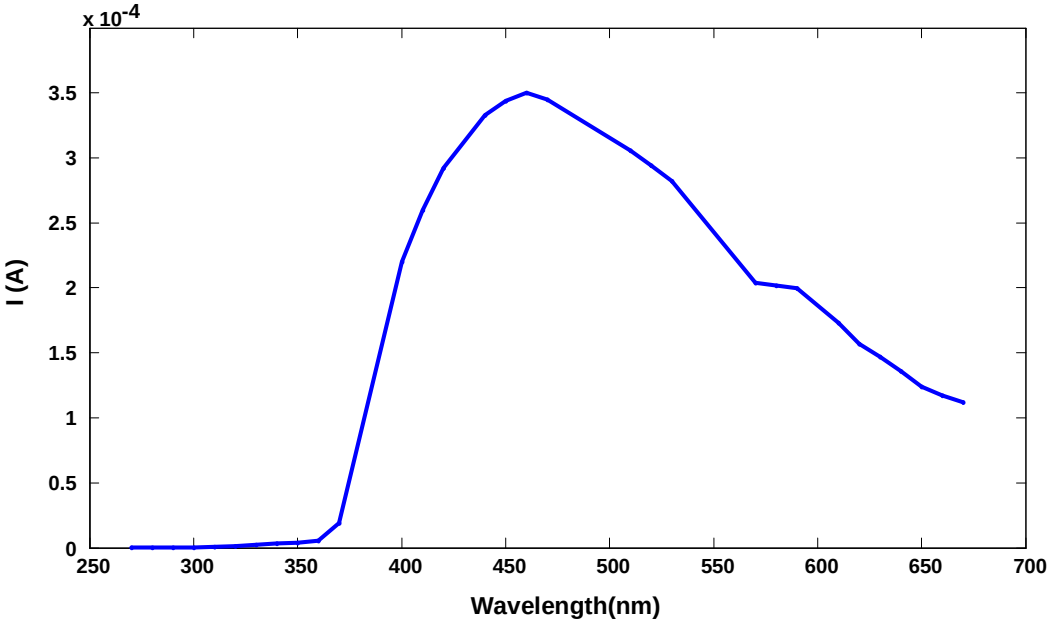
## 4.4 Device Fabrication and Characterization

The photodiodes were implemented in the BiCMOS5 process as described in Chapter 3. It exhibits the two outstanding features: simplicity and cheapness [15]. As discussed in Chapter 3, there are several trade-offs in the process design. An important trade-off here is between device parameters of photodiodes (junction depth, responsivity, and selectivity) and transistors (threshold voltage and saturation current). The dopant concentrations and parameters of the N-

and P-regions affect these different device parameters.




(a)




(b)

*Figure 4-6: (a) I-V simulation results of the single- and multi-stripe structures w/o 470 nm radiation, and (b) the resulted current vs. wavelength for the multi-stripe structure.*

However, the doping parameters applied in this study were adjusted using device and process simulations for the optimum performance of the photodiodes by using Synopsys TCAD. Figure 4-7 illustrates the doping profile of the $P^+$-doped/N-well area measured by electrochemical capacitance-voltage profiler (ECVP). Due to the fact that the ECVP measures the active carrier

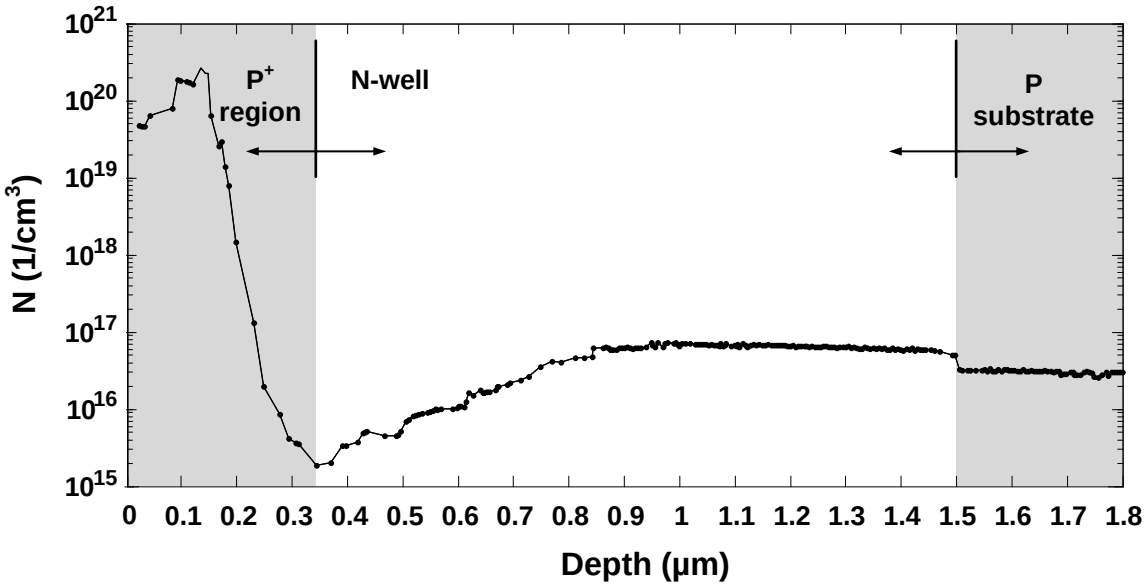



*Figure 4-7: ECVS profile of shallow $P^+$ region implanted in the N-well. The $P^+$-N junction is formed at 330 nm where the doping profile is first crossing N-well doping level.*



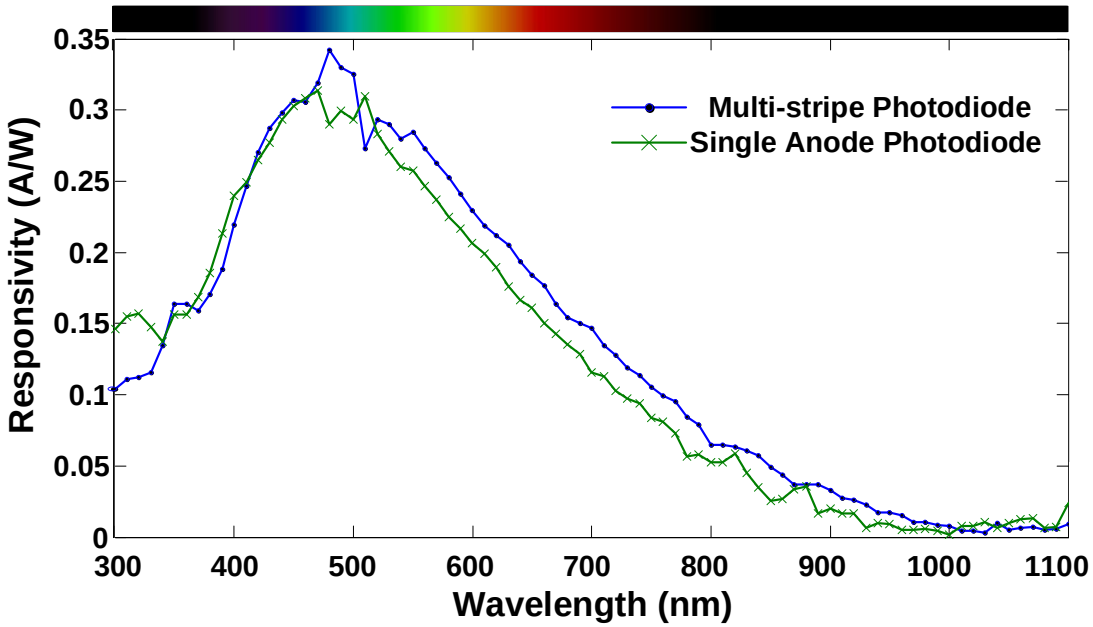



*Figure 4-8: Measured responsivity vs. wavelength for multi- and single-stripe shaped photodiodes.*

concentration, the dead layer cannot be observed in this figure. The minimum at 330 nm is the $P^+$/N-well junction and the N-well is extended for 1.5 µm into the substrate.

The spectral responsivity of photodiode was measured by a solar cell simulator using a monochromatic light with sweeping wavelength in 300-1100 nm range. The responsivity plot shows a peak at λ= 480 nm with 342 mA/W. Figure 4-8 shows the responsivity of two different

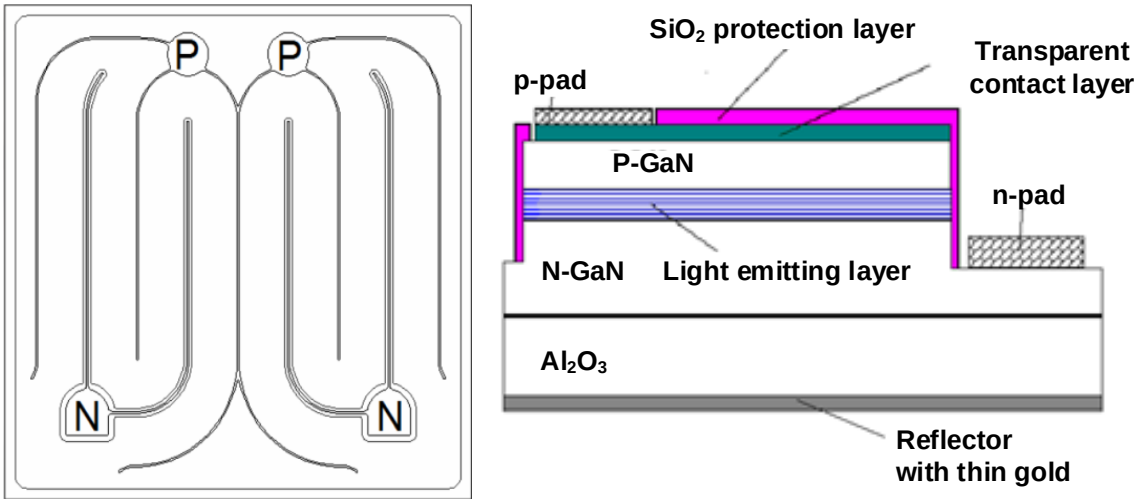



*Figure 4-9: PN junctions and die structure for Bridgelux blue power LED die.*



photodiodes vs. wavelength at 0 V bias condition. Comparing to the single anode structure, an improvement in responsivity is observed for the multi-stripe photodiode. IR range responsivity shows a dramatic fall above 470 nm range which indicates a high selectivity for the target wavelength. The measured responsivity has a good correlation to the simulation results in Figure 4-6(b).

A selectivity parameter can be defined as a ratio of responsivity for different wavelength, that is 42 for λ=470 nm and λ=1000 nm. It was seen that at high bias voltages, the responsivity can increase, while, because of the depletion area extension, selectivity would degrade.

## 4.5 Wafer Level System Integration

The target vertical LED in this study is a Bridgelux® Blue Power Die which is an InGaN-based blue color LED that can be later combined by a yellowish phosphor to generate the white output light. LED structure is shown in Figure 4-9 and its main specifications were summarized in Table 3-1. These LEDs are useful in a broad range of applications such as general illumination, automotive lighting, and LCD backlighting.

The photodiodes were also measured in the integrated system to study its performance for target LEDs and in real application platform. The package consists of an array of 4 LEDs which can be turned on separately or with different combinations. Figure 4-10 shows the package picture with mounted LED dies in “off” and “on” states and photodiode positions.

Each LED chip consists of two parallel P-N junctions which we just used one of them in the

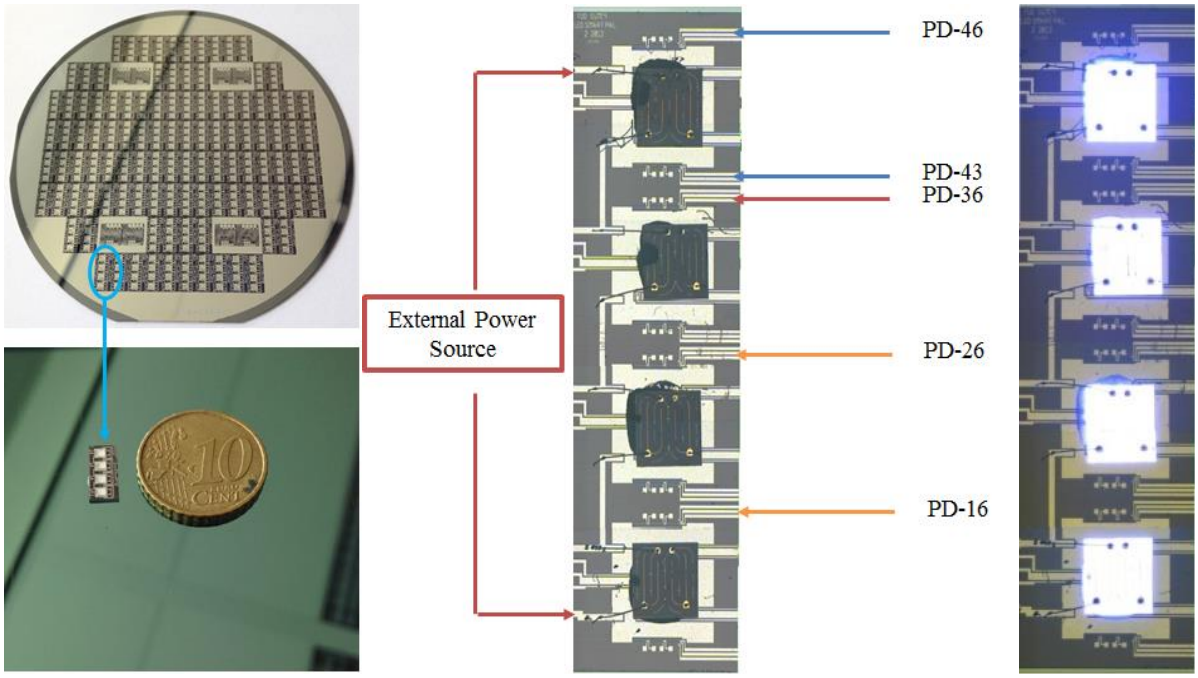


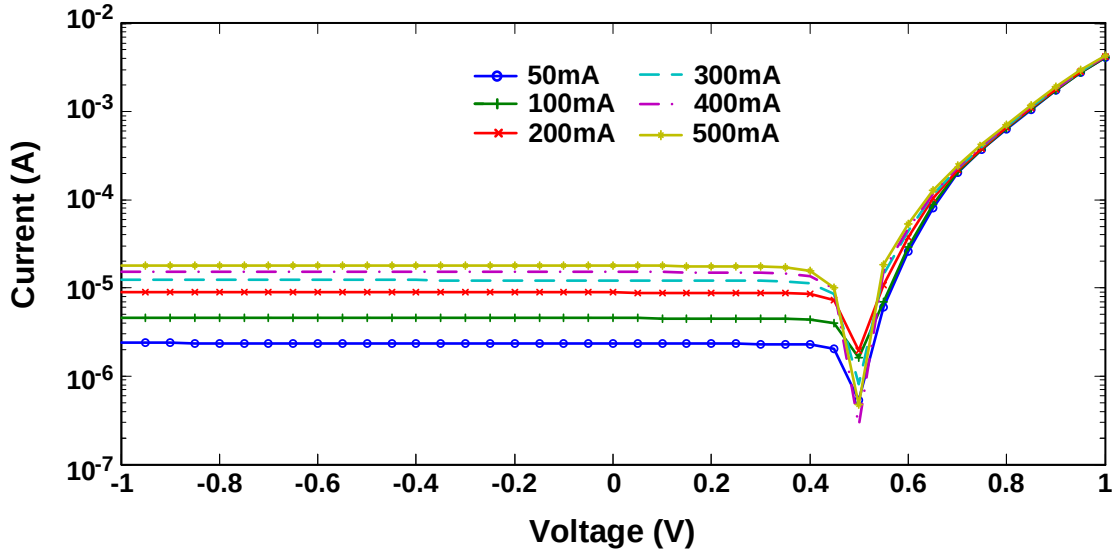

*Figure 4-10: Photodiodes in LED package with mounted LED dies in "off" and "on" states. For each LED two sets of photodiodes were used to perform output light measurement.*



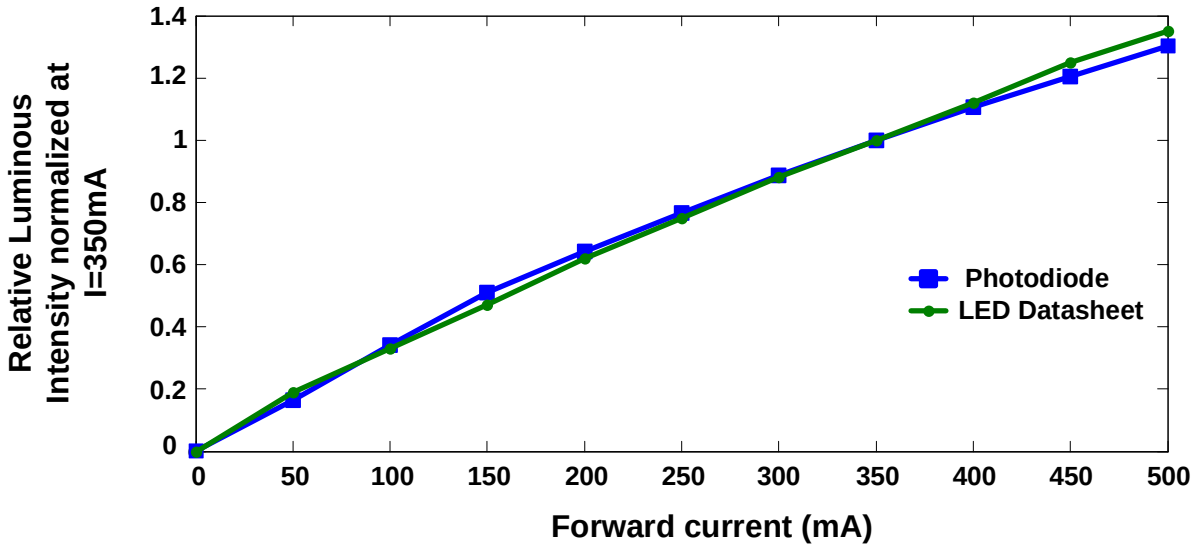
package. The light intensity of LED was measured with the photodiodes at different driving currents. The results are shown in Figure 4-11. When LED is off, the reverse current value is 1 pA. Figure 4-11(a) shows almost 6 orders of magnitude increase compared to when the LED is off. This difference is governed by the generation of lots of electron-hole pairs in the active part of the device and a numerous recombination dominantly close to the surface. By normalizing the output current and fitting to the datasheet amounts a remarkable consistency can be achieved (see Figure 4-11(b)).

The devices also were examined by some sort of stress test. Relative luminous intensity decays 0.9% within 2 hours with constant input current of 350 mA, see Figure 4-12 (a-b). This effect is caused by the temperature rise during the lighting. This is a proof of sanity for the importance and necessity of an intelligent control system for LEDs. It is worth mentioning that the ambient light rarely affects the performance of photodiode, due to its remarkable blue light selectivity.

Figure 4-13 compares the spectral responsivities of the fabricated photodiodes here and a calibrated UV-enhanced photodiode from Hamamatsu, S1226-18BQ. The commercial UV-enhanced device with an antireflection coating exhibits an almost non-selective behavior.




(a)

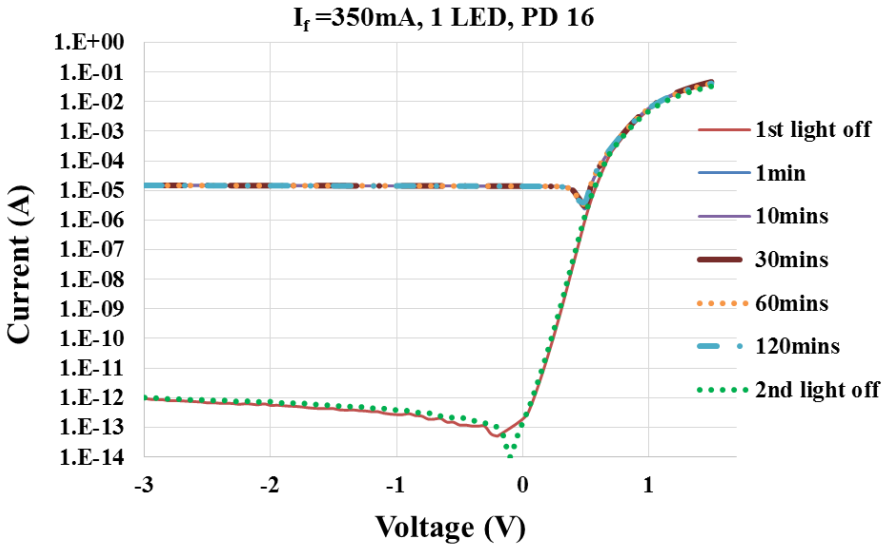



(b)

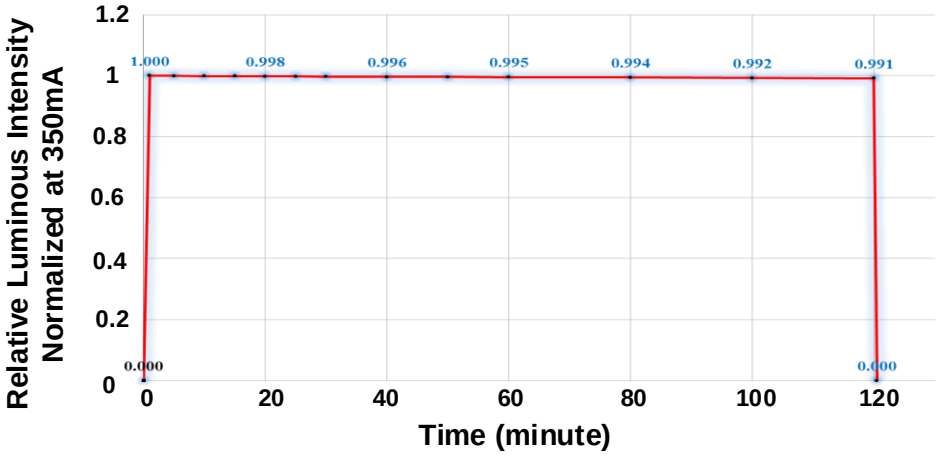
*Figure 4-11: (a) Measured photodiode IV characteristic at different LED driving current. (b) Relative luminous intensity vs. LED forward current comparing the measured photodiode performance with the datasheet amounts.*

However, our photodiode and the one manufactured in [10] demonstrate slightly lower responsivity for the deep ultraviolet spectral range. The responsivity of the device fabricated in [10] has a peak at 400 nm, while the photodiode in this study has shown a peak at exactly 480 nm which is remarkably matched with the illuminated wavelengths from the LED. A rapid decreasing trend is observed for the visible and IR ranges. Quantum efficiency is defined as:

$$QE_\lambda = \frac{R_\lambda}{\lambda} \times \left(1240\ W \cdot \frac{nm}{A}\right), \tag{4.2}$$




(a)




(b)

*Figure 4-12: (a) Measured photodiode IV characteristics over 120 min LED light exposure. (b) Normalized readout light intensity in LED working period of 2 hours.*

where λ is the target wavelength and $R_\lambda$ is the related responsivity. Moreover, a two-fold increase in quantum efficiency and comparable selectivity are evaluated for the LEDs fabricated in our work compared to the previously published devices.

## 4.6 Conclusion

A silicon stripe-shaped photodiode was designed and fabricated for sensing blue light in LED wafer level package. The device dimensions and doping were also designed and simulated using COMSOL Multiphysics. The maximum responsivity was at 480 nm which is matched with the blue LED's illumination. The single anode structure due to higher rate of recombination caused

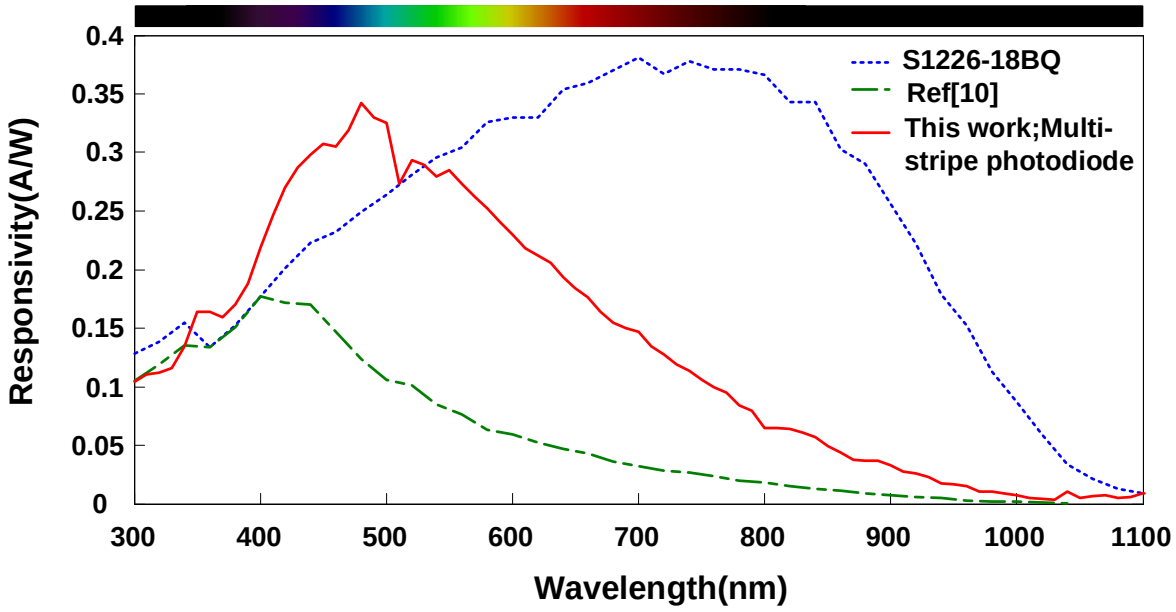



*Figure 4-13: Measured responsivity vs wavelength for the multi-stripe photodiode. The spectral response of a published and commercially available UV-enhanced photodiode is also added for comparison.*



by the dead layer formation showed lower responsivity compared to multi-stripe shaped one. The photodiode was fabricated in a 5 mask BiCMOS process with 2 µm gate length. These IC technology compatible photodiodes, with junction at 330 nm, demonstrated a very high selectivity to blue light. The fabricated devices presented a two-fold increase in the responsivity and quantum efficiency for blue spectra compared to similar devices published earlier.

## 4.7 References

[1] S. Chhajed, Y. Xi, Y.-L. Li, T. Gessmann, and E. F. Schubert, "Influence of junction temperature on chromaticity and color-rendering properties of trichromatic white-light sources based on light-emitting diodes," *J. Appl. Phys.*, vol. 97, no. 5, p. 54506, 2005.

[2] Y.-C. Lin, J. P. You, N. T. Tran, Y. He, and F. G. Shi, "Packaging of Phosphor Based High Power White LEDs: Effects of Phosphor Concentration and Packaging Configuration," *J. Electron. Packag.*, vol. 133, no. 1, p. 11009, 2011.

[3] J. Lau, R. Lee, M. Yuen, and P. Chan, "3D LED and IC wafer level packaging," *Microelectron. Int.*, vol. 27, no. 2, pp. 98–105, 2010.

[4] ETAP Lighting, "LED LIFETIME IN PRACTI C E - THE ETAP APPROACH." .

[5] R. Zhang, S. W. R. Lee, D. G. Xiao, and H. Chen, "LED Packaging using Silicon Substrate with Cavities for Phosphor Printing and Copper-filled TSVs for 3D Interconnection," in *Electronic Components and Technology Conference*, 2011, pp. 1616–1621.

[6] C. T. Tsou and Y.-S. Huang, "Silicon-Based Packaging Platform for Light-Emitting Diode," *IEEE Trans. Adv. Packag.*, vol. 29, no. 3, pp. 607–614, Aug. 2006.

[7] J. K. Kim and H. C. Lee, "A photo-sensor on thin polysilicon membrane embedded in wafer level package LED," in *Proceedings of the SPIE*, 2012, vol. 8431, pp. 8431–7.

[8] G. Corporation, "A Silicon Ultraviolet Detector," *Sensors and Actuators*, vol. 23, pp. 553–558, 1990.

[9] N. Kako and C. Suzuki, "Combustion detection with a semiconductor color sensor," *Sens. actuators*, vol. 4, pp. 655–660, 1983.

[10] A. Pauchard, P. Besse, and R. S. Popovic, "A silicon blue/UV selective stripe-shaped photodiode," *Sens. actuators*, vol. 76, pp. 172–177, 1999.

[11] M. Zhang, H. Zhang, K. Lv, W. Chen, J. Zhou, and L. Shen, "Ultraviolet photodetector with high internal gain enhanced by TiO 2 / SrTiO 3 heterojunction," *Opt. Express*, vol. 20, no. 6, pp. 1977–1981, 2012.

[12] J. W. Levell, M. E. Giardini, and I. D. W. Samuel, "A hybrid organic semiconductor / silicon photodiode for efficient ultraviolet photodetection," *Opt. Express*, vol. 18, no. 4, pp. 3219–3225, 2010.

[13] J. D. Plummer, M. D. Deal, and P. B. GRiffin, *Silicon VLSI Technology Fundamentals*,

*Practice and Modeling*. Prentice Hal, 2000.

[14] Z. Kolahdouz Esfahani, A. Rostamian, M. Kolahdouz, T. Ma, H. Van Zeijl, and G. Q. Zhang, "Blue Selective Photodiodes for Optical Feedback in LED Wafer Level Packages," in *ESSDERC*, 2014, pp. 174–177.

[15] N. S. Lawand, H. van Zeijl, P. J. French, J. J. Briaire, and J. H. M. Frijns, "Titanium nitride (TiN) as a gate material in BiCMOS devices for biomedical implants," in *IEEE Sensors*, 2013, pp. 1–4.

# Chapter 5

# Integration of Monolithic Light Feedback Control Circuit for Blue/UV LED Smart Package[6]



Given the performance decay of high power LED chips over time and package condition changes, having a reliable output light for sensitive applications is a point of concern. In this chapter, design and implementation of a light feedback control circuit for blue/UV LED using a low cost 7-mask BiCMOS process are elaborated. The feedback circuit was monolithically integrated in a package with 4 high power blue LED chips. For sensing the intensity of exact colored blue/UV light in the package, selective photodiodes at 480 nm wavelength were implemented. An opamp-based feedback circuit combined with a high power transistor controls the output light based on real-time sensor data. The whole system is a low-cost integrated package that guarantees a stable and reliable output light under different working conditions. Output light can be also controlled linearly by a reference input voltage.

[6] This chapter is partially submitted as: Z. Kolahdouz, M. Tohidian, M. Kolahdouz, H. van Zeijl, and K. Zhang, "Monolithically Integrated Light Feedback Control Circuit for Blue/UV LED Smart Package," to IEEE Photonics Journal.

## 5.1 Introduction

As discussed in Chapter 3 and 4, aging and high junction temperature affect light wavelength and intensity of phosphor-based white LED packages [1]–[3]. Controlling driving current of LED can well eliminate these problems.

Different groups reported integration of sensors and controlling blocks in Si-based LED WLP [3]–[6]. However, developing a complete real-time light output controlling block in a low-cost process is still a point of interest.

To address the above issues, a control circuit in LED package is designed and monolithically integrated. It controls the light output of the package with a real-time feedback signal from light sensor that receives emitted blue light of LED chips. The fabrication is done through a simple and low-cost 7-mask BiCMOS process (BiCMOS7). This integrated package incorporates a blue selective photodiode (as the light sensor) that was previously described in Chapter 4 [7]. The package guarantees a stable light output that is linearly controllable with a reference input voltage.



This chapter is organized as follows: in Section 5.2, system level design of feedback control circuit is discussed which explains: feedback circuit, design of operational amplifier (opamp), power transistor, target LED, and the blue selective photo diode. Section 5.3 summarizes system implementation. In Section 5.4, test procedure and measurement results are deliberated. Finally, conclusion comes in Section 5.5.

## 5.2 System-Level Design of Feedback Control Circuit

A control box for a smart LED package should fulfill several considerations:

1. Stability of the light intensity and color temperature against different working conditions: if due to any reason such as increased package temperature, there is a decay in intensity or a shift in color, the feedback circuit must keep the blue index of light output at desired value.
2. Compensation for aging effects of LED chips: according to the lifetime prediction of LED chips from some of the manufacturing companies [8], [9], the performance decays critically over the time. Although phosphor and material aging cannot be controlled electrically, package aging can be partially recompensed by controlling the driving

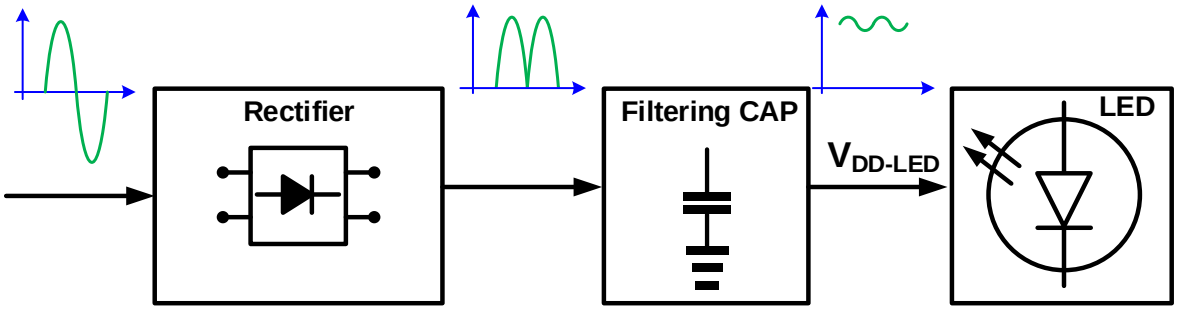



*Figure 5-1: Block diagram of AC to DC converter used in LED packages. A fast light feedback system can suppress the ripples on $V_{DD\_LED}$.*

current.

3. Dimming the light output intensity with a reference input: in some applications it is necessary to have a reliable level of light output with dimming capability controlled by an extra reference values.
4. Filtering ripples of power supply: usually power voltage of LED is provided by a rectifier from an AC source (an example is shown in Figure 5-1). To have a stabilized light output of the LED package, the rectified signal is then filtered with a capacitor to reduce its ripples. However, a good and clean DC signal requires a large capacitor which increases the cost. As studies reported [10]–[12], LED voltage and current ripples can decrease efficacy (lm/W) up to 4 %. Moreover, if dissipated power of the LED is not regulated, a high ripple may increase the LED junction temperature. This ripple can be substantially removed with a fast enough feedback circuit and avoids any efficacy degradation. Hence the filtering capacitor can be also smaller/cheaper. Moreover, it enables further integration of this capacitor that can result in additional cost reduction.

Using a linear feedback circuit that monitors selectively blue light output of the LED tackles all these concerns. This control circuit has been integrated together with a driving power transistor into the silicon package of LED to reduce cost and increase reliability.

### 5.2.1 Feedback Circuit

The control circuit basically consists of 2 operational amplifiers (opamp) and a power transistor. It is schematically shown in Figure 5-2. The input is a current signal from the blue selective photodiode, which instantly senses the light output of LED chip and turns it into current ($I_{in}$). This current makes a voltage drop over a 40 kΩ resistor ($R_1$) that is biased over a common-

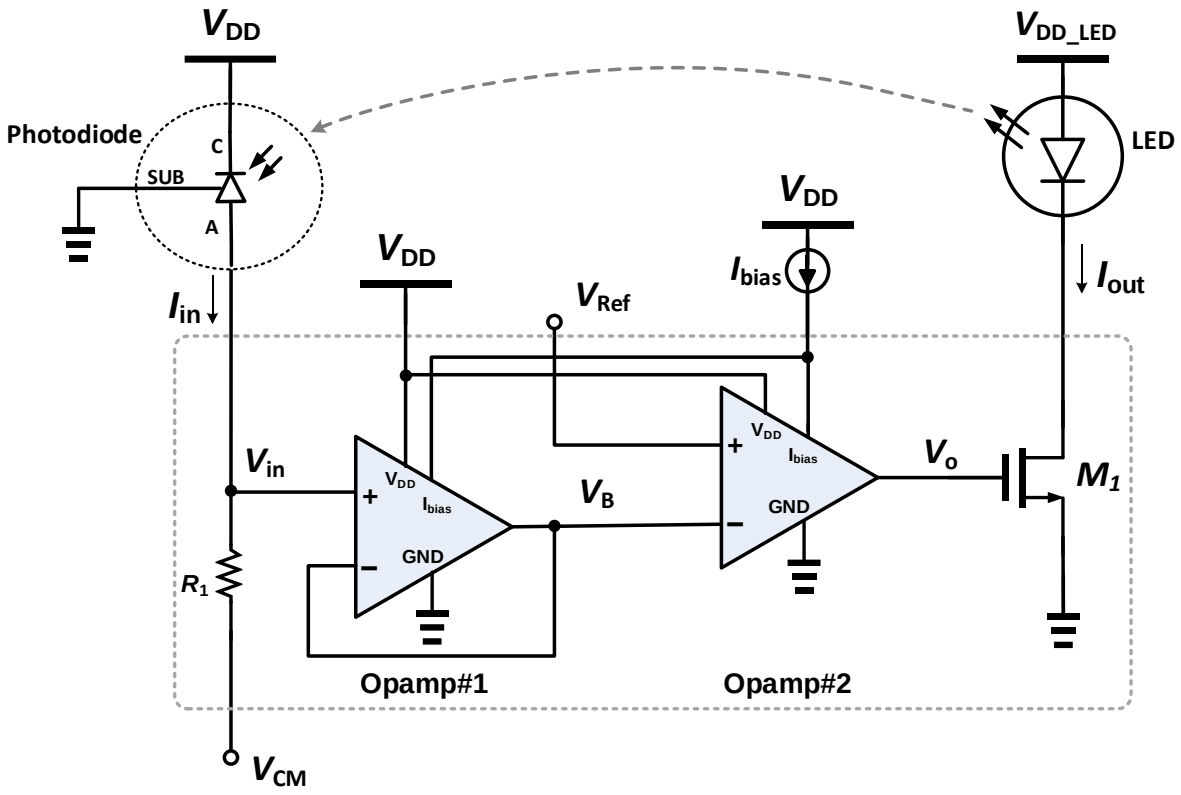



*Figure 5-2: Schematic of the light feedback control circuit.*



mode voltage ($V_{CM}$). Input voltage ($V_{in}$) is then buffered through the first opamp ($V_B$). This buffer stage avoids any unwanted capacitive loading in the sensing circuit. It also provides reverse isolation from output of the second opamp with a high gain to the sensitive (high impedance) node of the sensor ($V_{in}$) and improves loop stability. In the second stage, $V_B$ is compared with a reference voltage ($V_{Ref}$) and then amplified with a very high gain (>200×). The output voltage ($V_O$) is then fed to a power transistor ($M_1$). This transistor drains a current through the LED from $V_{DD\_LED}$.

Polarity of the whole feedback is set in a way to make a negative feedback loop. The photodiode senses intensity of the blue light emitted from the LED. The higher LED light intensity, the higher photocurrent ($I_{in}$). So, it increases $V_{in}$ and consequently $V_B$. This is then compared with $V_{Ref}$ and amplified with a high negative gain. Hence, $V_O$ is decreased. This reduces the drain current of the power transistor and in turn reduces and regulates the LED light intensity.

As the loop has a very high gain, it can be assumed that $V_B$ (and $V_{in}$) is forced by the feedback

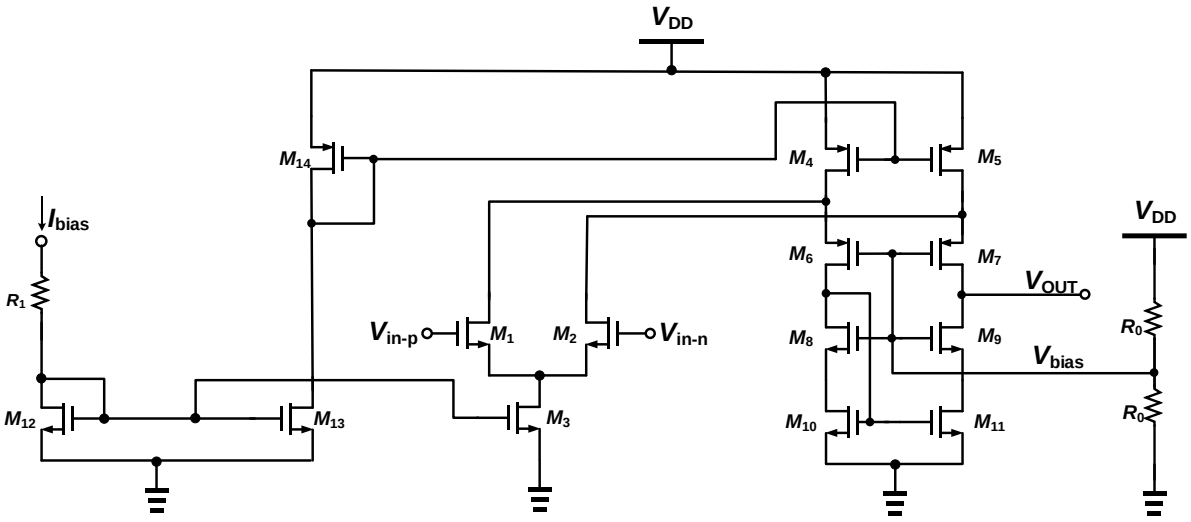



*Figure 5-3: Schematic of designed folded cascode opamp.*

to be equal to $V_{Ref}$. Therefore, we can have the following equation:

$$V_{in} = R_1 \times I_{in} + V_{CM} = V_{Ref} \quad \Rightarrow \quad I_{in} = \frac{V_{Ref} - V_{CM}}{R_1}, \tag{5.1}$$

Since $I_{in}$ is a linear function of its input light intensity, light output of the LED is a linear function of the reference input voltage, $V_{Ref}$.



### 5.2.2 Opamp

For the feedback control circuit, a high gain opamp structure is required to minimize feedback error. The first option can be a single stage opamp which has a good frequency stability. However, it cannot provide a high gain (< 30dB in our used process). Aiming a higher gain, there are two common options: cascode and two-stage structures [13], [14]. Although the two-stage structure provides a very high gain and excellent input common-mode (CM) range, it suffers from poor stability that makes frequency compensation techniques unavoidable. Thus, the cascode structure was chosen, which does not require any frequency compensation and has a single-pole like transfer function. This is very important to make the whole feedback system stable.

Implementation wise, telescopic cascode structure [13], [14] eats up all the voltage headroom for input CM range and output swing. Therefore, for the final implementation, folded-cascode structure (see Figure 5-3) was chosen. It can have a high input CM range with good enough output swing for our application. Additionally, it provides a high power supply rejection ratio (PSRR) [14] that makes supply variations less of a concern. The folded-cascode structure has an

inferior noise performance compared to both telescopic cascode and two-stage structures. This is mainly due to the additional current source used for folding ($M_{4,5}$). However, noise level of this opamp structure is still quite low for general illumination applications.

To calculate the gain, let us assume that a small voltage $\Delta V = V_{in-p} - V_{in-n}$ is applied to the opamp. The current flowing to the output will be $\frac{g_{m1}\,\Delta V}{2} + \frac{g_{m2}\,\Delta V}{2}$, where $g_m$ is small-signal voltage to current gain of transistors. The output resistance can be approximated as following [14]:

$$R_{out} \approx {}^{1}\!/_{2}\, g_m {r_{ds}}^{2}\,, \tag{5.2}$$

where $r_{ds}$ is small-signal drain-source resistance of the transistors. So, the total gain is:

$$\frac{V_{out}}{\Delta V} = R_{out} \times I_{out} = ({}^{1}\!/_{2}\, g_m {r_{ds}}^{2})(\frac{g_{m1}\,\Delta V}{2} + \frac{g_{m2}\,\Delta V}{2}) = {}^{1}\!/_{2}\, {g_m}^{2} {r_{ds}}^{2}. \tag{5.3}$$

Bias current flows through $R_1$ and then $M_{12}$ is mirrored in $M_3$, which provides the current of the input stage. It is also mirrored into $M_{4,5}$ throughout $M_{13,14}$. The bias voltage ($V_{bias}$) for the cascode stage is made out of a resistor ladder. Based on simulation, $V_{DD}/2$ value for $V_{bias}$ provides almost a symmetric output swing.

As shown in Figure 5-2, the second opamp does not have any local feedback. Thanks to the folded-cascode structure, the open loop transfer function of the second opamp can be approximated by a single-pole. Output resistance of this opamp together with input capacitance of the power transistor makes dominant pole of the system. The second pole is made by parasitic capacitance on node $V_{in}$ and the resistor $R_1$. The $R_1$ was designed in such a way that places the second pole far enough from the first one. Thereby, the feedback loop becomes stable considering its loop gain.

### 5.2.3 Power Transistor

Due to BiCMOS7 process limitation, the minimum gate channel length is 2 µm. To improve area yield and decrease the parasitic resistance, an interdigitated NMOS structure was used. Each unit cell transistor has a total W/L=1800µm/2µm. Source and drain are 5 finger-shaped $N^+$ areas in P-substrate that makes layout of each unit a square (optimum balance between parasitic resistance and capacitance). A higher number of fingers reduces parasitic series resistance, but also increases parasitic capacitance. The final transistor was made out of four parallel units to

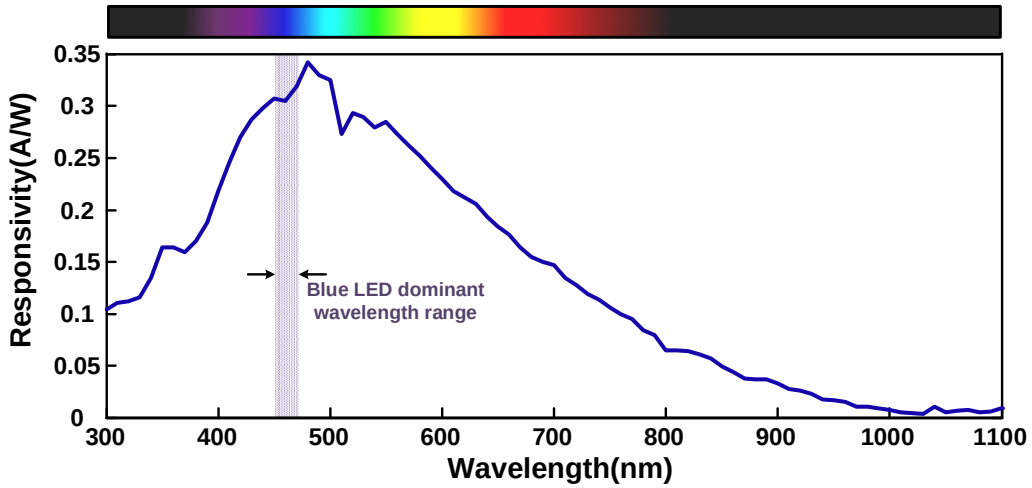



*Figure 5-4: Responsivity versus wavelength measurement result for the blue-selective photodiode (the patterned inset shows the dominant wavelength of target LED).*

supply the required output current (maximum 700 mA). More details and layout were discussed in Chapter 3.

### 5.2.4 Blue-Selective Photodiode

For blue selective photodiode, a silicon stripe-shaped photodiode was previously introduced in Chapter 4 [7]. It improves the responsivity by increasing active depletion region and consequently reducing the effect of dead layer formation of the shallow junctions. This photodiode with junction at 330nm, achieved a very high selectivity to blue light. Its maximum responsivity at 480nm wavelength fits to the blue light output of the target LED. The selectivity parameter (ratio of responsivity for different wavelengths) is 42 for wavelength of 470 nm compared to 1000 nm. The measured responsivity vs. wavelength for our target range is given in Figure 5-4.

### 5.2.5 Target LED

The target LED in this study is a Bridgelux® Blue Power Die, which is an InGaN-based blue color vertical LED. The LED dimension is 1143×1143×150 $\mu m^3$ and the maximum DC driving current is 700 mA. Dominant wavelength in nominal condition is in 450-470 nm range. It can be used for a broad range of applications including general illumination, street lights, portable lighting, architectural lighting, directional lighting, wide area lighting, display backlighting, digital camera flash, and automotive lighting, and the most remarkable one is lighting element in phosphor-based white LED package [15].

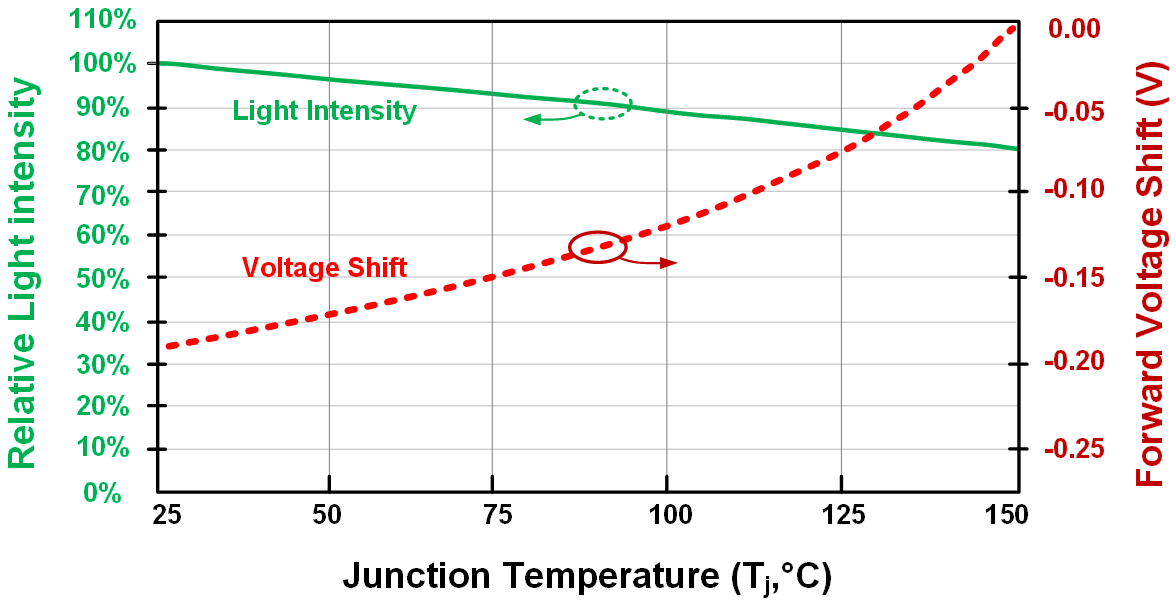



*Figure 5-5: Relative light intensity and forward voltage shift (normalized at 350mA, $T_j$=25°C) versus junction temperature. The data was reproduced from datasheet* [15].



According to the LED datasheet [15], high junction temperature leads to forward voltage shift, light intensity decay, and wavelength shift, as shown in Figure 5-5. The light intensity decays up to 20% and forward voltage changes up to -0.4 V at a junction temperature of 150 °C. Consequently, an integrated controlling block would have significant opportunities to enable a reliable light intensity and color temperature.

## 5.3 System Implementation

The complete package size is 4.5×10 $mm^2$. It integrates four LEDs on a silicon heat sink. The LEDs are connected in series and can be turned on with different combinations. This Si-based high-power, high-lumen package can illuminate up to 1200 lumen at the output. There were also some more sensors and devices integrated (such as electrostatic discharge -ESD- protection diode, temperature sensor, and readout circuit) that were previously discussed in previous chapters. For each of the LEDs, there are sets of temperature and light sensors.

Figure 5-6(a) illustrates complete schematic of the package with components used on its test PCB. As it is shown, instead of using extra source for different inputs, just one $V_{DD}$ was used and other inputs such as $V_{CM}$, $I_{bias}$ and $V_{Ref}$ were made by external potentiometers. The layout and chip micrograph is given in Figure 5-6(b).

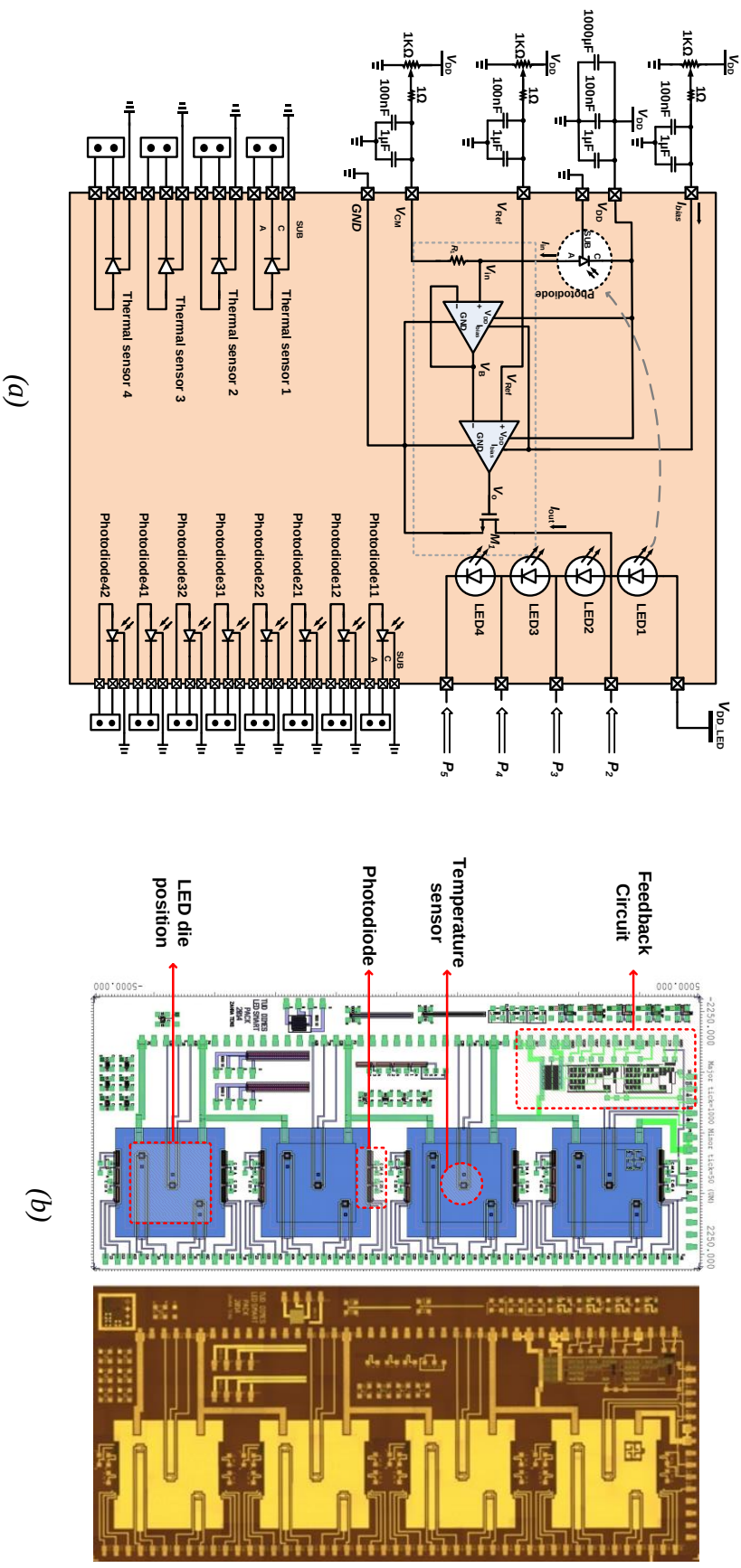



*Figure 5-6: (a) Schematic of the package, (b) layout, and chip micrograph showing component positions in the package.*

5

The whole system was fabricated using the 2 µm 7-mask BiCMOS process with 2 metal layers. Although the BiCMOS7 cannot fabricate advanced submicron transistors due to size and process flow limitations, it is a relatively low-cost and straightforward process. The seven masks include N-well, $N^+$ area, $P^+$ area, contact opening, first metal, via opening, and second metal. More details on BiCMOS process can be found in Chapter 2 and 3.

For process simplicity, metal gates instead of poly has been used in BiCMOS7. So resistors were implemented with $N^+$ area in P-substrate. It should be mentioned that resistance of this type of resistor shows a small dependency on temperature, light, and bias conditions which should be considered in the design. Also, leakage current of a reverse biased PN junction (P-sub is grounded) is always there but negligible in most of the designs. To have a simple and consistent layout design, all the transistors of the opamps are sized $W/L$ = 400µm/4µm.

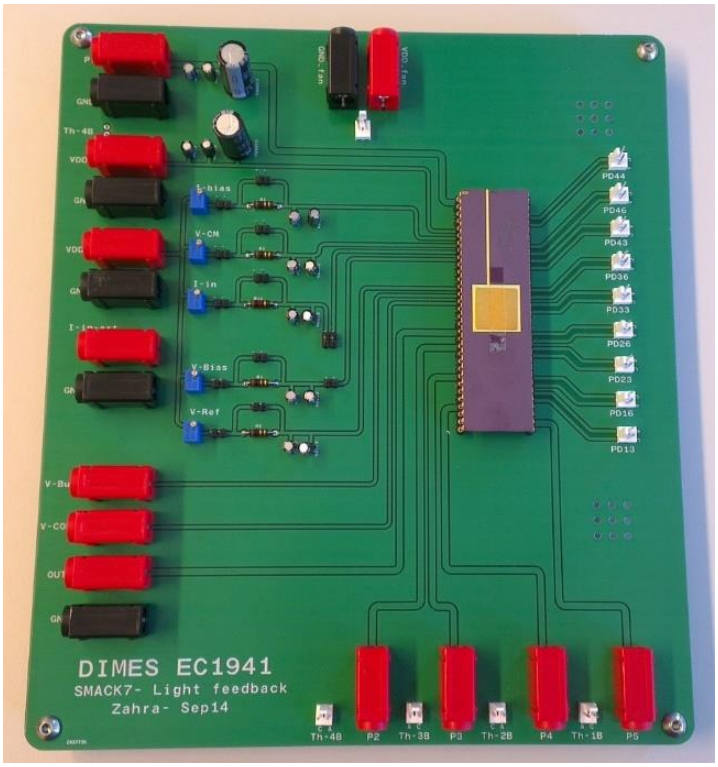
Transistor and device models were extracted from a sample run with same parameters and used for design and simulation. After preparing the Si package, it was diced and LED dies were mounted (with a thermal-conductive glue) and wire bonded in predefined positions, on top of the temperature sensors and next to the light sensors.

The PCB test board and characterization setup are shown in Figure 5-7(a-b), respectively.

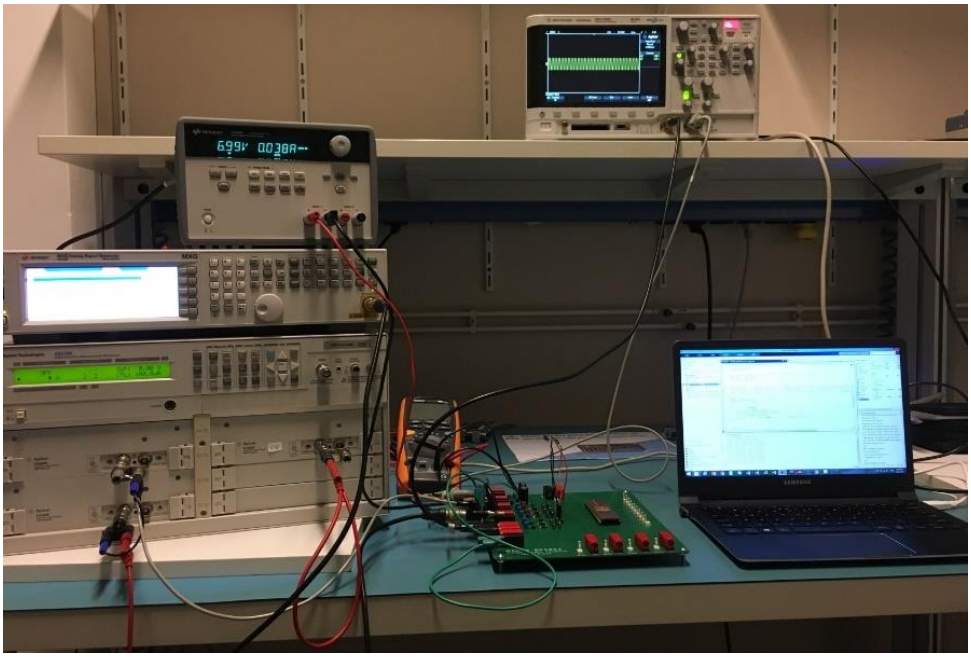
## 5.4 Measurement Results

### 5.4.1 Opamps

Firstly, the opamps were characterized. For all the tests $V_{DD}$ is set to 7 V and $I_{bias}$ is 100 µA (total for the two opamps). Opamp#1, see Figure 5-2, is in unity gain feedback configuration (voltage buffer). DC voltage on $V_{in}$ node of the chip was swept from 0 V to $V_{DD}$, and the output of opamp#1 was measured. Based on results of this measurement which is shown in Figure 5-8(a), the opamp achieved an input/output buffering range between 1.2 and 7 V. According to this result, $V_{CM}$ can be set to 1.5 V to be always on the safe side for operating input range of the opamps. Figure 5-8(b) shows measured frequency transfer function of opamp#1, including its output load (coming from input of opamp#2). In this test, a sinusoidal signal was applied to the input, and gain of the opamp was measured at different input frequencies. Based on the results, the opamp has 300 kHz unity gain bandwidth.



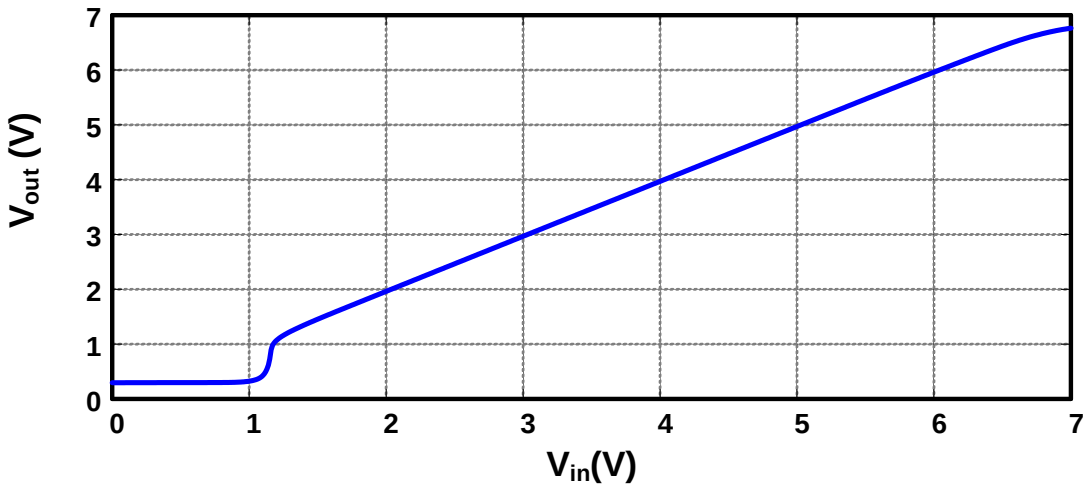

(a)



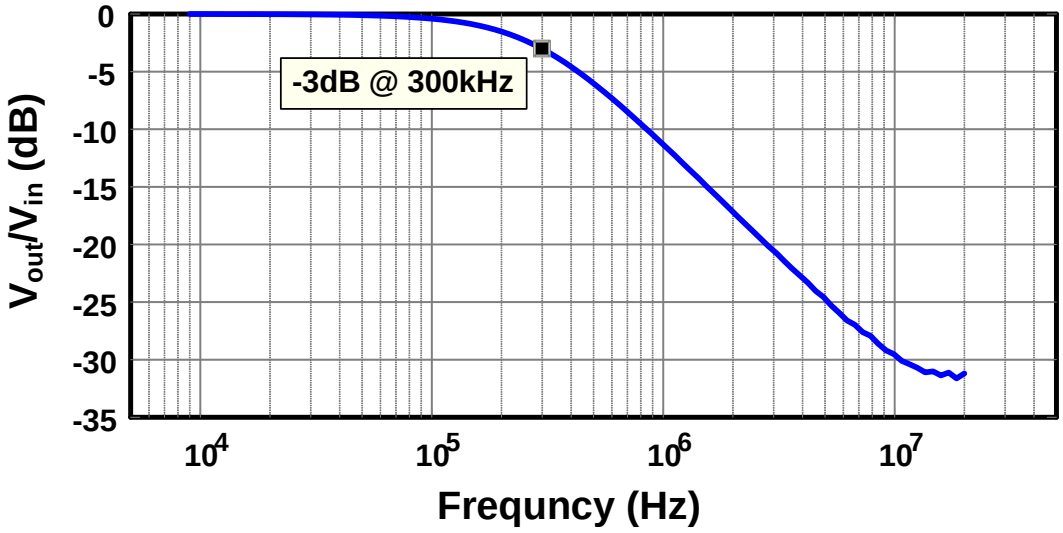
(b)

*Figure 5-7: (a) Designed PCB with assembled components, and (b) measurement setup for the light feedback control circuit.*

Opamp#2 is the main gain stage of the feedback system and is used in open loop configuration. To measure its open loop gain, its negative input ($V_{in\text{-}n}$: node $V_B$) was forced externally from a voltage source. Then, its positive input ($V_{in\text{-}p}$: node $V_{Ref}$) was swept in a range




(a)



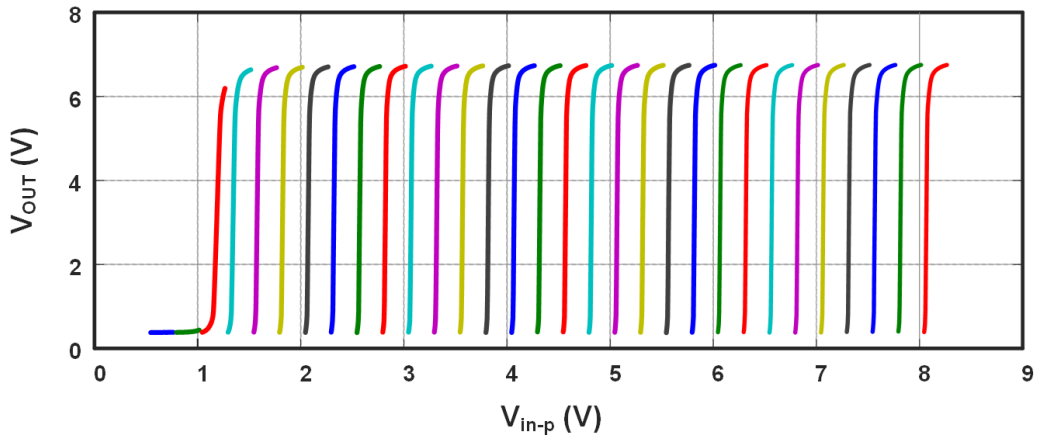

(b)

*Figure 5-8: (a) Input/output voltage characteristic, and (b) frequency response of opamp #1.*

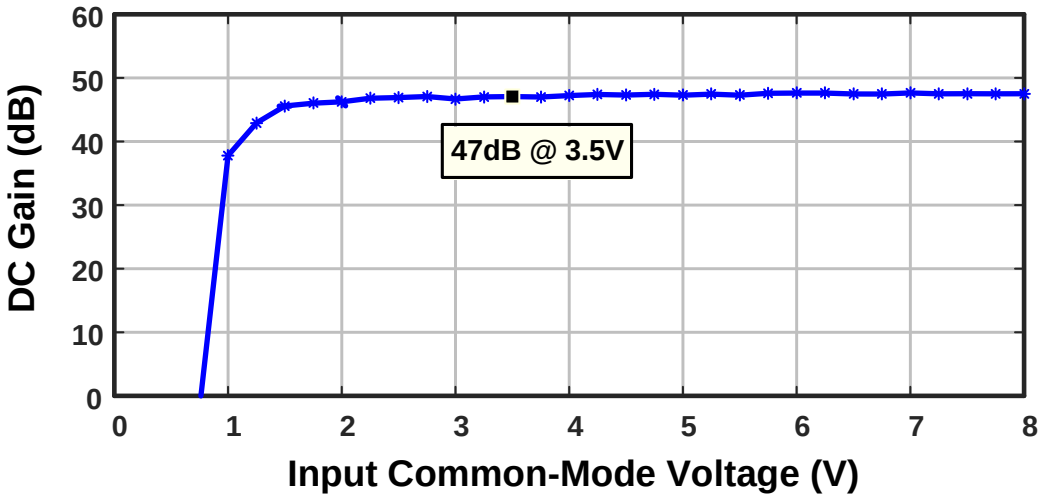
with very fine steps to measure the gain to its output ($V_O$). Figure 5-9(a) shows the results of this measurement for also sweeping $V_{in\text{-}n}$. Based on this, Figure 5-9(b) was extracted that shows open-loop gain of the opamp versus common-mode input voltage. It has demonstrated 47 dB (224×) gain for its typical operating points.

### 5.4.2 Feedback System

Secondly, the whole feedback loop was characterized. Feedback and controlling functionality of the system was investigated by a DC test. Input reference voltage ($V_{Ref}$) was swept from 1.3 V to 3 V, and output current of power transistor to the LED ($I_{LED}$) and current of photodiode were measured and are shown in Figure 5-10(a). As $V_{Ref}$ was increased from $V_{CM}$ =




(a)

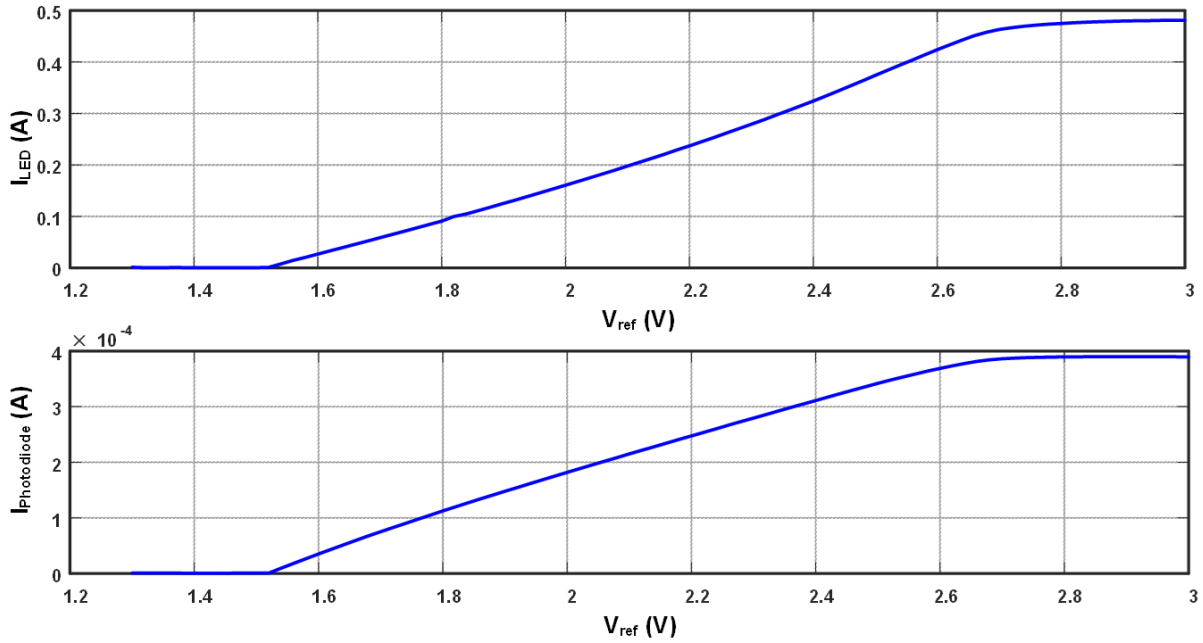



(b)

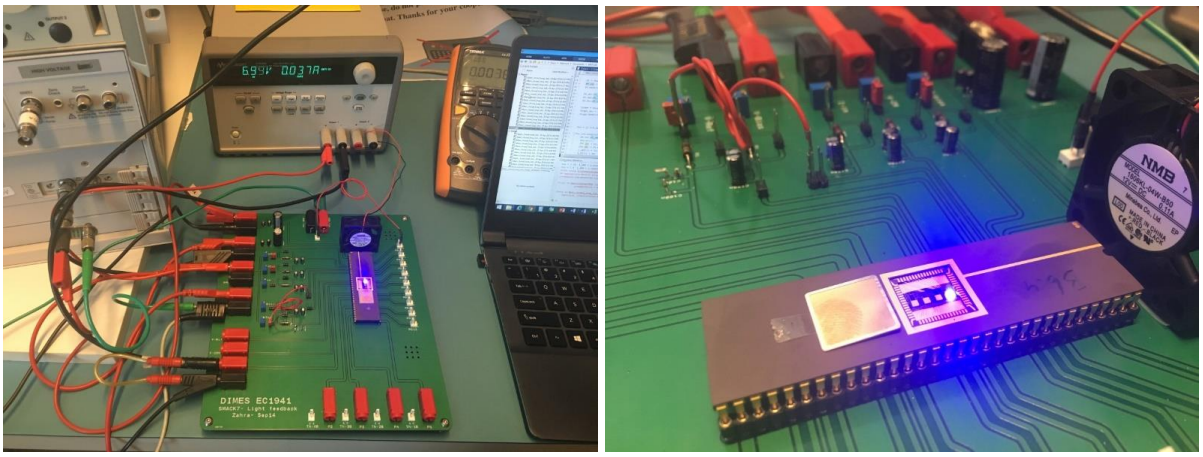
*Figure 5-9: Opamp #2 (a) $V_{out}$ versus $V_{in-p}$ for different $V_{in-n}$ and (b) DC gain versus $V_{CM}$.*

1.5 V, the feedback system operated such that light output of the LED and consequently the current of photodiode were increased linearly and proportionately. This is done through increasing output voltage of the feedback system ($V_O$) and output current of the power transistor ($I_{LED}$). In this way, light output of the LED is regulated. Each 0.1 V change in $V_{Ref}$ as the input control voltage results in 33 µA change in $I_{photodiode}$ and 36 mA in LED driving current. As the reference voltage reaches to about 2.7 V, the current of photodiode stops tracking the input. The reason is that after that point, $V_O$ has reached and saturated to $V_{DD}$ and consequently output current of the power transistor is saturated. Note that nominal current of the LED is 350 mA. Figure 5-10(b) shows the photos of the package while controlling the light output.

In the next step, dynamics of the feedback system were tested. While $V_{CM}$ was set constantly to 1.5 V, $V_{Ref}$ was instantly changed from 1.63 V to 1.83 V, corresponding to ~50 mA and ~100




(a)




(b)

*Figure 5-10: (a) Feedback system characteristic, currents of LED and photodiode versus input reference voltage, and (b) photos of the package while controlling the light output.*

mA of $I_{LED}$, respectively. As shown in Figure 5-11, $V_{out}$ tracked the change quite fast to set the light output to the new input (settling time of 1.87 µs). Based on this figure, cut-off frequency of the closed-loop feedback system is estimated to be about 680 kHz. Therefore, the control circuit is able to filter ripples on power supply source up to this frequency, far beyond the requirements of most of the lighting applications. For instance, in general illumination application photometric ripples of more than 100 to 120 Hz are not visible to human eyes [10], [11], [16], [17].

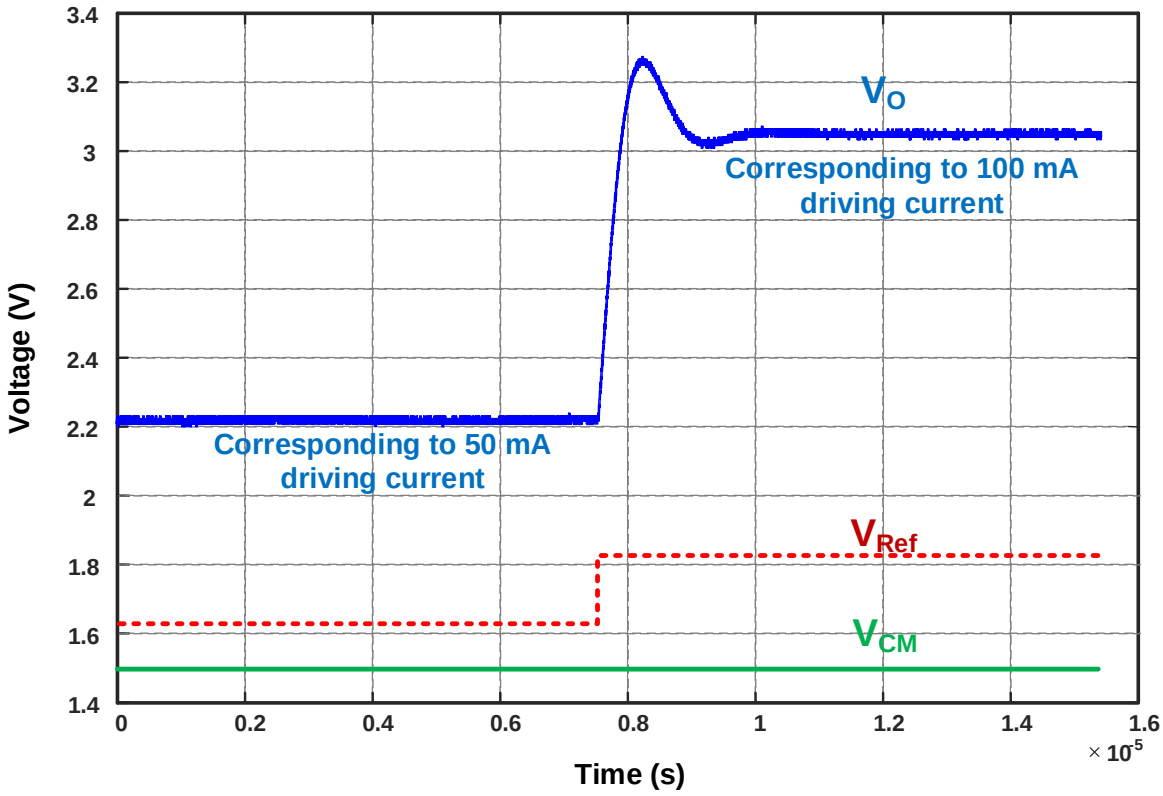



*Figure 5-11: Step response of feedback loop, $V_{Ref}$ is changed between 1.63 – 1.83 V.*



### 5.4.3 Robustness against Variations

Two different tests were performed to evaluate the accuracy and robustness of the feedback system against changes in the LED characteristics. In the first test, variations of the light intensity of the LED with current changes was considered. A common reason for this change could be LED aging, where the LED emits a lower light intensity for the same current over time [8], [9]. This can be modeled with an aging current source ($I_{aging}$) in parallel with a non-aged LED (see Figure 5-12(a)). In this test, $V_{Ref}$ was set in a way that the LED drains 100 mA net current. Then, the aging current was increased from 0 to 200 mA. Aging currents up to 150 mA decreased light intensity of the LED (calculated from measured current of the non-aged LED) by less than 1%.

In the second test, variation of the forward bias voltage to light intensity of the LED was investigated. The most common reasons for these changes could be change in junction temperature (as shown in Figure 5-5), LED aging [2], and aging of the LED interconnects [18]. This was modeled with a voltage source ($V_{aging}$) in series with the original LED (see Figure 5-12(b)). In this test, the aging voltage was swept from 0 to 1V, while $V_{DD\_LED}$ was set to 4.2 V. An aging voltage as high as 0.6 V caused less than 1% reduction in the light intensity of LED.

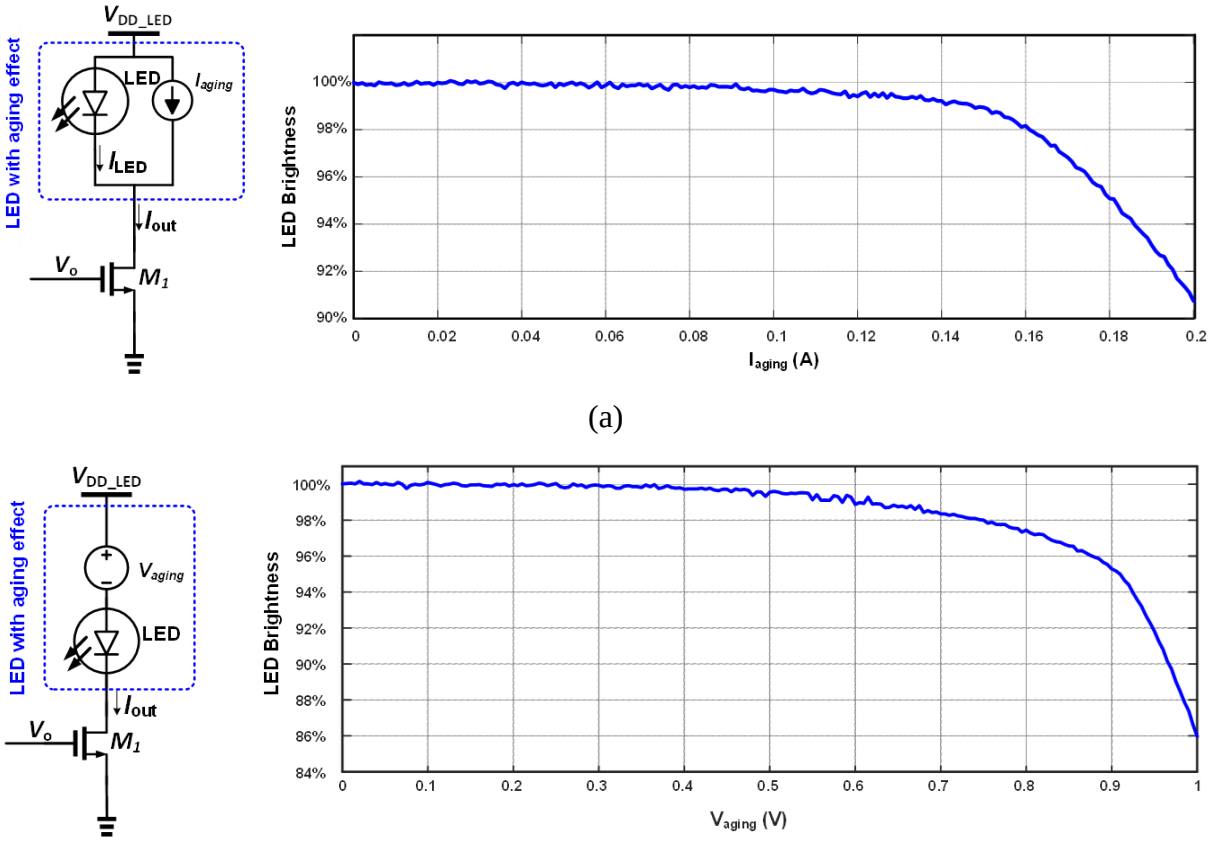



*Figure 5-12: Aging study (a) by modelling aging as a current source, and (b) by modelling aging as a voltage source.*

If $V_{aging}$ increases even more, there is no voltage headroom left for drain-source of the power transistor and it goes to triode. Hence, the feedback system cannot compensate anymore. Note that a higher $V_{DD\_LED}$ can substantially improve robustness of the system against $V_{aging}$ changes, while it degrades power efficiency of the whole package.

## 5.5 Conclusions

This chapter reports a successful monolithic integration of light output feedback control circuit in a blue/UV LED package. It is also a very appropriate solution for packaging a phosphor-based white LED module. Si-based wafer level smart control unit was integrated through our low-cost 7-mask BiCMOS process. For sensing blue/UV light in the package, optical sensors with peak responsivity at 480nm wavelength were implemented. For controlling functions, a feedback circuit with a power transistor for driving the LED current were monolithically integrated. The opamp functionality was successfully tested with having 47 dB

gain. The power transistor could provide up to 700 mA current. The whole feedback circuit could regulate light output based on a reference voltage with removing power supply ripples up to 680 kHz. Robustness of the feedback system was tested against changes in LED current/voltage to light intensity characteristics. Considering a tight error tolerance of 1%, the system was able to handle up to 150 mA and 0.6 V change in current and voltage characteristic of the LED while providing the same light intensity. Furthermore, it demonstrates the functionality of silicon based smart LED packaging with stable light output which can also be applied to other smart systems like interposer for high level electronics, MEMS, etc.

## 5.6 References

[1] S. Chhajed, Y. Xi, Y.-L. Li, T. Gessmann, and E. F. Schubert, "Influence of junction temperature on chromaticity and color-rendering properties of trichromatic white-light sources based on light-emitting diodes," *J. Appl. Phys.*, vol. 97, no. 5, p. 54506, 2005.

[2] H. Chen, A. Keppens, P. Hanselaer, Y. Lu, Y. Gao, R. Zhuang, and Z. Chen, "Failure analysis of electrical-thermal-optical characteristics of LEDs based on AlGaInP and InGaN/GaN," *Semiconductors*, vol. 46, no. 10, pp. 1333–1338, 2012.

[3] J. K. Kim and H. C. Lee, "A photo-sensor on thin polysilicon membrane embedded in wafer level package LED," in *Proceedings of the SPIE*, 2012, vol. 8431, pp. 8431–7.

[4] S. Chang and C. Tsou, "A novel silicon-based LED packaging module with an integrated temperature sensor," *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 4, no. 5, pp. 769–776, 2014.

[5] S. Y. Ron Hui, S. N. Li, X. H. Tao, W. Chen, and W. M. Ng, "A novel passive offline LED driver with long lifetime," *IEEE Trans. Power Electron.*, vol. 25, no. 10, pp. 2665–2672, 2010.

[6] K. Tseng and C. Tsou, "Novel silicon-based led packaging module with an integrated photosensing element," *IEEE Photonics Technol. Lett.*, vol. 25, no. 5, pp. 515–518, 2013.

[7] Z. Kolahdouz, A. Rostamian, M. Kolahdouz, T. Ma, H. van Zeijl, and K. Zhang, "Output blue light evaluation for phosphor based smart white LED wafer level packages," *Opt. Express*, vol. 24, no. 4, pp. 174–177, 2016.

[8] ETAP Lighting, "LED LIFETIME IN PRACTI C E - THE ETAP APPROACH." .

[9] "Calculate Reliable LED Lifetime Performance in Optocouplers." .

[10] P. Di Maso (Texas Instruments), "The Impact of Low Frequency Ripple Current on LEDs and LED drivers," 2010. .

[11] F. Zhang, J. Ni, and Y. Yu, "High power factor AC-DC LED driver with film capacitors," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4831–4840, 2013.

[12] M. A. Dalla Costa, M. F. de Melo, J. M. Alonso, W. D. Vizzotto, and L. Chies, "Analysis of low-frequency current ripple transmission in series-resonant LED drivers," *Electron. Lett.*, vol. 51, no. 9, pp. 716–717, 2015.

[13] B. Razavi, *Design of Analog CMOS Integrated Circuits*. Tata McGraw-Hill, 2002.

[14] T. C. Carusone, D. Johns, and K. Martin, *Analog Integrated Circuit Design*. Wiley, 2011.

[15] Bridgelux, *Bridgelux BXCD45 Product Data Sheet DS-C15 (10/22/2012)*, Revision C. Livermore: Bridgelux Inc., 2012.

[16] M. J. Mayer, C. B. Kim, a Svingos, and a Glucs, "Foveal flicker sensitivity in healthy aging eyes. I. Compensating for pupil variation.," *J. Opt. Soc. Am. A.*, vol. 5, no. 12, pp. 2201–9, 1988.

[17] H. De Lange Dzn, "Research into the dynamic nature of the human fovea --> Cortex systems with intermittent and modulated light. II. Phase shift in brightness and delay in color perception," *J. Opt. Soc. Am.*, vol. 48, no. 11, pp. 784–789, 1958.

[18] L. Zhang, Y. Zhu, W. Wang, X. Bi, H. Chen, K. Leung, Y. Wu, and J. Wu, "Study on ag-plated cu lead frame and its effect to LED performance under thermal aging," *IEEE Trans. Device Mater. Reliab.*, vol. 14, no. 4, pp. 1022–1030, 2014.

# Part II:

# 3D Wafer-Level Integration Approach Applied for LED SiP

# Chapter 6

# High-Aspect-Ratio Lithography for Litho-Defined Lateral Wire Bonding and 3D Integration[7]

In order to overcome some challenges and issues of conventional wire bonding such as limited interconnect density and crosstalk, a new interconnect technique is investigated in present chapter. Litho-defined wire bonding uses conventional CMOS interconnect toolset and processes in combination with the multi-level lithography aiming for "wire bond" like interconnect structures but on highly non-planar surface (high aspect ratio (HAR) interconnect). This new method for interconnection means to pattern the wire trace from the metal pads on a chip to the supporting substrate. It enables advanced heterogeneous integration of different components with less reliability issues and problems. This method consists of placing and attaching the chips on supporting substrate, passivation layer deposition, metal deposition and patterning through advanced HAR lithography. This litho approach can also be employed for 3D

[7] This chapter was partially presented in ECTC 2014 as: Z. Kolahdouz et al., "High Aspect Ratio Lithography for Litho-Defined Wire Bonding," in proceeding of IEEE Electronic Components and Technology Conference (ECTC), Florida, 2014. The extended version is submitted as : Z. Kolahdouz, H. van Zeijl, M. Kolahdouz and G. Q. Zhang, "High-Aspect-Ratio Lithography for Lateral Wire Bonding and 3D Heterogeneous Integration," to Advances in Optics and Photonics.

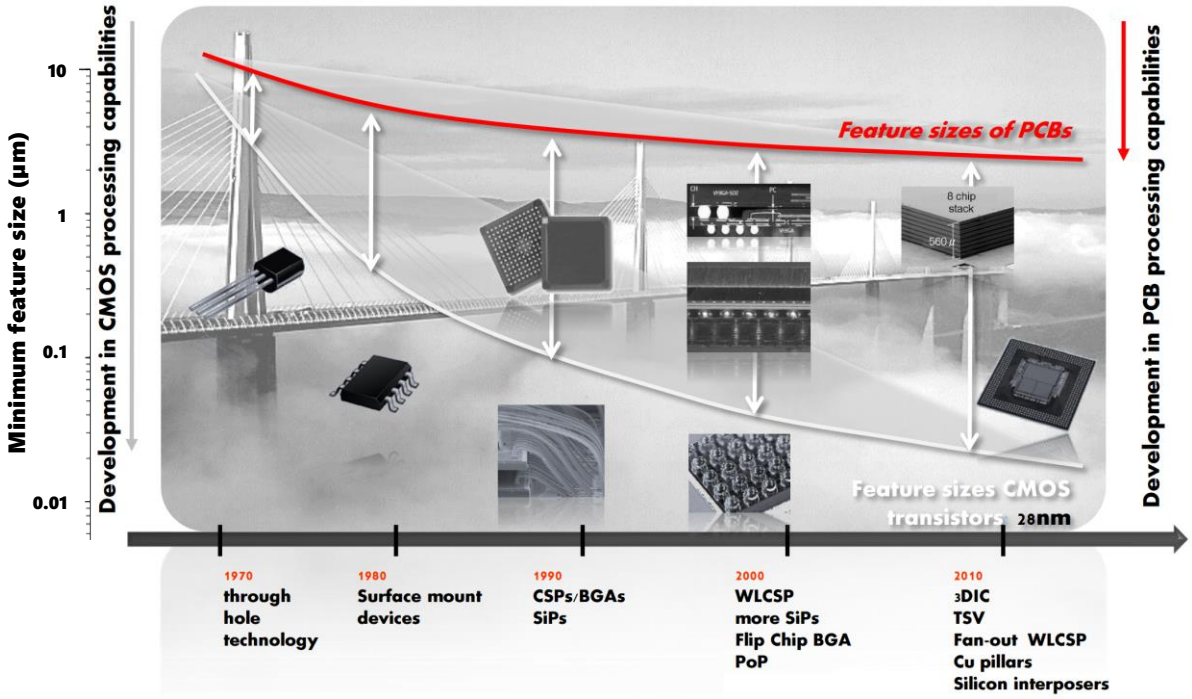



*Figure 6-1: The bridge between the IC and PCB feature sizes is getting severe that needs to be caught up by advanced packaging [1], [2].*

heterogeneous integration and making 3D devices.

## 6.1 Introduction



With proceeding of the Moore's law, the conventional interconnect method faces new challenges. All the feature sizes of ICs are shrinking rapidly which cannot be followed on the package side. In addition, as the scaling of the transistor advances, number of I/Os increases rapidly (in 28 nm technology, it is more than 10,000 I/O per $cm^2$) [1]. With conventional interconnect technology, there is a major gap between the interconnect density developed on the IC and wiring density on the printed boards (Figure 6-1).

Because of its high reliability, wire bonding is still the leading chip to package interconnection technique in spite of the rapid development in chip and wafer level packaging technology. Gold wire bonding is the first developed wire alloy. Because of material performance, it was the mainstream semiconductor packaging process for many decades [3]. Recently, copper wire bonding was introduced for its huge merit in cost reduction (about 20%) [4]–[7]. However, it has gained the gold wire bonding position for the commercial semiconductor devices for the latest technology nodes [7].

There are some important issues with conventional wire bonding for advanced devices. The bond forming process is performed at a relatively high temperature [5], [8]. That may lead to oxidation of the bonding pad. There are also other reliability issues like intermetallic compound (IMC) growth, aluminum pad squeeze, and mechanical issues like inducing stress into the Si active regions. Besides, there are various challenges in wire bonding for multi-domain packaging such as temperature limitations, deep access capability (e.g. over cavity), limited aspect ratio, and bonding on sensitive devices and cantilever leads [4], [9]–[11].

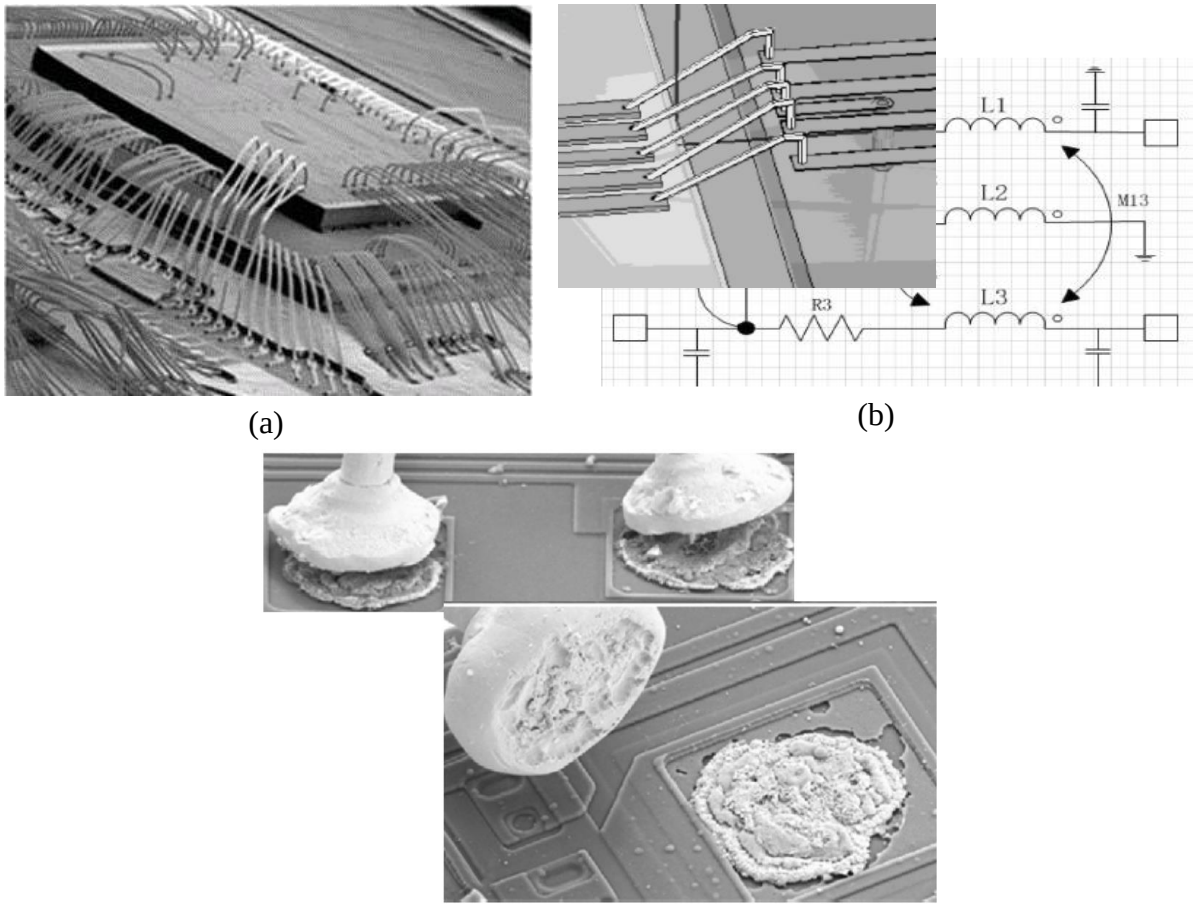
Different challenges and reliability issues with conventional interconnect technologies especially wire bonding, introduce an increasing demand for developing new I/O interconnect techniques. Two of the major drives are:

1) The fragile nature of low-k dielectrics and their relatively poor adhesion to the surrounding materials that makes it critical to minimize the mechanical stresses on the chip.
2) Wire bonding difficulties to obtain fine interconnections with high density and its limited form factor.

Figure 6-2(a-c) present some examples of wire bonding challenges.

Furthermore, RF, millimeter wave and micro-wave IC applications encounters different problems with wire bonding:

- Wire bond inductance is a really big problem for high frequency input and output signals.
- It has a high impedance at GHz ranges and creates matching problems.
- Due to the impedance of wire bonding, several decoupling capacitors are required close to the chip for supply voltages.
- There is high number of extra needed decoupling components and limited space near the chip. Wire bonding requirements does not allow to place them at the optimal close distances.
- In some high frequency application, the required space for wire bonding limits the multi-chip integration of different ICs or RF components. Since they should be located as closest as possible to minimize the interconnection impedance.
- Wide PCB traces (compared to I/O size) and clearance requirements (~100um) do not




(a) (b)

(c)

*Figure 6-2: Examples of wire bonding interconnect challenges: (a) complexity* [12], *(b) crosstalk* [13], *and (c) reliability* [14].



allow the traces to become close enough to IC pads. Therefore, it increases wire bonding length. In other words, wire bonding spacing is very little on IC, but as they come to PCB, they become very far.

At chip level, many of these issues are addressed by tailoring the IC traces based on their functions such as wider power lines and ground -signal- ground configuration for RF signals. The required layouts are made through lithography and etching. Hence, extending litho capabilities from chip to package, in an area currently covered mainly by wire bonding, seems to be a reasonable step.

One of the novel techniques recently used for some limited areas is “lithographic-defined wire bonding,” which includes the deposition of metal film and then patterning a “wire-like” trace through lithography. The proposed interconnect method may be deployed where wire bonding, flip-chip (face-down) and TSV interconnections are difficult to carry out. This

technique offers new benefits such as better interconnection reliability, less stress introduced into the Si active region, higher interconnect density, and applicable for 3D heterogeneous integration applications. Furthermore, using advanced packaging and interconnection technology, such as lithography-defined wire bonding, can help for better redistribution of the wiring traces at the interface of the IC and the package.

Many of previously discussed issues with conventional wire bonding can be resolved in this method. Using standard IC fabrication steps does not impose extra temperature and mechanic stress to the devices. Moreover, the wiring density is determined with lithography resolution instead of wire bonding machinery.

Recently some other groups proposed this approach [15]–[20] (see Figure 6-3). In most cases, it was carried out on a tapered Si sidewall [16], [17]. In another study by M. Murugesan et al, they fabricated a high-step-coverage Cu-lateral interconnection vertically over 100 µm thick LSI die via Cu electroplating [18]. These works just cover wiring over maximum 100 µm and interconnect density was not that much improved. One of the main challenges in these reports is lithographic imaging over high topographies, for which mask aligner were employed.

Although mask aligners are more cost effective compared with wafer steppers, nowadays, wafer steppers are being used for advanced wafer level packaging [21]. They can offer higher resolution, less mask damage and superior yield. Their rather high resolution is good motivation to use the wafer steppers in packaging. Currently, the wafer steppers are normally used for planar substrates. But their high resolution (R) is linked with limited depth of focus (DOF). Consequently, this method cannot be applied for 3D topography substrates and non-planar redistribution layer (RDL) in a fan-out packaging with high interconnect density. The multi-step imaging (MSI) on a wafer stepper is perhaps a future option, which can provide high resolution and enable increased DOF for high topography substrates. MSI functionality, developed by ASML for MEMS industry, allows increasing the global focus offset range up to ±200 µm from the standard specification of ± 30 µm [22].

Double patterning was previously proposed to overcome physical limitations in optical lithography. Previously, it was employed to improve the resolution. We would like to suggest multi-step imaging method to overcome the focus limitations for high aspect ratio (HAR) lithography.

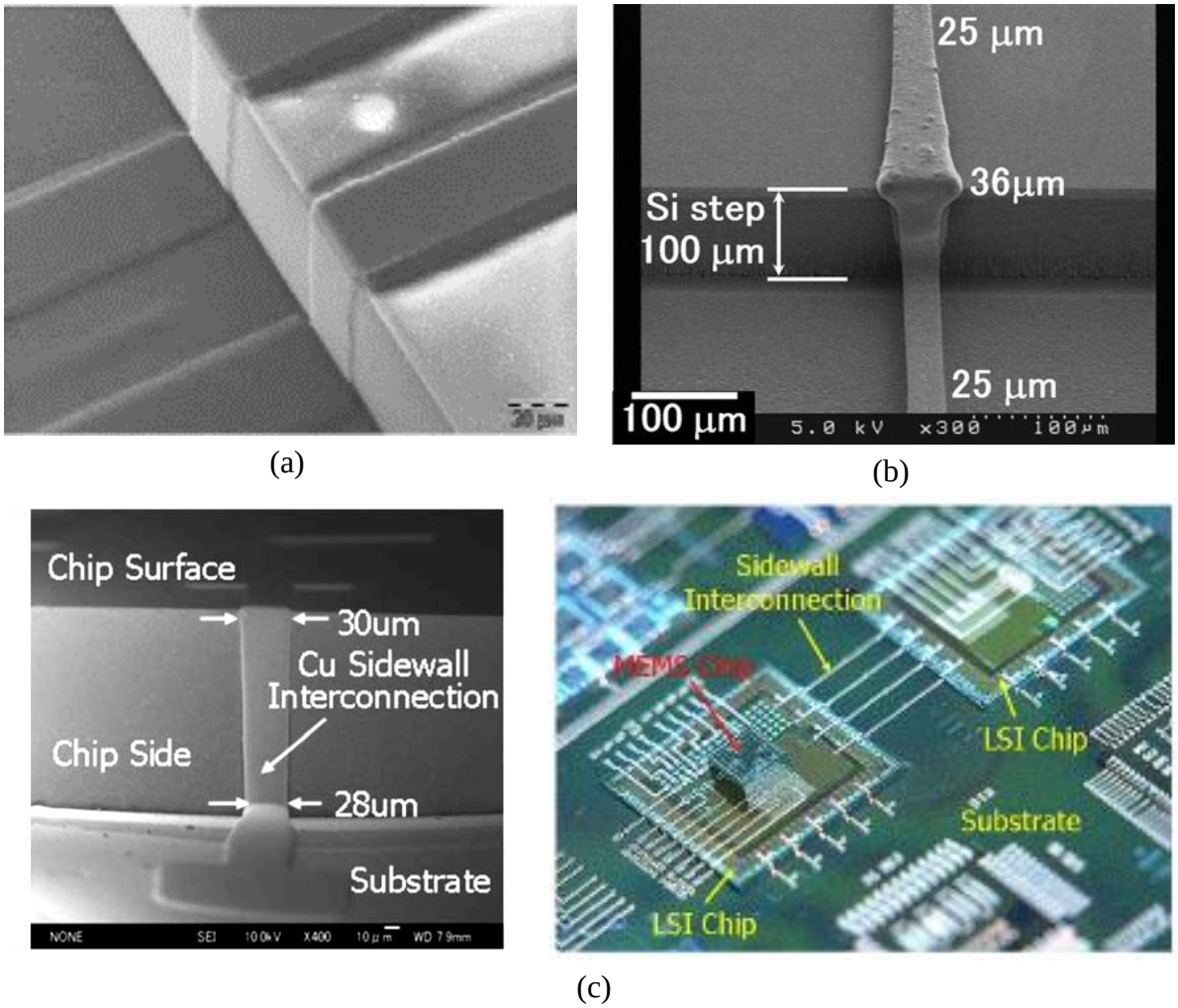



*Figure 6-3: (a) Using SU8, 20 µm wide lines, 20 µm apart, 60 µm DRIE etched channel* [19], *(b) Cu high-step-coverage lateral interconnections over a 100 µm thick chip* [18], *and (c) Cu sidewall interconnection crossing-over the chip with step height of 100 µm* [20].

In this work, we fabricated HAR interconnect structures over cavities with different depths from 25 to 200 µm. The main goal is to overcome lithography challenges on highly non-planar surfaces. Different lithography methods were examined. To understand the properties of MSI lithography process on a KOH etched cavity sidewall, aerial image calculation and resist pattern simulation were also done using a newly developed model for this work. From these simulation, an imaging strategy was derived in which the pattern on the sidewall was split in different partial patterns each with its own focus level. Next, MSI with split masking was applied to pattern the full 3D HAR interconnects over the whole sidewall of the cavities. Using MSI on ASML projection tool, we achieved high resolution of 2 µm from top to bottom of 200 µm cavities.

This chapter is organized as follows: Section 6.2 elaborates on litho-defined lateral

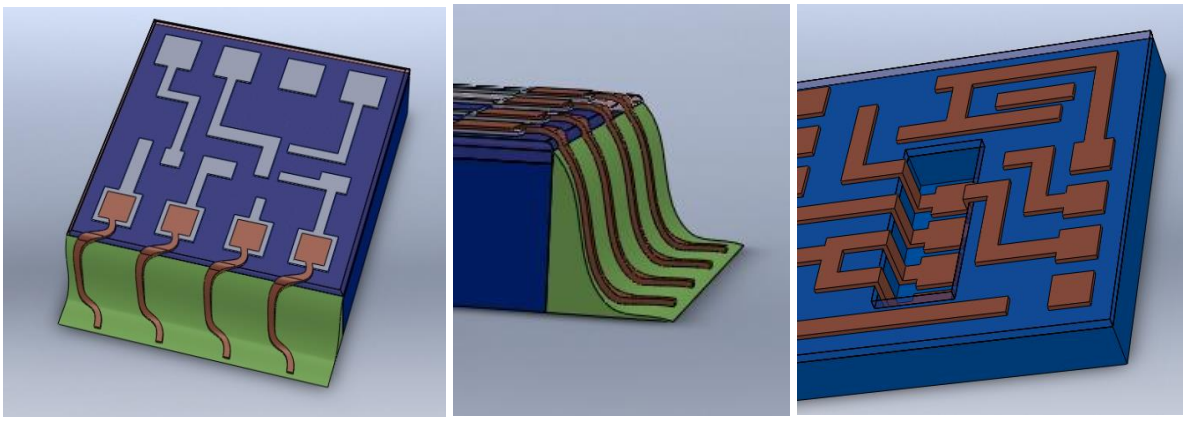


*Figure 6-4: Schematic of Litho-defined lateral wire bonding. The right image shows advanced version aiming to form wires and TSV like structures on straight sidewalls.*

interconnect for system-in-package (SiP). Section 6.3 explains lithography methodologies in three phases: resist coating, exposure, and resist development over highly non-planar topographies. Section 6.4 describes resist coating and developing process. Exposure is divided in two categories: contact/proximity approach which comes in Section 6.5 and projection method in Section 6.6. Also, MSI for smart LED package is described including simulation and experiment results. Finally, conclusion comes in Section 6.7.

## 6.2 Outlook to Litho-Defined Lateral Interconnect for SiP

Lithographic Defined Wire Bonding (LDWB), generally consists of three different steps:

1) Passivation layer deposition which is both for tapering the sidewall and passivation
2) Metal film deposition
3) Patterning through HAR lithography

Figure 6-4 schematically shows the concept. The green layer can be a supportive tapering material to form the softer corners for LDWB and isolate the chip sidewall when needed.

LDWB can offer various benefits and potentials compared to conventional methods such as:

- Improved packaging reliability: it is a low temperature process and less material interfaces are involved. Also, the process stress is reduced due to optimized interconnect lines at critical transitions.
- Improved line density: litho defined pitch rather than tooling defined pitch.
- Enhanced precision.

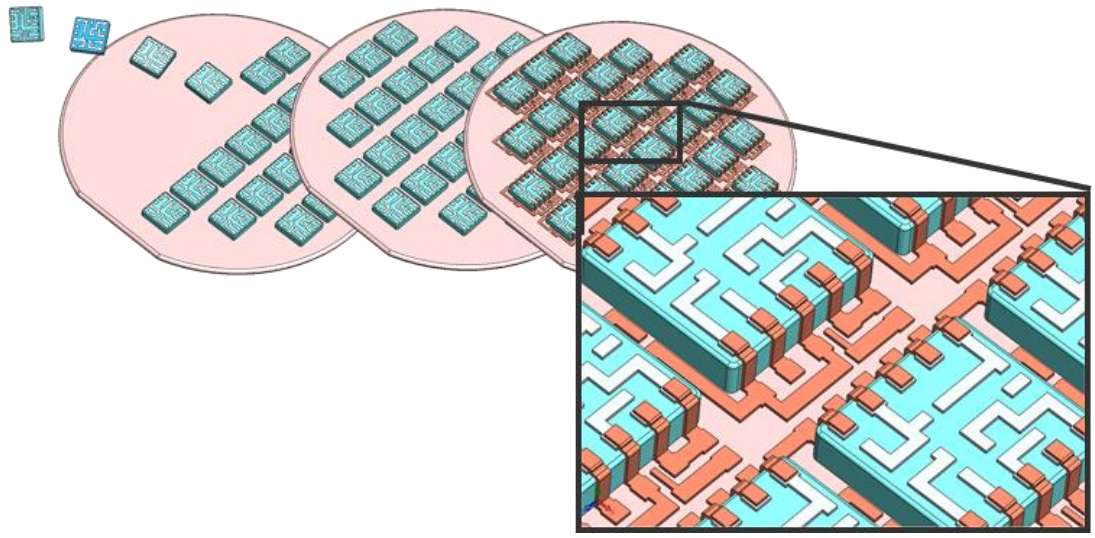


*Figure 6-5: Lithographically defined interconnect can be applied for SiP and hybrid wafer level integration.*

– Suggesting to reduce bond pad area.

– Heterogeneous integration: it can be used for conventional chips without special requirements (such as restrict design requirements for flip-chip and TSV). This is especially useful when spatial limitation or mechanical consideration exist.

– Low-K compatibility used in modern IC technology nodes.

– Compatibility with ultra-thick metal option interconnect on advanced IC.

– Alternative for TSV on smaller ICs.

– RF optimized structures (ground-signal-ground).

– Reduction of parasitic inductance: the unescapable wire bonding loop height is replaced by the thickness of wire traces in LDWB [18].

– Shorter interconnect lengths: interconnection with minimized resistive-capacitive delay for high frequency applications.

Figure 6-5 shows schematically how litho-defined lateral interconnect can be employed for system-in-package (SiP) and hybrid wafer level integration.

Different materials can be used for tapering and passivation such as various polymers, under-fills and thick photoresists. In conventional underfill processing, a controlled amount of liquid underfill is dispensed along the edges of the component/substrate joint. Figure 6-6 presents an example of underfill dispensing. Diverse metals can be used as interconnection layer using

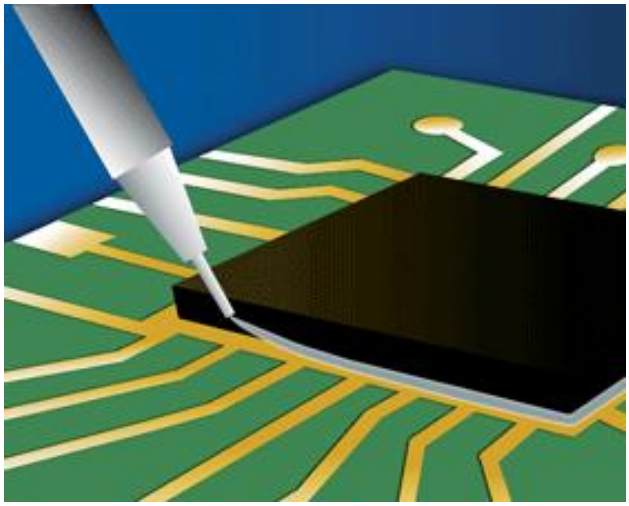


*Figure 6-6: Example of underfill dispensing and curing* [23].

evaporation, sputtering, electroplating, etc.

## 6.3 Methodology

Photolithography is the process of printing the patterns in a thin film of photosensitive layer. It is the common method for patterning the microsystem substrates in high volume manufacturing of IC and MEMS devices. Generally, its pattern capabilities is in 2 directions and there are significant limitations for 3D patterning. Before going to 3D lithography process, we discuss some details about 2D process and realize why they cannot be employed for high topography. The conventional 2D lithography is composed of three footsteps:

1) Coating: applying a thin photosensitive film (photoresist) on the *surface*.
2) Alignment and exposure: alignment of the markers on the surface and exposing the *surface* (a new pattern is firstly aligned to the previous process layer and then exposed in the resist).
3) Developing: dissolve exposed photoresist from the *surface* (in case of negative tone resist unexposed parts are dissolved).

The substrates are usually spin coated with a layer of photoresist. For spin coating, a small amount of the liquid resist is dispensed on a thin and flat substrate. Next, the substrate is rotated with high speed to spread and dry the resist, this results in a thin uniform film. After resist film formation, a baking step is performed to remove residual solvents. The final dry, thin and uniform resist can be exposed and patterned in next step. Figure 6-7 shows the schematic of spin-

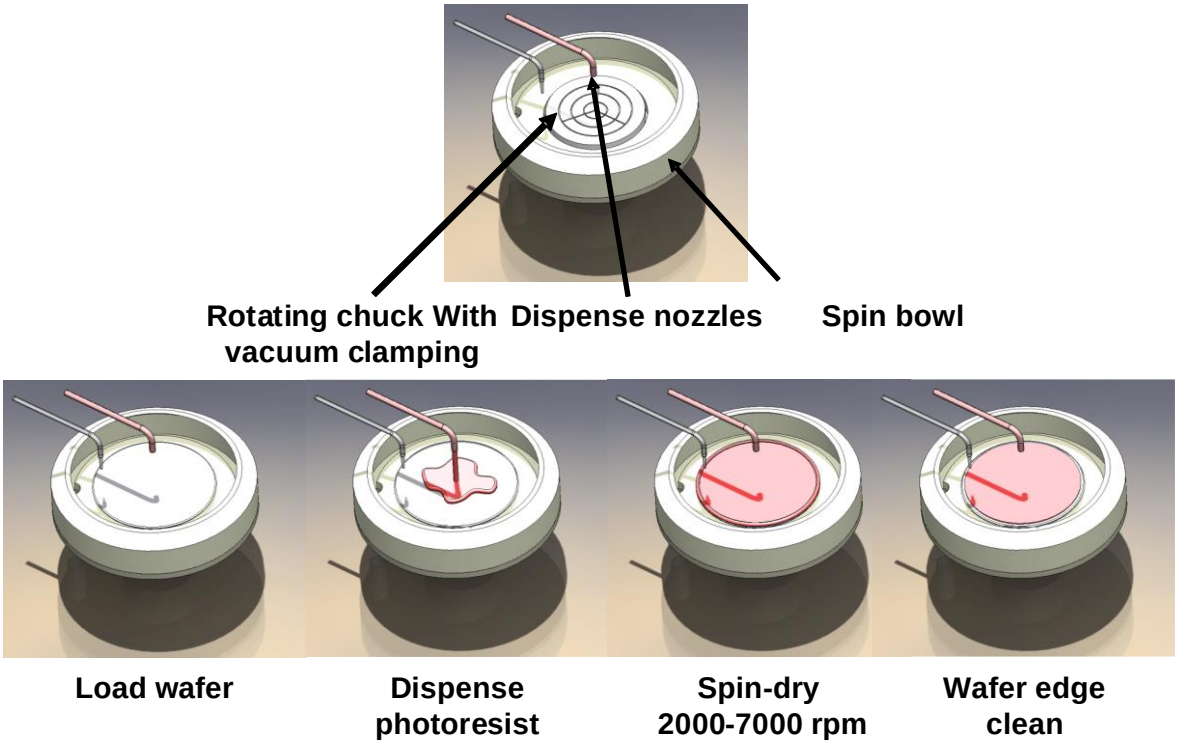



*Figure 6-7: Spin coating setup and steps on a planar wafer.*

coating steps.

Unfortunately, this method is not applicable on a substrate with high topographies as it cannot form a uniform thickness resist layer. The resist tends to mount up in corners, and be thinner or even excluded over the edges. So it can limit the pattern quality and integrity on large nonplanar substrates [24].

For alignment and exposure, the mainstream IC production tools require planar substrates. However, MEMS solutions for high topography are available. The two conventional alignment/exposure tools are contact/proximity mask aligner and projection aligner. Both have difficulties to obtain high resolution structures over non-planar topographies. To see the limitations of both methods, we can discuss the related diffraction expressions.

Proximity lithography is described by near-field (Fresnel-Kirchhoff) diffraction. For mask feature sizes considerably larger than the wavelength of the illuminating light and for sufficiently large proximity gaps, approximate methods (such as scalar diffraction theory) can be applied. The realizable resolution for lines and spaces, half-pitch, in proximity lithography is derived from the Fresnel integral formula and given by the following equation:

$$R = Line\ width\ (\ half - pitch) = \frac{3}{2}\sqrt{\lambda(g + \frac{d}{2})} \approx \sqrt{\lambda g}, \tag{6.1}$$

where λ is the wavelength, $g$ the proximity gap, and $d$ the resist thickness. The resolution degrades with the square root of the proximity gap [25]. So as the gap increases while exposing a high topography surface, the resolution gets worse. As a result, using conventional mask aligners for high resolution HAR patterning is not feasible.

Projection lithography is described by far field (Fraunhofer) diffraction equations. The achievable resolution and DOF can be formulated as

$$R = K_1.\frac{\lambda}{NA}, \tag{6.2}$$

$$DOF = \pm K_2.\frac{\lambda}{(NA)^2}, \tag{6.3}$$

where $K_1$ is an experimental parameter (which depends on the lithography system and resist properties), NA (numerical aperture) stands for opening angle of the lens, and $K_2$ is usually determined experimentally. So lenses with higher NA improve the resolution but also decrease the DOF [26]. While advanced projection aligners provide higher resolution because of the projection lenses, the limited DOF restricts using them for HAR structures.

For mask aligner, alignment can be done on either wafer front or backside. For projection lithography, alignment axis and exposure axis are not parallel and there is limited DOF for the alignment system. For standard planar process, front side alignment is done with a good precision. The ASML PAS5500 wafer stepper alignment system is laser based alignment on a phase grating alignment target. Figure 6-8 shows the schematic of the alignment setup for front side alignment. Alignment system is fully functional over a large optical path difference between 2 layers for overlay error of less than 200-300 nm (3σ) in each XY direction. For non-planar surfaces, we confront some challenges such as alignment offset calibration, overlay measurements, and tool stability.

In order to lithographically pattern a HAR wire structure over a step height of hundreds of microns, a complete process should be developed in different phases:

1) Resist coating: having a good resist coverage over high topography surfaces, especially on convex corners.
2) Exposure: solving defocusing problem and different leveling requirements.

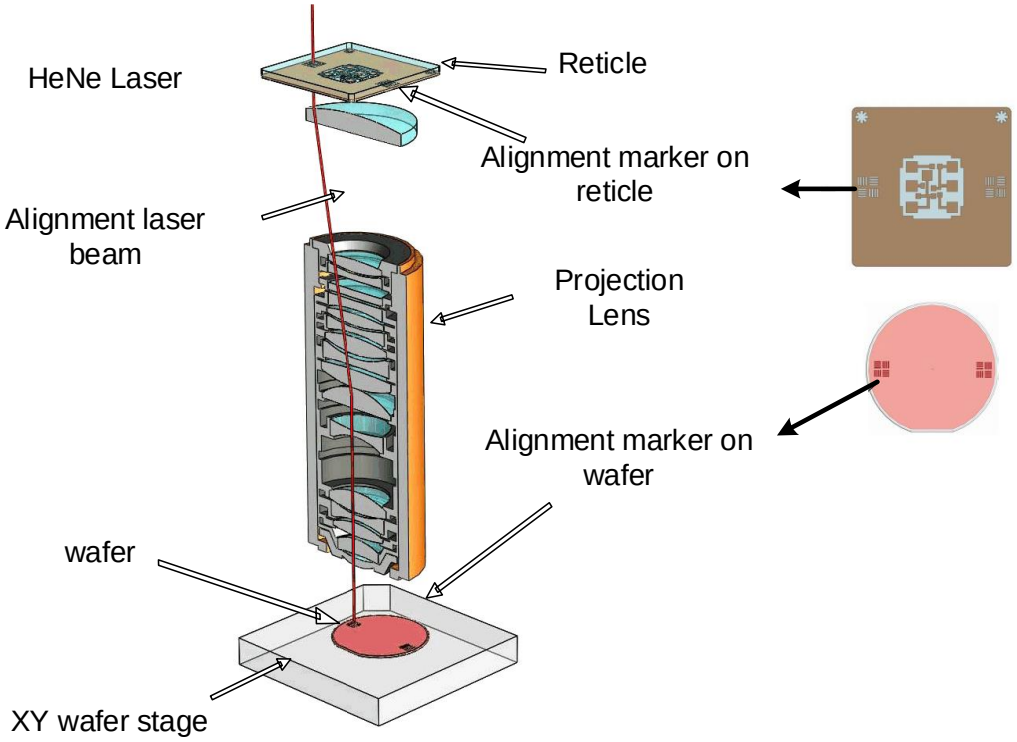



*Figure 6-8: Schematic of alignment setup and steps on a planar wafer in ASML PAS5500 wafer stepper.*

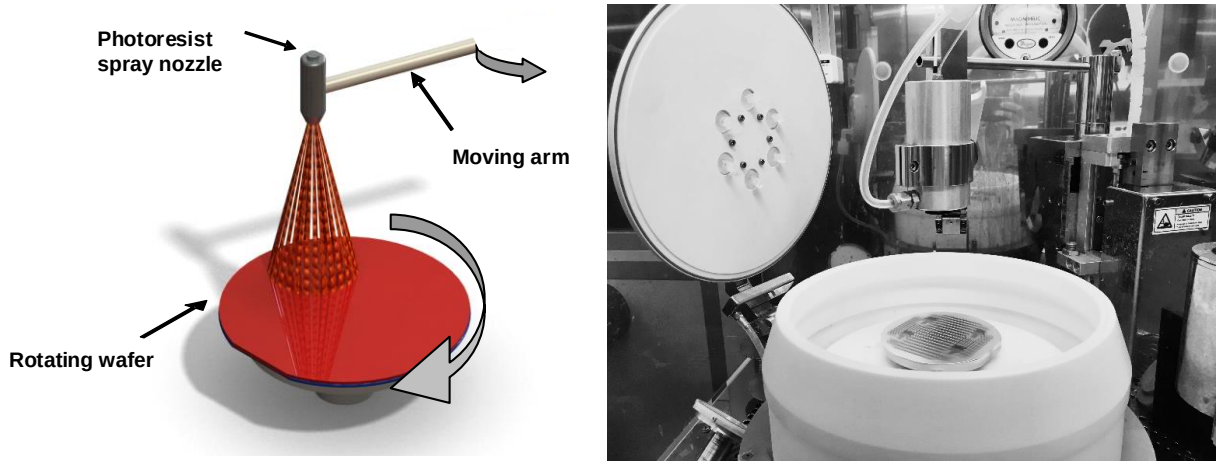
3) Resist development: different resist thickness over a topography needs different time to react in development solution.

The full description of each of these phases are coming in the following sections. In this work, we are going to develop the litho phase. The KOH etched cavities are used as the test structures for developing the full process. An anisotropic KOH wet etch on a silicon wafer forms a cavity with a trapezoidal cross-section. The bottom of the cavity is a (1 0 0) plane, and the sides are (1 1 1) planes. These cavities with certain angle (54.7° at bottom corner, determined by Si lattice structure) can be etched in the Si wafer with different sizes and depths that are appropriate for HAR litho test platform. To show the feasibility to form an interconnect over the KOH etched topography, an aluminum film was deposited on the wafer, with sputtering on Trikon Sigma 204 machine, and patterned through HAR lithography and etching.

## 6.4 Resist Coating and Developing over High Topography

### 6.4.1 Resist Coating

To obtain a good photoresist coverage over high topography, spray coating was used to apply




(a) (b)

*Figure 6-9: (a) Schematic of spray coating setup, and (b) a photo of EVG 101 spray coater while spraying resist on a high topography wafer.*

the resist. Figure 6-9(a) shows spray coating schematically. The spray coating experiments are performed on an EVG®101 spray coater (from EV group, Austria) on 4 inch wafers (shown in Figure 6-9(b)). A diluted positive/negative tone resist solution was used in this work.

To get a proper droplet size of resist for uniform distribution, it is necessary to have a suitable resist viscosity. An ultrasonic atomizer is used to produce an aerosol of small resist droplets. Pressure tunable air current, which carries the aerosol, ejects the droplets onto the sample surface through photoresist spray nozzle. Meanwhile, the wafer holder chuck is slowly rotating while the spray moving arm scans across from one side to the other side of the wafer with changing speed. Spraying direction is perpendicular to the wafer surface with tunable distance between spray nozzle and the chuck. Since the wafer is spinning with a constant rate, the speed of moving arm should be adjusted according to its distance to the center of wafer (the closer to the center, the higher scan speed of the arm) [16], [27]. In this way, the same amount of resist is sprayed over the whole wafer.

Spin rate, ultrasonic energy, spray nozzle scanning speed and profile, spray pressure, and resist dispense volume are relevant parameters adjusted to optimize deposition of a thick resist layer on topographic wafers. The coating is done in multiple steps of multi-layer spraying over the whole wafer to make sure of having conformal coverage all over the topographies. To increase the resist coherency, some baking steps can be added during thick coating processes [28].

However, spray coating process should be optimized for different aspect ratios of cavities and topographies. For wider and shallower cavities, the resist thickness has better uniformity and the layer is thicker [29]. Considering the reflection of light in exposure step on cavity sidewall for target mask pattern, both negative and positive resists might be used. For negative and positive tone resists, diluted AZ® nLOF 2070 and AZ® 9260 were used, respectively.

### 6.4.2 Resist Development

The resist was developed using manual process. For negative resist, after exposure a cross-link baking was done at 115°C for 3 min. Then, it was developed in pure MF322 solution for 2 min.

For positive resist, it was developed in diluted AZ400K (diluted with 2 parts of DI water) for 1-2 min.

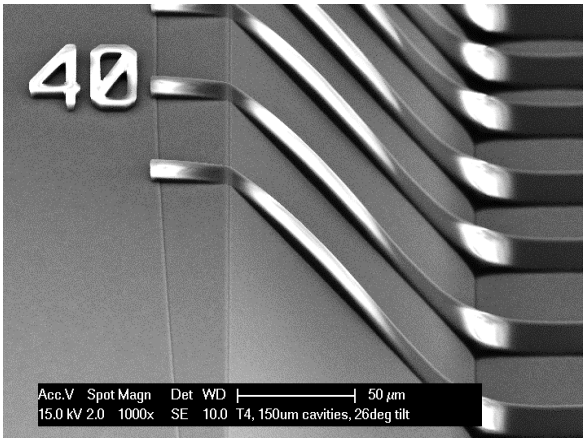
## 6.5 Exposure over High Topography: Contact/Proximity Approach

First set of experiments were designed and run with contact aligner, EVG®420. It should be considered that, in high topography, Fresnel diffraction of UV light causes loss of resolution. For deeper cavities, gap between mask and surface increases and so the effect is more severe [30]. In contact aligner, the alignment was performed on the wafer surface. The mask was designed to cover different wiring parameters such as wire width and density. This was later applied on a 1.4 μm aluminum sputtered layer in Si cavities with different depths from 25 to 150 μm.

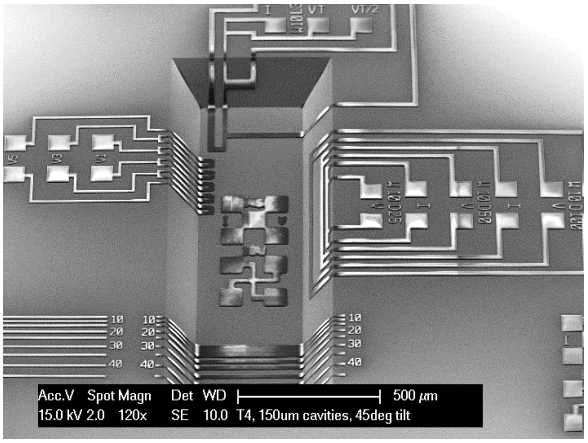
For having less reflection from sidewalls of the cavities, diluted negative AZ® nLOF 2070 resist was coated in 2 steps of 4-layer spraying. Each step followed by baking at 100°C hotplate for 1 and 5 min, respectively. Although there was a considerable thickness difference between top and bottom corners of cavities (few micrometers), the good coverage over top corner resolves the problem of pattern splitting (Figure 6-10(a)).

For wire pitches less than 20 μm, the lines are merged together. For pitches bigger than 20 μm, lines with minimum width of 10 μm were successfully developed and etched. Some of the results are shown in Figure 6-10(b-e).

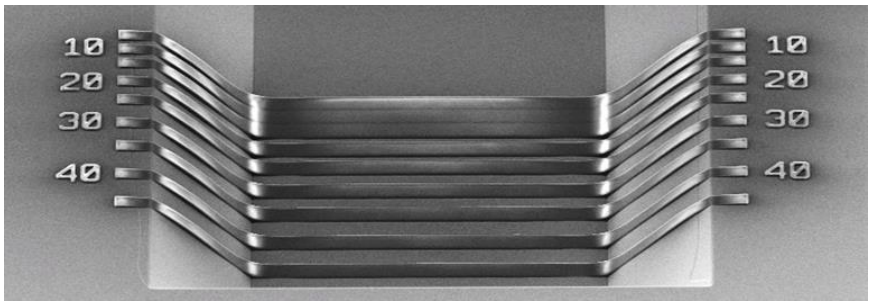
Because of low resist thickness in the upper corner of cavities, in aluminum etching step, dry etching does not work selective enough and may cause in line split. In contrast, wet etching



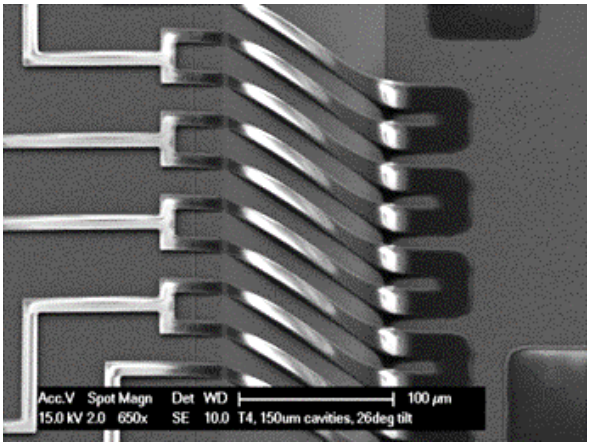

(a)



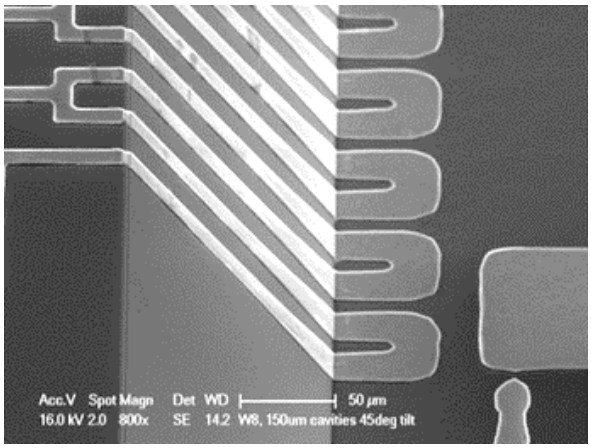

(b)




(c)




(d)

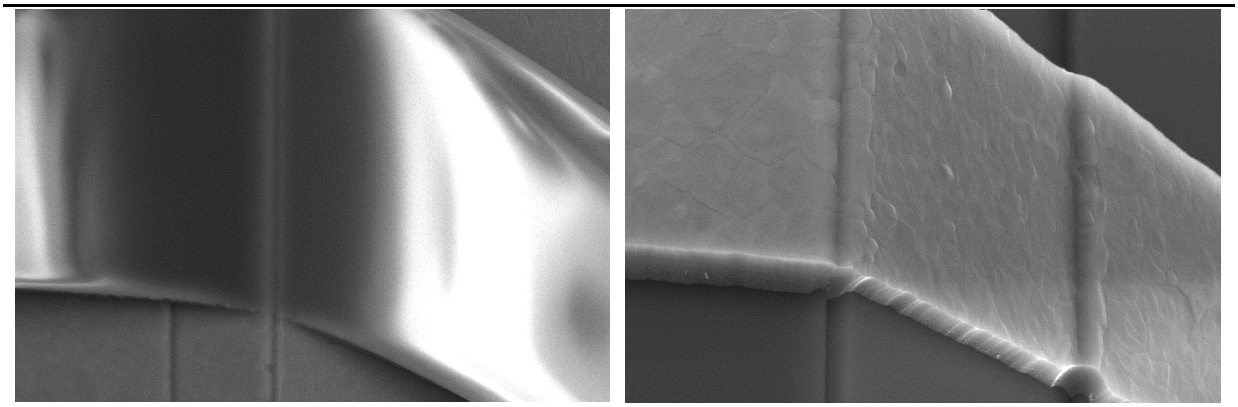



(e)

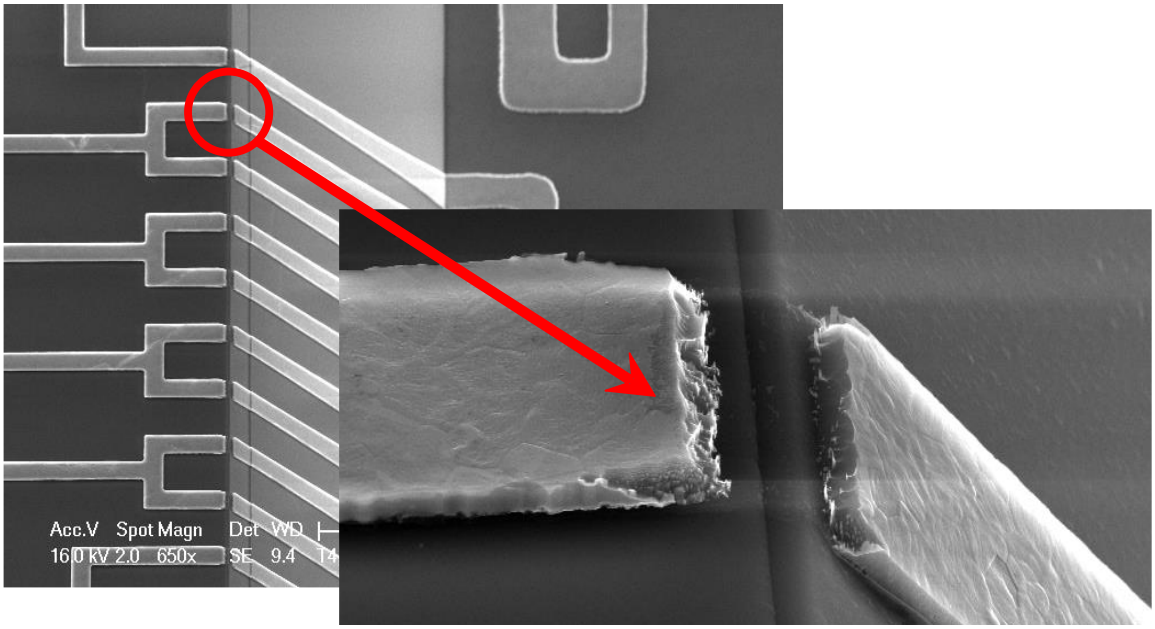
*Figure 6-10: The SEM images showing (a) resist coverage over 150 µm cavity coated with spray coating, (b) different structures of 10 µm lines over 150 µm cavity, (c) lines with various gaps from 10 to 40 µm (it can be observed that the lines with 20 µm pitch are merged), (d) 10 µm width /30 µm pitch wire traces on resist film, and (e) the same feature after etching in aluminum layer.*

process is selective enough. Figure 6-11 shows the different result of two processes.

Moreover, there are other techniques in literature for high aspect ratio patterning with mask aligners, such as using SUSS LEGO and Talbot lithography. For the SUSS method, the dedicated



(a) (b)




(c)

*Figure 6-11: The SEM images of a line structure over upper corner of the cavity: (a) resist pattern, (b) Al line after wet etching, and (c) Al line after dry etching.*

SUSS MO exposure optics are employed in combination with diffractive mask patterns [31], [32]. In Talbot lithography, the self-imaging of periodic objects is used. In this method a periodic structure (grating) is illuminated with monochromatic collimated light to form self-images of the grating pattern at periodic intervals after the grating [33]–[35]. However, both methods are limited to periodical patterns and not applicable for generic patterns such as various interconnection structures.

## 6.6 Exposure over High Topography: Projection Approach

In comparison to contact aligner, MSI is more flexible for imaging over high topographies.

In this method, imaging is done in several steps at different focus levels. The exposure dose with MSI can be controlled at different focus levels. It has the potential to adapt the dose in the aerial image at different focus levels to match well with local resist thickness. Therefore, it can compensate for thickness variations of spray coated resist. The constant dose of exposure in contact aligner causes problems in developing patterns for different resist thicknesses. For example, considering thick resist at the bottom corner of the cavity, the exposure dose and developing time should be increased. This may cause over-exposure and loosing features for thinner part of resist layer at the edges.

For MSI, exposure is done using a pre-defined single leveling point. In this case, leveling takes place in 2 steps (illustrated in Figure 6-12(a)):

- Global leveling: determine height reference points.
- Field by field leveling: red level sensor measurement at a given location. Exposure takes the closest measurement point as a reference (max. 200 points). It gives the flexibility to define the locations for leveling that are used to determine the nominal focus plane.

The MSI option, developed by ASML for MEMS application, allows increasing the global focus offset ranged up to ±200 µm from the standard specification of ±30 µm. Additionally, a local focus offset of ±5 µm can be added for each die to the global focus offset to adapt to the process induced thickness non-uniformity of the high topographic wafers [22]. The typical depth of focus for PAS5500/80 machine, which was used in this study, is 2 µm.



As shown in Figure 6-12(b), there are different scenarios suggested by ASML for multi-step imaging:

1) Imaging on the surface of a (deep) trench: 2 steps imaging.
2) Imaging on the multiple surfaces of trenches: 3 steps imaging.
3) Imaging on the surfaces of a die attached on a wafer: 2 steps imaging.
4) Imaging the connections between the die and the wafer.

However, in our case, we should consider imaging over the whole topography up to 200 µm. It is the combination of different scenarios and might include several imaging steps.

To make features just at the bottom of cavities, the average depth of the cavities is considered as the global focus offset. The focal plane is thus at the same level as the bottom of the cavities. To keep the same resolution, all over the wafer, several issues need to be taken into account:

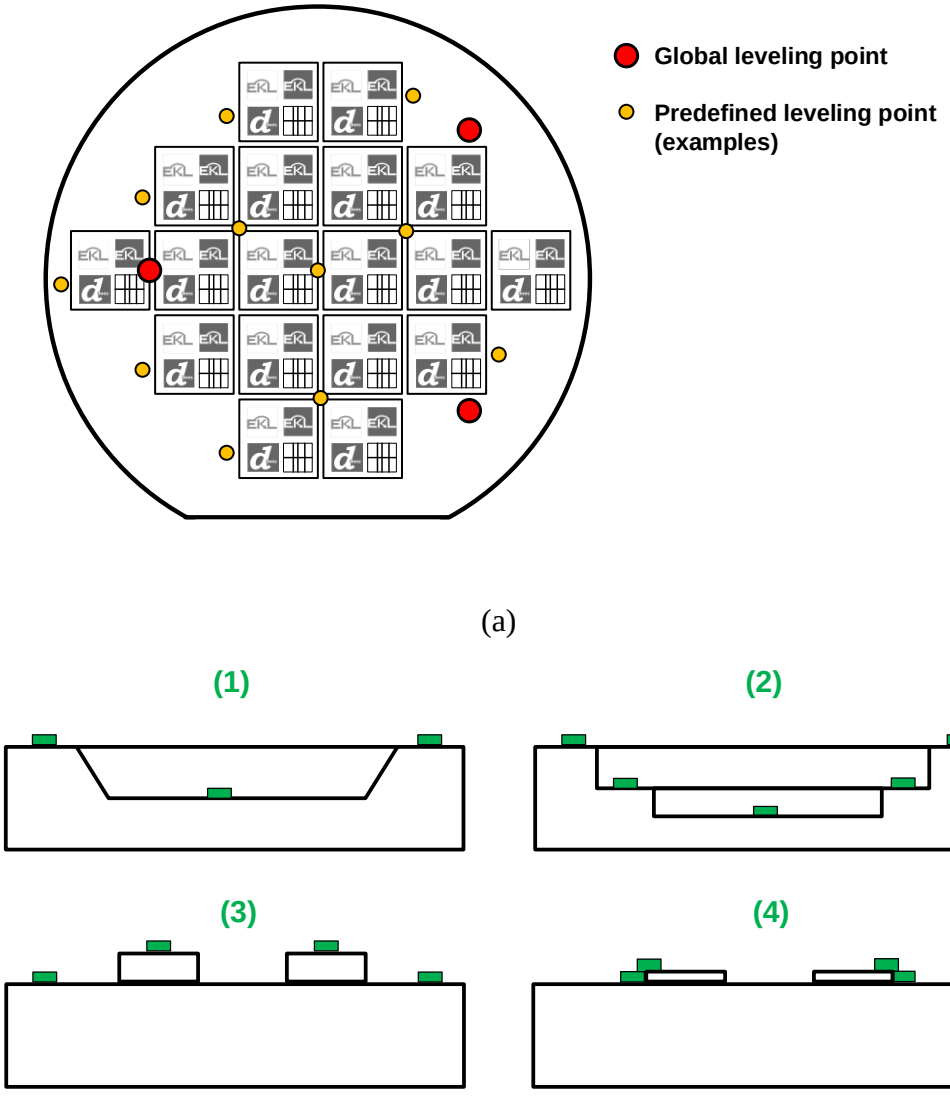



*Figure 6-12: (a) Definition of leveling points in MSI, and (b) different strategies for multi-step imaging.*

1) Non-uniformity and roughness of surfaces (in this study, the KOH etched cavities) due to chemical nature of the process,
2) Spray-coated resist is not uniform all over the wafer and also on different positions of the steps and topographies.

These types of issues can be addressed in the local focus offset.

For second sets of experiment, the same resist coating process was used. Using multi-step imaging on an ASM PAS5500/80 projection aligner (NA = 0.48), we achieved a resolution down to 2 µm on the bottom of a 150 µm deep cavity (see Figure 6-13). However, for sidewall imaging processing of wires, further developments are needed which come in the following.

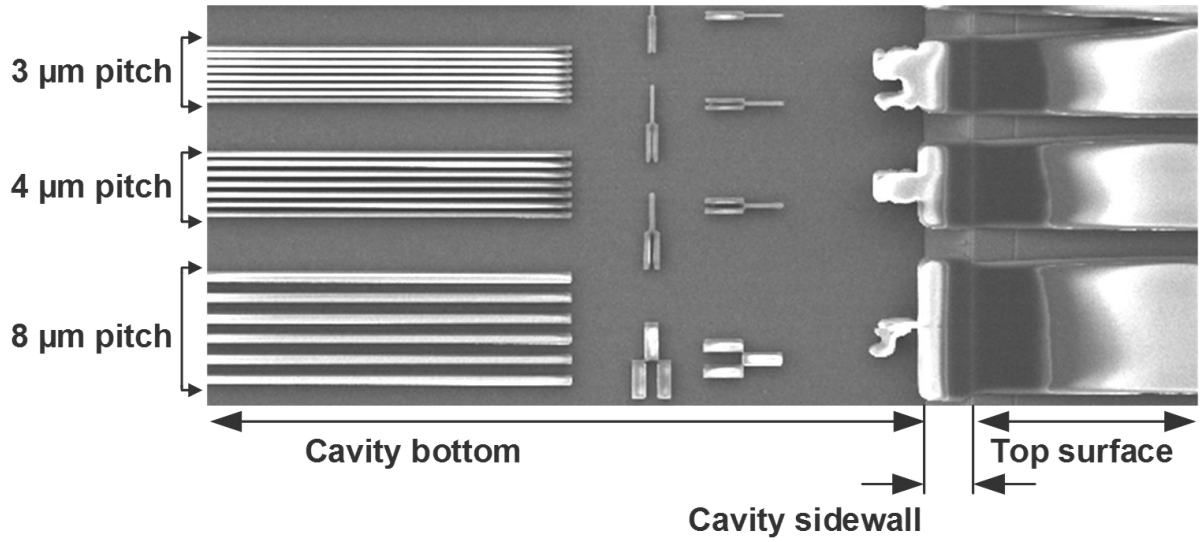



*Figure 6-13: The top view SEM image of different line structures at bottom of 150 µm cavity using multi-step imaging with a wafer stepper. 2 µm resolution was realized.*

### 6.6.1 MSI with Single Mask

#### 6.6.1.1 Simulation of aerial image

Simulation of aerial image can help to explore and get a better vision of defocus effect over the topography. It is also useful in optimization of multi-step imaging.

Simulation of aerial image for projection exposure was done based on Fraunhofer diffraction equations [26]. The normalized light intensity over 200 µm cavity in different depth from top to the bottom is calculated and 3D color map image is plotted. These simulations can be done for masks including lines with different parameters.

Figure 6-14 displays the simulation results for repetitive interconnect lines of 10 µm width and 20 µm pitch (selected based on previous experiment parameters). For this purpose, 2D aerial images for various focus offsets were calculated using Puptool software from ASML. Right side of Figure 6-14(a) shows two examples of the 2D aerial images at the focused plane and with 200 µm defocus offset. By combining all 2D calculation in z-axis, the 3D graphs were plotted in MATLAB. For simplicity and better illustration, only 3 lines are displayed. In Figure 6-14(a), the focal plane is the same as the wafer level at the top of the cavities (shown by the blue arrow in the figure). It is seen that as going deeper to the cavity bottom and so more defocus, the lines are getting wider and pattern sharpness is getting worse. The same defocusing issues are shown in Figure 6-14(b-c), when focus is on mid-level and bottom of the cavity sidewall. As we go

further from the focal plane, image distortion becomes more severe. These results suggest that one step imaging for high aspect ratio patterning would not be enough for a high-resolution pattern.

In the next step for getting better resolution and pattern sharpness, we applied multiple imaging at different focal planes. In Figure 6-14(d), imaging was done in double steps with focus at the top and bottom corners of cavity. The light intensity is the total light intensity summed over two exposures. In this case the patterns are formed with a better quality at 2 focal planes, since it seems that in each step of imaging defocusing problem of the other step is compensated. In addition, pattern sharpness at sidewall is improved comparing to Figure 6-14(a-c).

In order to get a better pattern quality and resolution at cavity sidewalls, we can add more imaging steps with focal planes at different level of cavity sidewalls. In Figure 6-14(e), one more imaging is done at mid-level of sidewall. In this case the line patterns are split rather sharply over the topography.

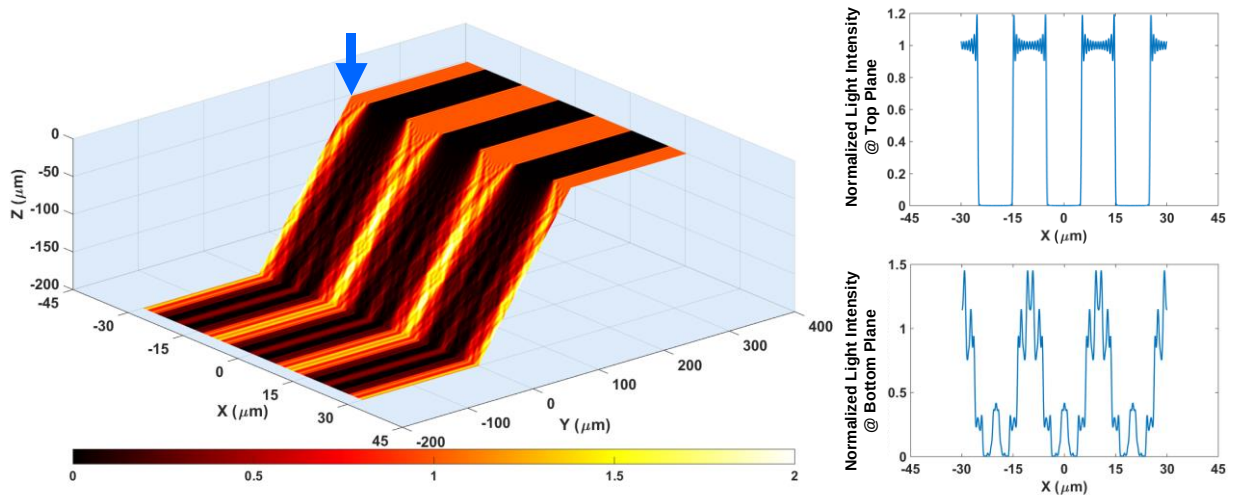
For different line resolutions and heights, the number of imaging steps can be optimized. There is a trade-off between the number of imaging steps (i.e. proportional to the lithography time) and pattern sharpness.

#### 6.6.1.2 MSI Experiments with a Single Mask

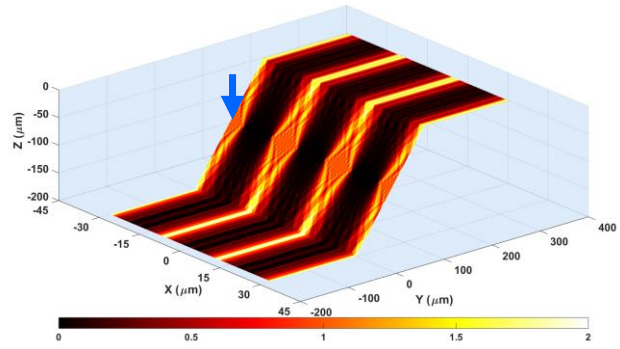


In this part, we are going to use a 200 µm cavity as a reflector cup for placing LED chips. This is one of the important application of such a method for heterogeneous 3D integration. In this test design, the Al coated cavity sidewalls are used for light reflection. It also contains wires for LED driving current and some sensors for system monitoring. So it should get patterned all the way from top to the bottom of 200 µm cavities. There are also some lateral structures on sidewall for optical sensor with 2 µm features. In the rest of this chapter, the aim is to find and propose a lithography method for such a 3D structure.

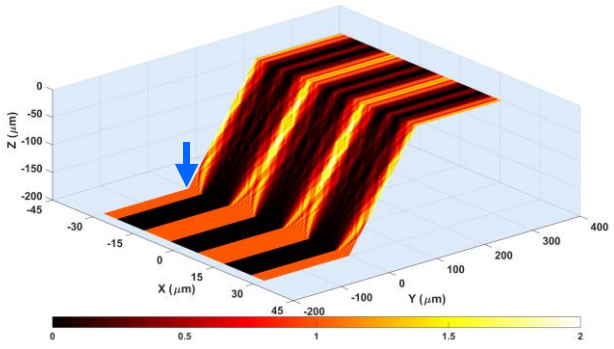
In this experiment, positive diluted AZ® 9260 resist was used. It is from AZ® 9200 thick film photoresist group, which is designed for the more demanding higher-resolution thick resist requirements. It provides high resolution with superior aspect ratios, as well as wide focus and exposure latitude and good sidewall profiles [36]. The resist was spray-coated in 2 sets of 8-layer spraying. Each step followed by a hotplate baking at 115 °C for 1 and 5 min, respectively.



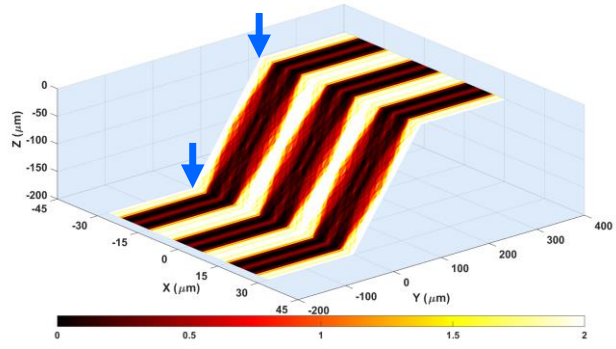

(a)



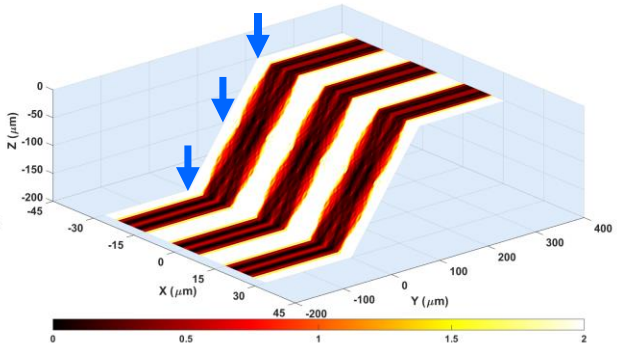

(b)




(c)




(d)




(e)

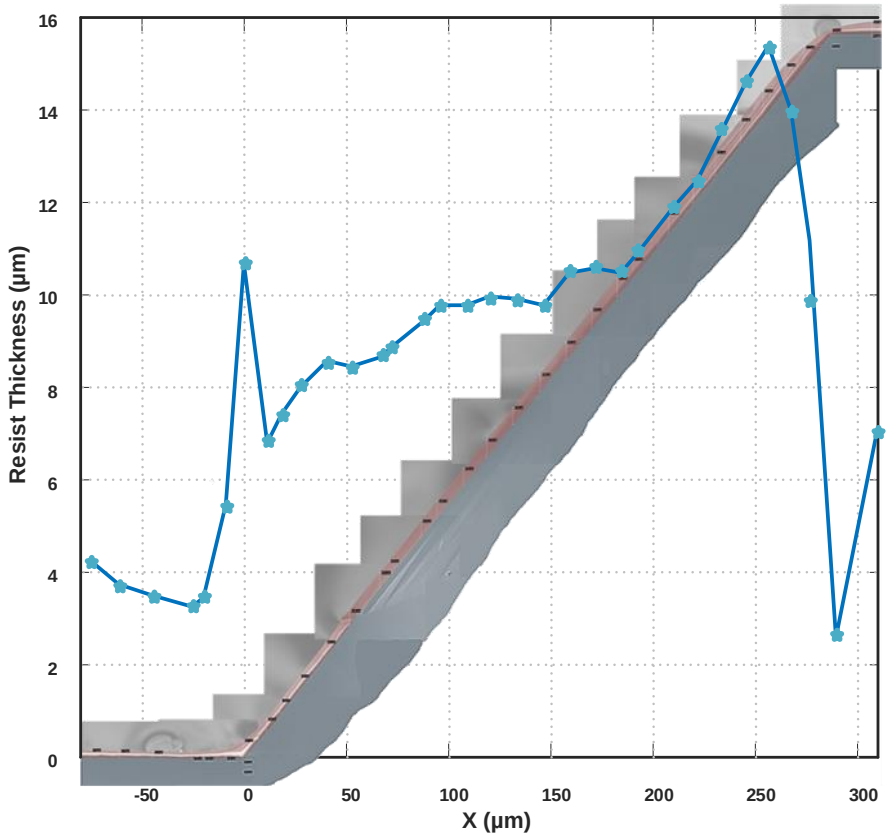
*Figure 6-14: Light intensity simulated plots over 200 μm cavity for mask of lines with 10 μm width/20 μm pitch for, (a) one step exposure focusing at top, (b) focusing at mid-level of sidewall, (c) focusing at bottom, (d) double exposure focusing at both top and bottom, and (e) triple exposure focusing at top, bottom and, mid-level of sidewall. The arrows point to the focal plane positions. In multi-exposure parts, light intensity of more than 2 is clipped and saturated. The light intensity amount is scaled to its nominal value (dose to clear).*

To have a better vision over how resist thickness changes over cavity sidewall, sets of SEM cross-section images were taken. The thickness was measured and shown in Figure 6-15(a). The cavity depth in this case is 410 µm. Starting from nominal thickness at the top (x>310 µm), resist thickness suddenly drops to its minimum value at the top edge (x=290 µm). This occurs due to flowing the resist from the edge down to the sidewall. Consequently, top side of the sidewall becomes thicker than the nominal value (the maximum at x=260 µm). The thickness gradually drops, until a local peak happens at the bottom corner (x=0 µm). At the bottom plain (x<0 µm), the thickness initially drops and then returns to the nominal value of the top plane. Figure 6-15(b) shows SEM images of the spray coated resist wall at the top plane demonstrating several sprayed layers. Also, for our main experiment with 200 µm deep cavities, resist thickness has a very similar behavior.

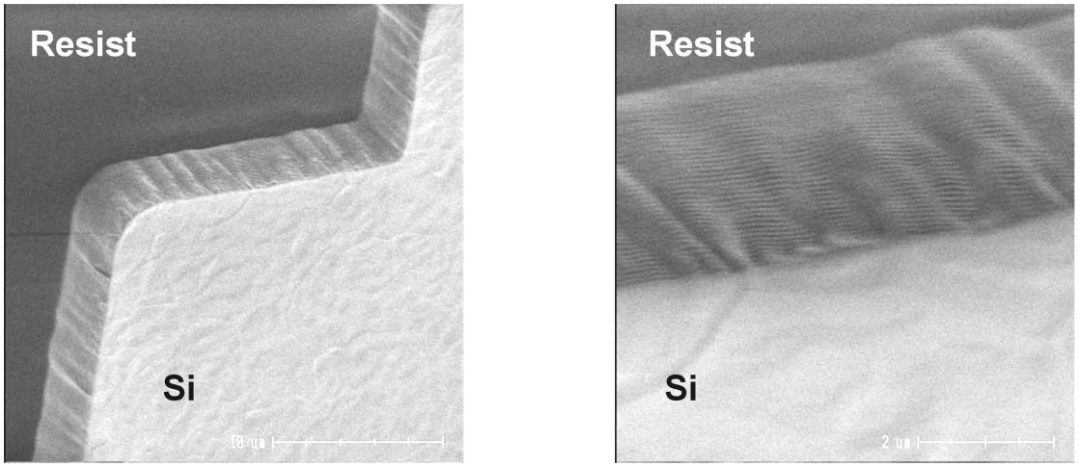
To validate the simulation model of aerial images in the MSI method with a single mask, we used different focus levels. In the first set of runs, the focus was set on the top plane, middle of sidewall, and bottom plane of the cavity. Figure 6-16 displays the interconnect mask layout from top view. The resulting patterns in photoresist on Si wafer are shown in Figure 6-17(a-c). As it can be seen, the features are dramatically deformed as the height gets far from the focus plane. Considering for example Figure 6-17(a) with the focus at the top plane, while the top plane has received just enough exposure dose to be developed well, the bottom plane has also received a high level of defocused exposure. Therefore, unlike what our previous simulation suggested, it cannot easily be compensated just by exposing at different levels.



In second set of experiments, the same mask was exposed at three focus levels. Figure 6-18 (a-b) show the SEM images. It is observed that the triple exposure caused feature loss in some areas including the corners of cavities. Also, from Figure 6-18(a), we can see that, even on the top plane, proper feature formation is disturbed by some extra lines between closely spaced parallel lines. It can be explained by two effects: 1) the ringing exists in the aerial images (see Figure 6-14(a)) which was also seen in Figure 6-17, and 2) Talbot effect due to defocus issue. It is worth mentioning that in Figure 6-18(b) even by under-exposure of the resist, the patterns are lost in the top corners. It is due to large mismatch of resist thickness over such a deep cavity. So applying the same exposure dose for whole resist due to large non-uniformity prevented a correct patterning in high resolution features.




(a)




(b)

*Figure 6-15: (a) The cross-section SEM image of the spray-coated resist over cavity sidewall, the graph shows how thickness changes at different distance (bottom corner is set as x-axis reference point), and (b) SEM images of wall of sprayed resist showing different layers.*

To explain self-imaging or Talbot effect, when different wavelength components of the transmitted light-field passes through the mask, they form a secondary image farther than a certain distance. That is unchanged with respect to extra increase in distance [33]. Although most of the reports and studies on this effect have been in near field diffraction area [33], [35], [37],

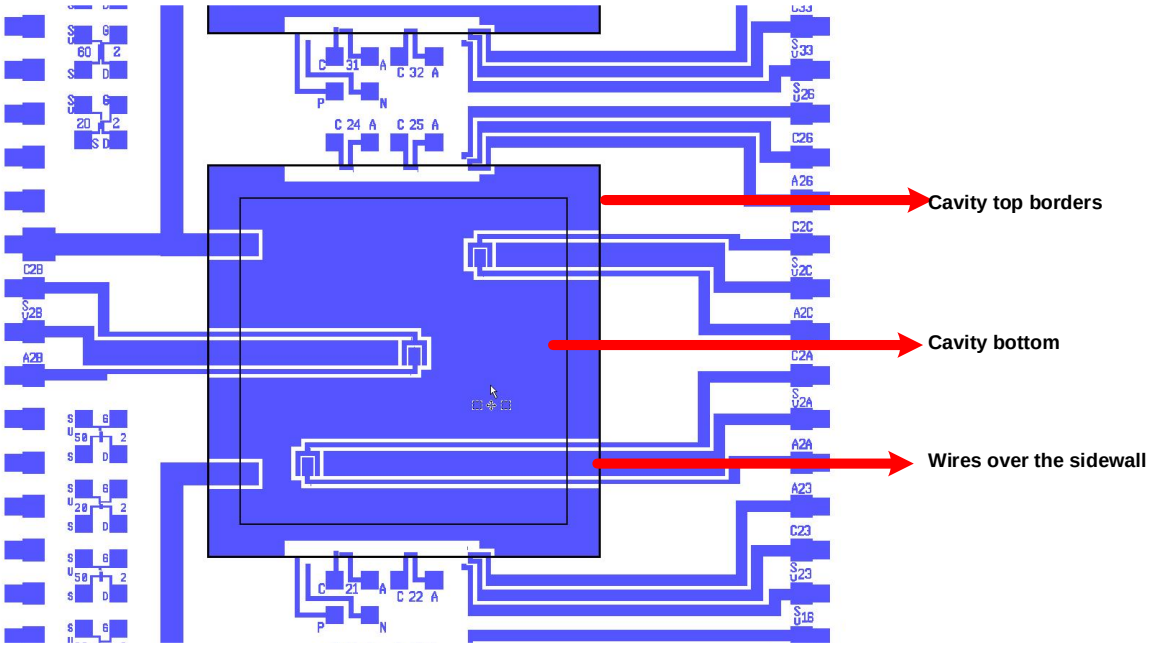



*Figure 6-16: Interconnect mask pattern from top view.*

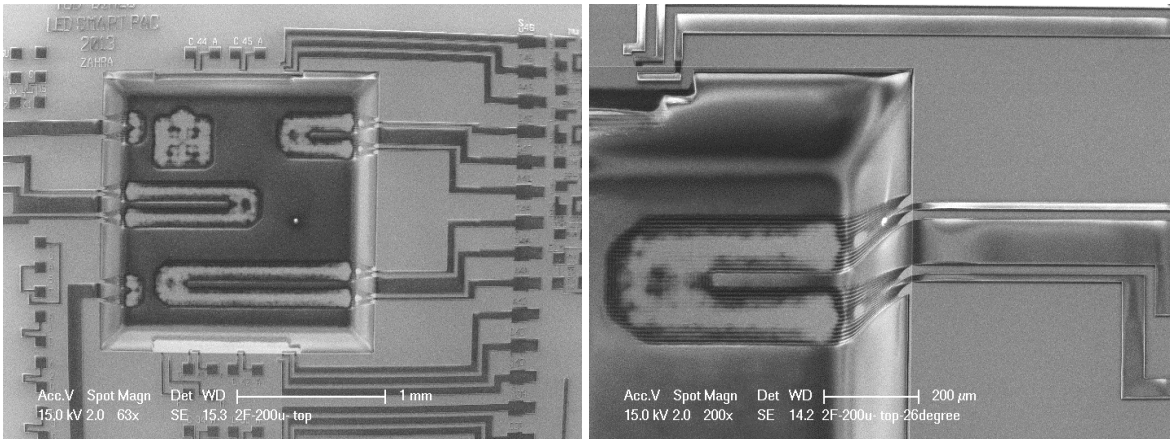
it was also reported in far field as a non-linear effect [34].

To find a process window for sidewall patterning using a single mask, more tests were carried out changing number of focus planes and exposure parameters. However, using single mask for exposure over the whole depth of cavity with non-uniform resist thickness is very challenging.

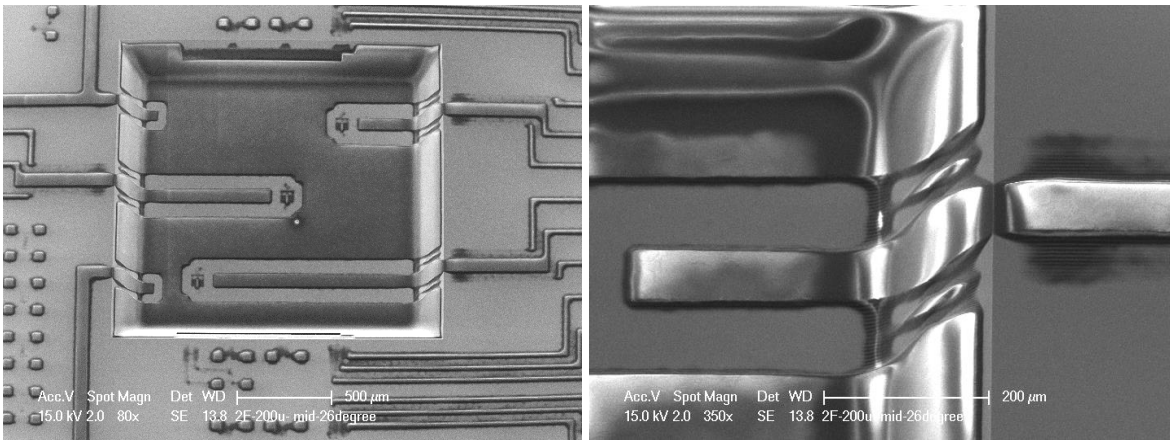
#### 6.6.1.3 Simulation of Complete Resist Profile after Patterning

To improve our simulation method, in addition to aerial image calculation, we should consider more parameters. Firstly, different resist thicknesses over the sidewall and especially at the corners should be included. Furthermore, the sensitivity of the resist in each exposure and over multi-exposure should be reflected. It means that for each imaging step and over the total exposures, if the light intensity goes higher than sensitivity of the resist, it would be developed in the final pattern (see Figure 6-19).

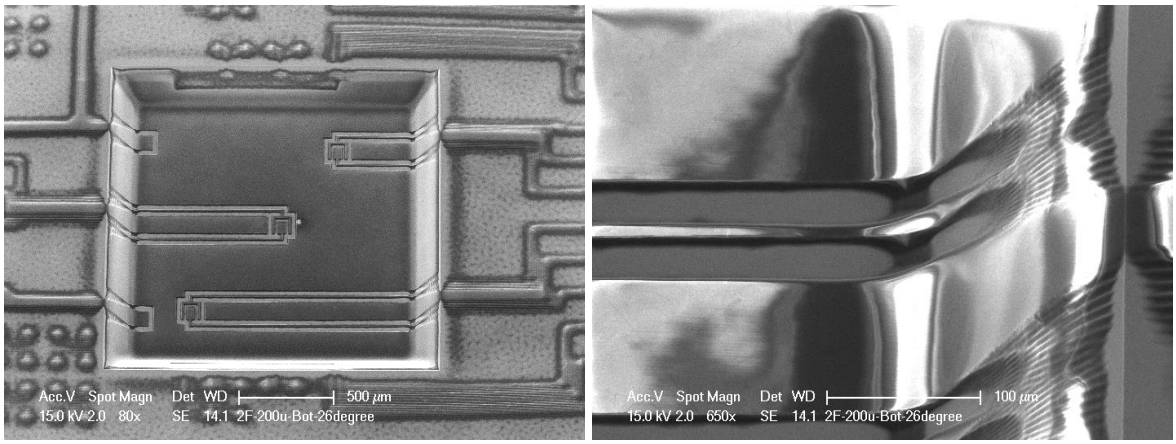
Resist thickness profile was interpolated using our measurement data and revealed the trend from Figure 6-15(a). Resist contrast ($\gamma$) and sensitivity ($D_f$) are not intrinsic properties of the resist and they depend on process conditions (developer, development time, baking time, exposure wavelength ($\lambda$), substrate, etc.) [26], [38], [39]. They were also extracted using the experimental results. The updated simulations with the similar cases to Figure 6-14 were done. The final resist profiles were extracted and 3D plots are shown in Figure 6-20(a-e). For the sake




(a)




(b)

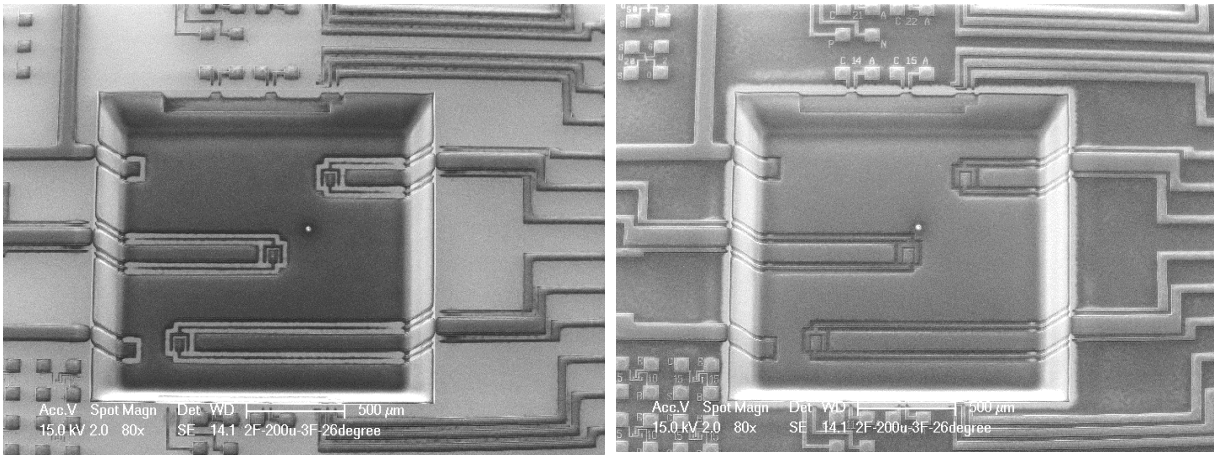



(c)

*Figure 6-17: The SEM images of MSI experiments with focusing at (a) top plane, (b) mid plane (100 µm), and (c) bottom plane (200 µm).*

of simplicity, the dose to clear changes versus resist thickness was assumed linear.

The updated simulation results are greatly consistent with the experiment results shown in Figure 6-17 and Figure 6-18. If one just considers the defocus effect on light intensity over the




(a) (b)

*Figure 6-18: The SEM images of MSI experiments with 3 focus planes with one mask, with (a) higher exposure dose, and (b) under-exposure dose.*

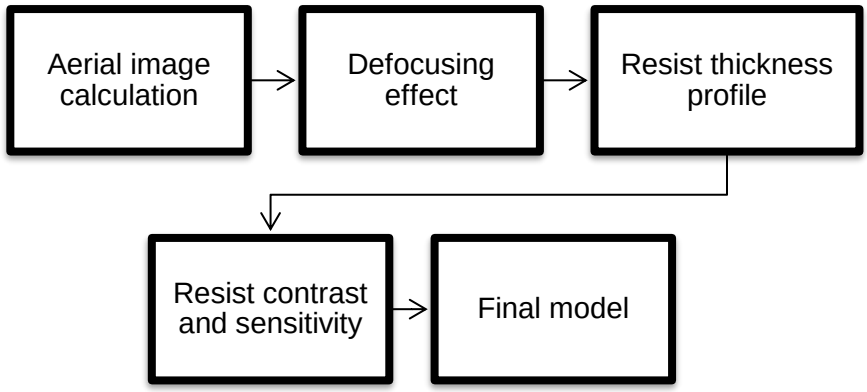
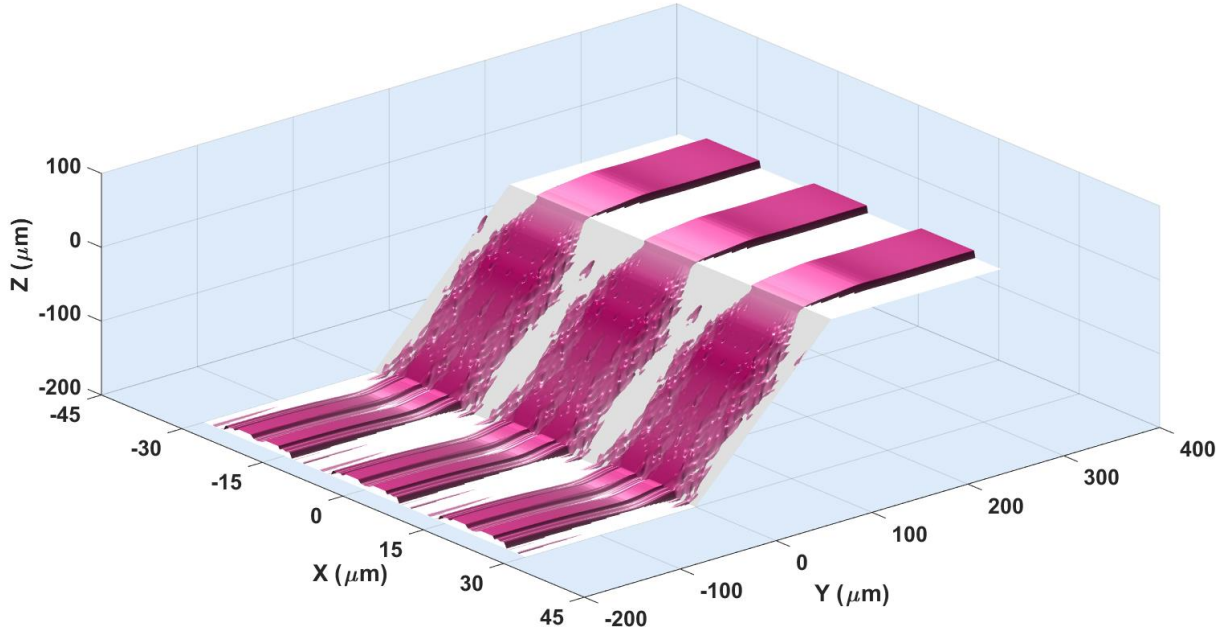



*Figure 6-19: Different modeling steps for MSI.*

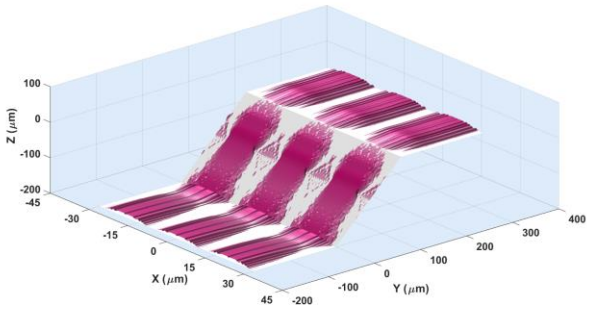
topography, it seems that using only one mask with multi-exposure and in sufficient focus steps should be enough for a successful patterning. However, including the resist profile and sensitivity, it is extra challenging. It was observed that as the difference between min and max of resist thickness increases, the overall intensity contrast should rise accordingly. This is not easily possible with counting defocusing effect of exposure on further focal points.

For bigger dimensions and pitches, using single mask and adjusting the parameter of MSI might work. However, it is a pattern and case depending method.

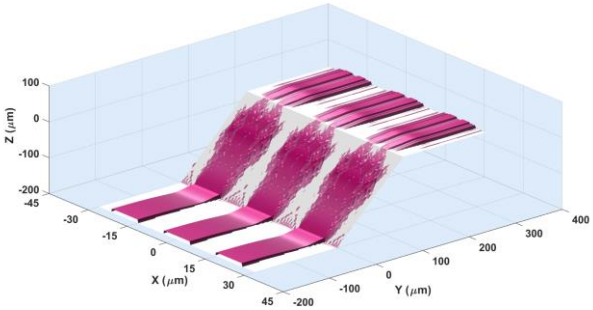
Nevertheless, to achieve a higher resolution or to have a generic pattern, using MSI in combination with split masks for each defined focal range is more promising.



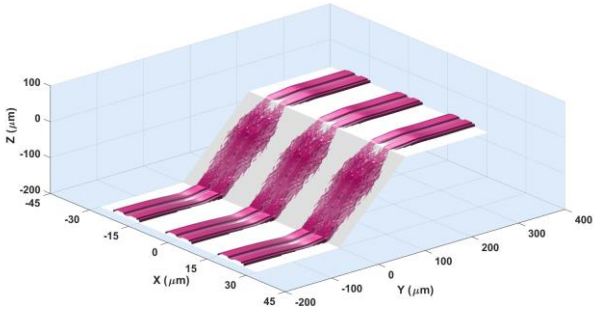

(a)



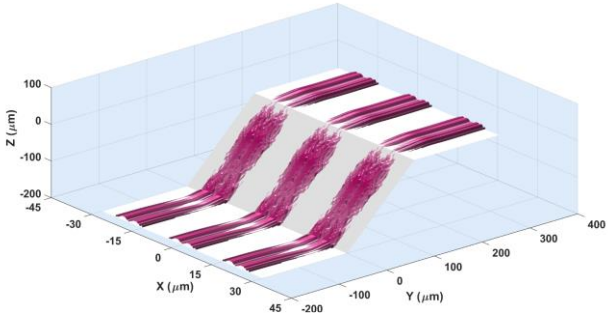
(b)



(c)

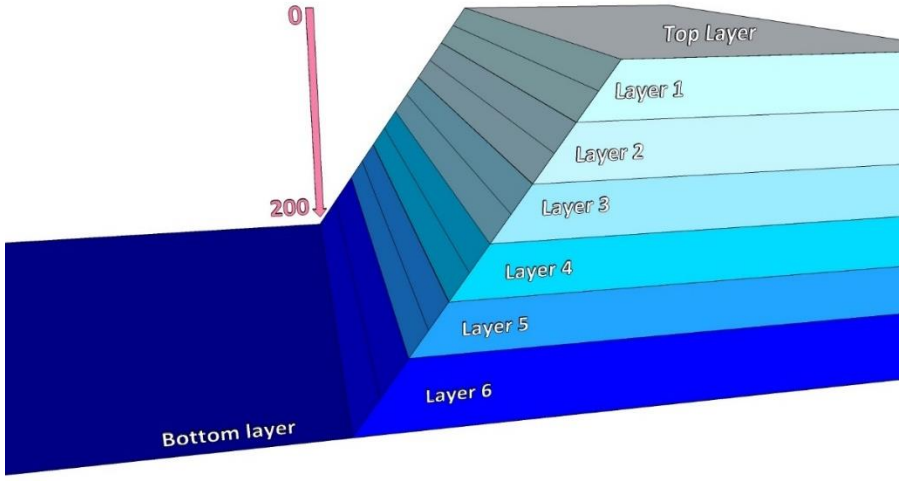


(d)

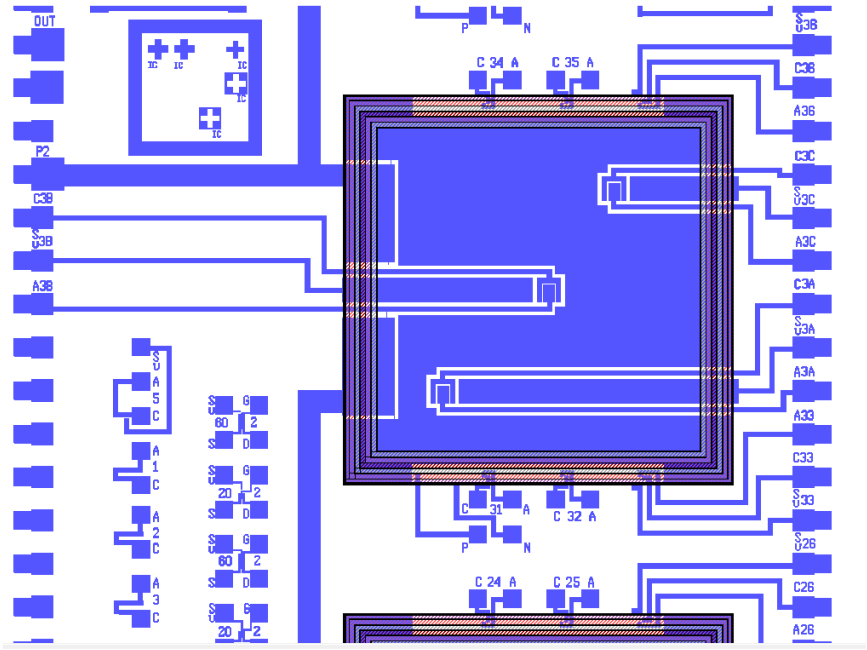


(e)

*Figure 6-20: Resist thickness profile simulated over 200 μm cavity for mask of lines of 10 μm width/20 μm pitch for, (a) one step exposure focusing at top, (b) focusing at mid-level of sidewall, (c) focusing at bottom, (d) same structure with double exposure focusing at top and bottom, (e) with triple exposure focusing at top, bottom and mid-level of sidewall.*




(a)



(b)

*Figure 6-21: (a) Different layer definition for MSI in 200 µm deep cavity, and (b) split mask layers for each imaging step (different colors on the sidewall represent 6 focus layers).*

### 6.6.2 MSI with Split Masking

Due to our design parameters for lateral features on the sidewall and interconnects, the max focus range which we could achieve an acceptable pattern resolution from focus plane is ± 18 µm. We call this a *focus layer*.

In the next phase, the mask was split to different segments for each focus layer. Thus, we can presume 35 µm as our focus layer depth and the center of this interval would be determined

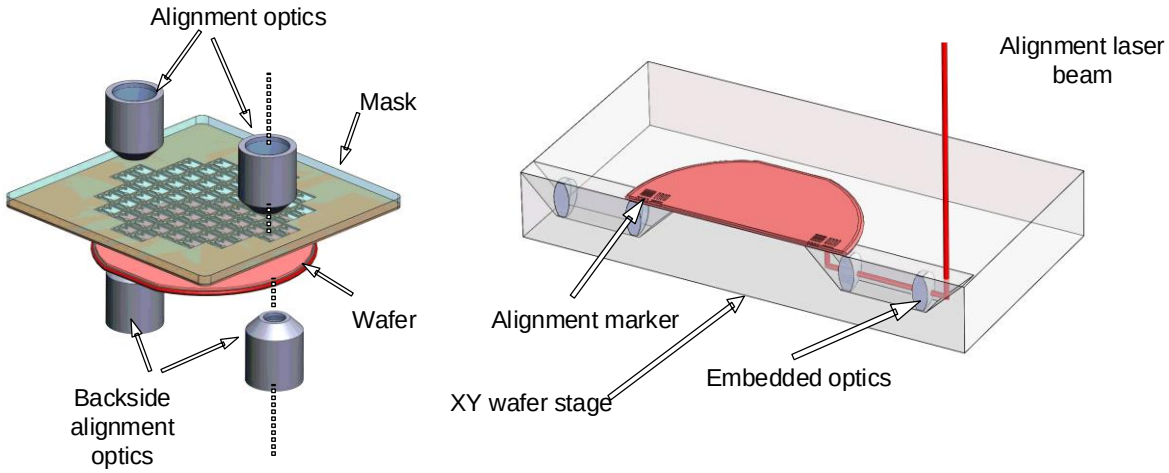



*Figure 6-22: Front to backside alignment principle in the wafer stepper.*

as the focus plane (see Figure 6-21(a)). Subsequently, for the 200 µm cavities, 8 multi-step images are defined, which are from top plane (focus offset is 0 µm) to bottom plane (focus offset is 200 µm). The final interconnect mask was split into 8 layers, each two neighbor layer has 1 µm overlap to ensure pattern integrity. The mask layers are shown in Figure 6-21(b). The predefined focus offsets were 0, 18, 53, 88, 124, 159, 188 and 199 µm for the 8 imaging steps from the top to the bottom of the cavities.

In ASML PAS55000 wafer stepper, which is used in this work, the alignment system is laser based on a phase grating alignment target. Using front side alignment due to rough surface of spray-coated resist is challenging and makes some shifting errors. Therefore, front to backside alignment (FTBA) is preferred. In this way, the overlay error is less than 200 nm (3σ). The principle of FTBA is shown in Figure 6-22, where there are some embedded optics in XY wafer stage. For this option, alignment markers were exposed and etched on both side of wafers in the former steps.

Using the capabilities of MSI, different exposure dose can be used for defined layers considering the local resist thickness profile. The bottom and the sixth layers need higher energy while layer 1 due to thin resist coverage over the top corner needs less. To optimize pattern quality, different tests were done. Figure 6-23 demonstrates the SEM images of resist pattern for just exposing even numbered focus layers. It can be observed that in all the exposed focus layers, all the features are successfully realized.

In the last part, the whole layers where exposed. Figure 6-24(a- c) display the SEM results

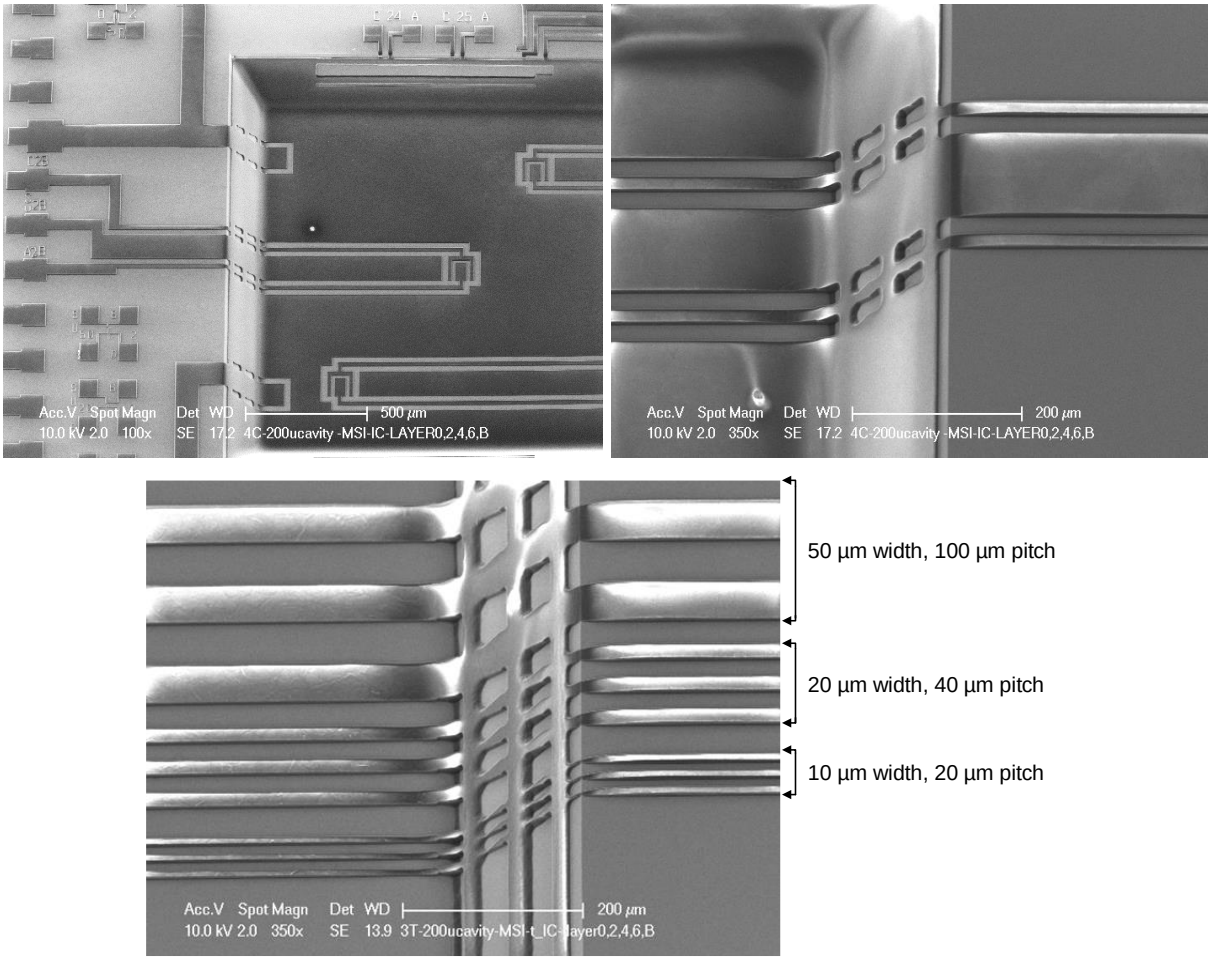
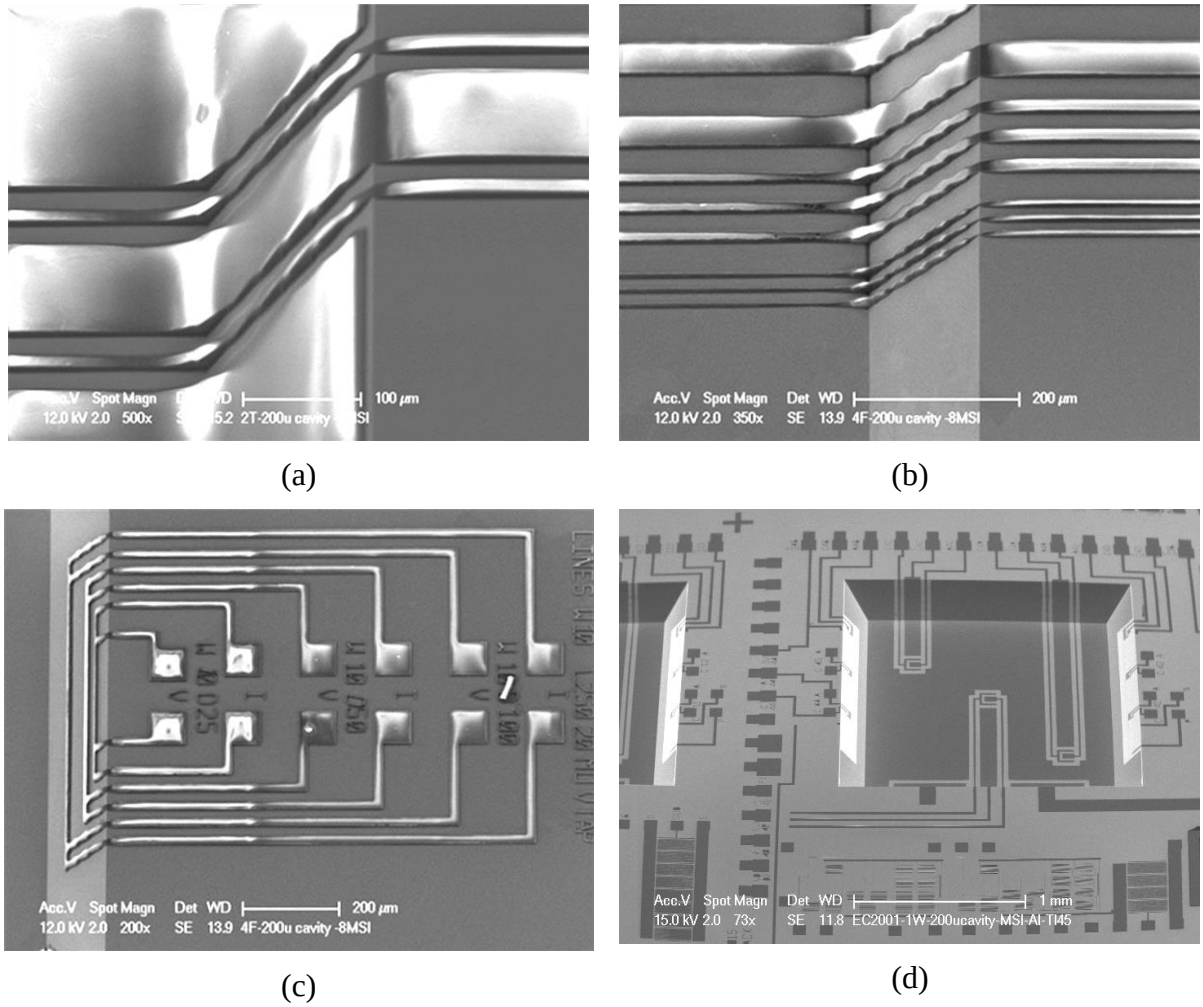



*Figure 6-23: SEM images of MSI results with split mask layers by exposing just even numbered focus layers.*

6

of the full exposure on resist layer. Thanks to the 35 µm focus depth for individual layers, lateral structures were also successfully developed. The wave like features on resist sidewall represent different imaging steps. Figure 6-24(d) shows the final result of very well patterned Al layer after a wet etching.

This method can be applied to wafer-level integration of LED chips and other functional devices. The wafer-level results are depicted in Figure 6-25(a-c) using optical imaging. Figure 6-25(b) shows the magnified top view of a cavity. The microscope focus is on the cavity bottom. The wires for LED driving current and temperature sensors went from top to bottom. The connections for optical sensors ended in sidewall and the rest of cavity surface was covered by Al for better reflectivity and thermal management. The controlling circuit and readout system were located on the top plane. The minimum feature size in this application is 2 µm for different layers. Figure 6-25(c) shows a photo of the whole wafer.




(a) (b)

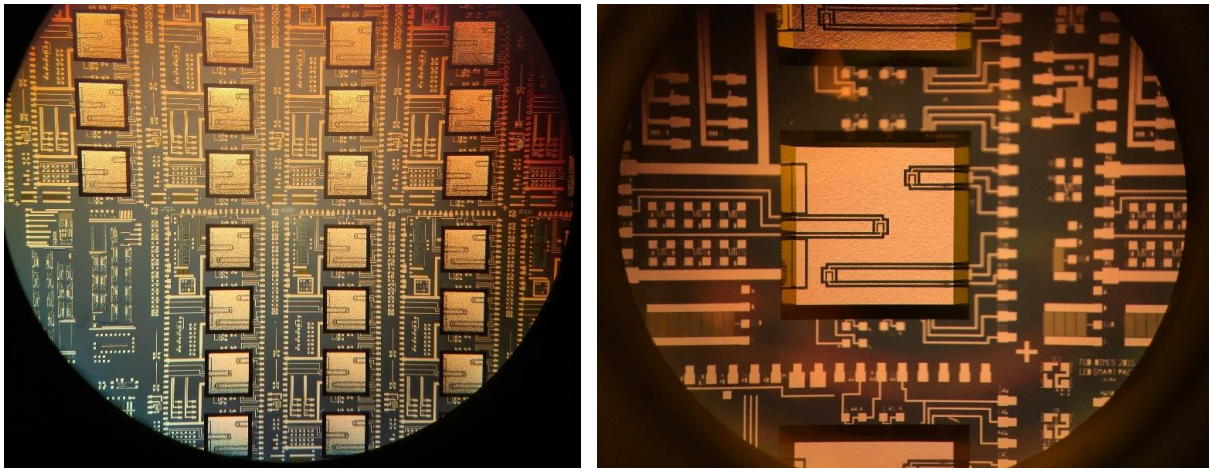
(c) (d)

*Figure 6-24: The SEM images of MSI results over 200 µm cavities, (a)-(c) patterns on the resist, and (d) the same feature after etching in aluminum layer.*

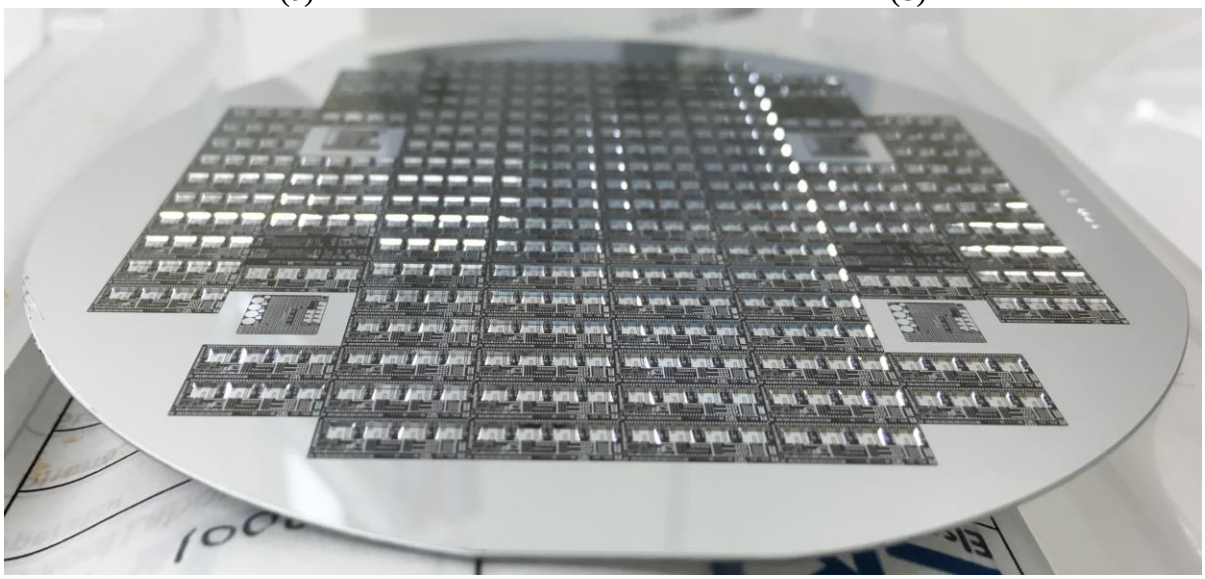
6

## 6.7 Conclusions

In this work "lithographic defined lateral wire bonding" was introduced as a new approach to overcome limitations and challenges of conventional wire bonding for special applications. It includes metal film deposition and patterning wire traces through high aspect ratio lithography, which is the main key for such a method. Different challenges and process details were discussed. Two sets of experiments were done to make various line structures over KOH cavities of different depths up to 200 µm. Multilayer spray-coating was used to have a good resist coverage over deep cavities. Exposure was done with EVG 420 mask aligner and multi-step imaging on an ASML PAS5500/80 projection aligner. Aluminum interconnect lines with different parameters were achieved after etching process. For sidewall imaging of wires using



(a) (b)



(c)

*Figure 6-25: Wafer level MSI results over 200 μm cavities, (a) optical microscope image showing top view of several adjacent dies, each composed of four cavities and related circuits, and (b) the magnified image of a single cavity, and (c) a photo of the whole wafer.*

MSI on stepper, a simulation method was proposed to predict 3D aerial image projected on the resist. As experimental results showed, only the aerial image was not enough and other parameters such as resist thickness profile and its sensitivity should be considered. Including these, the final simulation methodology was able to predict the final resist profile on 3D structures. The MSI with single mask was also experimentally investigated, but it was very challenging for high resolution features and a pattern depending method. Lastly, MSI with split masking was developed. It showed promising results for high resolution and generic patterns. This method can be applied for heterogeneous integration area where a reliable and flexible

interconnection method is critical. It also demonstrates integration beyond wire bonding capabilities such as monolithically implementation of 3D devices.

## 6.8 References

[1] T. Buisson, R. Beica, A. Pizzagalli, and J. Azemar, "2014 –Yole Business Update Report: 3DIC & 2.5D TSV Interconnect for Advanced Packaging," 2014.

[2] R. Beica (Yole developpements), "Business trends in Advanced Packaging," in *SEMI Networking Day:Packaging -Key for System Integration*, 2013.

[3] C. Goh, W. Chong, T. Lee, and C. Breach, "Corrosion Study and Intermetallics Formation in Gold and Copper Wire Bonding in Microelectronics Packaging," *Crystals*, vol. 3, no. 3, pp. 391–404, 2013.

[4] P. Liu, L. Tong, J. Wang, L. Shi, and H. Tang, "Challenges and developments of copper wire bonding technology," *Microelectron. Reliab.*, Dec. 2011.

[5] C. D. Breach, "What is the future of bonding wire? Will copper entirely replace gold?," *Gold Bulletin*, vol. 43, no. 3. pp. 150–168, 2010.

[6] C. L. Gan and U. Hashim, "Evolutions of bonding wires used in semiconductor electronics: perspective over 25 years," *J. Mater. Sci. Mater. Electron.*, 2015.

[7] E. Rutkowski and M. J. Sampson, "Body of Knowledge (BOK) for Copper Wire Bonds," 2015.

[8] G. Harman, *Wire bonding in microelectronics*, 3rd ed. McGraw-Hill electronics packaging and interconnection series, 2010.

[9] J. Pan and P. Fraud, "Wire Bonding Challenges in Optoelectronics Packaging," in *Proceedings of the 1st SME Annual Manufacturing Technology*, 2004.

[10] F. Iacopi, S. Brongersma, B. Vandevelde, M. O'Toole, D. Degryse, Y. Travaly, and K. Maex, "Challenges for structural stability of ultra-low-k-based interconnects," *Microelectron. Eng.*, vol. 75, no. 1, pp. 54–62, Jul. 2004.

[11] J. C. J. Chen, D. Degryse, P. Ratchev, and I. De Wolf, "Mechanical issues of Cu-to-Cu wire bonding," *IEEE Trans. Components Packag. Technol.*, vol. 27, no. 3, 2004.

[12] M. Romig and V. Gupta, "System-in-package provides viable integration solution," 2012. [Online]. Available: http://www.embedded.com/print/4236765. [Accessed: 23-Aug-2016].

[13] Y. Kun, G. Wei, L. Zhihua, and W. Lixi, "The impact of wire bonding on the transmission performance of high-speed links in SiP," in *ICEPT-HDP 2011 Proceedings - 2011 International Conference on Electronic Packaging Technology and High Density*

*Packaging*, 2011, no. 3, pp. 912–915.

[14] C. J. Vath and R. Holliday, "Bonding Wire options and their impact on product reliability," in *International Conference on Electronic Packaging Technology & High Density Packaging*, 2011, pp. 835–841.

[15] Y. Joung and M. Allen, "A micromachined chip-to-board interconnect system using electroplating bonding technology," *IEEE Trans. Adv. Packag.*, vol. 31, no. 2, pp. 357–366, 2008.

[16] N. Pham, M. Bulcke, and P. Moor, "Spray coating of photoresist for realizing through-wafer interconnects," *2006 8th Electron. Packag. Technol. Conf.*, pp. 831–836, 2006.

[17] C.-H. Ji, F. Herrault, and M. G. Allen, "A metallic buried interconnect process for through-wafer interconnection," *J. Micromechanics Microengineering*, vol. 18, no. 8, p. 85016, Aug. 2008.

[18] M. Murugesan, T. Fukushima, K. Kiyoyama, J.-C. Bea, T. Tanaka, and M. Koyanagi, "High-step-coverage Cu-lateral interconnections over 100 µm thick chips on a polymer substrate—an alternative method to wire bonding," *J. Micromechanics Microengineering*, vol. 22, no. 8, p. 85033, Aug. 2012.

[19] T. M. Verhaar, J. Wei, and P. M. Sarro, "Pattern transfer on a vertical cavity sidewall using SU8," *J. Micromechanics Microengineering*, vol. 19, no. 7, p. 74018, Jul. 2009.

[20] K.-W. Lee and M. Koyanagi, "Novel interconnection technology for heterogeneous integration of MEMS–LSI multi-chip module," *Microsyst. Technol.*, vol. 16, no. 3, pp. 441–447, Oct. 2009.

[21] W. Flack, R. Hsieh, G. Kenyon, K. Nguyen, M. Ranjan, N. Silva, P. Cardoso, E. O. Toole, R. Leuschner, W. Robl, and T. Meyer, "Lithography technique to reduce the alignment errors from die placement in fan-out wafer level packaging applications," in *Proceedings - Electronic Components and Technology Conference*, 2011, vol. 1, pp. 65–70.

[22] P. Maury, J.-M. Quemper, S. Pocas, D. Van Vliet, N. Noordam, P. Ten Berge, and K. Best, "Sub-micron imaging on high-topography wafers using spray coating and projection lithography," *Microelectron. Eng.*, vol. 87, no. 5–8, pp. 904–906, May 2010.

[23] "Use Underfill Encapsulants To Enhance Flip-Chip Assembly Reliability | Boards content from Electronic Design." [Online]. Available: http://electronicdesign.com/boards/use-underfill-encapsulants-enhance-flip-chip-assembly-reliability.

[24] G. L. Williams, I. Wallhead, V. Sarojiniamma, P. A. Ivey, and N. L. Seed, "The patterning

of fine-pitch electrical interconnections on non-planar substrates: A comparison between methods utilising laser ablation and electro-deposited photoresist," *Sensors Actuators, A Phys.*, vol. 112, no. 2–3, pp. 360–367, 2004.

[25] R. Voelkel, U. Vogler, A. Bramati, A. Erdmann, N. Ünal, U. Hofmann, M. Hennemeyer, R. Zoberbier, D. Nguyen, and J. Brugger, "Lithographic process window optimization for mask aligner proximity lithography," in *Proc. of SPIE*, 2014, vol. 9048.

[26] J. D. Plummer, M. D. Deal, and P. B. Griffin, *Silicon VLSI technology: Fundamentals, Practice and modeling*. Prentice Hall, 2000.

[27] N. Pham and E. Boellaard, "Photoresist coating methods for the integration of novel 3-D RF microstructures," *J. Microelectromechanical Syst.*, vol. 13, no. 3, pp. 491–499, 2004.

[28] Z. Kolahdouz Esfahani, H. Van Zeijl, and G. Q. Zhang, "High Aspect Ratio Lithography for Litho-Defined Wire Bonding," in *ECTC*, 2014, pp. 1556–1561.

[29] P. Maury, J. M. Quemper, S. Pocas, D. Van Vliet, N. Noordam, P. ten Berge, and K. Best, "Sub-micron imaging on high-topography wafers using spray coating and projection lithography," *Microelectron. Eng.*, vol. 87, no. 5–8, pp. 904–906, 2010.

[30] N. P. Pham, E. Boellaard, W. Wien, L. D. M. van den Brekel, J. N. Burghartz, and P. M. Sarro, "Metal patterning on high topography surface for 3D RF devices fabrication," *Sensors Actuators A Phys.*, vol. 115, no. 2–3, pp. 557–562, Sep. 2004.

[31] U. Vogler, F. Windrich, A. Schenke, R. Völkel, M. Böttcher, and R. Zoberbier, "Cost-effective lithography for TSV-structures," in *Proceedings of Electronic Components and Technology Conference*, 2011, pp. 1407–1411.

[32] M. Hornung, "LED Wafer Level Packaging – Motivation, Challenges and Solutions to Meet Future Cost Targets," *SUSS Rep. 02/2012*, 2012.

[33] H. H. Solak, C. Dais, and F. Clube, "Displacement Talbot lithography: a new method for high-resolution patterning of large areas.," *Opt. Express*, vol. 19, no. 11, pp. 10686–10691, May 2011.

[34] J. M. Wen, Y. Zhang, S. N. Zhu, and M. Xiao, "Theory of nonlinear Talbot effect," *J. Opt. Soc. Am. B-Optical Phys.*, vol. 28, no. 2, pp. 275–280, 2011.

[35] L. Urbanski, M. C. Marconi, a. Isoyan, a. Stein, C. S. Menoni, and J. J. Rocca, "Analysis of a scheme for de-magnified Talbot lithography," *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct.*, vol. 29, no. 2011, p. 06F504, 2011.

[36] (c) Clariant AG, *AZ ® 9200 Photoresist Product data sheet*. 2007.

[37] A. Isoyan, F. Jiang, Y. C. Cheng, F. Cerrina, P. Wachulak, L. Urbanski, J. Rocca, C. Menoni, and M. Marconi, "Talbot lithography: Self-imaging of complex structures," *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct.*, vol. 27, no. 6, p. 2931, 2009.

[38] W. M. Moreau, *Semiconductor Lithography: Principles, Practices, and Materials*. Plenum Press, 1988.

[39] H. J. Levinson, *Principles of lithography*, 2nd ed. Bellingham, WA : SPIE Press, 2005.

# Chapter 7

# 3D Silicon-Based Smart Interposer[8]

The final 3D LED system-in-package (SiP) is described in this chapter covering the design concepts, process flow, challenges, and some measurement results. It uses cavity not only as a precision LED site, but also as an active reflector cup. It is active since the cavity bottom contains local temperature sensors and the sidewalls carry blue light detectors in addition to the high aspect ratio interconnects. This is for the first time that an active device (the photodiode) is fabricated on the sidewall of a silicon cavity. The other controlling circuits described in 2D package are also integrated on top surface of the Si interposer.

## 7.1 Introduction

Silicon-based wafer level packaging is an appropriate packaging approach for LEDs, especially for high-power and high-lumen applications. Superior yield and advanced integration has been already developed in Si technology for different areas. Moreover, Si substrate provides good heat conduction because of the high thermal conductivity and low strain incorporation due to the low coefficient of thermal expansion [1]–[4]. In order to have a high reliability and smart package, it is essential to monitor and control the package performance. Temperature and output light are two critical parameters in such a system.



[8] The extended version of this chapter will be submitted as : Z. Kolahdouz, H. Abdy, H. van Zeijl, M. Kolahdouz and G. Q. Zhang, “3D Silicon-Based Smart Interposer for LED WLP,” to Scientific Reports.

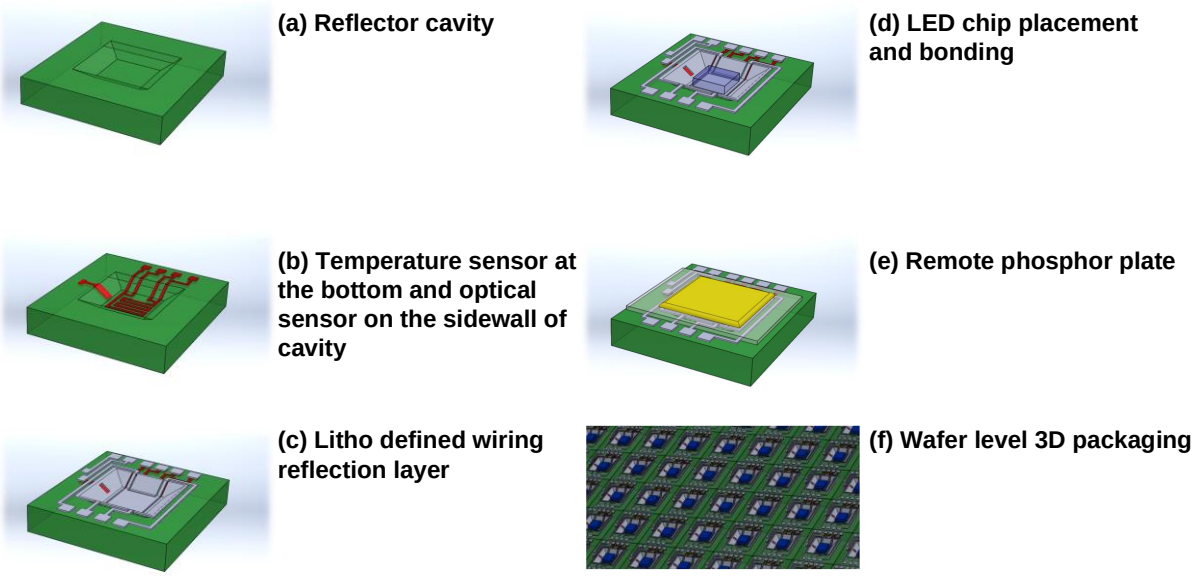



*Figure 7-1: Schematic of the suggested 3D LED WLP with the active in-situ reflector cup.*

In previous chapters, Chapter 3-5, a 2D multi-functional package for phosphor-based LED packages were thoroughly introduced and discussed. The 2D package was implemented in a low cost 7-mask BiCMOS process. It contained different functional blocks such as temperature and light sensors, sensor readout circuit, high power switches, and light feedback control circuit. Later, in Chapter 6, a new method for high aspect ratio (HAR) lithography based on multi-step imaging (MSI) was explained. In the next step, we have combined these 2 parts to make a 3D package for LEDs.

In this process, HAR lithography was not only used for litho-defined wire bonding, but also to fabricate functional 3D devices on the cavity bottom and sidewalls. That is a novel approach for making 3D devices.

The new package, see Figure 7-1, integrates the same functions but with an in-situ reflector cup which can enhance the light extraction efficiency of the package. This is fabricated with deposition of a thin aluminum layer on a KOH etched Si cavity. This cup is not only a reflector, but also an active LED container, one can call active reflector cup. The LED chip would be later mounted on the cavity bottom. The light sensors are positioned on the cavity sidewalls to have a better line of sight for the emitting light from the LED chip. Temperature sensors are located at cavity bottom directly beneath the LED chip. Litho-defined wires are patterned on the sidewalls to drive LED currents and also as the interconnections of the temperature sensor and

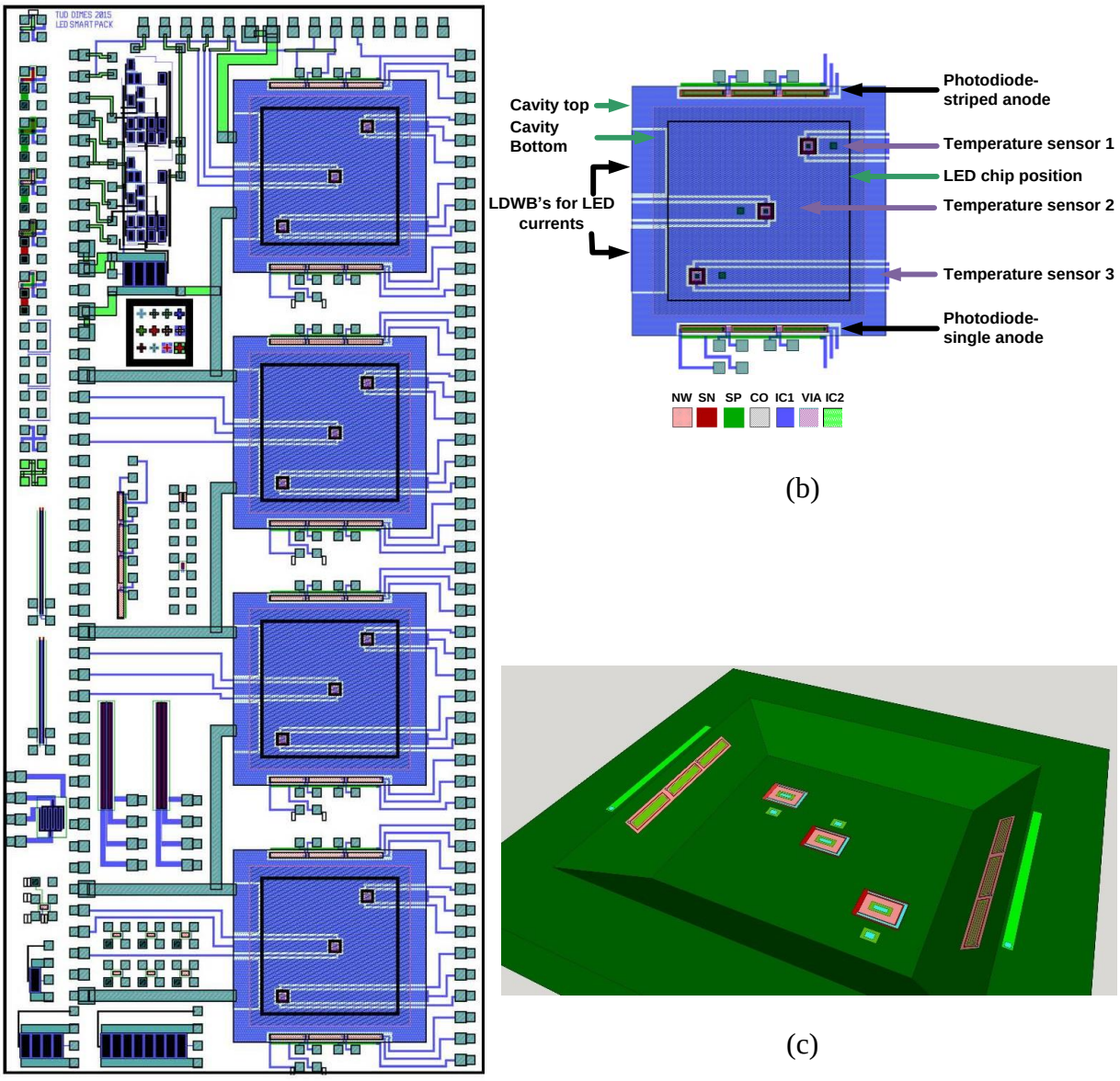



*Figure 7-2: Layout of the 3D package and positions of LEDs, sensors and circuit blocks. (a) Full die layout, (b) reference cavity, and (c) 3D layout of different layers in the cavity before metallization.*



photodiodes to other blocks. The other control circuit and blocks are placed on top plane of the wafer.

The advantages of such a LED SiP are:

– Capability of wafer-level optics and phosphor remote coating for stable color uniformity.
– Higher brightness efficiency: on chip reflector cup (cavity with mirror coating) reflecting the side light can improve light extraction efficiency up to 15% [5].

- Better thermal management: high thermal conductivity of Si substrate ($K \sim 150\ W/(m.K)$).
- Lifetime improvement: self-monitoring system.
- High reliability: better interconnect reliability, circuit trick for stability and aging compensation.

The proposed 3D interposer is not just applicable for LED wafer level packaging. It can also be employed for a wide range of applications that need to monitor and control a functional device in a smart system. The relatively low cost and small fully integrated interposer is a promising packaging solution for high reliability and multi-disciplinary areas.

This chapter is organized as follows: in Section 7.2, the design of our 3D LED wafer level package (WLP) is presented in 3 main groups of bottom temperature sensors, sidewall photodiodes and control circuits. In Section 7.3, fabrication process is described with presenting the main challenges and steps of the 3D BiCMOS method. In Section 0, the implementation and measurement results are discussed. Finally, it will end by a short conclusion of this chapter.

## 7.2 Design of 3D Smart LED WLP

The package is designed as a high lumen output package integrating 4 blue power LED dies. There is one cavity for holding each LED chip. The complete die size is 4.5×10 $mm^2$ including the test and main structures. The design is such that 4 LEDs can be turned on in series with any combinations of 1 to 4. The target LED chip in this study is again a vertical Bridgelux® Blue Power Die. Its dimension is 1143×1143×150 $\mu m^3$ with max DC forward current of 700 mA.

The whole design was based on 2 µm 7-mask BiCMOS process. But to make a 3D package, we should consider HAR lithography requirements. To do so, we defined 8 different focus layers from top to bottom of the cavity. Each cavity is 1800×1800 $\mu m^2$ on top and 1517×1517 $\mu m^2$ at the bottom. The cavity depth is 200 µm.

This process comprises a 7-mask process that involves both Bipolar and CMOS transistors. The low cost and low number of litho steps make it also appropriate for 3D configuration of the package. Furthermore, the relative low area costs for IC processing enable 3D integration of IC's with large area devices such as LED chips, in our case 1.1×1.1$mm^2$. Figure 7-2(a) shows the complete die layout which monolithically integrated different components for the

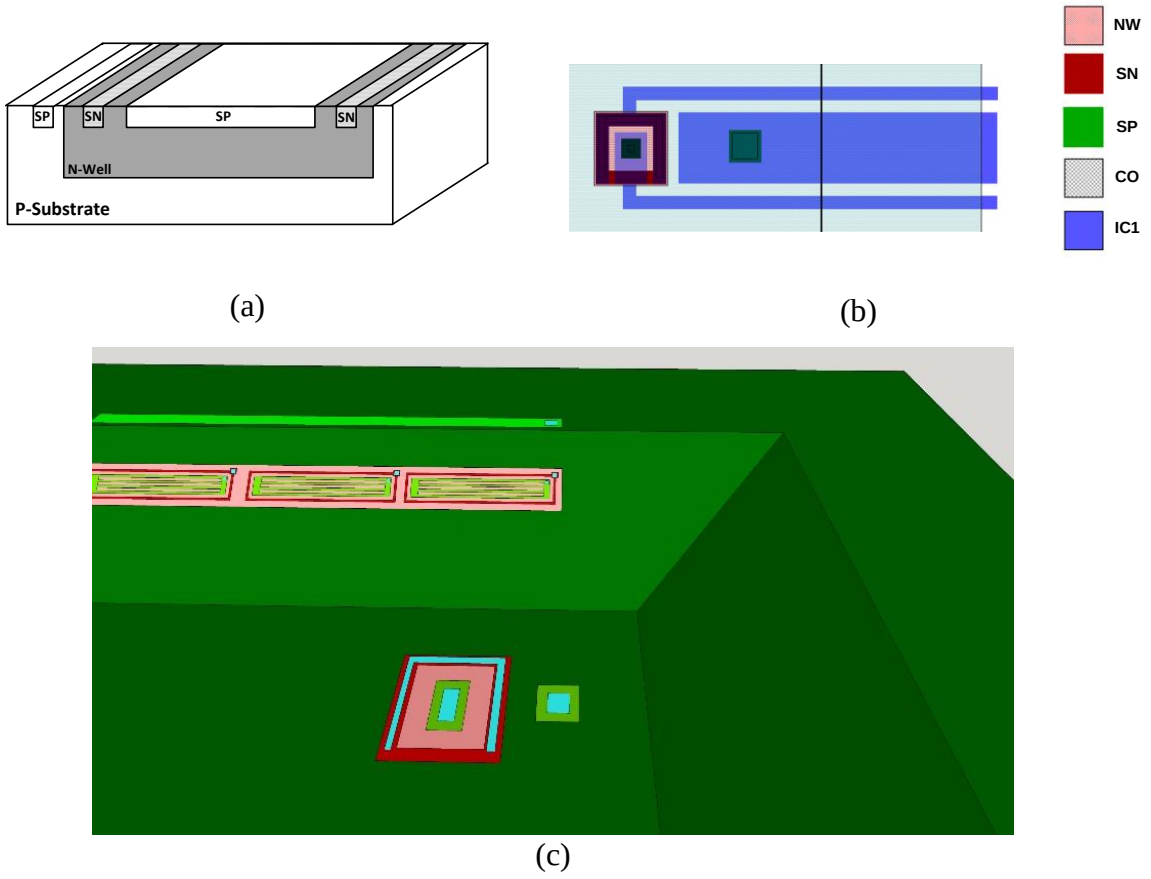



*Figure 7-3: (a) Schematic of a temperature sensor, (b) relative mask layout, the wires pass through the cavity sidewall, and (c) 3D positioning of the sensor on cavity bottom.*

multifunctional LED system. It contains 4 similar cavities, let's call each as a reference cavity. Figure 7-2(b) illustrates the top view of a reference cavity. The 3D layout of implantation areas for the sensors are shown in Figure 7-2(c).

### 7.2.1 Bottom Temperature Sensor

For temperature sensing, three PNP dual junctions are located at different positions under the LED dies at the bottom of each reference cavity. It consists of a $P^+$ in an N-well (SP area) on a P-substrate, as shown in Figure 7-3(a). The lower N-P junction is short-circuited to eliminate the effect of surrounding charges and upper $P^+$-N junction is forward biased at constant current to evaluate the voltage as the temperature indicator. Figure 7-3(b) illustrates the mask layout of a temperature sensor. It can be seen that the related wires through the sensors passes the cavity sidewall. Figure 7-3(c) depicts the positioning of the sensor in 3D schematic.

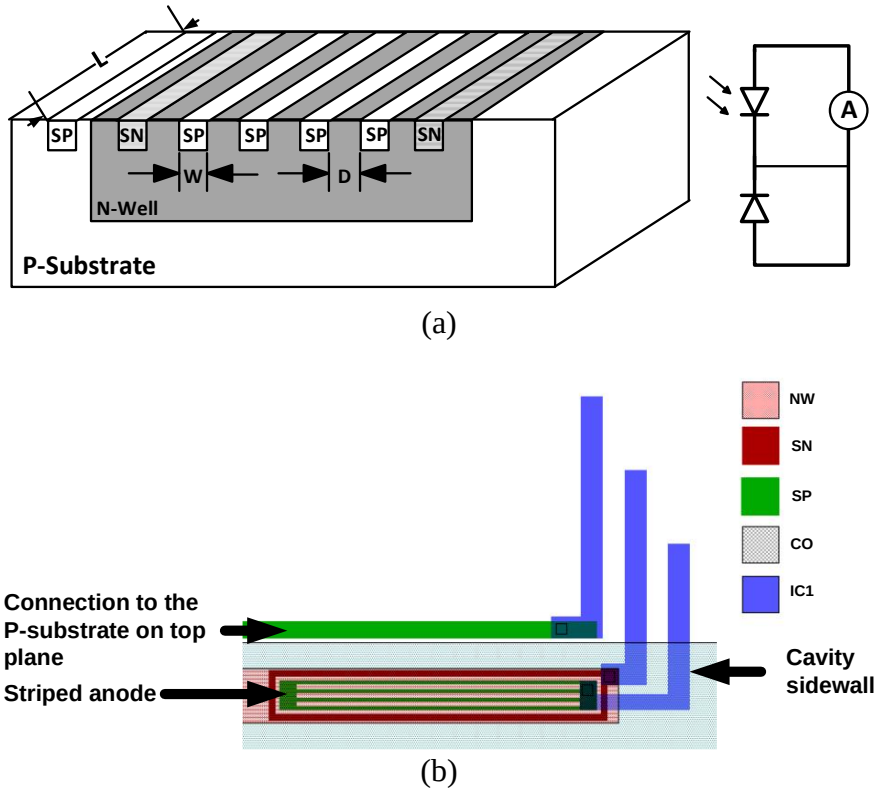



*Figure 7-4: (a) Schematic of a striped-shape photodiode and the equivalent circuit, and (b) relative mask layout.*

### 7.2.2 Sidewall Light Sensor

For output light sensing in 2D package, a blue selective photodiode was designed and fabricated which was completely discussed in Chapter 4. This photodiode, with upper junction at 330 nm, demonstrated a very high selectivity to the blue light with maximum responsivity at 480nm which is matched with the blue LED's illumination [6]. In 3D package, the diodes are located on the cavity sidewalls for better line of sight for the emitting light. In each cavity, there are 2 sets of photodiodes, the single anode and multi-stripe anode diodes (Figure 7-2(b)). The structure is almost the same as the 2D package in Chapter 4, with $W$ =3 µm and $D$ =5 µm. Nevertheless, in order to reduce the number of the involved focus layer for HAR litho, the finger number is changed to 4 (instead of 5 in previous design). To keep the junction area the same as before, the finger length (L) is increased to 300 µm. The schematic of cross-section of multi-stripe photodiodes and related mask layout are shown in Figure 7-4(a-b).

### 7.2.3 Control Circuits

The same control blocks as the 2D package were integrated on the top plane. For instance,

*Table 7-1: Overview of involved focus layers for main mask steps in 3D BiCMOS7 process. The colored boxes show the involved layers for each mask.*

| Focus layers | Focus offset (µm) | Main mask steps | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | NW | SN | SP | CO | IC1 | VIA | IC2 |
| **Top** | 0 | | | | | | | |
| **Level 1** | 18 | | | | | | | |
| **Level 2** | 53 | | | | | | | |
| **Level 3** | 88 | | | | | | | |
| **Level 4** | 124 | | | | | | | |
| **Level 5** | 159 | | | | | | | |
| **Level 6** | 188 | | | | | | | |
| **Bottom** | 199 | | | | | | | |

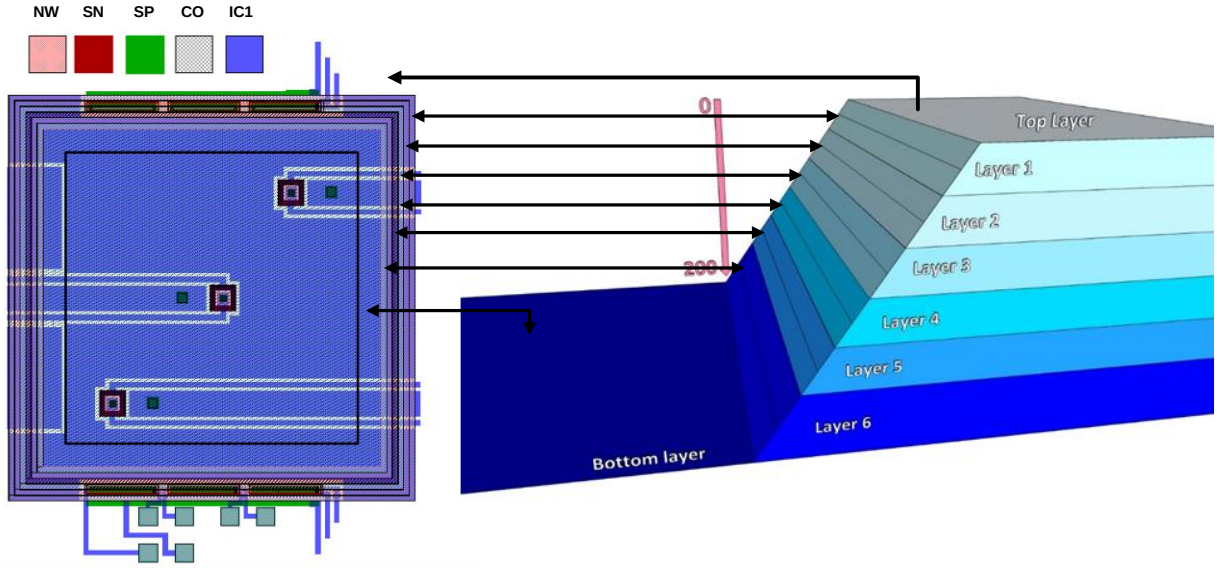
the light feedback control circuit (consisted of the power switch, 2 opamps, and the multi-stripe photodiode) were integrated. Except the photodiode and the connecting wires, the rest is located on the top plane and implemented as before.

## 7.3 Fabrication Process

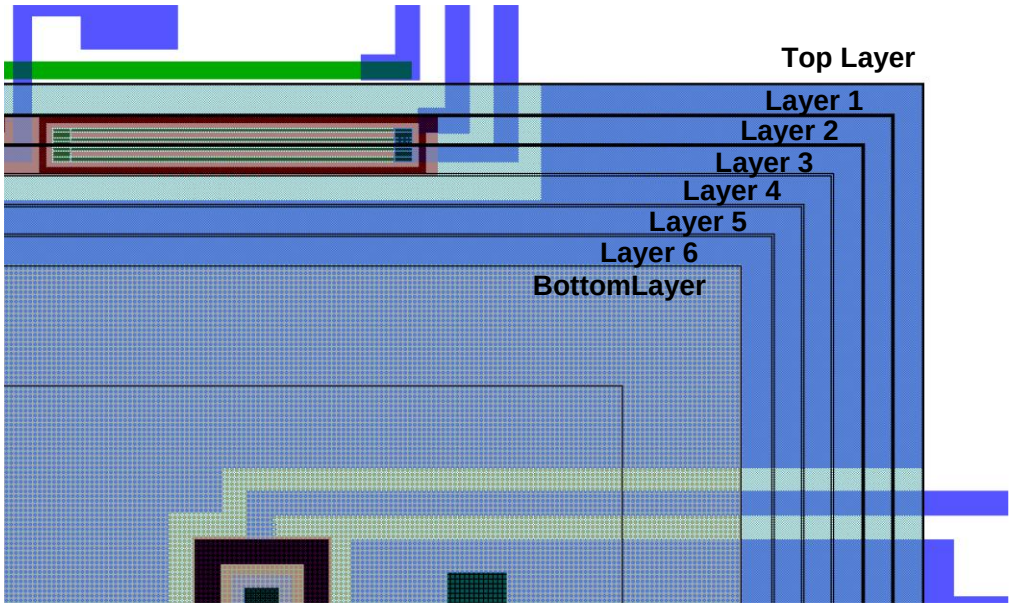
In previous chapters, the planar 7-mask BICMOS process was clearly explained. It consists of seven main mask steps: three for implantations (N-well (NW), $N^+$ area (SN), and $P^+$ area (SP)), two for first metal interconnect (contact opening (CO) and interconnect1 (IC1)), and two for second metal (via (VIA) and interconnect2 (IC2)). For 3D package, the process should have been modified. There were some new challenges for 3D implementation of BiCMOS7 that are explained in the following.

### 7.3.1 Lithography

The HAR litho approach using MSI on ASML PAS5500 wafer stepper was elaborated in Chapter 6. To use the same method, the total involved focus depth (200 µm) should be split into 8 focus layers. The focus layer depth is 35 µm. So, for complete patterning from top to bottom we have 8 imaging steps; one at top plane, one at bottom plane and six for covering the 200 µm sidewall. Nevertheless, the only layer that needs the full patterning is first metal layer, IC1. It is used for connecting the sensor interconnects, feeding the driving current of LED chips located at the cavity bottom, and forming the mirroring surface of the micro-reflector cavity. Table 7-1 summarizes the required focus layers for the main mask steps.




(a)




(b)

*Figure 7-5: (a) Top view of reference cavity on left, with mapping the defined focus layers to 3D schematic of the cavity on right, and (b) zoom-in of top right corner of reference cavity showing different mask layers.*

The sidewall sensor design was optimized for minimum involved focus layer for N-well, SN, SP and CO. Figure 7-5(a-b) shows the top view of the defined focus layers in the reference cavity mapped to the 3D schematic of a 200 µm cavity.

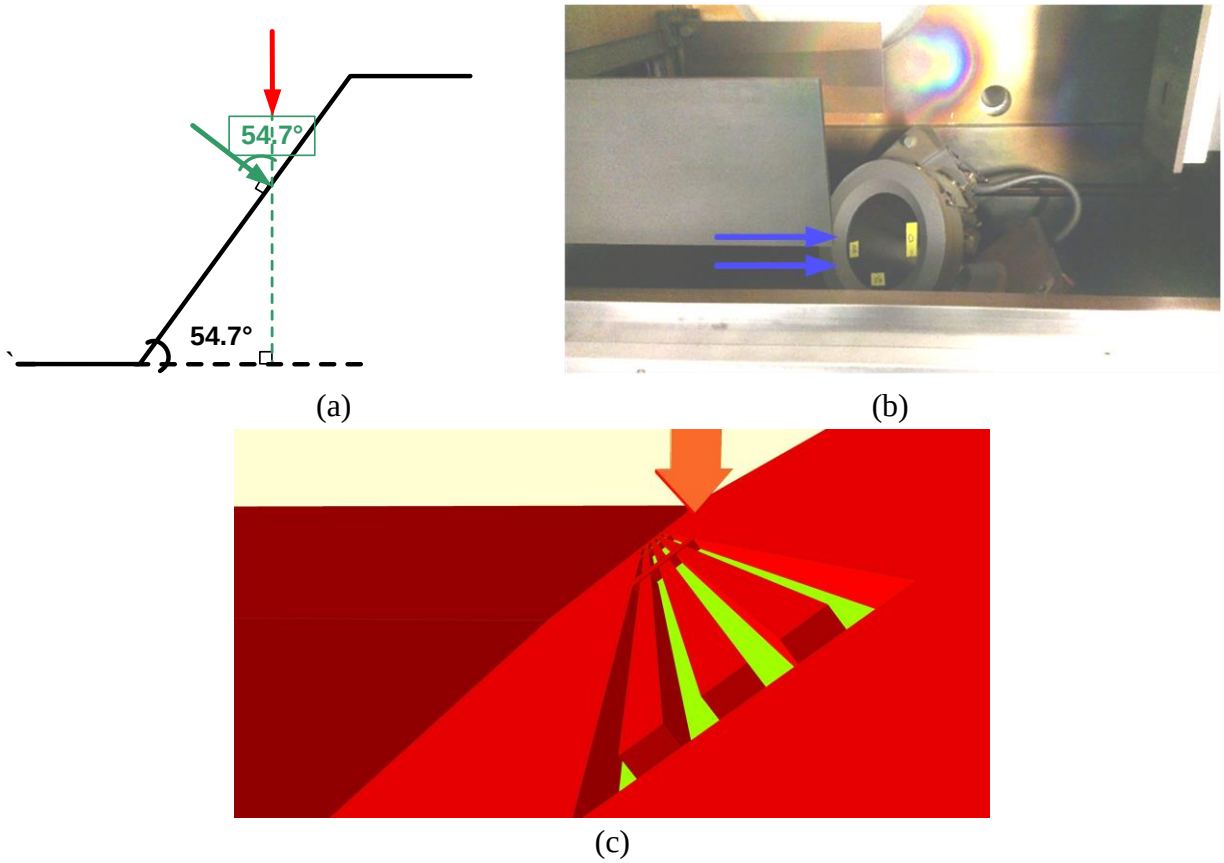
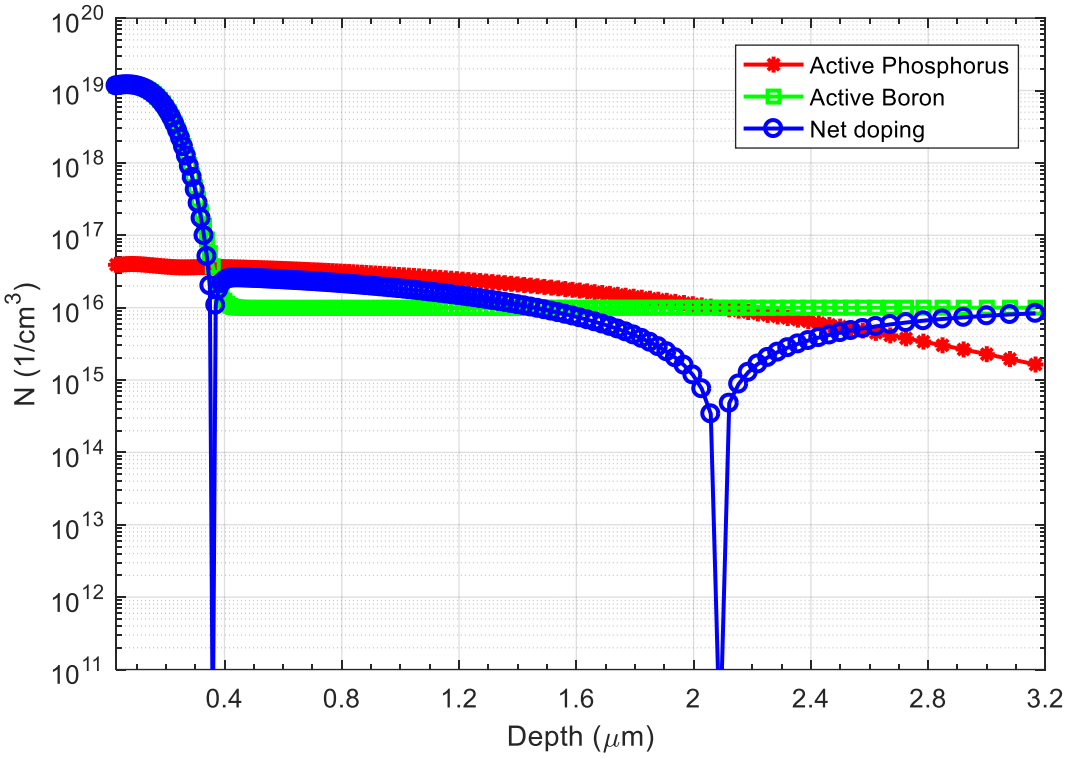


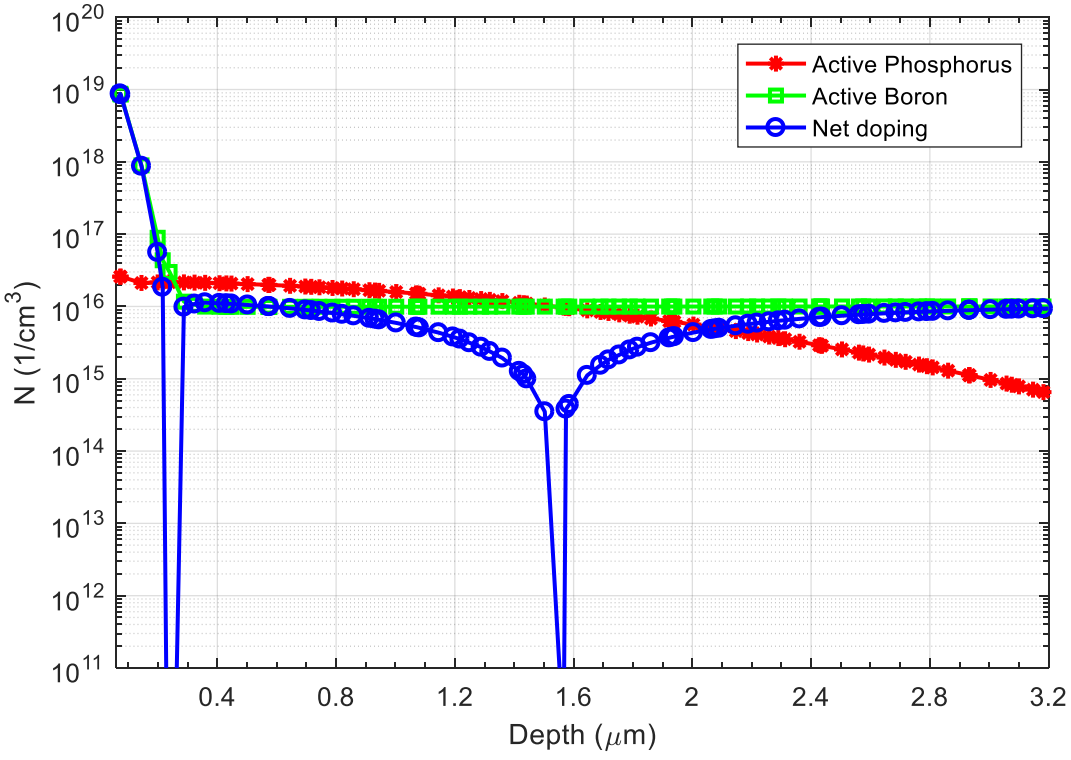

*Figure 7-6: (a) Implantation direction on the cavity sidewall: the standard and modified directions are shown with red and green arrows, respectively, and (b) a photo of tilted wafer in implanter setup. It was 55° tilted and twisted 90° for first angular implantation. The arrows show the direction of the ions. (c) The 3D schematic of thick resist sidewalls (shown in red) that cause shadowing effect of dopants on multi-stripe implantation areas in case of standard process.*

### 7.3.2 Implantation

In a planar implantation, the dopant bombardment occurs approximately in the perpendicular direction to the surface (usually small tilting, 7 degree, is applied to avoid dopant channeling). For the sidewall photodiodes, we should take into account that perpendicular implantation will enter the surface with 35° angle instead of 90° (see red arrow in Figure 7-6(a)). To see the corresponding effect on the junction depth and so the photodiode selectivity, doping profiles were simulated for SP area on the NW. Figure 7-7(a) shows the doping profile for (1 0 0) plane, top plane and bottom of the cavity (the junction depth is at 330 nm). This is the appropriate depth for max blue light selectivity of the photodiodes [6], as previously explained in Chapter 3. Figure 7-7(b) displays the doping profile for (1 1 1) plane, which is the cavity sidewall. It is observed that the junction depth is 0.6 times of the intended value and will affect the sensor performance.




(a)




(b)

*Figure 7-7: Simulated implantation profile on (a) (1 0 0) plane that is the top plane, and (b) (1 1 1) plane that is the same as the cavity sidewall.*

The thick resist sidewall may also mask dopants to enter small windows. This can

considerably change effective junction area, which is responsible to absorb the light, and so reduce the final sensor responsivity. To have a better vision, Figure 7-6(c) shows schematically the resist thick sidewall surrounding multi-stripe structures.

To avoid such issues, angular implantation is suggested. Thus, the normal implantation was primarily done for the top and bottom plane devices and then angular implantation was performed for the sidewall diodes. To do so, the wafer is 55° tilted before the implantation. The new direction is shown with green arrow in Figure 7-6(a). Considering the direction of the 2 involved sidewalls, the wafer is primarily twisted 90° and half dose implantation is done. For the opposite sidewall, it is twisted 180° more and the second half dose implantation is done. The dose is divided to 2 equal portions each for one of the opposite sidewall that includes the diodes. These opposite sidewalls can be observed in Figure 7-2(c). Figure 7-6(b) shows a photo of the wafer tilted 55 degree in the implanter setup.

This special implantation can just be applied for SP layer, because the upper P-N junction of the diodes is formed between SP-NW areas and is the responsible one for detecting blue/UV light. It also helps save the process simplicity. It is worth mentioning that the sidewall features in NW and SN layers are rather large and not so sensitive.

### 7.3.3 Process Details

The process started with double-side polished P-type wafers. For better control over threshold voltage of CMOS, a 2 µm epi layer was grown on the front side with boron doping of 1E16 atoms/cm$^3$ at 1050 °C. Alignment markers were then patterned on both side of the wafers for further HAR lithography. In the next step, KOH cavities should be formed. The mask layer was 300 nm low stress $Si_3N_4$ deposited with LPCVD, then patterned and etched with plasma etching. The cavity etching was done in 33% KOH solution at 85 °C. The final cavity depth was (200 ± 2) µm. For better surface quality (less roughness), different solutions (TMAOH and KOH) with/without added surfactant were tested [7], but a fresh KOH solution showed the best results in our case. Next, the nitride layer was stripped in phosphoric acid.

In the second phase, implantation areas (NW, SN and SP) were formed. To do so, firstly, a 20 nm dirt barrier oxide layer was thermally grown. For resist, spray coating was used due to high topography (the details and principles are described in Chapter 6). The wafer was first

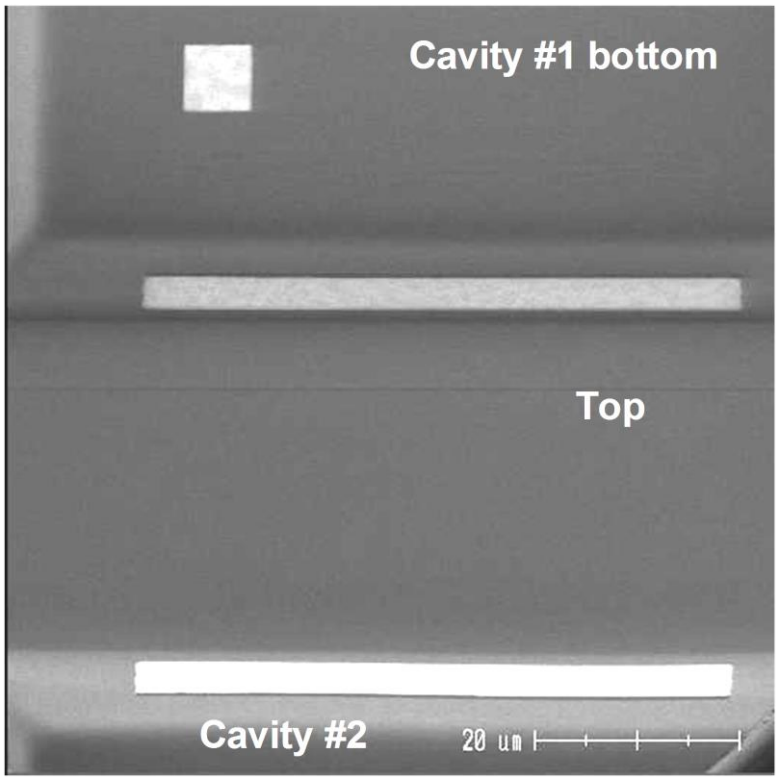
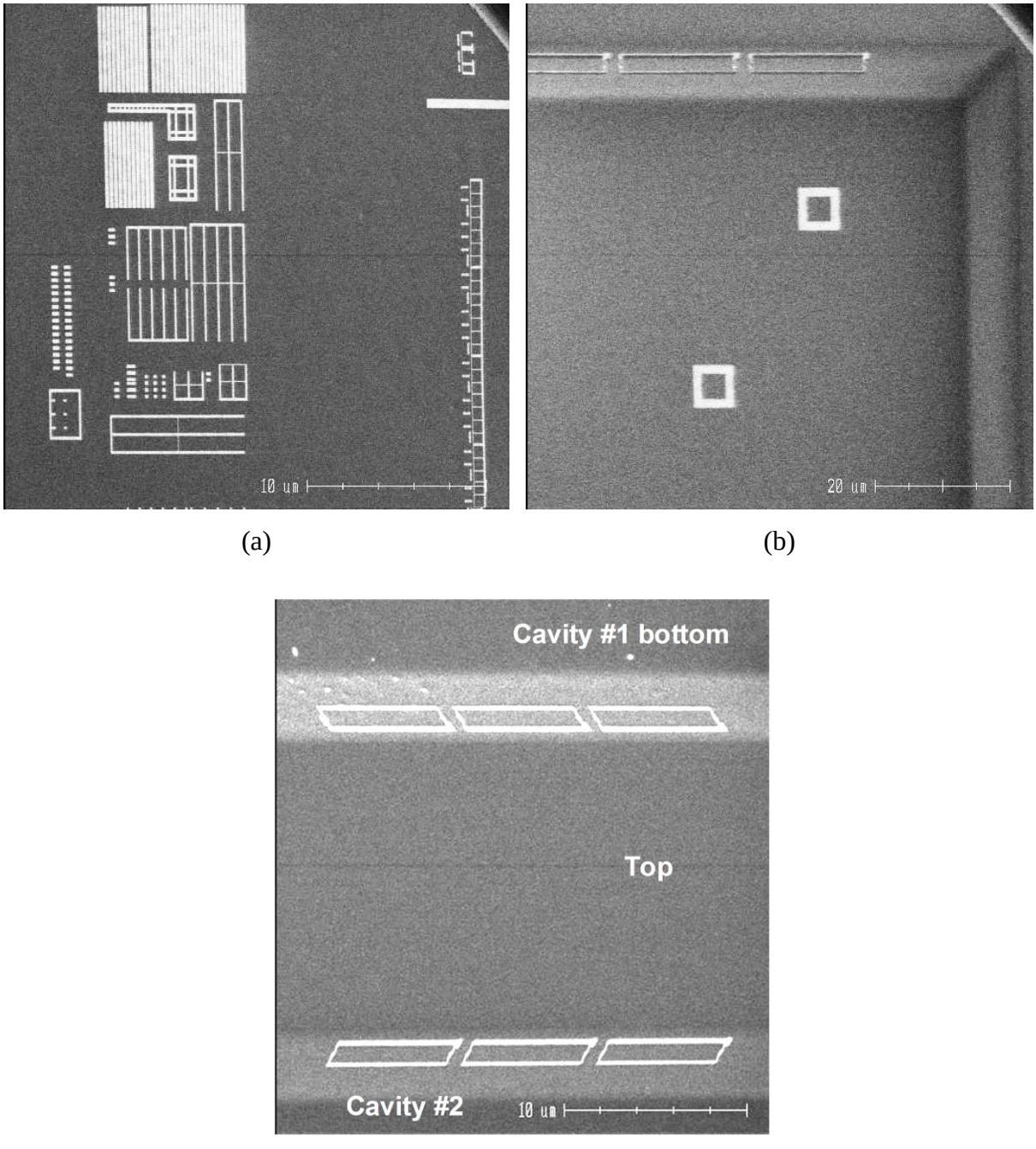



*Figure 7-8: SEM image of resist patterns for NW areas formed on bottom and sidewall of 2 cavities from top view.*

pretreated with HMDS vapor. Then, 8 layers of diluted positive resist (AZ® 9260) was sprayed in EVG 101 spray coater. The wafer was then baked at 115 °C for 1 min. Another 8 layers were sprayed and again baked at 115 °C for 5 min. To pattern NW areas, the N-wells of the PNP diodes and PMOS transistors, MSI lithography was performed in 4 focus layers, top, layer 2, layer 3 and bottom. This was followed by a phosphor implantation and a deep diffusion. Figure 7-8 displays the SEM image of the NW areas on the cavity sidewall and bottom from top view.



After a deep diffusion step, previous oxide layer was stripped and another 20 nm dirt barrier layer was formed with thermal oxidation. The third litho step was used to create the SP regions: the base of the NPN, the upper $P^+$ area of PNP diodes, the source and drain of the PMOS transistors and the isolating rings around the NMOS transistors. They were doped using a shallow boron implant. The fourth litho step was for the SN areas, highly doped shallow N-regions. They were used for the emitter and (contact regions of) collector of the NPN transistor, contact region to NW of PNP diodes, the source and drain of the NMOS, and the isolating ring around the PMOS. This was performed by a shallow arsenic implantation. The litho steps were done with the same procedure as NW. Figure 7-9(a- c) and Figure 7-10(a-b) depict the SEM



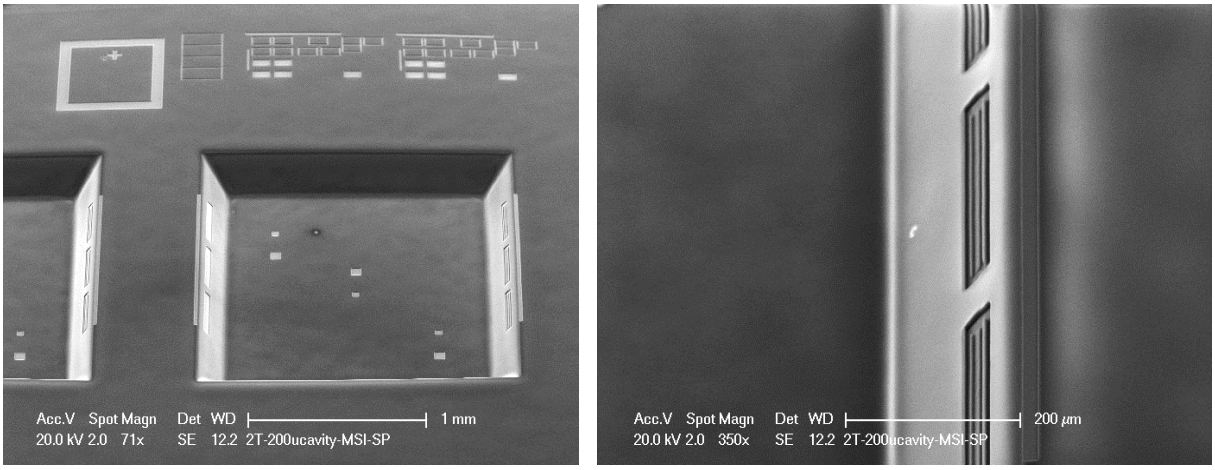

(a) (b)

(c)

*Figure 7-9: SEM images of resist patterns for SN areas formed on (a) top, (b) bottom, and (c) sidewall of cavities from top view.*

images of the patterned areas for SN and SP, respectively.

In additional step, two extra implantations were done for threshold voltage adjustment. They were low dose boron implantation (3.0E11 and 6.0E11 ions/cm$^2$) at right and bottom half of the wafer, made 4 quadrants with 4 different doping doses (0, 3.0E11, 6.0E11, and 9.0E11 ions/cm$^2$).




(a) (b)

*Figure 7-10: SEM images of resist patterns for SP areas: (a) formed on top, bottom and sidewall of 200 µm cavities with 26 degree tilt, and (b) magnified image of multi-stripe SP structure on the sidewall.*

After this step, the wafer was annealed/oxidized for 10 minutes at 1000 °C and the surface got an isolation layer of 100 nm of silicon dioxide (by thermal oxidation). This layer will act as an isolation layer between the first interconnect layer and the substrate as well as the gate material of the PMOS and NMOS transistors.

The fifth litho step was used to make the contact openings in the isolation layer. This litho was done in 3 focus layers; top, layer 2 and bottom. In this step, we encountered a new challenge with HAR patterning that was poor adhesion of spray coated resist to the thermal oxide (see Figure 7-11(a-c)). Especially on top plane, for contact openings of the power transistors, the resist detached the surface during development.

For process optimization, the additional treatment was applied to the wafer surface. It was first cured with 1000 Watt oxygen plasma for 5 min and next, the HMDS vapor treatment time was tripled. Besides, the annealing time after two step spraying was increased to 3.5 min and 10 min, respectively. Figure 7-12(a-d) show the SEM images of the patterned areas for CO after the optimization. The windows were then etched using buffered HF solution.

The sixth litho step was utilized to pattern IC1, the first interconnect layer. This was the first metallization step for the contact openings and locally connecting different components. It also formed the mirroring layer on the cavity sidewall as it was designed to fill the area that was not used for sensors and wires. This can significantly improve the light reflection from the sidewalls

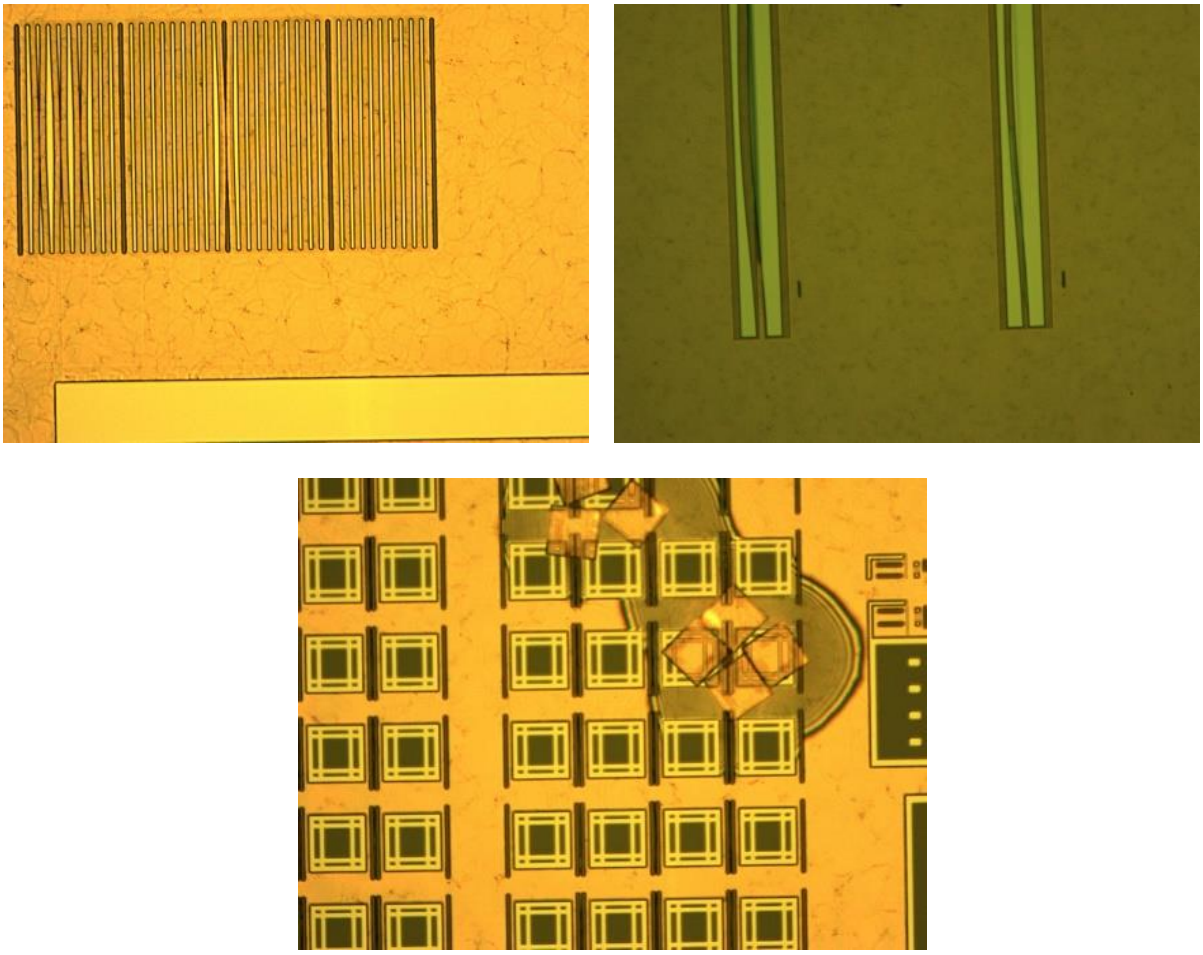


*Figure 7-11: Optical microscope images of CO resist patterns suffering from poor adhesion of spray coated resist on thermal oxide layer.*

and so output efficiency of the package.

Immediately after a dip etching in 0.55% HF solution, 300 nm AlSi (1%) was sputtered on the surface at 350 °C (the target existence of 99% Al and 1% Si). IC1 is the only layer that traveled all the way from top to the bottom. Again, the spray coated resist showed poor adhesion to Al. To solve this issue, before the spray coating, a thin layer of SPR3012 resist (from Shipley Company) was spin coated on wafer surface with high spin speed of 5000 rpm. It came from our previous tests with spin coating of SPR3012 that showed a very good adhesion behavior on aluminum. Figure 7-13(a-f) represent the SEM images of the patterned IC areas after the optimization.

Before etching, the patterned wafer was baked at 120 °C for 1 hour for better resist adhesion during the etching. Then, the aluminum traces were etched with wet etching process. It was explained in previous chapter that due to the thin resist coverage over the top corners, dry etching

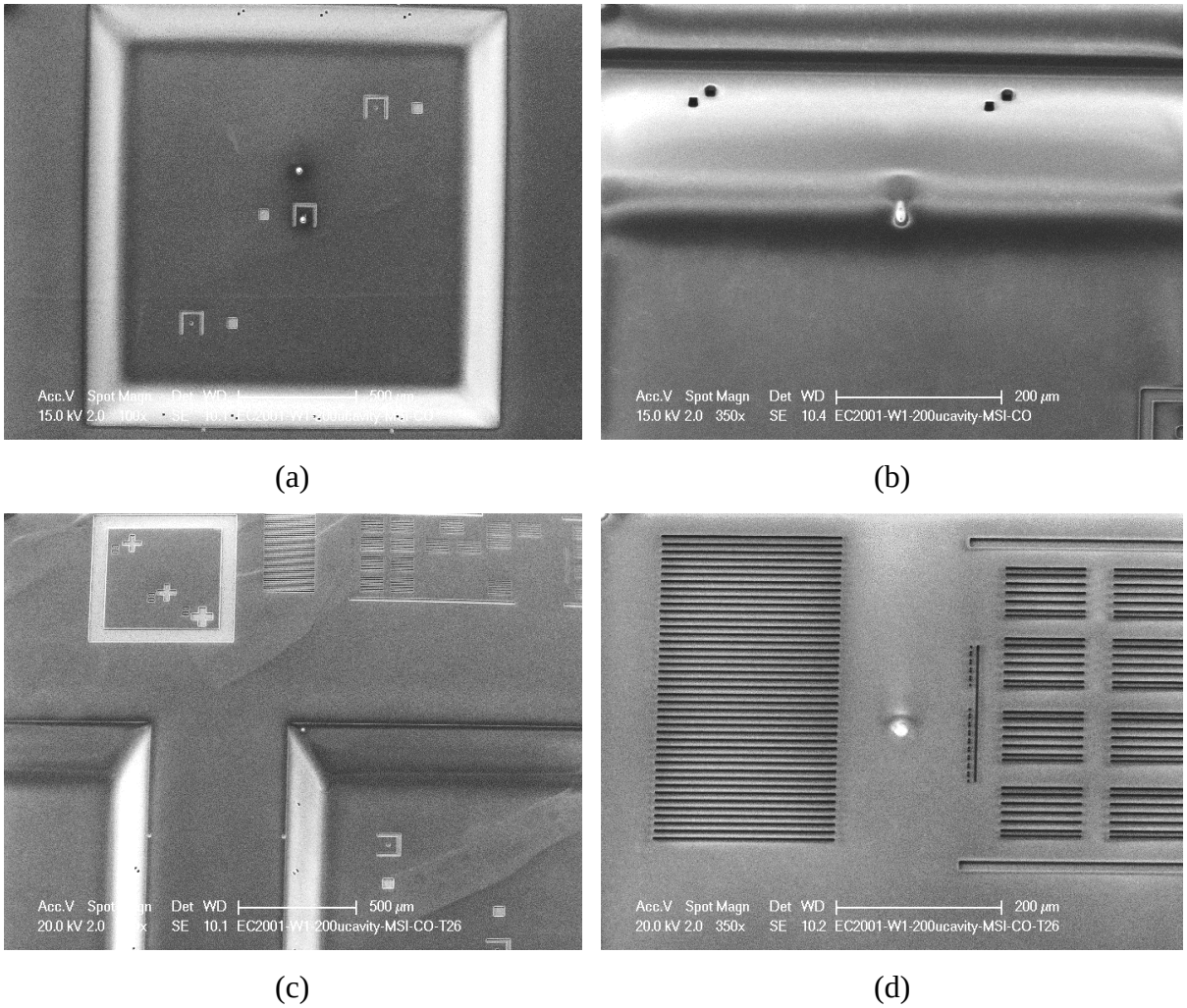
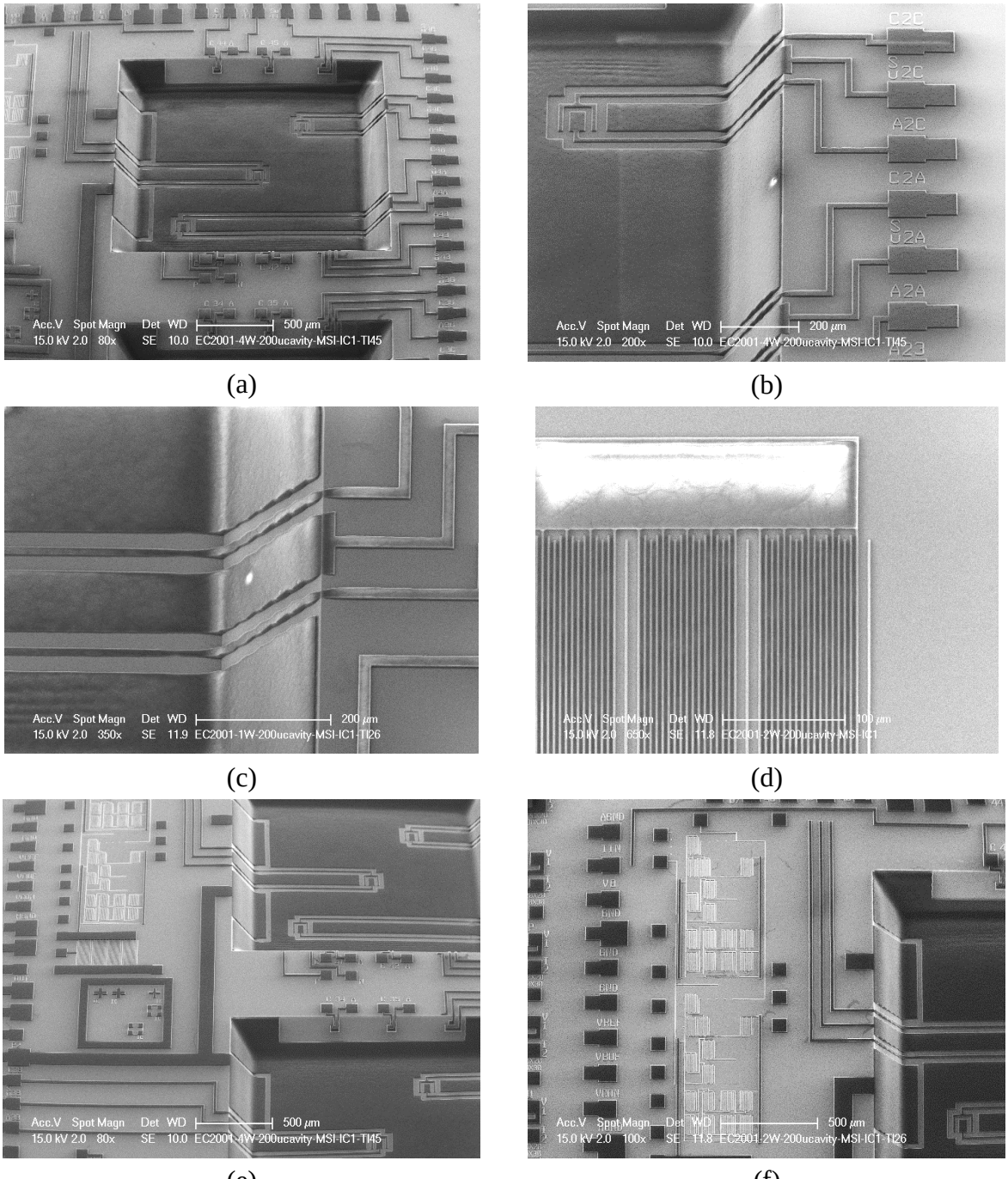



*Figure 7-12: SEM images of CO resist patterns formed on top, bottom and sidewalls of 200 µm cavities, from top view: (a) a cavity with open windows on the bottom and sidewalls, (b) magnified image of windows on the cavity sidewall, with 26 degree tilted view: (c) patterns on 3 surfaces, and (d) CO windows with small features on top with good resist adhesion.*

7

is problematic. After the wet etching, a poly silicon dip etch (30 seconds) was performed to remove the poly-Si grains that might be deposited on the wafer surface. Figure 7-14(a-d) display the SEM images of the etched aluminum traces.

The next layers were just patterned on the top plane as previously shown in Table 7-1. For isolating two metal layers, 200 nm CVD oxide was deposited. The seventh litho step was for patterning the vias between metal 1 and 2. Then, 2 µm AlSi (1%) was sputtered at 50°C as the second metal layer. The eighth and final mask was for patterning the second interconnect layer. The process is finished with final alloying at 400 °C. Figure 7-15(a-b) show the optical microscope images of the final cavity with all the layers. Figure 7-15(c) depicts a photo of full



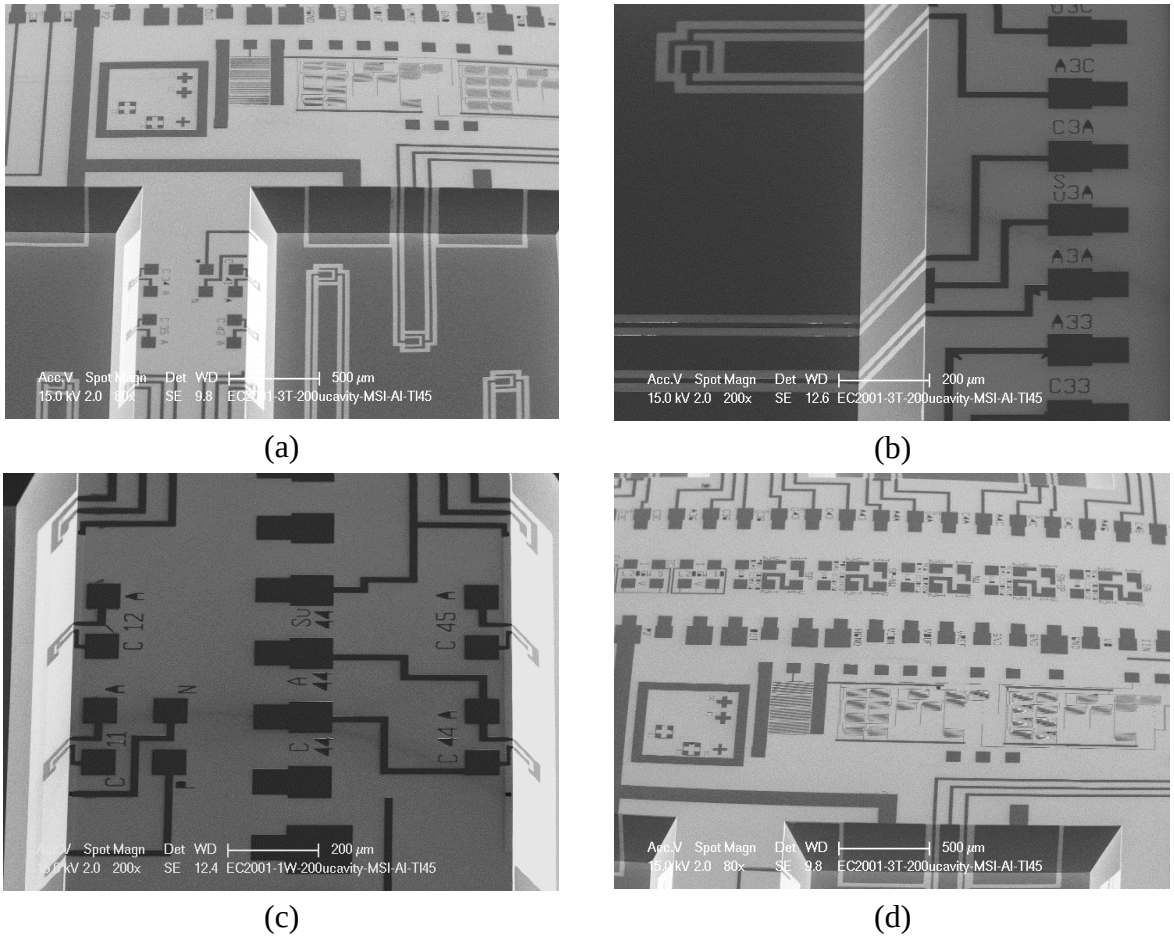

(a) (b)

(c) (d)

(e) (f)

*Figure 7-13: SEM images of resist patterns for IC1 layer formed on top, bottom and sidewall of 200 µm cavities, (a) a cavity with wires to sensors at the bottom and sidewall and LED chip connection wires (45 ° tilted view), (b) magnified image of wires going to the cavity bottom for the bottom temperature sensor, (c) a closer view to the resist HAR pattern and effect of the split focus layers (26 ° tilted view), (d) top view of a power transistor on top plane, (e) the feedback control circuit and the active reflector cup with 45 ° tilted view, and (f) small features from top to the bottom of the cavity with 26 ° tilted view.*

wafer after the last step.




(a) (b)

(c) (d)

*Figure 7-14: SEM images of first aluminum traces formed on top, bottom and sidewall of 200 µm cavities, with 45° tilted view: (a) a cavity with wires to sensors at the bottom and sidewall and LED chip connection wires (b) connections to the bottom temperature sensors, (c) connections to the sidewall light sensors, and (d) control circuits and pads on the top plane.*

## 7.4 Implementation and Measurement Results

Temperature and light sensors are two main sensing elements in the package. Light sensors are located close to each LEDs on cavity sidewalls with good line of sight for the emitted light to accurately estimate the output light. Temperature is known as one of the challenging parameter for monolithic integration of electronics in such a LED package. It may cause severe effects on the performance of both LEDs and other electronic components in the package. So, three temperature sensors were located at the bottom of the cavity and beneath each LED die for in-situ investigation.

### 7.4.1 Bottom Temperature Sensor

The sensors were electrically characterized on the Cascade probe station. The IV

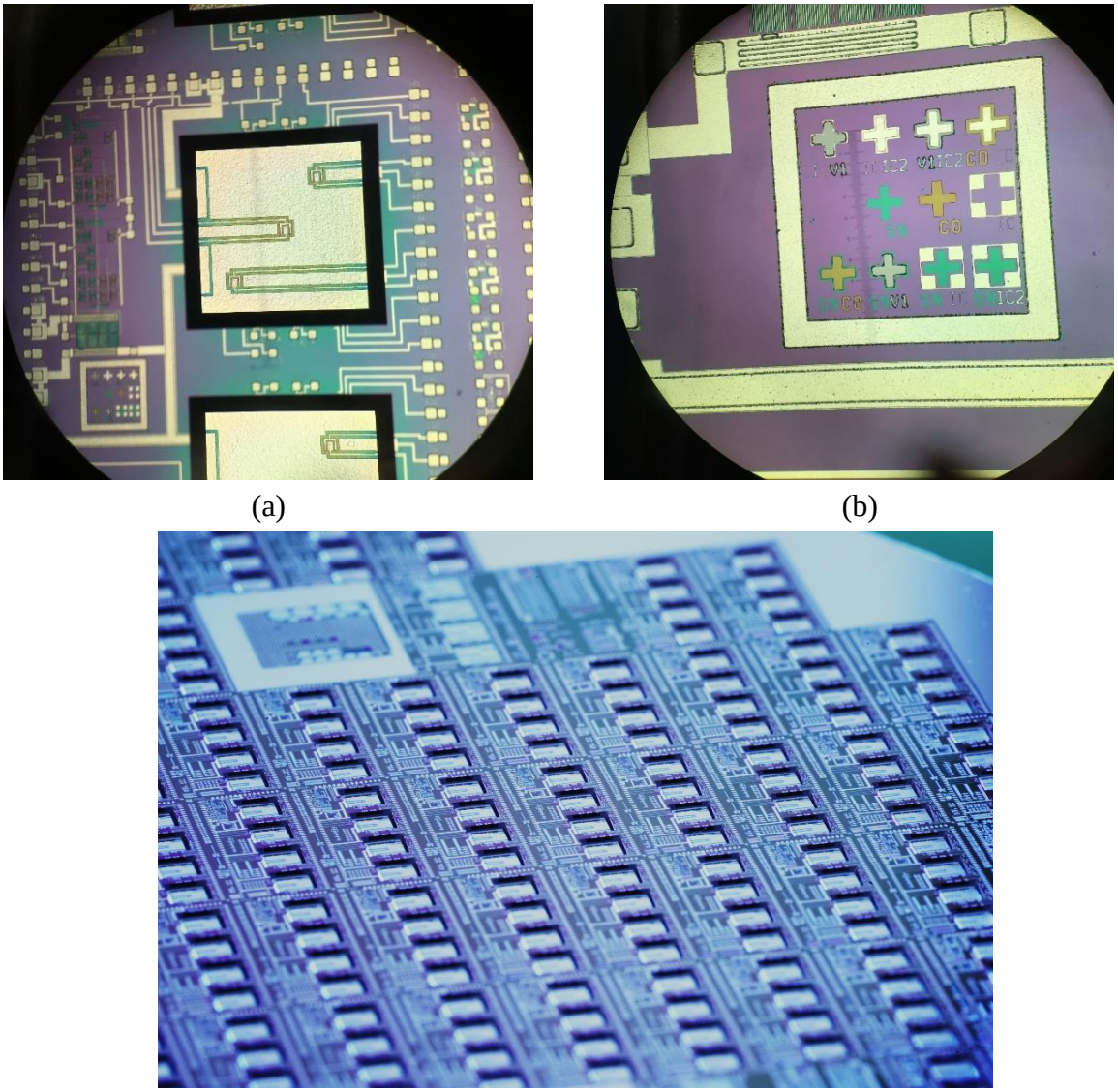


*Figure 7-15: Optical microscope picture of (a) cavities with via and IC2 patterning, (b) different layer optical alignment markers in the last step. (c) A photo of full wafer after the final process step.*



characteristic of the temperature sensors was extracted with external temperature controller. Lower N-P junction was grounded and anode voltage was swept between -4 to 2 V. Figure 7-16(a) shows the IV characteristic at different temperatures from 25 to 150 °C.

At constant forward driving current, the voltage drop over the upper P-N junction can be considered as the linear function of temperature (so called one point technique [8])

$$V_{f_{|I_f}} = \alpha\, T_j + \beta, \tag{7.1}$$

where $\alpha$ and $\beta$ are calibration parameters obtained from measurements at two known temperatures and voltages ($V_f$) at the same forward current $I_f$. In this case, we chose the forward

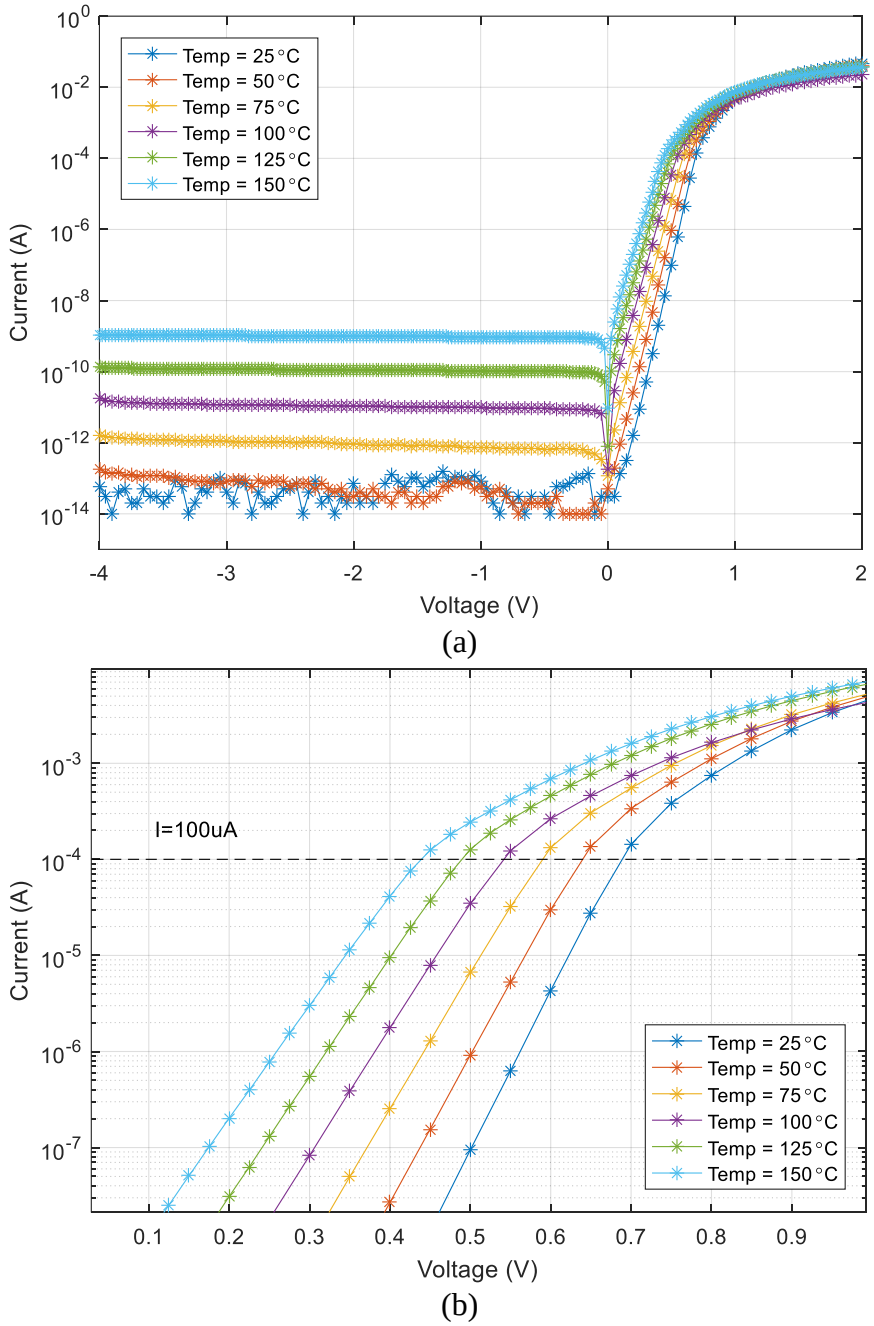



*Figure 7-16: (a) IV characteristic of the bottom temperature sensor at different temperature, and (b) forward bias data enlarged around forward current of 100 µA to study linear behaviour of the sensor.*

voltage data recorded at $I_f$ = 100 µA (see Figure 7-16(b)). The measured results and corresponding fitted line are plotted in Figure 7-17.

It can be observed that despite rather rough surface of the etched Si at bottom of the cavity, the result is quite linear.

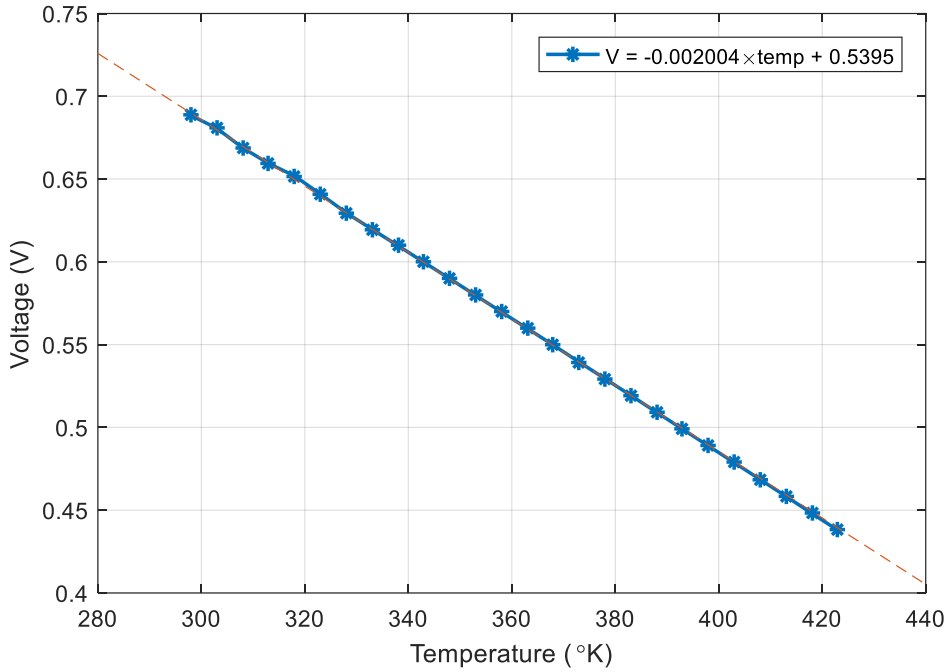


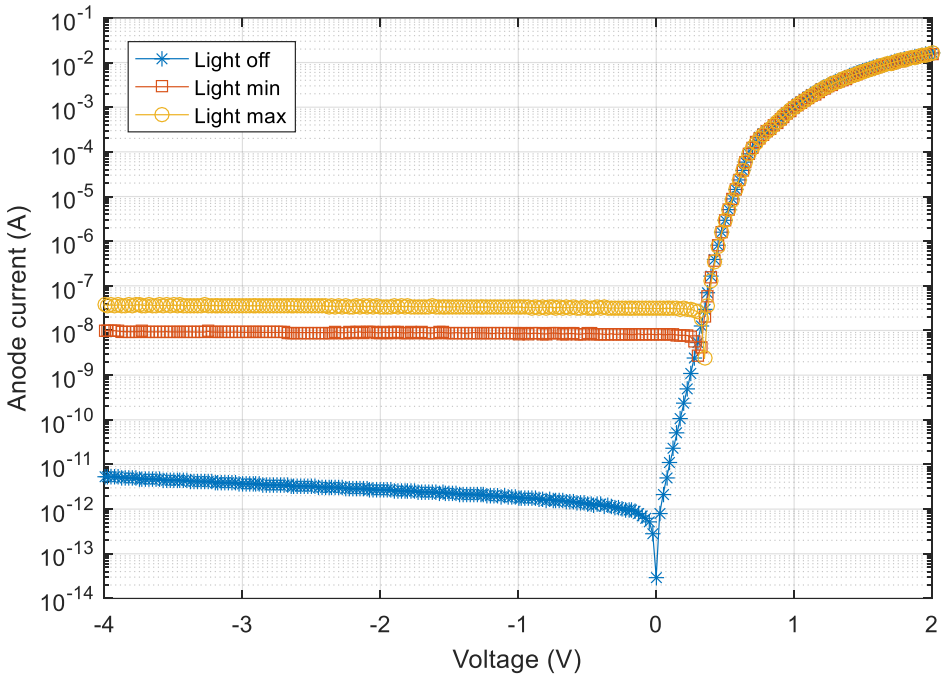

*Figure 7-17: Forward P-N junction voltage versus temperature and corresponding fitted line.*

### 7.4.2 Sidewall Photodiode

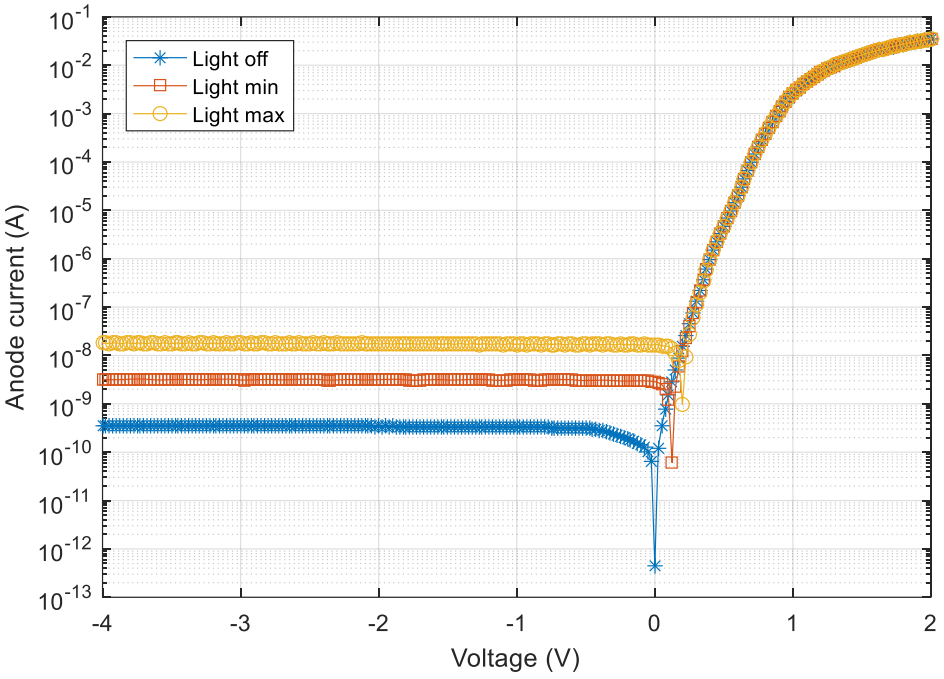
For each LED, two sets of photodiodes were used to measure output light, striped anode and single anode versions. The initial characterization of the sensors was done using cascade white light source. This is a non-calibrated source but can help us to study the sensor behaviors. Further accurate measurements can be added to calculate the sensor responsivity and selectivity. The measurement was done with dark condition, minimum and maximum light of the source. Again, the lower junction was grounded and anode voltage was swept between -4 to 2 V. Figure 7-18(a-b) depict the result for both configurations.

For striped anode structure, when light is “off”, the reverse current value is 1 pA. Current measurement showed almost 4 orders of magnitude increase when the light became on. This difference is governed by the generation of lots of electron-hole pairs in the active part of the device and a numerous recombination dominantly close to the surface.

For single anode structure, dark current is 250 nA, 80 times of the one for striped anode. It can be explained due to the higher current cross-section area and more surface defects. However, multi-stripe device showed a 2.9 times improvement in the output current under similar light illumination compared to the single anode one, which is a proof of concept for the significance of the dead layer and active depletion region [6]. The single anode structure, due to higher rate




(a)




(b)

*Figure 7-18: IV characteristic of the sidewall photodiodes at different light levels of the cascade light source, (a) for striped anode structure, and (b) for single anode structure.*

of recombination caused by the dead layer formation, showed lower responsivity compared to multi-stripe shaped one.

### 7.4.3 Planar Devices

The rest of the devices on the top plane were exactly implemented the same as the 2D

package. The only concern is higher leakage current of the CMOS transistors that can be due to different implantation and other process variations in 3D implementation.

## 7.5 Conclusions

A 3D silicon demonstrator was designed and fabricated for smart wafer level packaging of phosphor based white LED module. It integrates different planar control blocks in addition to an on chip active reflector cup, which can improve light output efficiency of the package. The cup was implemented with a 200 µm KOH cavity coated later with a thin aluminum layer to form mirroring sidewall. Furthermore, temperature and light sensors were fabricated on the cavity bottom and sidewall, respectively. The wires for LED driving current and sensor connections were patterned the whole way from the top surface to the cavity bottom. Different challenges and solutions for 3D implementation were described. The main process challenge was HAR lithography which was resolved using multi-step imaging on wafer stepper. The fabrication process was modified BiCMOS7 with 2 µm gate length. This new process enabled integration of different sensors and transistor on top plane, cavity sidewall and bottom. It also provides integration of large area LED chips with other functional devices. Different sensors were characterized. The bottom temperature sensor showed linear behavior of forward voltage versus package temperature at constant forward bias current. Two configuration of sidewall photodiode were studied. The sidewall photodiodes with multi-stripe anode, with shallow P-N junction, demonstrated a high responsivity to the emitted light.

## 7.6 References

[1] J. K. Kim and H. C. Lee, "MSM Photodetector on a Polysilicon Membrane for a Silicon-Based Wafer-Level Packaged LED," *IEEE Photonics Technol. Lett.*, vol. 25, no. 24, pp. 2462–2465, 2013.

[2] J. K. Kim and H. C. Lee, "A photo-sensor on thin polysilicon membrane embedded in wafer level package LED," in *Proceedings of the SPIE*, 2012, vol. 8431, pp. 8431–7.

[3] W. K. Jeung, S. H. Shin, S. Y. Hong, S. M. Choi, S. Yi, Y. B. Yoon, H. J. Kim, S. J. Lee, and K. Y. Park, "Silicon-Based, Multi-Chip LED Package," in *2007 Proceedings 57th Electronic Components and Technology Conference*, 2007, pp. 722–727.

[4] C. T. Tsou and Y.-S. Huang, "Silicon-Based Packaging Platform for Light-Emitting Diode," *IEEE Trans. Adv. Packag.*, vol. 29, no. 3, pp. 607–614, Aug. 2006.

[5] S. W. R. Lee, R. Zhang, K. Chen, and J. C. C. Lo, "Emerging trend for LED wafer level packaging," *Front. Optoelectron.*, vol. 5, pp. 119–125, 2012.

[6] Z. Kolahdouz, A. Rostamian, M. Kolahdouz, T. Ma, H. Van, and K. Zhang, "Output blue light evaluation for phosphor based smart white LED wafer level packages," *Opt. Express*, vol. 24, no. 4, pp. 174–177, 2016.

[7] C.-R. Yang, C.-H. Yang, and P.-Y. Chen, "Study on anisotropic silicon etching characteristics in various surfactant-added tetramethyl ammonium hydroxide water solutions," *J. Micromechanics Microengineering*, vol. 15, no. 11, pp. 2028–2037, Nov. 2005.

[8] M. M. Moslehi, "United States Patent," 5,436,494, 1995.

# Chapter 8

# Conclusion

In this dissertation, design, modeling, and implementation of a fully integrated 2D and 3D smart package for LEDs, including the local active reflector cup and controlling circuit, in 2D and 3D BiCMOS process are discussed. We have now arrived at the final chapter of this work. Section 8.1 summarizes the thesis and also repeats the accomplishments achieved throughout the thesis. Finally, Section 8.2 proposes some suggestions in order to expand this work.

## 8.1 The Thesis Outcome

In Chapter 2, the BICMOS5/7 process was introduced. It is a straightforward process that by just using 5-7 mask steps (corresponding to 1-2 metal layers) can monolithically implement different devices such as MOSFETs, BJTs, diodes, and resistors. Due to large die size of LED chips, BiCMOS5/7 has a large potential to be utilized for wafer level packaging of smart LED systems. A design and fabrication framework based on BICMOS process was suggested. This framework covers the whole process from device modeling to system fabrication and measurements. It can be well applied for circuit design based on BiCMOS process.

Chapter 3 reported a successful integration of different functions appropriate for a phosphor-based white LED wafer-level package (WLP) and also any blue/UV LED. Silicon-based WLP through low cost 7-mask BiCMOS process, gives us the opportunity for integration of different passive and active components for a complete smart system. For sensing functions, thermal and optical sensors were implemented, characterized and calibrated. Light measurement of the LED chip through the blue selective photodiode showed notable consistency to the LED datasheet

values. Temperature sensors integrated just beneath LED chips, measured the temperature in real time and the results were confirmed with IR photos. For controlling functions, a 4-bit flash ADC for reading out sensing output light, and a power switch for driving the LED current were monolithically integrated. The ADC functionality was successfully tested with better than 0.16 LSB accuracy and the power transistor could provide more than 700 mA current. The reported components provides an essential platform for future work to have an analog or digital control system for any specific application. Furthermore, other technologies with large area demands such as Lab-on-Chip can benefit from this approach by utilizing smart silicon interposers.

In Chapter 4, details and design concept for the blue selective photodiodes were elaborated. A silicon stripe-shaped photodiode was designed and fabricated for sensing blue light in LED wafer level package. The device dimensions and doping were also designed and simulated using COMSOL Multiphysics. The maximum responsivity was at 480nm, which is matched with the blue LED's illumination. The single anode structure due to higher rate of recombination (caused by dead layer formation) showed lower responsivity compared to multi-stripe shaped one. This IC technology compatible photodiode, with junction at 330 nm, demonstrated a very high selectivity to blue light. The fabricated device presented a two-fold increase in the responsivity and quantum efficiency for blue light spectra compared to similar devices published earlier.

In Chapter 5, a successful monolithic integration of light output feedback control circuit in a blue/UV LED package was presented. It is also an appropriate solution for packaging a phosphor-based white LED module. Si-based wafer level smart control unit was integrated through our low-cost 7-mask BiCMOS process. For sensing blue/UV light in the package, the photodiode with its peak responsivity at 480nm wavelength were reused. For controlling functions, a feedback circuit with a power transistor for driving the LED current were monolithically integrated. The opamp functionality was successfully tested with having 47 dB gain. The whole feedback circuit could regulate light output based on a reference voltage with removing power supply ripples even at very high frequencies (up to 680 kHz). Robustness of the feedback system was tested against changes in LED current/voltage to light intensity characteristics, which can be caused by aging or temperature changes. Considering a tight error tolerance of 1% for the light intensity, the system was able to handle up to 150 mA and 0.6 V change in current and voltage characteristic of the LED. Furthermore, it demonstrates the

functionality of silicon based smart LED packaging with stable and regulated light output. This can also be applied to other smart systems like interposer for high level electronics, MEMS, etc.

In Chapter 6, “lithographic defined lateral wire bonding” was introduced as a new approach to overcome limitations and challenges of conventional wire bonding for special applications. It includes metal film deposition and patterning the wire trace through high aspect ratio (3D) lithography, which is the main key for such a method. Different challenges and process details were discussed. Two sets of experiments were done to make various line structures over KOH cavities of different depths up to 200 µm. Multilayer spray-coating was used to have a good resist coverage over deep cavities. Exposure was done with mask aligner and multi-step imaging on an ASML PAS5500/80 projection aligner. Aluminum interconnect lines with different parameters were achieved after etching process. For sidewall imaging of wires using multi-step imaging (MSI) on stepper, a simulation method was proposed to predict 3D aerial image projected on the resist. As experimental results showed, only the aerial image was not enough and other parameters such as resist thickness profile and its sensitivity should be considered. Including these, the final simulation methodology was able to predict accurately the final resist profile on 3D structures. The MSI with single mask was also experimentally investigated, but it was very challenging for high resolution features and a pattern depending method. Lastly, MSI with split masking was developed. It showed promising results for high resolution and generic patterns. This method can be applied for heterogeneous integration areas, where a reliable and flexible interconnection method is critical.

Finally, in Chapter 7, a 3D silicon interposer was designed and fabricated for smart wafer level packaging of phosphor based white LED module. It integrates different planar control blocks in addition to an on chip active reflector cup, which can improve light output efficiency of the package. The cup is implemented with a 200 µm KOH cavity coated later with a thin aluminum layer to form mirroring sidewall. Furthermore, temperature and light sensors were fabricated on the cavity bottom and sidewall, respectively. The wires for LED driving current and sensor connections were patterned the whole way from top surface to cavity bottom. Different challenges and solutions for the 3D implementation were described. The fabrication process was modified BiCMOS7 with 2 µm gate length. This new process enables to integrate different sensors and transistor on top plane, cavity sidewall, and bottom. It also provides

integration of large area LED chips with other functional devices. Different sensors were characterized. The bottom temperature sensor showed linear behavior of forward voltage versus package temperature at a constant forward bias current. Two configurations of sidewall photodiode were studied. The sidewall photodiodes with multi-stripe anode, demonstrated a high responsivity to the emitted light. This is for the first time that a functional active device is fabricated on the sidewall of a silicon cavity.

The suggested smart Si- based interposer is not only applicable for LED WLP but for broad range of applications especially the ones with large area devices. It can monolithically integrate different performance monitoring and controlling blocks, in a low cost/area process line, which make a smart interface for the main device.

## 8.2 Suggestions for Future Developments

The findings of this dissertation indicate that the silicon based demonstrator will be the proper approach of choice for future development of commercial wafer level packaging for LEDs.

- As showed in this dissertation, many active and passive devices can be monolithically integrated through low cost BiCMOS process that can be a promising method for full integration of LED drivers in such a wafer level package. However, integration of on chip capacitors is still a challenge. Enhanced surface capacitor using nano structure on wafer backside can be a big step for full driver integration. Previous works suggested use of carbon nanotube to increase electrode surface. But to keep the processing temperature in the safe area for front side circuits and devices, doped Zinc-Oxide nanowires can be a possible solution. Rather low temperature growing process (90 °C) is a good motivation to save the large unemployed area of wafer backside for capacitor integration.
- UV LED's have been in the point of interest for large variation of applications such as medical and scientific areas, due to their outstanding features of low power, long and reliable lifetime, and premeditated wavelengths. However, their packages suffer from several critical drawbacks, which limit the product desired performance. Low package efficiency and weak thermal management seem to be the bottlenecks. More developments for such systems are needed in terms of: increasing the output light

efficiency by minimizing the absorption and loss of UV light in the package, promotion in the quality and work conditions of the UV LEDs, and reduction in the production and utilization costs. The idea of 3D full wafer level packaging of LED chips can be specially extended for ultraviolet LEDs (UVCs). The main motivations are: 1) the cost per chip of this LED's are relatively high (e.g.100 €), 2) the applications are normally sensitive, and 3) light output efficiency of the existing packages is reported very low. 3D integration approach for a multifunctional package is a promising way for further package improvement. Our proposed package can be modified for best fit to UVC applications.

- The proposed lithographic-defined wire bonding (LDWB) is particularly suitable for high-wire density and special demand applications, such as digital and RF chips. Multi-step imaging solution with split masking layer is the first but time consuming approach. Applying special mask design method such as holographic lithography in combination with MSI can lower the number of imaging and save the cost. Holographic lithography was previously suggested for contact/proximity exposure for limited patterns, but developing this method for projection lithography in combination with MSI capability can be a big step forward in commercialized LDWB.

# Summary

LEDs are believed to dominate all lighting applications in near future. However, integration and packaging are two of the critical issues that resolving them enables efficient and reliable solutions for lighting requirements. Among different packaging schemes, wafer level packaging is a promising method to have a lower cost, higher scale, and superior yield.

In this dissertation, a new integration approach for LED lighting is introduced: smart LED system in package (SiP). It combines a smart LED wafer level package (WLP) and a smart driver by monolithic integration which is the focus of this dissertation. The final smart package is a high lumen output lighting module, which includes high current blue LEDs and different sensors in a reflector cavity. Silicon substrate is used as a high topography interposer for the LED WLP, in which lithography defined wiring technique is used as a reliable interconnect solution. Additionally, control circuit of the LED output light are integrated on the same die to reduce costs of any required external circuitry.

The proposed smart Si-based interposer is not only applicable for LED WLP, but also for broad range of applications especially the ones with large area devices. Generally, smart interposers can monolithically integrate different performance monitoring and controlling blocks in a low cost/area process line and make a smart interface for the main device.

In the first part of this dissertation, the principles, design and implementation of a monolithically integrated 2D LED SiP are covered. To start with (**Chapter 2**), the required low cost processing scheme is explained and design framework from modeling to measurement is established. This simple BiCMOS 5/7 (1-2 metal layers) process allows on-chip integration of different Si based sensors, functioning blocks and circuits to be used for an advanced lighting system. It is followed by description of different components for using in monitoring and

controlling blocks in the 2D system (**Chapter 3-5**). This package integrates 4 high-power blue light LED dies with temperature sensors, and blue selective light sensors for monitoring the system performance. With the same technology, an interdigitated power transistor, a 4-bit flash analog-to-digital converter, and a light feedback control circuit are also designed, integrated in the process flow and characterized. Also, in the same process flow, a light sensor, an innovative multi-stripe blue selective photodiode with a maximum responsivity for light with a wavelength of 480 nm is developed. This sensor demonstrates a very high selectivity to the target blue LED's illumination. The monolithic light feedback control circuit is an opamp-based feedback circuit combined with a high-power transistor and the blue-selective photodiode. It controls the output light based on real-time sensor data. The integrated system is characterized by simulations and measurements and guarantees a stable and reliable output light under different working conditions and linear dimming control by a reference input voltage. This part accompanies measurement and simulation results for different components

In the second part, challenges, design and implementation of 3D system are elaborated. Primarily, a high aspect ratio (HAR) lithography approach is developed, which is a significant key for 3D processing.

"Lithographic defined lateral wire bonding" is introduced as a novel approach to overcome limitations and challenges of conventional wire bonding for special applications (**Chapter 6**). It includes metal film deposition and patterning the wire trace through high aspect ratio (3D) lithography, which is the main key for such a method. This method can be applied for heterogeneous integration areas, where a reliable interconnection method is critical. To enable high resolution 3D patterning, multi-step imaging (MSI) on projection aligner (ASML PAS5500/80) with split masking is proposed. Feasibility of the required 3D patterning in photoresist is confirmed by simulation and experiments. It demonstrates promising results for high resolution and generic patterns over high topographies (few hundred microns).

Finally, a 3D silicon interposer is designed and fabricated for smart wafer level packaging of phosphor based white LED module (**Chapter 7**). It integrates different planar control circuits in addition to an on chip active reflector cup and the final 3D package is characterized by simulation and measurements. The cup is implemented with a 200 µm KOH cavity, later coated with a thin aluminum layer to form mirroring sidewall. It uses the cavity not only as a precision

reflective LED site for its sidewall mirrors, but also as an active reflector cup. The cavity bottom contains local temperature sensors and the sidewalls carry the output light sensor in addition to the high aspect ratio (HAR) interconnects for LED driving current and sensor connections. Also, different challenges and solutions for such a 3D implementation are described. This is for the first time that a functional active device is fabricated on the sidewall of a silicon cavity. Other controlling circuit described in 2D package is also integrated on Si top surface of this package.

The achieved 3D smart Si- based interposer integrates monolithically various sensors and controlling circuits, in a low cost/area process line and with a novel high aspect ratio lithography approach.

# Samenvatting

Verwacht wordt dat alle verlichting in de nabije toekomst door Licht emitterende diodes (LED) wordt gedomineerd. Hiervoor zijn integratie en systeemverpakking twee belangrijke problemen die, indien opgelost, bepalend zijn voor efficiënte en betrouwbare LED verlichtingen. Systeemverpakking op wafer niveau (wafer level package, WLP) is een veel belovende methode om efficiënte integratie, betrouwbaarheid, maar ook hoge volume productie en hoge opbrengst, te verkrijgen.

In dit proefschrift wordt een nieuwe benadering voor de integratie van LED verlichting geïntroduceerd: slimme (smart) LED in systeemverpakking (system in package, SiP). Dit bestaat uit een slim LED WLP in combinatie met een slimme aansturing. De slimme WLP LED systeem integratie is hiermee de focus van dit proefschrift. De uiteindelijke systeemverpakking is een verlichtingsmodule met hoog lumen opbrengst, waarin hoge stroom blauwe LED's en verschillende sensoren zijn ondergebracht in een geometrisch gevormde reflectie kamer in silicium. Voor de LED systeemverpakking is een silicium substraat toegepast als basis tussenlaag (interposer) met hoge topografie (hoogteverschillen), waarin lithografisch gedefinieerde bedrading is gefabriceerd als betrouwbare verbindingstechnologie. De controle circuits voor de LED licht opbrengst zijn ook geïntegreerd in hetzelfde silicium waarmee de kosten van externe circuits worden gereduceerd.

De voorgestelde op silicium gebaseerdeslimme interposer is niet alleen geschikt als toepassing voor LED WLP, maar kan breder worden gebruikt voor toepassingen met relatief grote geavanceerde en kostbare componenten. Er kan verschillende monitor en controle circuits monolithisch worden geïntegreerd in een proces met lage kosten per oppervlak, waarmee een silicium interposer kan worden gefabriceerd als slimme koppeling voor geavanceerde

componenten.

In het eerste gedeelte van dit proefschrift worden de principes, het ontwerp en de implementatie van een monolithisch geïntegreerd vlak (2 dimensionaal, 2D) LED SiP behandeld. In **hoofdstuk 2** wordt het benodigde lage kosten proces beschreven, dit is een 5-7 masker lagen bipolair-CMOS (BiCMOS) proces met 1 of 2 metaal lagen. Op basis van metingen zijn de benodigde parameters verkregen voor ontwerp en integratie van diverse in-chip sensoren, circuits en andere functionele blokken. Dit ten behoeve van het ontwerp en de fabricage van een geavanceerd verlichtingssysteem. Vervolgens worden de verschillende onderdelen voor de inspectie en controle circuits in het 2D systeem beschreven (zie **hoofdstuk 3-5**). Dit 2D systeem integreert hoog vermogen blauwe LED chips met temperatuur sensoren en blauw licht gevoelige detectoren, waarmee de prestatie van het systeem kan worden bepaald. Een tralie vormige vermogenstransistor, een 4-bits flash analoog-naar-digitaal omzetter en een licht gestuurd terugkoppel circuit zij geïntegreerd in hetzelfde silicium en verbonden met de uitlezing van de sensoren ten behoeve van extra controle functies. Als licht sensor is een innovatieve multi-spoor blauw licht gevoelige foto diode ontwikkeld met een maximum responsiviteit bij een golflengte van 480 nm. Hiermee is een hoge gevoeligheid voor de bedoelde blauwe LED verlichting gerealiseerd. Het monolithisch geïntegreerd light terugkoppel systeem is een op een operationele versterker (opamp) gebaseerd terugkoppel circuit dat is gecombineerd met de hoog vermogen transistor en de blauw licht gevoelige foto diode. Hiermee wordt de licht opbrengst geregeld op basis van direct verkregen sensor data. Metingen en simulaties tonen aan dat met dit nieuwe systeem de licht opbrengst kan worden geregeld met een eenvoudig referentie spanning en dat een stabiele licht opbrengst onder variabele omgevingscondities kan worden gerealiseerd.

In het tweede gedeelte van dit proefschrift worden de uitdagingen, ontwerp in implementatie van een 3-dimensionaal (3D) systeem behandeld. In het bijzonder, een hoog aspect ratio (High Aspect Ratio, HAR) lithografie techniek is ontwikkeld welke belangrijk is voor 3D processen. Ook de implementatie van een 3D systeemverpakking is beschreven.

Een nieuwe techniek om, in speciale toepassingen, de beperkingen van conventionele draadverbindingen te ondervangen, de zogenoemde “lithografisch bepaald laterale draadverbinding”, wordt geïntroduceerd in **hoofdstuk 6**. Deze techniek omvat de depositie van dunne metaal films en opeen volgend patroneren van metaal sporen over hoge aspect ratio (3D)

door middel van hoge resolutie lithografie. Hoge resolutie lithografie over 3D structuren kan worden gerealiseerd door middel van multi-stap afbeeldingen (Multi-Step Imaging, MSI) op een stap & belichting projectie apparaat (waferstepper) van het type ASML PAS5500/80, dit in combinatie met een gepartitioneerd masker ontwerp. De toepassing van MSI is aangetoond door middel van 3D simulaties en experimenten. De resultaten zijn veelbelovend om generieke patronen af te beelden met hoge resolutie over topografieën van enkele honderden micrometers.

Tot slot, in **hoofdstuk 7**, is de simulatie, het ontwerp, de fabricage en metingen aan een 3D silicium interposer voor de WLP van een slimme, op fosfor gebaseerde wit licht LED module beschreven. In deze module zijn de diverse planaire controle circuits en sensoren, evenals de reflectie kamer voor de LED geïntegreerd. Deze integratie kan de efficiëntie van de licht opbrengst van een LED systeem verbeteren. De reflectie kamer voor de LED is 200 micrometer diep en door middel van KOH etsen in het silicium gefabriceerd. De zijwanden en de bodem zijn voorzien van een dunne hoog-reflecterende aluminium laag. De reflectie kamer is niet passief, maar actief door middel van integratie van licht sensoren in de zijwand en temperatuur sensoren in de bodem. Het reflectieve aluminium fungeert ook als verbindingsmetaal voor sensoren en is in patroon gebracht door middel van HAR lithografie. De componenten in de reflectie kamer zijn geïntegreerd met de 2D circuits op het silicium oppervlak. De diverse uitdagingen en oplossingen die leiden tot deze 3D implementatie zijn in dit hoofdstuk beschreven. Het is voor de eerste keer dat een functionele actieve component gefabriceerd is in de zijwand van een in silicium KOH geëtste kamer.

De 3D, slimme, op silicium gebaseerde interposer, tot stand gekomen in dit proefschrift is een monolithische integratie van diverse sensoren en controle circuits welke zijn gefabriceerd in een proces met lage kosten per oppervlakte eenheid. De elektrische verbindingen in deze 3D structuur zijn gefabriceerd met behulp van een ongekende hoog aspect ratio lithografie techniek.

# List of Publications

## Journal Papers

- **Z. Kolahdouz**, A. Rostamian, M. Kolahdouz, T. Ma, H. van Zeijl, and G.Q. Zhang, "Output Blue Light Evaluation for Phosphor Based Smart White LED Wafer Level Packages", ***OSA Optics Express***, vol. 24, no. 4, pp. 174–177, 2016.
- **Z. Kolahdouz**, T. Ma, H. Abdy, M. Kolahdouz, H. van Zeijl, and G.Q. Zhang, "Silicon-Based Multi-Functional Wafer-Level-Package for LEDs in 7-Mask BiCMOS Process", submitted to ***Elsevier Sensors and Actuators A***.
- **Z. Kolahdouz**, M. Tohidian, M. Kolahdouz, H. van Zeijl, and G.Q. Zhang, "Monolithic Light Feedback Control Circuit for Blue/UV LED Package", submitted to ***IEEE Photonics Journal***.
- **Z. Kolahdouz**, H. van Zeijl, M. Kolahdouz, W. Wien, and G.Q. Zhang, "High-Aspect-Ratio Lithography for Litho-Defined Lateral Wire Bonding", submitted to ***OSA Advances in Optics and Photonics***.
- **Z. Kolahdouz**, M. Kolahdouz, H. Abdi, H. van Zeijl, and G.Q. Zhang, "3D LED Package for Smart Lighting Systems", to be submitted to ***Scientific Reports***.
- E. Esmaeli, M. Ganjian, H. Rastegar, M. Kolahdouz, **Z. Kolahdouz**, and G. Q. Zhang, "Humidity sensor based on the ionic polymer metal composite", submitted to ***Elsevier Sensors and Actuators B***.
- R. Soleimanzadeh, M. S. S. Mousavi, A. Mehrfar, **Z. Kolahdouz**, M. Kolahdouz, and G. Q. Zhang, "Sequential microwave-assisted ultra-fast ZnO nanorod growth on optimized sol–gel seed layers," ***Elsevier Journal of Crystal Growth***, vol. 426, pp. 228–233, Sep. 2015.
- F. Karegar, M. Kolahdouz, F. D. Nayeri, R. Soleimanzadeh, M. Hosseini, **Z Kolahdouz** and G. Q. Zhang, "Light-Emitting n-ZnO Nanotube/$n^{+}$-GaAs Heterostructures Processed

at Low Temperatures," ***IEEE Photonics Technology Letters***, vol.27, no.13, pp.1430-1433, July1, 1 2015.

- R. Soleimanzadeh, M. Kolahdouz, M. A. Charsooghi, **Z. Kolahdouz**, and G. Q. Zhang, "Highly selective and responsive ultra-violet detection using an improved phototransistor," ***Applied Physics Letters***, vol. 106, no. 23, p. 231102, Jun. 2015.

## Conference Papers and Presentations

- **Z. Kolahdouz,** A. Rostamian, M. Kolahdouz, T. Ma, H. van Zeijl, and G.Q. Zhang, "Implementation of Advanced Multi- Functional Wafer Level package for LEDs in 7Mask BiCMOS Process," presented at ***China Solid-State Lighting (SSL)***, Beijing, 2014.
- **Z. Kolahdouz,** A. Rostamian, M. Kolahdouz, T. Ma, H. van Zeijl and G.Q. Zhang, "Blue Selective Photodiodes for Optical Feedback in LED Wafer Level Packages," in proceeding of ***IEEE ESSDERC***, Venice, 2014.
- **Z. Kolahdouz,** H. van Zeijl, and G.Q. Zhang, "High Aspect Ratio Lithography for Litho-Defined Wire Bonding," in proceeding of ***IEEE Electronic Components and Technology Conference (ECTC)***, Florida, 2014.
- **Z. Kolahdouz,** H. van Zeijl and G.Q. Zhang, "Hybrid 3D Wafer Level Integration Using Lithography-defined Wire Bonding," invited talk at ***ICT.OPEN***, SAFE Section, Rotterdam, 2012.

## Patents

- **Z. Kolahdouz**, H. van Zeijl, and G.Q. Zhang, "Insitu 3D Wafer Level Monitor/Control Unit for LED Color-shifting," European Patent Office, Application No. PCT/NL2016/050688, Filed Oct. 2015.
- **Z. Kolahdouz**, H. van Zeijl, and G.Q. Zhang, "Lithographic defined 3D lateral wiring," European Patent Office, Application No. 2015P00066 NL, Filed Jan. 2016.

# List of Figures

# List of Tables

# Acknowledgement

At final steps of my official student life, this is the time to address and appreciate all the people who have helped and contributed, in one way or another, in my education and achievements.

Growing up in a family with 5 electrical engineers from the same University (University of Tehran- UT) was far more than enough good inspiration towards Electronics world. Confidence, self-motivation, competitive/collaborative spirit, and deep faith in God's will were my first provisions from my great family. I would like to express my deepest appreciation to my lovely parents, Maman and Agha joon. Agha joon, you are my first and last teacher and honor in the world, and the foremost inspiration for all efforts in my life. Maman joon, having you with all your passions and supports is my biggest treasure. I am so fortunate and blessed to have the best 4 brothers, one could ever imagine: Mahdi, Mohammadreza, Mohammadjavad, and Mostafa. With you, I had the biggest and kindest supportive team. Thank you so much for your dedications, love and supports.

I would like to express my gratitude to my promotor and supervisor: Prof Kouchi Zhang and Dr. Henk van Zeijl. Dear Kouchi, I greatly appreciate your support and motivation during my PhD research. Your insisting on taking our own project leadership and freedom in all the steps was so stimulating and sometimes even fearful for a newly started researcher. However, at last, I learned a lot. Dearest Henk, you are a great supervisor with so many creative and impressive engineering solutions. When working with you, there is no dead-end even in the most frustrating moments. Our regular/irregular weekly meetings were so valuable for me, not only for their scientific/technical parts but also for discussing many different social/cultural topics. The most interesting part was that whenever I came to you with one question, you would unbelievably

send me back with ten! Your priceless experience and knowledge in cleanroom experiments are unique and so beneficial for me. Further thanks for your help in translating my thesis summary in Dutch and your 3D graphics that you kindly shared with me. I cannot express my appreciation to you in words.

I had also a privilege to have an outstanding internal supervisor, my older brother, Mohammadreza: You had started with your new position in UT as a fresh assistant professor, as I started my PhD. We had many discussions about building up the ideas and how to implement them. You were also a big help with your revision and comments in writing my thesis. I am so thankful for all of your help and wish you great success in your academic life.

I would also like to thank Prof. Lina Sarro, our best head of ECTM for all her support and guidance. Lina, I will always keep you in my mind as a fabulous successful woman with an impressive character.

A major part of my research has been done in Dimes Technology Center (now EKL) cleanrooms. I should state my biggest thanks to all the past and present technical staff for their helps and outstanding support, especially with my long processes which involved too many machineries and non-standard recipes. I would like to specially address: Tom Scholtes (for sharing your unique excellent expertise, experience and supports in my long-long processes), Silvana Milosavljevic (for being my greatest CR trainer), from our litho team: Wim Wien (for your precious advices on the litho process) and Johannes van Wingerden (for letting me run several long non-standard exposures on waferstepper), Mario Laros (for your great trainings and magical support with several tools), Willem van der Vlist (for training me in MEMS lab with your positive attitude), Alex van den Bogaard, Loek Steenweg and Koos van Hartingsveldt (for helping me in packaging and wirebonding my chips), Peter Swart (for all your support in electrical measurements), Jan Cornelis Wolff, Johan van der Cingel, Gregory Pandraud, Hugo Schellevis, Jia Wei, and Cassan Visser. From other labs in TUD, I would like to acknowledge Martijn Tijssen in TUD Solar Cell group (for you great help in measurement with Solar Cell Simulator and ZNO deposition), Charles de Boer at Kavli Nano Lab (for helping me with plasma etching for our super-capacitor structures) and Wil Straver at EWI 18th floor lab (for helping in micro assembling and packaging). Special words of appreciation go to our kind secretaries Marian Roozenburg and Bianca Knot for their kind administrative help and pleasant supports.

I would like to especially thank Rutger Voets at ASML Company for giving me the opportunity of a nice collaboration on utilizing MSI in my project.

During my PhD, I had the pleasure to work with several bright MSc students and parts of this thesis would not possible without them. I would like to thank Ali Rostamian, Hamed Abdi, and Mahya Ganjian at UT for their help in device and process simulations, measurements of implantation doping profiles and ZNO nano rod/wire processing. From TUD, firstly, I would like to mention Teng Ma. We developed together the first complete framework for circuitry design based on BiCMOS5/7 process (which was formerly developed by Henk for training purposes). We also made the first fastest record of full BiCMOS7 in just 6 days for the SMACK7 prototype. You also had a big contribution for readout circuits. Secondly, I would like to thank Harsha Achanta for our UV-C LED package work and his non-stop hard work. I wish all of you the best in your academic careers and lives.

During my presence in ECTM, I had the opportunity to share my office with several people. I would like to thank all of you: Vahid Mohammadi (for sharing your experiences generously with me), An Tran, Huaiyu Ye, Nikolas Gaio (you are a great motivated researcher with the heaviest visitor traffics per a day to the point where I had to make my first famous IN/OUT status sign for you on the door. You changed our office from the tidiest/most quiet to the funniest/busiest one ever!), Miki Trifunovic, Daniel Yi and William Solano. I am particularly thankful to my two superior Iranian friends in Dimes: Sima Trashioon and Maryam Yazdan Mehr (for all our nice talks, your kindness, and support). And all other colleagues I've had the chance to work with in "Micro/Nano System Integration and Reliability" group: Rene Poelma (your generous help and helpful comments), Cinzia Silvestri, Jing Zhang, Pan Liu (for our collaboration on your Queen prototype and also my phototransistors), Manjunath R. Venkatesh (for your always welcoming attitude for any help), Yelena Grachova, Xueming Li, Robert Sokolovskij, Fabio Santagata, Elina Iervolino, Joost Meerwijk, Daniel Farely, and Dr. Willem van Driel. I would like to express my highest gratitude to all my other colleagues I've had the fortune to work with in Dimes (current and alumni): Sten Vollebregt (special thanks for your proofread of my Dutch summary), Amir Sammak, Daniel Tejari, Agata Sakic, Aleksandar Jovic, Aslihan Arslan, Violeta Prodanovic, Pengfei Sun, Marta Kluba, Bruno Morana, Gianpaolo Lorito (for your kind help and advices in CR), Jiaqi Tang, Lin Qi , Paolo Sberna, Giuseppe

Fiorentino, Benjamin Mimoun, Negin Golshani and Jaber Derakhshandeh. My acknowledgement also goes to all the people that I have forgotten to add.

Special thanks to my gorgeous cousin ‘Sogol’ and my nice friend ‘Marzieh’ for our talks and their help for preparing the propositions.

Moreover, I want to send my gratitude to my former supervisors, colleagues and friends during my previous educational life, particularly: Prof. Shams Mohajer Zadeh from UT (for your wonderful encouragement and support to start and continue my research, I am always enthused by your brightness and ambitions for empowering all impossible missions) and Mrs. Zaferani (for giving me the chance to believe in myself and become a strong confident Iranian woman).

During my 5-year stay in Delft, I had many amazing friends that made my life, away from home and family, easier and more pleasant. Words cannot describe how grateful I am for your generous support. First, I want to thank my dearest and closest friends: Fatemeh Mohammad (as a true sister), Amir Abbas Zadpoor (for your kind help and our scientific/non-scientific discussions), and Fatemeh Adibzadeh (for our pleasurable friendship). Next, my nice friends at EWI which we had many enjoyable discussions during our daily lunch and tee/coffee breaks: Amir-Reza Ahmadi-Mehr and Iman Madadi. Third, my dear friends at TPM: Vahideh Ghorbani and Yashar Araghi. And last, all my other great friends in our small Iranian community in Delft.

Lastly, my greeting story ends with my beloved husband and adored friend, Massoud. I would like to state my highest heartfelt appreciation for your kindness, understanding, and patience. You were also so compassionate to give me your kindest support for many parts of my project, especially trainings for circuit design and measurements. Although we are from two wings of Electronics, far like from EWI building first to 18th floors, our great discussions are always like brainstorming moments for me. Words can never state my love and gratitude to you. I would also like to thank your respected family.

Al-hamdu lillahi rabbil 'alamin

Zahra Kolahdouz Esfahani

Delft, January 2017

# About the Author

Zahra Kolahdouz Esfahani received the B.Sc. and M.Sc. degrees in Electrical Engineering (with honors) from University of Tehran, Iran, in 2009 and 2011, respectively. She was a researcher in Thin Film and Nanoelectronic Laboratory, in 2007–2011. During her master study, she was working on gradual tilting exposure photo and nanolithography technique, growth control of oriented multi-wall CNTs, structural modification, and Graphene nano- ribbon synthesis through plasma unzipping. In late 2011, she commenced her Ph.D. work in Microelectronics at Delft University of Technology, The Netherlands, where she worked on high aspect ratio lithography, monolithic 3D wafer level integration, and smart LED wafer level packaging. Since Dec. 2016, she is pursuing her career as a postdoctoral research fellow at Kavli Institue of Nanosicence, TU Delft, in the group of prof. Henny Zandbergen on liquid cell nanoreactors for in-situ transmission electron microscopy. Her research interest includes advanced lithography techniques, developing MEMS/NEMS devices for different applications, and hybrid wafer level integration. She holds three patents and patent applications in the field of advanced nano and high aspect ratio lithography and 3D Si interposers.