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A CMOS Readout Circuit for Resistive Transducers Based on Algorithmic Resistance and Power Measurement

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***Abstract*— This paper reports a readout circuit capable of accurately measuring not only the resistance of a resistive transducer, but also the power dissipated in it, which is a critical parameter in thermal flow sensors or thermal-conductivity sensors. A front-end circuit, integrated in a standard CMOS technology, sets the voltage drop across the transducer, and senses the resulting current via an on-chip reference resistor. The voltages across the transducer and the reference resistor are digitized by a time-multiplexed high-resolution analog-to-digital converter (ADC) and post-processed to calculate resistance and power dissipation. To obtain accurate resistance and power readings, a voltage reference and a temperature-compensated reference resistor are required. An accurate voltage reference is constructed algorithmically, without relying on precision analog signal processing, by using the ADC to successively digitize the base-emitter voltages of an on-chip bipolar transistor biased at several different current levels, and then combining the results to obtain the equivalent of a precision curvature-corrected bandgap reference with a temperature coefficient of 18 ppm/°C, which is close to the state-of-the-art. We show that the same ADC readings can be used to determine die temperature, with an absolute inaccuracy of ±0.25°C (5 samples, min-max) after a 1-point trim. This information is used to compensate for the temperature dependence of the on-chip polysilicon reference resistor, effectively providing a temperature-compensated resistance reference. With this approach, the resistance and power dissipation of a 100 Ω transducer have been measured with an inaccuracy of less than ±0.55 Ω and ±0.8%, respectively, from –40°C to 125°C.**

***Index Terms*— resistive transducer; bandgap reference; temperature measurement; power measurement; algorithmic readout**

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I. Introduction

RESISTIVE TRANSDUCERS can be used to measure various physical parameters, such as temperature, flow, pressure, gas concentration and gas composition [1-7]. In many resistive-sensor systems, e.g. thermal sensors or thermal flow sensors [3, 4, 7], readout of the transducer's resistance is not sufficient for an accurate measurement. This is because the transducer's power dissipation also needs to be either stabilized or accurately measured. However, most integrated readout circuits for resistive transducers only measure resistance, without measuring or stabilizing power dissipation [1, 2, 5, 6].

Accurate stabilization or measurement of the power dissipated in a resistive transducer is challenging, because it relies on a stable power reference, which is typically derived from a voltage reference and a resistance reference. As a result, the previously-reported constant power circuits, based on translinear loops or other feedback loops, still rely on the accuracy of external voltage and current (or resistance) references. The stability reported for prior constant-power circuits in CMOS technology is typically not better than 1%, and is reported over load variations only, without addressing temperature dependency [8-10]. For instance, [8] presents a power control circuit using discrete resistors and monolithic ICs achieving less than 2.2% power errors. Using translinear loop in CMOS, [9] reports power errors from 1% to 3%. This level of stability is insufficient for demanding applications, such as the readout of thermal-conductivity-based resistive CO_2 sensors [3, 4]. In many applications, the variations of power dissipation are not only caused by load changes but also by the variations of ambient temperature due to the temperature dependence of the resistor. In addition, the system is preferred to be self-contained, and thus any external voltage, current or reference references are to be circumvented.

Instead of stabilizing the dissipated power, an alternative is to directly measure the power dissipation in the transducer along with its resistance, the impact of which can then be evaluated in obtaining the final measurement results. However, to accurately measure power dissipation, an accurate power reference is still needed, inherently requiring accurate voltage and resistance references that should be insensitive to process variations and temperature drift.

In standard CMOS, bandgap voltage references are the best-in-class voltage references. They combine a voltage that is proportional to absolute temperature (PTAT) with a voltage

that is complementary to absolute temperature (CTAT), both generated using the parasitic BJTs available in any CMOS process, to obtain a temperature-independent reference voltage [11]. Using precision circuit design techniques as well as appropriate calibration and correction schemes, bandgap references can achieve high accuracy over a wide temperature range with low chip-to-chip variations [12-15]. For instance, in [14] a temperature dependency of 5-12 ppm/°C over the temperature range of -40°C to 125°C has been achieved after a single room-temperature trim that compensates for the process spread of the BJTs. A key factor limiting the accuracy of most existing bandgap references are the errors introduced by the analog circuit that combines the PTAT and CTAT voltages (e.g., offset and gain errors), since these errors typically cannot be removed by a single trim [15]. Alternatively, the PTAT and CTAT voltages can also be combined in the charge domain by a switched-capacitor integrator, and it has been experimentally proven that the accuracy of a bandgap voltage thus synthesized can be very high [16]. In addition, accurate voltage measurements with algorithmic curvature correction have also been proposed, resulting in 12-bit accuracy over the temperature range of -40°C to 125°C [17].

Compared with voltage references, on-chip resistance references are even more difficult to realize, as resistors in IC technology are subject to significant process variation and temperature drift. Especially the latter results in errors which cannot be easily removed by calibration and trimming. Polysilicon resistors are relatively stable over temperature, but still exhibit a temperature dependence typically from ±0.1%/°C to ±1%/°C [15, 18-20]. Several circuit techniques have been reported to achieve a near-zero temperature coefficient of resistance (TCR), which typically involve combining resistors and/or linear MOSFETs with positive and negative temperature coefficients [18-20]. However, such combinations will be process-dependent, typically resulting in a residual temperature dependence of at least 100 ppm/°C. In consequence, the accuracy of reported on-chip power references [8-10] is much lower than that of voltage references [12-15]. Switched-capacitor resistors have been investigated in literature as a substitute for resistors in systems that require a stable resistance reference, such as current references [21] or resistor-based temperature sensors [2]. However, this approach requires stable capacitors and a stable clock. The latter is typically an off-chip quartz crystal, since on-chip oscillators typically exhibit temperature dependences of about 30 ppm/°C [22, 23], i.e. several times higher than that of the voltage reference. This makes this solution less attractive from a cost point of view.

In this paper, we present a circuit capable of accurately measuring resistance and power dissipation without relying on off-chip references. It operates algorithmically, by successively digitizing the voltage drop across the transducer (V_{load}), the voltage drop across an on-chip reference resistor carrying the same current (V_{ref}), and the base-emitter voltages of a single BJT (V_{be}) biased at different current levels, and then processing the results in the digital domain. The ratio of V_{load} and V_{ref} provides information about the transducer resistance R_{load} relative to the reference resistance R_{ref}. Rather than using an analog bandgap reference circuit, the reference voltage needed to calculate the power dissipation is obtained by combining the digitized base-emitter voltages to construct an equivalent reference voltage in the digital domain. To obtain the temperature information required to compensate for the temperature dependence of R_{ref}, the same digitized based-emitter voltages are used to construct an equivalent PTAT voltage in the digital domain, which, combined with the reference voltage, provides accurate information about the die temperature. The precision of the circuit is determined by the BJT and its bias circuit, and by the linearity and resolution of the ADC. It is independent of the analog reference voltage of the ADC, which, as we will show, cancels out. As will be detailed later in this paper, the main target of this work is to design a complete measurement system that processes the signals as much as possible in the digital domain, and thus circumvents the errors due to analog signal processing.

Experimental results obtained using a CMOS front-end prototype combined with an off-chip high-resolution ADC show that the proposed architecture works as expected. The digitally-constructed temperature sensor achieves an inaccuracy of ±0.25°C (min-max) across the temperature range of –40°C to 125°C after a 1-point trim, and the digitally-constructed bandgap reference achieves a temperature dependence of 18 ppm/°C, which are both close to the state-of-the-art. The inaccuracy of power measurements (load variations and temperature variations across the mentioned range) is better than ±0.8% after a single-temperature individual trim. Prior works [8-10] report comparable levels of accuracy, but do not address temperature variation, and rely on stable external voltage and/or current references.

The paper is organized as follows. In Section II, details of the measurement principle are presented. Section III is devoted to the circuit implementation of the readout circuit. Experimental results and discussions are presented in Section IV, and the paper is concluded in Section V.

II. Operating Principle

A. Algorithmic resistance and power measurement

Measuring resistance and/or power involves both voltage and current measurements. As shown in Fig. 1, the transducer R_{load} is biased at a desired voltage V_{bias} by an opamp circuit, while a reference resistor R_{ref} is included in the same branch as the transducer in order to measure the resulting current. The voltages across the transducer and across the reference resistor are measured sequentially by a multiplexed precision ADC, giving two digital outputs:

$$\mu_1 = \frac{V_{load}}{V_{ref}} \tag{1}$$

$$\mu_2 = \frac{V_{iload}}{V_{ref}} \tag{2}$$

where V_{ref} is the reference voltage of the ADC. This needs to be a low-noise voltage that is stable during the measurement, but does not have to be accurate, as it will eventually be replaced by an accurate reference voltage constructed in the digital domain, as will be discussed below.

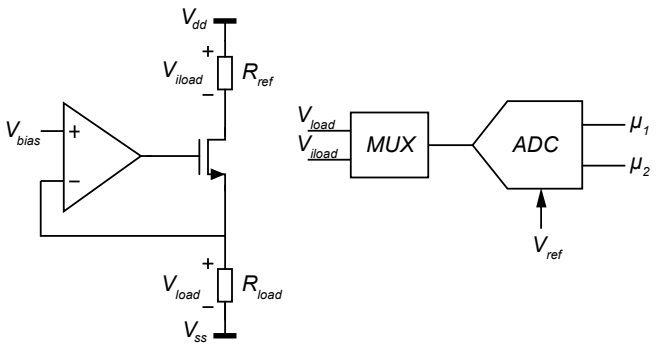

Fig. 1. Transducer front-end for resistance and power measurement.

From these results, the transducer's resistance and power dissipation can be calculated:

$$R_{load} = \frac{V_{load}}{I_{load}} = \frac{V_{load}}{V_{iload}} \cdot R_{ref} = \frac{\mu_1}{\mu_2} \cdot R_{ref} \tag{3}$$

$$P_{load} = V_{load} \cdot I_{load} = V_{load} \cdot \frac{V_{iload}}{R_{ref}} = \mu_1 \mu_2 \frac{V_{ref}^2}{R_{ref}} \tag{4}$$

These results depend on the ADC's reference voltage V_{ref} and on accurate knowledge of the value of R_{ref}. As detailed below, to eliminate the dependence on V_{ref}, we algorithmically construct an accurate bandgap voltage reference, by digitizing several base-emitter voltages. We use the temperature information contained in these base-emitter voltages to compensate for the temperature dependency of R_{ref}.

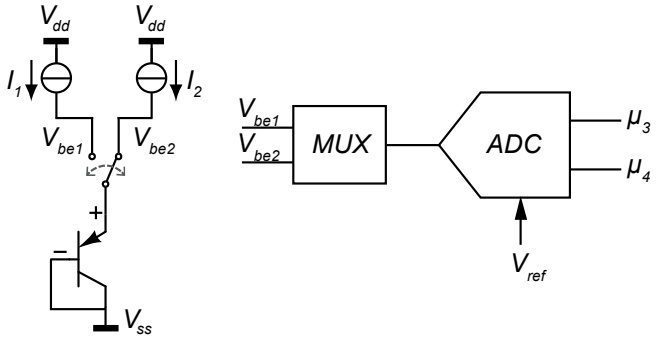

Fig. 2. BJT front-end for algorithmic voltage measurement.

B. Algorithmic bandgap voltage reference

To obtain an accurate bandgap voltage reference, we use the same ADC to digitize the base-emitter voltage V_{be} of a single BJT that is successively biased at two different collector currents I_1 and I_2, as shown in Fig. 2:

$$V_{be1,2} = \frac{nkT}{q} \ln\left(\frac{I_{1,2}}{I_S}\right) \tag{5}$$

in which n is the BJT's non-ideality factor, k is Boltzmann's constant, q is the electron charge, T is absolute temperature, and I_S is the BJT's saturation current ($I_S << I_{1,2}$) [24]. Note that this is a simplified expression; the impact of non-idealities of the BJT will be discussed in Section II-D. These base-emitter voltages are approximately linear functions of temperature,

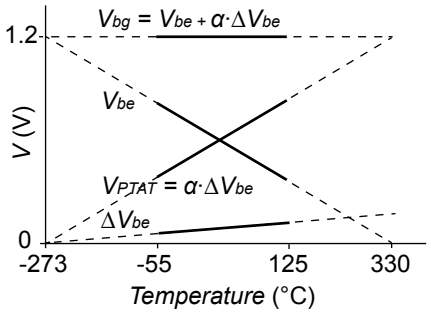

Fig. 3. Temperature dependency of the key voltages for constructing a bandgap reference.

with an extrapolated value at 0 K that is equal to the bandgap voltage of Silicon of about 1.2 V, and a negative temperature coefficient of about 2 mV/K that depends on the current level, as illustrated in Fig. 3 [24]. The difference of the two base-emitter voltages is a PTAT voltage that depends, to first order, only on the current ratio $p = I_1 / I_2$:

$$\Delta V_{be} = V_{be1} - V_{be2} = \frac{kT}{q} \cdot \ln(p) \tag{6}$$

In a conventional bandgap reference, a temperature-independent reference voltage is obtained by adding a scaled ΔV_{be} to V_{be}:

$$V_{bg} = V_{be1} + \alpha \cdot \Delta V_{be} = a_1 V_{be1} + a_2 V_{be2}, \tag{7}$$

where $a_1 = 1 + \alpha$, $a_2 = -\alpha$, and the optimal coefficient α is subject to tolerances on the BJT's saturation current and the bias current, and can be found based on a single-temperature calibration [15].

Rather than generating a bandgap reference voltage in the analog domain, we successively digitize $V_{be1,2}$ in two additional conversions, giving:

$$\mu_3 = \frac{V_{be1}}{V_{ref}}, \ \mu_4 = \frac{V_{be2}}{V_{ref}}, \tag{8}$$

These results are then combined digitally to obtain the equivalent of (7):

$$V_{bg} = V_{ref} \cdot (a_1 \mu_3 + a_2 \mu_4) \tag{9}$$

which allows us to express the (inaccurate) analog reference of the ADC V_{ref} in terms of the (accurate) bandgap reference V_{bg}. Note that the coefficients a_1 and a_2 in (9) can in principle be defined with arbitrary precision, which is not possible in a conventional analog implementation.

The voltage drop across the transducer can now be found independently of V_{ref} by combining (1) and (9):

$$V_{load} = \frac{\mu_1}{a_1 \mu_3 + a_2 \mu_4} \cdot V_{bg} \tag{10}$$

Similarly, the power dissipated in the transducer can be found by combining (4) and (9):

$$P_{load} = \frac{\mu_1 \mu_2}{(a_1 \mu_3 + a_2 \mu_4)^2} \cdot \frac{V_{bg}^2}{R_{ref}} \tag{11}$$

C. Algorithmic temperature measurement

Expressions (3) and (11) still depend on R_{ref}, which will generally be subject to process tolerances and temperature drift:

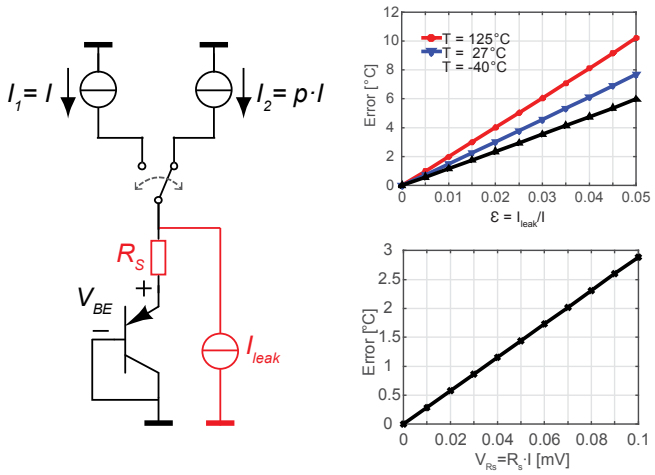

Fig. 4. (a) BJT front-end with series resistance R_s and leakage current I_{leak}; (b) temperature errors due to I_{leak}; (c) temperature errors due to R_s.

$$R_{ref} = R_{ref0}\left\{1+\alpha_{Rref}\left(T-T_0\right)\right\} \tag{12}$$

where R_{ref0} is the value of R_{ref} at temperature T_0 and α_{Rref} is the resistor's TCR. The tolerances of R_{ref0} can be compensated for by a single-temperature calibration, which is done by replacing the transducer by an off-chip precision resistor in the calibration setup.

To compensate for the resistor's temperature drift, information about the die temperature T is needed. Fortunately, this can readily be obtained from the PTAT voltage given by (6):

$$\begin{aligned} T &= \frac{q\Delta V_{be}}{k\cdot\ln(p)} = \left(\mu_3-\mu_4\right)\frac{qV_{ref}}{k\cdot\ln(p)} \\ &= \frac{\mu_3-\mu_4}{a_1\mu_3+a_2\mu_4}\cdot\frac{qV_{bg}}{k\cdot\ln(p)} \end{aligned} \tag{13}$$

where the relation (9) between V_{ref} and V_{bg} is again used to obtain an expression independent of V_{ref}. The result only depends on the current ratio p, the bandgap scale factors $a_{1,2}$, the bandgap voltage V_{bg} and physical constants k and q. The temperature reading thus obtained is substituted into (12) to calculate the value of R_{ref} so as to obtain a temperature-compensated resistance and power measurement.

D. Compensation for BJT non-idealities

As mentioned, expression (5) for the base-emitter voltage ignores various non-idealities of the BJT [15]. First of all, the non-linear temperature dependence of I_S will lead to a (slightly) non-linear temperature dependence of V_{be}, which leads to a small non-linear temperature dependence of the bandgap reference voltage, also referred to as curvature [24]. Rather than applying analog curvature-correction techniques, in our algorithmic approach, we will use the temperature information obtained using (13) to correct for this curvature in the digital domain.

Second, the transistor's finite current gain causes the collector current to deviate from the bias current, which is applied to the transistor's emitter. We assume the transistor is operated at current levels at which the current gain is only a weak function of the current level, so that this effect leads to small gain error in the bias current that can be compensated for using an appropriate bias circuit [25], as will be shown in Section III-B.

Further non-idealities associated with the BJT can be captured by replacing (5) by

$$V_{be} = \frac{nkT}{q}\ln\left(\frac{pI-I_{leak}}{I_S}\right)+pIR_s \tag{14}$$

where the transistor is assumed to be biased at a multiple p of a bias current I, and in which I_{leak} accounts for leakage currents (including the transistor's own saturation current), and R_s accounts for the voltage drop across the BJT's emitter (series) resistance, as illustrated in Fig. 4. Leakage current and series resistance lead to errors in the bandgap reference and the temperature measurement that cannot be corrected based on a single-temperature calibration [14]. The conventional approach to dealing with this is to choose the current level and transistor size such that these errors are sufficiently small.

Our algorithmic approach offers the unique possibility to correct for leakage and series resistance by combining more than two base-emitter voltages digitally. Equation (14) can be rewritten as:

$$V_{be} = V_{be,ideal} + \Delta V_{be,ideal}\frac{\ln(p-I_{leak}/I_S)}{\ln(p)} + pIR_s \tag{15}$$

where $V_{be,ideal}$ and $\Delta V_{be,ideal}$ are the ideal voltages given by (5) and (6). From base-emitter voltages measured at a minimum of four different values of p, $V_{be,ideal}$ and $\Delta V_{be,ideal}$ can be found by curve fitting to (15). These values can then be used, as before, to construct the voltage reference and measure temperature, without errors due to series resistance or leakage current.

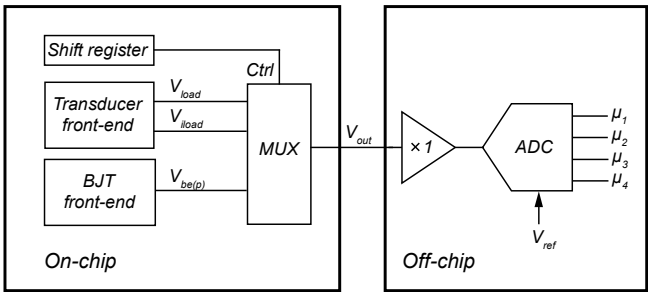

Fig. 5. Block diagram of the entire readout circuit (on-chip and off-chip).

III. Circuit Implementation

The block diagram of the readout circuit is shown in Fig. 5. The on-chip circuits, including the transducer front-end for resistance and power measurement, the BJT front-end for the construction of the algorithmic voltage reference and temperature sensor, and the multiplexer to select the desired voltage for measurement, have been designed and fabricated in a 0.16 µm CMOS technology.

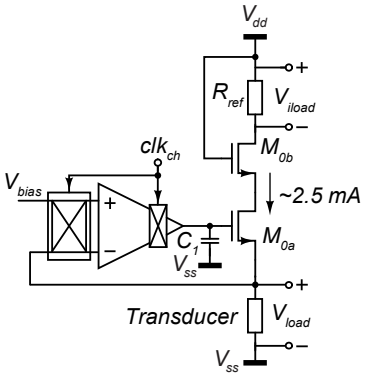

Fig. 6. Circuit diagram of the transducer front-end.

Since the algorithmic readout relies on the accuracy of the ADC, the non-idealities of the ADC must be taken into account when selecting or designing the ADC. First, the ADC's quantization noise and thermal noise should be non-dominant compared with the noise from the front-end circuits. Second, the non-linearity of the ADC (INL) will introduce signal-dependent errors, which cannot be readily removed by digital post-processing. Similarly, CMRR also plays an important role due to the different common-mode voltage levels to be measured. In this work, an off-chip ADC with a maximum ENOB of 23.5 bit [26] is used in this prototype. For future on-chip integration, the ADC presented in [27] can be adopted for its low INL (±6 ppm), low input-referred noise (0.65 µV, rms), as well as fast conversion rate (25 S/s).

In addition, for accurate measurement the input impedance of the ADC must also be considered. To avoid loading the front-end circuit, the output of the multiplexer is buffered by an off-chip unity-gain precision operational amplifier [28] before connecting to the ADC.

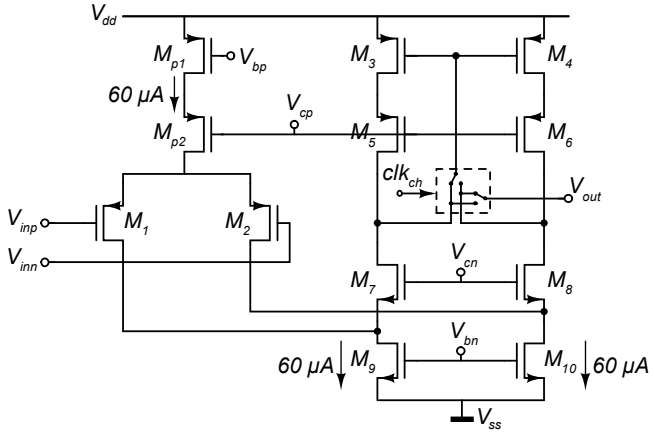

Fig. 7. Schematic of the operational transconductance amplifier (OTA) used in both bandgap core and transducer front-end.

A. Circuit Implementation of the Transducer Front-End

The transducer front-end circuit for resistance and power measurements is shown in Fig. 6. The voltage-to-current converter includes a chopped operational transconductance amplifier (OTA) in a feedback loop. The voltage across the transducer is thus stabilized to V_{bias}. Since the actual voltage will be measured by the precision ADC, the requirements on the OTA's precision can be relaxed. Chopping is mainly applied to reduce the impact of the amplifier's $1/f$ noise on the measurement.

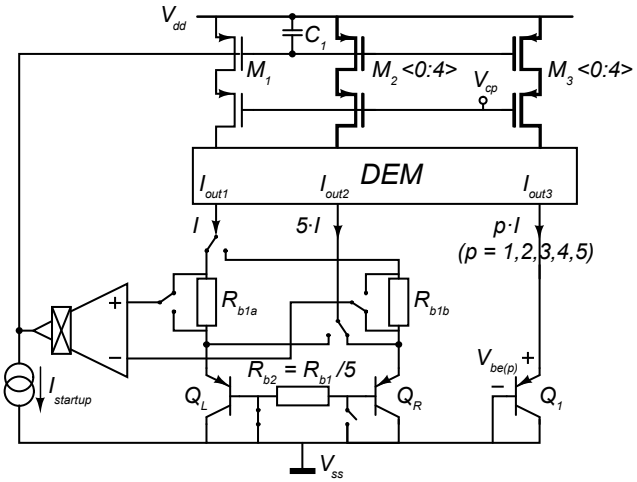

Fig. 8. Circuit diagram of the proposed bandgap core including bias generation.

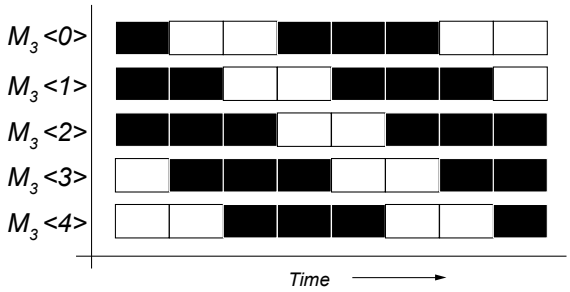

Fig. 9. DEM algorithm (p = 3 current sources are selected in this example).

Compared with Fig. 1, an additional cascode transistor M_{0b} is added. Simulation shows that leakage current due to Hot Carrier Injection to the bulk of the transistor becomes non-negligible when the supply voltage increases 10% above its nominal value (1.8 V). The added cascode transistor M_{0b} decreases the drain-source voltage of the main transistor M_{0a}, effectively reducing this leakage current. The capacitor C_1 is used to reduce the output integrated noise contributed by the OTA.

Fig. 7 shows the schematic of the OTA, which is a PMOS-input, folded-cascode amplifier. PMOS transistors are chosen for the input pair as the voltage across the transducer is relatively low (about 0.3 V). The output chopper switch is integrated in the output current mirror.

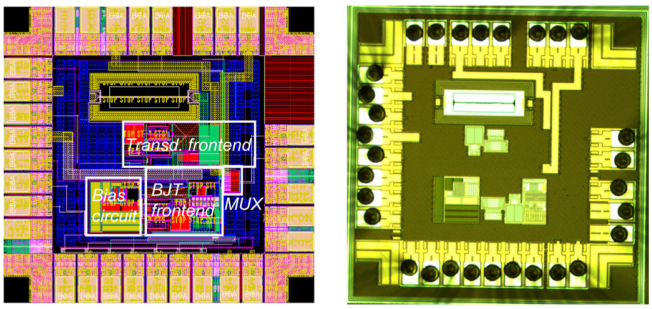

Fig. 10. Chip layout and photograph.

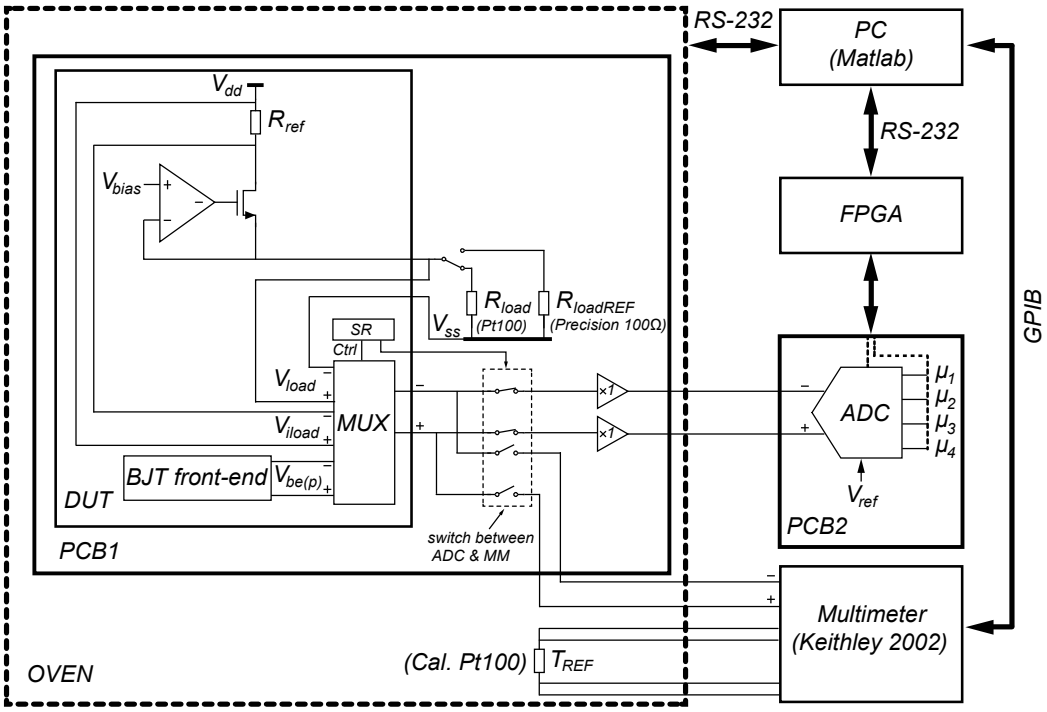

Fig. 11. Experimental setup.

B. Circuit Implementation of the BJT Front-End

The BJT front-end circuit shown in Fig. 8 generates the base-emitter voltages needed for the construction of the voltage reference and temperature sensor. A PTAT bias generation circuit is used to provide a well-defined bias current that is an integer multiple p of a unit bias current of nominally 6 μA [24]. Resistor R_{b2} is used to remove the current-gain dependence of the base-emitter voltage by making the generated bias current dependent on the base current in such a way that the collector current of Q_1 is PTAT and independent of the current gain, provided the current gains of Q_1, Q_L and Q_R are matched [25].

The OTA used in the BJT front-end is the same as the one used in the transducer front-end (as shown in Fig. 7). The amplifier needs to have low offset and high open-loop gain to minimize errors in the bias current [25]. To attain low offset, the amplifier is chopped. The open-loop gain is above 60 dB at all corners.

As indicated in (6), an accurate PTAT voltage ΔV_{be} requires a well-defined current ratio p that is stable over time and temperature. This is achieved by applying dynamic element matching (DEM) in the current mirror in Fig. 8. The DEM algorithm is illustrated in Fig. 9. To generate a current of p times the unit bias current I, in every DEM step p unit current sources are selected and in successive DEM steps, the selected current sources are shifted by one in a cyclic manner. Thus, the mismatch of the current sources is modulated by the DEM clock, and the resulting average current is close to p times the average unit current. Since the following signal processing is done by an oversampled ADC, the voltage ripple associated with the modulated current mismatches is averaged out by the digital filtering of the ADC.

IV. Experimental Results And Discussion

A chip photograph and a plot of the chip layout with the main circuit blocks are shown in Fig. 10. A block diagram of the experimental setup is shown in Fig. 11. The chip (DUT), mounted on a PCB (PCB_1), is placed inside a climate chamber (Vötch VTM 7004) to perform measurements at temperatures ranging from -40°C to 125°C. A Pt100 resistive temperature detector (R_{load}), with a nominal resistance of 100 Ω at 0 °C and a temperature coefficient of 0.39%/K, is used as the transducer whose resistance and power dissipation are to be measured. For calibration purposes, a switch allows R_{load} to be replaced by a precision resistor $R_{loadREF}$. A second calibrated Pt100 resistor is used as a reference temperature sensor (T_{REF}). A second PCB (PCB_2) with the ADC [26] is placed outside the oven. Control signals for the on-chip MUX and DEM switches and the ADC are generated by an FPGA, and the ADC's output data is transferred to a PC via an RS-232 connection and processed in MATLAB. A precision multimeter (Keithley 2002) is used to measure the resistance of the transducer and the voltage drop across the transducer when it is biased by the chip, so that power dissipation in the transducer can be independently determined for comparison.

A. Voltage Reference

To evaluate the accuracy of the algorithmic voltage reference, the digitized base-emitter voltages as well as the voltage drop across the transducer V_{load} were measured sequentially by the ADC, and the value of V_{load} was calculated relative to the algorithmic voltage reference using (10), including compensation for series resistance, leakage and curvature using the techniques described in Section II-D. Fig. 12 compares the result, for 5 samples of the chip, with a direct measurement of V_{load} using the precision multimeter. The results show good agreement, with errors below ±1.1 mV.

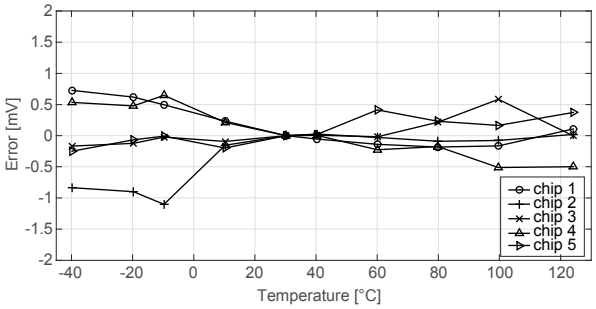

Fig. 12. Measured voltage error of the transducer by the algorithmic reference voltage (compared with the measurements by the multimeter).

To obtain the result shown in Fig. 12, the value of V_{bg} in (9) was determined iteratively so as to obtain the smallest temperature dependence. This is a batch calibration [15], leading to a fixed optimal value of V_{bg} that is common for all samples. To correct for sample-to-sample spread of the base-emitter voltages, the optimum value of α, which gives the value of $a_1 = 1 + \alpha$, $a_2 = -\alpha$ in (9), was determined for every individual sample by means of a one-point calibration at room

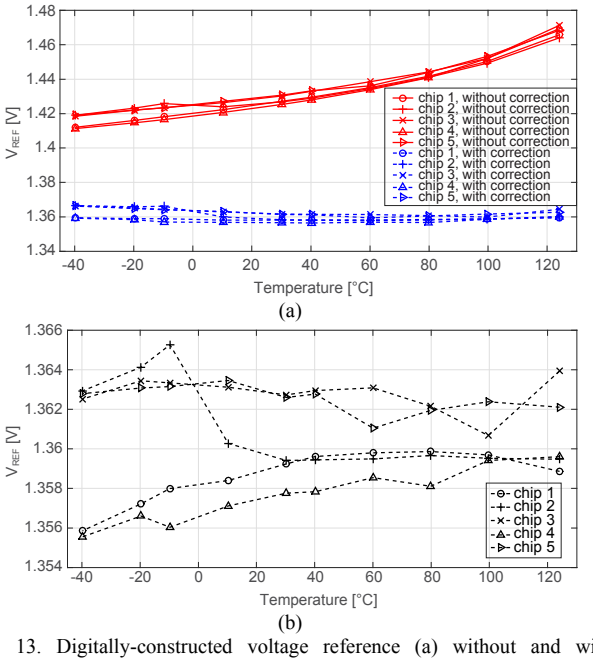

Fig. 13. Digitally-constructed voltage reference (a) without and with compensation and correction for series resistance and leakage; (b) with compensation and correction for series resistance and leakage as well as curvature

temperature (27ºC), at which α was adjusted to make the calculated V_{load} equal to the value measured using the precision multimeter.

From the same data set, the value of the algorithmic reference voltage is calculated using (9), where the value of the ADC's reference voltage V_{ref} is obtained from (1), by dividing the value of V_{load} as measured using the precision multimeter by μ_1. The result is shown in Fig. 13. To illustrate the impact of the series resistance, leakage current and curvature, results are shown with and without compensation for these non-idealities. The temperature coefficient without compensation for any of these non-idealities is about 220 ppm/°C, mainly due to the impact of leakage current, which is rather large in our design due to the sizing of the MOS transistors in the on-chip multiplexer. This is improved to about 24 ppm/°C after compensation for series resistance and leakage using the method described in Section II-D. After compensation for the systematic quadratic curvature, the temperature coefficient is further improved to 18 ppm/°C (Fig. 13(b)).

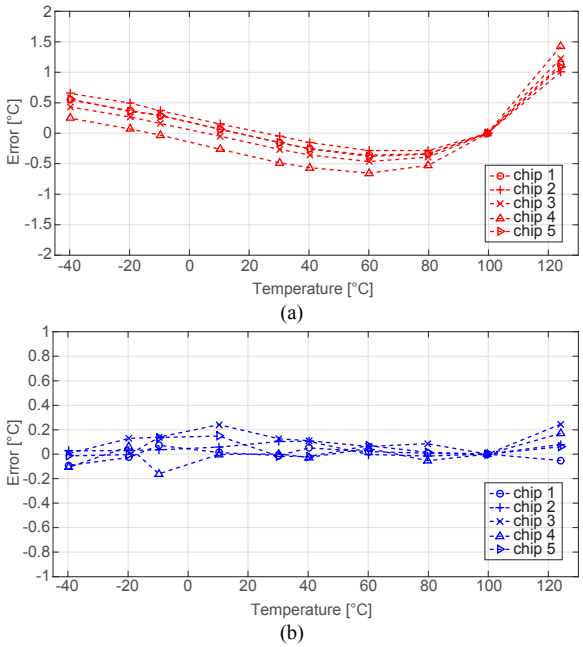

Fig. 14. Measured temperature error of the algorithmic temperature sensor (a) without and (b) with correction for leakage and series resistance

B. Temperature Measurement

Fig. 14 shows the error in the temperature measured using the method described in Section II-C, relative to the reference temperature sensor, for 5 samples of the chip. When ΔV_{be} is directly measured without any compensation, significant errors occur at high temperatures due to leakage currents (up to 180 nA in this design). By applying the algorithmic approach described by (13) and (14), a leakage-free PTAT voltage $\Delta V_{be,ideal}$ can be obtained, which can then be converted to temperature by linear scaling. Thus, the errors after error compensation are reduced to ±0.25°C (min-max) after a 1-point trim at 100°C (Fig. 14(b)). The trimming, to cancel the PTAT error due to V_{be} spread, was done in the digital domain [15]. These errors are relatively large compared to the state of the art [25], which can be attributed to the large initial errors due to the leakage currents in the multiplexer switches, which can be reduced in a re-design by reducing the transistor sizes. Nevertheless, the accuracy currently obtained is sufficient to

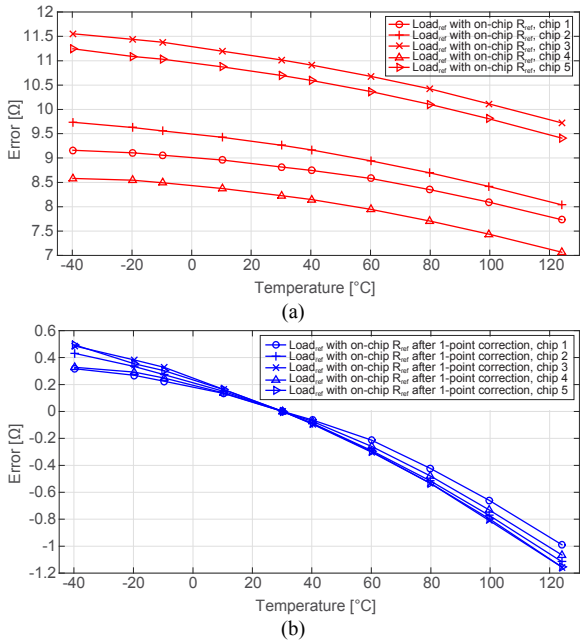

Fig. 15. Measured resistance error of a precision resistor as a function of temperature; (a) without calibration; (b) with calibration and correction at one-temperature point (27°C)

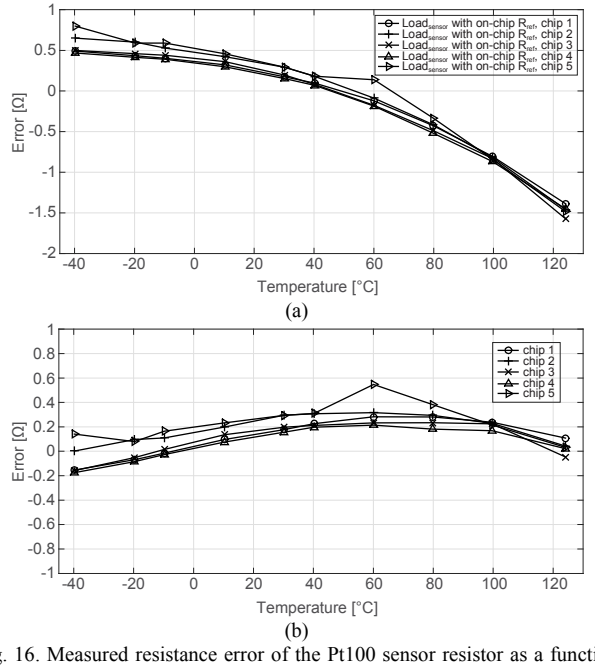

Fig. 16. Measured resistance error of the Pt100 sensor resistor as a function of temperature; (a) with calibration and correction at one-temperature point (27°C); (b) with calibration and correction at two-temperature points (27°C and 100°C)

effectively compensate for the temperature dependence of the on-chip reference resistor.

C. Resistance Measurement

As described in II-A, the resistance of the transducer is measured relative to an on-chip reference resistor R_{ref} in series with the transducer (Fig. 6). Since R_{ref} is subject to process tolerances, it is first calibrated by connecting a precision resistor ($R_{loadREF}$ in Fig. 11) instead of the transducer. Fig. 15(a) shows the error in the measured resistance of this precision resistor as a function of temperature relative to the resistance measured using the precision multi-meter.

First, a one-point correction is performed by using the error at 27°C to determine the nominal resistance of R_{ref}, i.e. R_{ref0} in eq. (12), while assuming its temperature coefficient α_{Rref} is zero. The error in the measurement of the precision resistor then reduces significantly, as shown in Fig. 15(b). The resistance of the Pt100 is then measured using this same correction. The error in this measurement relative to the multimeter is less than ±1.6 Ω, as shown in Fig. 16(a). A substantial temperature drift is observed due to the fact that the temperature dependence of R_{ref} is not compensated for.

Second, the temperature coefficient α_{Rref} is determined by a two-point batch correction (at 27°C and 100°C) in the calibration result of Fig. 15(a). When measuring the Pt100, these coefficients and the temperature information obtained from the algorithmic temperature measurement are used to compensate for the temperature dependence of R_{ref}, as discussed in Section II-C. This reduces the error to less than ±0.55 Ω, as shown in Fig. 16(b). A further reduction could be achieved by also compensating for the higher-order temperature dependence of R_{ref}.

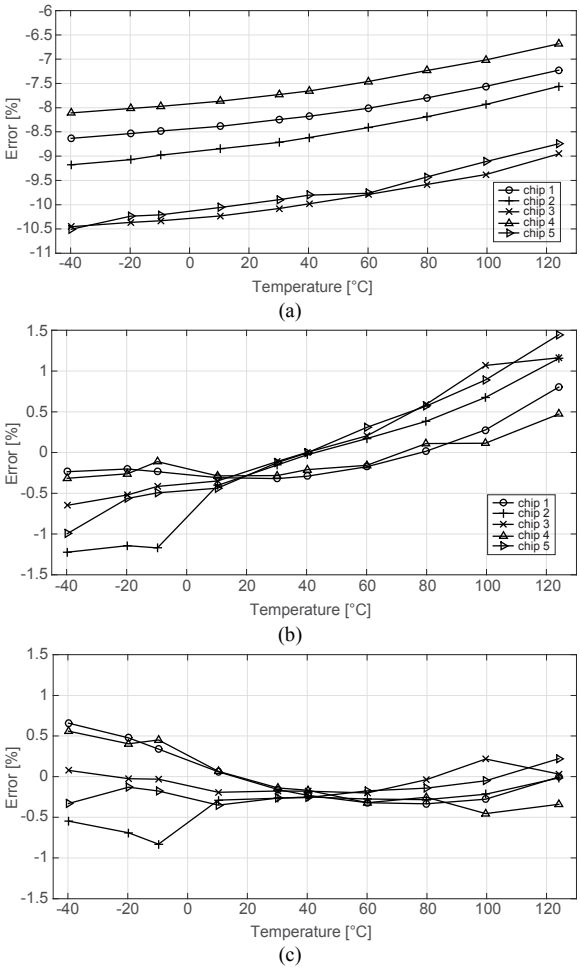

Fig. 17. Measured power error as a function of temperature; (a) without calibration; (b) with 1-point calibration and correction of the resistance measurement; (c) with 2-point calibration and correction of the resistance measurement

TABLE I
PERFORMANCE SUMMARY

Temperature range	-40°C – 125°C
Temperature inaccuracy	±0.25°C (min-max)
Temperature dependence of voltage reference	18 ppm/°C
Resistance inaccuracy	±0.55 Ω†
Power inaccuracy	±0.8%†

†after a single temperature calibration for the on-chip reference resistor, 5 samples.

D. Power Measurement

The power consumption of the transducer was measured using the method described in Section II, eq. (11). Fig. 17(a) shows the results of the power dissipation in the transducer without compensating for the tolerance and temperature drift of the on-chip reference resistor R_{ref}, and Fig. 17(b) shows the results when a one-point calibration at 27°C is performed to compensate for spread in the nominal resistance of R_{ref}, i.e. R_{ref0} in eq. (12), in a similar way as described above. With this calibration, the errors are less than ±1.5%. As described above, the accuracy of the on-chip reference resistance can be further improved by a room-temperature individual trim and a two-point batch calibration (27°C and 100°C) to find R_{ref0} and α_{Rref}. This reduces the errors in the power dissipation measurement to ±0.8% as shown in Fig. 17(c).

V. CONCLUSIONS

In this paper, we have reported a readout architecture for resistive transducers, which is capable of accurately measuring their resistance and power dissipation. Its performance is summarized in TABLE I. The key idea behind the readout architecture is to avoid analog signal processing as much as possible, by first digitizing the analog signals and then combining the results in the digital domain. This algorithmic approach greatly improves the flexibility of the signal processing and facilitates the removal of errors such as leakage current, series resistance, and systematic nonlinearity in the digital domain. In addition, the accuracy of the analog reference voltage of the ADC in this system does not impact the measurement accuracy, as this reference voltage is replaced by the constructed bandgap reference voltage in further data processing. Experimental results have shown that the resistance and power dissipation of a Pt100 resistor can be measured with an inaccuracy of ±0.55 Ω and less than ±0.8% respectively over the military temperature range of -40°C and 125°C, showing the effectiveness of the applied techniques. The digitally-constructed bandgap reference and temperature sensor achieve performance close to that of other state-of-the-art voltage references and temperature sensors. Although our prototype uses an off-chip ADC for an initial proof-of-concept, making it more costly and power hungry than prior solutions, suitable ADCs implemented in standard CMOS technology have been reported [27], which can readily be co-integrated to realize a fully-integrated low-cost solution. The ability to accurately measure the resistance and power dissipation of a resistive transducer as well as ambient temperature makes this readout architecture well-suited, for instance, to the interfacing of thermal-conductivity-based gas sensors.

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