Optimized Control of LCL-VSC Converter With Refined s-Parameter

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Optimized Control of LCL-VSC Converter with Refined *s*-Parameter

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***Abstract*—For the control of high-voltage DC (HVDC) systems, especially for that of the multi-terminal HVDC (MTDC) systems, the voltage source converter (VSC) is a good option because of its high controllability. Nowadays, different types of VSC converters have been realized such as two/three level converter and modular multilevel converter. However, VSC converters are vulnerable against DC faults because the paralleled diodes may experience large fault currents. In order to maintain the sustainability of electricity delivery, efforts have been paid on protecting the HVDC networks, such as the novel converter topologies with capability to tolerate faults and also the DC circuit breaker (DCCB). Among which, the concept of the LCL (inductor-capacitor-inductor circuit)-VSC converter aims at enhancing the ability of converter to ride through DC faults, which limits currents flowing from AC side to DC side. The proposed method in this paper optimizes the control of LCL-VSC for partial load so that the power loss can be drastically decreased. Additionally, the preferable working range for the LCL converter is introduced to guarantee the ability of restraining fault currents. The method is verified on the PSCAD/EMTDC platform.**

***Index Terms*— high-voltage DC (HVDC), modular multilevel converter (MMC), multi terminal HVDC (MTDC), PSCAD/EMTDC, voltage source converter (VSC)**

I. Introduction

The voltage source converter (VSC) has increasingly gained attention from industry to be a crucial component in future power systems with high penetration of power electronics. By far, there have been several types of VSC converter: two-level converter, three-level converter and modular multilevel converter (MMC or M2C) [1]. Compared with high-voltage AC (HVAC) system, the HVDC system has obvious advantages in long-distance bulk power transmission [2][3]. Besides the high efficiency, the self-commutating ability, small footprint of construction and low requirement of passive AC filter make it an optimal solution for the future power network [4][5].

On the contrary, because of the low impedance in DC grids, the DC short-circuit faults penetrate deeply in the network. On the other hand, the two-level, three-level and half-H bridge (HB) MMC converters become uncontrolled diode bridge when the insulated-gate bipolar transistors (IGBTs) are switched off during faults. Although the full-H bridge (FB) MMC can block faults successfully, it is not a preferable option because of its higher cost. The fault currents discharged from AC side to DC side will climb to an excessive value. Therefore, problems occur under this situation:

- The converter becomes uncontrollable thus the power transmission is not possible.
- The short circuit on DC side finally crumble the AC system due to the uncontrollable bridge.
- The short-circuit currents are extremely high for the diodes which will be burnt after certain period; although the fault can be cleared by an AC circuit breaker, the clearing time is too long for these electronic elements (exceeding 10ms).
- In multi-terminal HVDC (MTDC) systems, all the converters will contribute to the fault current; thus, it will increase to an unacceptable value.

At present, travelling-wave protection and voltage derivative protection work as primary protection, while undervoltage protection and differential protection work as backup protection [3][6][7]. However, they are insufficient for the HVDC system. The shortcomings of these protection methods have been reported in [7].

For the sake of a sustainable HVDC system, efforts have been put not only on the protection algorithms but also on the converter topologies.

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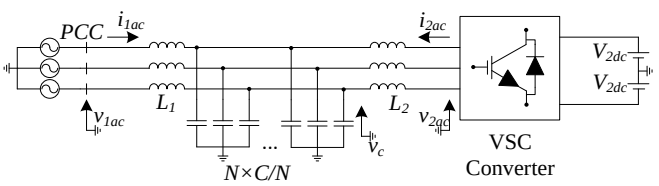

Fig. 1. Topology of LCL-VSC converter

In [8], a quick-action protection is developed which uses only one-end current and is capable of distinguishing internal and external faults. However, this method is much more applicable for the line-commutated converter (LCC) as the main algorithm is based on different firing angles and overlap angles. In [9], the principle of protecting the MMC converter from non-permanent faults is presented. Extra anti-paralleled thyristors are applied in each submodule as the path for fault currents. Although the fault current can decrease to zero within a certain time after firing these supplementary thyristors, the installation of extra thyristors increases the investment and maintenance expense. Additionally, the fault will propagate to AC side when the thyristors are switched on as there is no diode bridge anymore at this moment. Although the new type converter in [10] can block fault and has similar efficiency of traditional HB MMC, its requirement of wave shaping circuits one three phases makes it less affordable.

A fault-tolerable converter configuration is proposed in [11]; an inductor-capacitor-inductor (LCL) circuit is introduced on the AC side of VSC converter (two/three-level or MMC). The LCL circuit is used to restrain fault currents flowing from AC side to DC side. One short coming of the design is that it cannot realize zero reactive power transfer, which is a common option for a VSC converter from a viewpoint of efficiency. To improve this, in [12] a design that enables an LCL-VSC to work at full load is proposed. At the same time, this paper puts forward a solution to operate an LCL-VSC converter under partial loads by disconnecting the capacitor banks accordingly. Nevertheless, it has been found that the reactive power does exist between the LCL circuit and the converter bridge under partial loads, and this brings down the efficiency of converter.

This paper focuses on the decreasing reactive power transfer in LCL-VSC converters. First, the reactive power balancing condition of LCL circuit is derived. The optimization of reactive power is then achieved by flexibly adjusting the step ratio of LCL circuit (*s*-parameter) according to different partial-load conditions. This improvement can be easily applied by a transformer with tap changer. In addition, it was proved that this method has negligible effects on the performance of limiting the fault currents. Thus, the proposed method can improve the working efficiency of LCL-VSC converter while ensuring the purpose of restraining the current feeding from AC side during faults. Additionally, this paper proposes the criterion of selecting the rated step ratio s_r of LCL and clarifies the reason for the necessary derating of a converter when s_r<1. The relationship between refined step ratio and short circuit current is also depicted. The proposed method was verified in PSCAD/EMTDC environment.

The whole paper is organized as follows. In Section II, the basic idea of LCL-VSC converter is revised and the condition for zero active power transfer is obtained. The selection of LCL step ratio is discussed in Section III. The Section IV demonstrates the results of simulation, and Section V concludes the paper.

II. The Optimized Control of LCL Circuit

A. Basic Design Idea

The topology of LCL-VSC converter is introduced in Fig. 1 and the basic equations for one phase are as follows:

$$\begin{aligned} j\omega L_1\overline{I_{1ac}} &= \overline{V_{1ac}} - \overline{V_c} \\ j\omega C\overline{V_c} &= \overline{I_{1ac}} + \overline{I_{2ac}} \\ j\omega L_2\overline{I_{2ac}} &= \overline{V_{2ac}} - \overline{V_c} \end{aligned} \tag{1}$$

in which the $\overline{I_{1ac}}$, $\overline{I_{2ac}}$, $\overline{V_{1ac}}$, $\overline{V_{2ac}}$ and $\overline{V_c}$ are phasors in rms, standing for the AC currents (i_{1ac}, i_{2ac}), line-to-neutral AC voltages (v_{1ac}, v_{2ac}) on the two sides of LCL circuit, capacitor voltage (v_c) respectively. The converter shown in Fig. 1 can be either type of VSC: two/three level or MMC converter.

And we can get the expressions of $\overline{I_{1ac}}$, $\overline{I_{2ac}}$, $\overline{V_c}$ as (2) shows, and the coefficients k_1, k_2 and k_3 are described in (3) :

$$\begin{cases} \overline{V_C} = \left(L_1\overline{V_{2ac}} + L_2\overline{V_{1ac}}\right)\Big/ k_3 \\ \overline{I_{1ac}} = \left(k_1\overline{V_{1ac}} - \overline{V_{2ac}}\right)\Big/ j\omega k_3 \\ \overline{I_{2ac}} = \left(k_2\overline{V_{2ac}} - \overline{V_{1ac}}\right)\Big/ j\omega k_3 \end{cases} \tag{2}$$

$$\begin{cases} k_1 = 1-\omega^2 L_2 C \\ k_2 = 1-\omega^2 L_1 C \\ k_3 = L_1 + L_2 - \omega^2 L_1 L_2 C \end{cases} \tag{3}$$

We can transfer these equations from rotating frame to *dq* frame

$$\overline{V_{1ac}} = V_{1acm}\angle\theta_1 = V_{1acd} + jV_{1acq} \quad (4)$$

$$\overline{V_{2ac}} = V_{2acm}\angle\theta_2 = V_{2acd} + jV_{2acq} \quad (5)$$

and $\overline{V_{2ac}}$ should be controlled. After assuming the *d*-axis is aligned with $\overline{V_{1ac}}$, (4) and (5) could be rewritten as

$$\overline{V_{1ac}} = V_{1acd} = V_{1acm} \quad (6)$$

$$\overline{V_{2ac}} = \left(M_d + jM_q\right)\cdot\frac{V_{2dc}}{\sqrt{2}} \quad (7)$$

M_d and M_q are modulation indices of *d*- and *q*- axis, and:

$$V_{2acm} = M\frac{V_{2dc}}{\sqrt{2}} \quad (8)$$

$$M = \sqrt{M_d^2 + M_q^2} \quad (9)$$

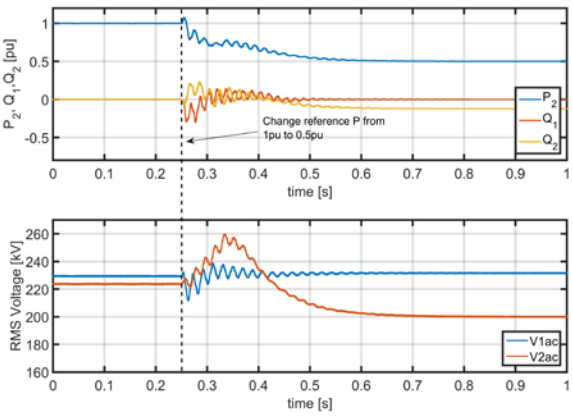

Fig. 2. The behaviour of converter after decreasing power reference

We can then obtain the active power and reactive power transfer at rated design (which is normally a desired design):

$$P_{1r} = -P_{2r} = \mathrm{Re}\left[\overline{V_{1acr}}\cdot\overline{I_{1acr}}^{*}\right] = \frac{s_r M_r M_{qr} V_{2dc}^2}{2\omega k_{3r}} \quad (10)$$

$$Q_{1r} = \mathrm{Im}\left[\overline{V_{1acr}}\cdot\overline{I_{1acr}}^{*}\right] = \frac{\left(k_{1r}s_r M_r - M_{dr}\right)s_r M_r V_{2dc}^2}{2\omega k_{3r}} \quad (11)$$

$$Q_{2r} = \mathrm{Im}\left[\overline{V_{2acr}}\cdot\overline{I_{2acr}}^{*}\right] = \frac{\left(k_{2r}M_r - s_r M_{dr}\right)M_r V_{2dc}^2}{2\omega k_{3r}} \quad (12)$$

from (10) to (12), the parameter s_r represents the rated step ratio of LCL circuit:

$$s_r = V_{1acm}/V_{2acm} \quad (13)$$

subscript "r" stands for rated values, superscript "*" represents corresponding conjugate phasors. We can observe that the *q*-axis is used to control active power while *d*-axis to control reactive power, which is quite different from conventional design.

A tradeoff is made in [11] on rated power efficiency and partial-load efficiency. If one wants to realize zero reactive power transfer, (11) and (12) can be set to zero, and then the following equations can be derived:

$$k_{1r}s_r M_r = M_{dr} \quad (14)$$

$$k_{2r}M_r = s_r M_{dr} \quad (15)$$

$$k_{2r} = k_{1r}s_r^2 \quad (16)$$

Another important parameter is the ratio between the rms values of the steady-state fault current i_{2acf} and the rated i_{2acr} for DC faults. According to (2), assume v_{2ac}=0:

$$r = \frac{1}{\sqrt{1 - k_{1r}^2 s_r^2}} \quad (17)$$

Then, it is also possible to obtain the relation between *r* and k_{1r}, which is:

$$k_{1r} = \frac{\sqrt{1 - 1/r^2}}{s_r} \quad (18)$$

The above design is for the rated power, however, the converter will always be over-rated for safe operation. In other words, a converter always works at partial-load states. The Q_2 is high at partial load because of the difference of voltage v_2 and current i_2 angles. In order to decrease Q_2, it is possible to mathematically find an optimal capacitor to achieve lowest current I_2 and it can be obtained through condition $M_d^2 + M_q^2 \le M_r^2$. It should be noticed that M_d and M_q are no longer the rated modulation indices. After rearranging and substituting (10) and (11) into this condition, it comes to:

$$\left(s_r k_1 M_r\right)^2 + \left(2P_{part}\omega k_3 / s_r M_r V_{2dc}^2\right) \le M_r^2 \quad (19)$$

P_{part} means the partial load. Then the minimal capacitor could be calculated by (20):

$$
\begin{aligned}
C_{\min} &= \frac{-b-\sqrt{b^2-4ac}}{2a} \\
a &= \frac{4\omega^6 P_{part}^2 L_1^2 L_2^2}{s_r^2 M_r^2 V_{2dc}^4} + s_r^2 M_r^2 L_2^2 \omega^4 \\
b &= -2\left(\frac{4P_{part}^2 \omega^4 (L_1+L_2) L_1 L_2}{s_r^2 M_r^2 V_{2dc}^4} + s_r^2 M_r^2 L_2^2 \omega^2\right) \\
c &= \frac{4P_{part}^2 \omega^2 (L_1+L_2)^2}{s_r^2 M_r^2 V_{2dc}^4} + s_r^2 M_r^2 - M_r^2
\end{aligned}
\tag{20}
$$

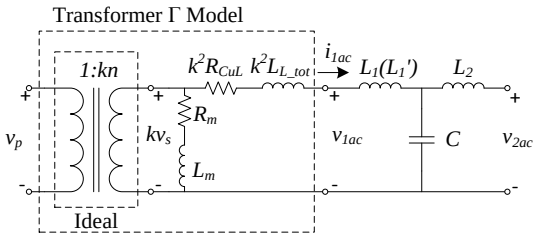

Fig. 3. LCL circuit connecting transformer (only shows phase A)

B. Regulating s of LCL Circuit Under Partial Loads

Although the capacitor can be decreased, there is still a basic reactive power requirement. The controller automatically changes M_d to compensate this demand. The Fig.2 shows the simulation case when change P_2=1.0pu to 0.5pu at 0.25s. In this case, the Q_2 is not zero anymore; the VSC is now absorbing reactive power from LCL circuit. Consequently, the current flowing through the converter bridge is still high which will result to a high power loss. The power losses are estimated in section IV.

The relatively high power loss is the disadvantage of LCL-VSC under partial-load conditions. The reason for it is that the voltage of V_{2ac} decreases, but V_{1ac} remains at same level. Then, the redundant reactive power from capacitor C is delivered to VSC.

The solution could be found if we analyze the reactive power in the LCL circuit itself. In order to ensure that there is no reactive power transferring, one condition must be met within LCL circuit: the reactive power generated by capacitor must be consumed totally by two inductors; this condition can be satisfied, as the Q_2=0 before changing the reference of P_2 in Fig. 2. Then we make the difference of generated and consumed reactive power as follows:

$$
\begin{aligned}
diff &= Q_{generated} - Q_{Consumed} = \mathrm{Im}\left[\overline{V_C}\cdot\left(-\overline{I_{1ac}}-\overline{I_{2ac}}\right)^*\right. \\
&\left.-\left(\overline{V_C}-\overline{V_{L1}}\right)\cdot\left(-\overline{I_{1ac}}\right)^* - \left(\overline{V_C}-\overline{V_{L2}}\right)\cdot\left(-\overline{I_{2ac}}\right)^*\right] \qquad (21) \\
&= \frac{\left(CL_2\omega^2-1\right)V_{1acd}^2 + \left(CL_1\omega^2-1\right)V_{2acm}^2 + 2V_{1acd}V_{2acd}}{\omega\left(L_1+L_2-CL_1L_2\omega^2\right)}
\end{aligned}
$$

The "-" before $\overline{I_{1ac}}$ and $\overline{I_{2ac}}$ in (21) means the opposite current direction referred to Fig. 1 when calculating the complex power. Make (21) equal to zero, then substitute (2), (3) and (15) into it, the following equation can be obtained

$$
s = f(C) = \sqrt{\frac{CL_1\omega^2-1}{CL_2\omega^2-1}} \qquad (22)
$$

Equation (22) means that the step ratio is the function of capacitance C, and inductances L_1 & L_2. Given that the inductors are connected in series in the AC grid, it is not applicable to change them; thus, (22) is solely the function of capacitance C.

Then, we can conclude that using an optimal capacitor $C_{\min}$ calculated from (20), a specific refined step ratio $s_{refined}$ is possible. If we can change the step ratio s accordingly, (21) can be close to zero. As a result, the power loss will decrease.

C. Recalibrate Tap Considering the Impact of Transformer

The change of s can be mathematically achieved by either tuning V_{1acm} or V_{2acm}. In practice, using a tap-changeable transformer to adjust V_{1acm} is convenient. Although it is possible to ensure Q_2=0 by modulating V_{2acm}, the Q_1 could be large under partial loads at this moment. It still needs to tune the transformer and capacitor banks to decrease it.

On the other hand, with the interface of a transformer, the AC system can work at arbitrary voltage, so it is advisable to install the tap changer on the secondary side of the transformer while connecting the primary side to PCC. A real transformer is not an ideal ratio changer. Therefore, the impact of windings needs to be considered. The voltage drop on leakage inductance and winding resistance decreases the output voltage. As a consequent, the step ratio of LCL circuit cannot be kept at the refined value.

The equivalent transformer model of phase A is shown in Fig. 3. The Γ model is applied for its simple configuration. The v_p and v_s mean the primary and secondary voltage respectively. Related tap size is presented by k. L_m and R_m are the magnetizing inductance and resistance respectively, while $k^2L_{L\_tot}$ and k^2R_{CuL} represent the total leakage inductance and total winding resistance seen from secondary side. The coefficient k^2 is due to the secondary base impedance $Z_{base2}=(kV_{s\_rms})^2/S_{base}$ (V_{s_rms} is set to V_{1acm} as a transformer parameter now: the rms value of v_s).

1) Solution 1

Considering a more practical situation, one needs to recalibrate k. After applying the KVL in phasor domain, we obtain (23):

$$k\overline{V_s} = \overline{V_{1ac}} + k^2\left(R_{CuL} + j\omega L_{L\_tot}\right)\cdot\overline{I_{1ac}} \qquad (23)$$

Remember that the phase is locked with $\overline{V_{1ac}}$, and the purpose is zero reactive power. Then (23) can be derived to (24):

$$kV_{1acm}\angle\theta = s_{re\_pu}V_{1acm} + \frac{k^2\left(R_{CuL} + j\omega L_{L\_tot}\right)\cdot P_{part}}{s_{re\_pu}V_{1acm}} \qquad (24)$$

In which, the s_{re_pu}=$s_{refined}$/s_r. Equation (24) informs that the power consumption of leakage inductance and windings could be compensated by adjusting the amplitude of $\overline{V_s}$; thus, the k. After taking the real part of (24), the expression of k is as (25):

$$k = \frac{\sqrt{V_{1acm}^2 - \alpha - \sqrt{\left(V_{1acm}^2 - \alpha\right)^2 - 4\beta^2\chi^2}}}{\sqrt{2}\beta}$$

$$\begin{cases} \alpha = 2R_{CuL}P_{part} \\ \beta = \sqrt{R_{CuL}^2 + \omega^2 L_{L\_tot}^2}\,P_{part}\Big/\left(s_{re\_pu}V_{1acm}\right) \\ \chi = s_{re\_pu}V_{1acm} \end{cases} \qquad (25)$$

The χ in (25) is the required secondary voltage after tapping the transformer, and it reflects the $s_{refined}$=$V_{1acm\_refined}$/V_{2acm}. If we check (20), (22) and (25), the k and $s_{refined}$ are the functions of P_{part}. It means that an LCL-converter-based system is able to work under different load conditions with certain $s_{refined}$ and k: a minimal required capacitor and a transformer tap selection.

2) Solution 2

If we examine (23) and (24), we can find that they are obtained under the assumption that only active power is imported from transformer secondary. Therefore, the reactive power required by the transformer is totally provided by the primary side, thus the outer AC grid. In order to save the capacity of transmission line system, it is also favorable to use the capacitor banks to offer the transformer the reactive power.

Similar to the deduction of (22), we can have (26) considering the leakage inductance as a part of LCL:

$$s_{refine} = s_{re\_pu}\cdot s_r = \sqrt{\frac{C\left(k^2 L_{L\_tot} + L_1'\right)\omega^2 - 1}{CL_2\omega^2 - 1}} \qquad (26)$$

After comparing (26) and (22), the L_1 is divided in two parts: the fixed part L_1' and the changeable part $k^2L_{L\_tot}$. The L_1' should be L_1-L_{L_tot}, so under full load k= s_{re_pu}=1 (assume the transformer is lossless), (26) is equal to (22). This mathematical transformation simplifies the design: as the leakage inductance is given, one could follow the procedure in the upcoming chapter, then use the obtained L_1 to find L_1', and replace L_1' into the LCL circuit. More importantly, the k can be represented:

$$k = \sqrt{\frac{CL_1'\omega^2 - 1}{s_r^2\left(CL_2\omega^2 - 1\right) - CL_{L\_tot}\omega^2}} \qquad (27)$$

The only difference between *Solution 1* & *2* is the source of the reactive power required by the transformer, as Fig. 4 depicts: for the *Solution 1*(Sol.1) the reactive power is imported from primary side (Q_p), but from capacitor (Q_1) for the *Solution 2*(Sol.2).

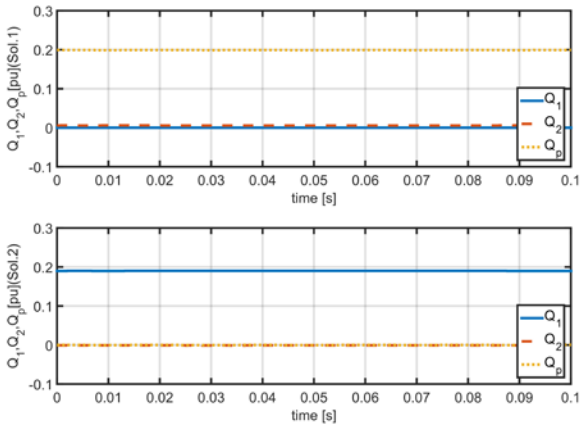

Fig. 4. The reactive powers for the Solution 1 and 2 (P=1pu).

D. Performance of DC Voltage Control Converter

In an HVDC network, it is understandable that the power flow is determined by the DC voltage, which is significant for keeping an HVDC system from collapsing. The converter that is responsible for controlling DC voltage works as a slack bus in an AC system.

If an LCL-VSC converter is assigned to manipulate the DC voltage for the whole grid, it is unlikely to make it work with full load, especially for a multi-terminal HVDC system. Otherwise, there will be a large amount of reactive power exchanging

between LCL circuit and converter bridge when there is only a small amount of active power transferred through it. Therefore, it is advisable to design a voltage control converter at 120%-150% P_{part} to cope with power floating situation. For example, a converter controlling DC voltage works at 400MW (rated at 800MW), but the LCL circuit could be over rated to 500MW or 600MW.

III. The Effect of *S* on The Performance of Converter

A. Selection of Original s and Derating of Converter

As a design parameter, the step ratio *s* could be selected at random if the converter is required to work at rated power. However, attention must be paid when disconnecting the capacitor under partial load. Fig. 5 shows the relationship between the required capacitor $C_{\min}$ and P_{part} with different LCL step ratio. We can find that if *s* is selected below 1, the optimal $C_{\min}$ is minus when P_{part} is lower than a certain level, which is physically impossible. Therefore, when the *s*- parameter needs to be designed lower than 1, it is advisable to plot Fig. 5 first and then determine the minimum partial load, e.g. the minimal partial load for s_r=0.85 is around 0.32pu.

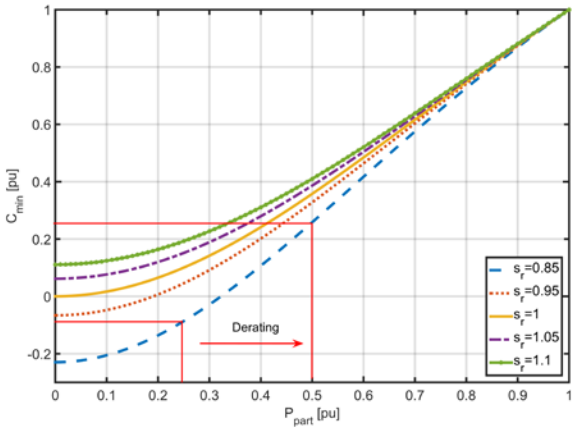

Fig. 5. Required capacitor versus P_{part} (r=1.02)

However, when a converter operates under a low partial load for specific purposes, the rated power of a converter should be set to a lower value. This derating actually moves the working point of P_{part} close to 1 on the abscissa. As shown in the same figure, when a converter is rated at 800MW, s_r=0.85, it may not operate at 200MW, as P_{part}=0.25pu. After derating the converter to 400MW, P_{part} becomes 0.5pu, $C_{\min}$ is around 0.25pu now.

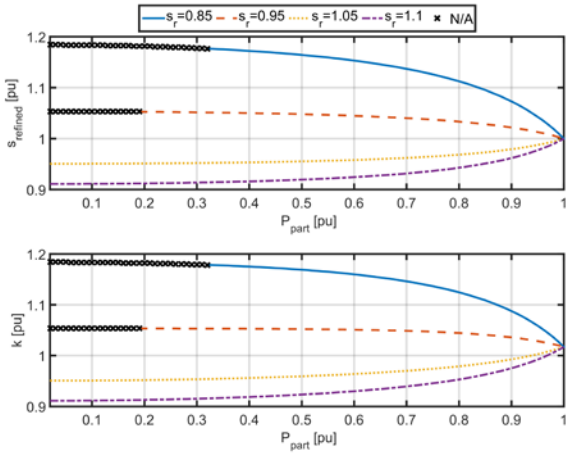

Fig. 6. Refined step ratio and tap versus P_{part} (r=1.02).

With the method of refining *s*-parameter, the procedures of designing LCL circuit can be given. Here, only the procedure of *Solution 1* is given, as that of *Solution 2* only has small difference.

1) Determine the DC voltage V_{2dc}, M_r, P_r, P_{part} and fault current ratio r.
2) Calculate V_{2acm} according to (8).
3) Calculate V_{1acm} according to (13), with selected rated s_r.
4) Calculate k_{1r} according to (17).
5) Calculate k_{2r} according to (16).
6) Calculate M_{dr} according either to (14) or (15).
7) Calculate M_{qr} according to (9).
8) Calculate k_{3r} according to (10).
9) Calculate L_1 and L_2 according to (3).

When under partial loads, follow the procedures:

10) Find the required $C_{\min}$ according to (19) and P_{part} (Derate a converter if it is necessary).
11) Refine *s* according to (22).
12) Find the tap according to (25).
13) Regulate the tap changer and capacitor accordingly.

For the sake of flexible operation, the capacitor could be connected into the network as capacitor banks ($10\times C_{\min}/10$ or $20\times C_{\min}/20$). Under partial-load situations, specific amount of capacitor banks could be disconnected. This method is preferred for the long-term load scheme of the whole network as it concerns power loss, and step 13) is relatively slow. On the other hand, the frequent adjustment may cause potential damage to the transformer and the capacitor. Thus, it is advisable to consider the economical factor and make a compromise when determining the control scheme of this type of converter.

Fig. 6 shows the diagrams of $s_{refined}$ and k versus P_{part} with different s_r. To obtain the k from (25), leakage inductance and copper losses are respectively set to 0.18pu and 0.006pu [13]. The black-cross parts on the traces in Fig. 6 result from the not available (N/A) operation regions under partial loads of s_r=0.95&0.85 in Fig. 5. Because of the leakage inductance and winding resistance, the value of $s_{refined}$ is slightly lower than k, even when P_{part}=1pu. The gap reflects the voltage drop on the winding. We can observe that the original s_r influences the working conditions of the transformer. Additionally, it is foreseeable that with the decrease of

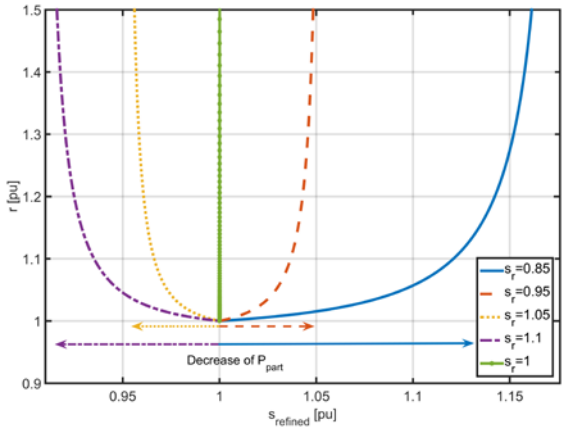

Fig. 7. Fault current ratio *r*[pu] versus refined *s*[pu] (r=1.02)

original s_r that lower than 1, the k and $s_{refined}$ will climb to unacceptable levels, which are vice versa for s_r higher than 1. The special condition s_r=1 makes k_{1r}= k_{2r}, which is not a preferable working condition for an LCL converter, and we can see it in next section.

B. The Effect of Optimization on Fault Current Ratio

The main purpose of LCL circuit is limiting fault current. Therefore, changing step ratio of former must have negligible or acceptable effect on the latter.

We can obtain the relationship between r and s according to (17) and (22), which is expressed as

$$r=\left\{1-\left[\frac{(L_2-L_1)s}{L_2s^2-L_1}\right]^2\right\}^{-\frac{1}{2}} \tag{28}$$

The solution of r in pu are plotted in Fig. 7 (with different s_r). As aforementioned, the $s_{refined}$ is the function of P_{part}, and it is monotonic in Fig. 6. However, it is monotonic decreasing for the s_r<1, and monotonic increasing for s_r>1. The trace with a certain s_r in Fig.7 also shows the monotonicity, which is corresponding to that in Fig. 6. For these reasons, the domains of (26) are different under the considered s_r: they all start from $s_{refined}$=1pu but in different directions, and they are consistent with the decrease of partial load from P_{part}=1pu, which are categorized by arrows with different colors and line types.

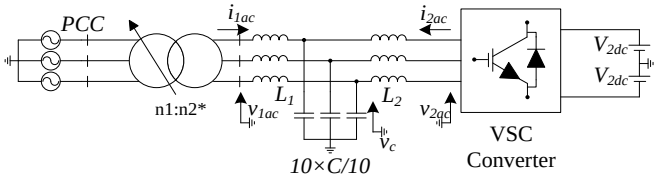

Fig. 8. Test system schematic

TABLE I
TEST SYSTEM DATA

Parameters	
DC voltage	400kV
PCC voltage	145kV
Three-phase rated activepower	800MW
Original step ratio *s*	1.05
Fault current ratio *r*	1.02
Inductor L1	0.1639H
Inductor L2	0.1681H
Capacitor C	49μF
Voltage V1ac	231.57kV
Voltage V2ac	220kV
Tansformer turn ratio	145/231.57*
Tansformer leakage reactance	0.18pu
Tansformer copper losses	0.006pu
Tap Changer	±1.25%×4
* means where the tap changer is put.	

TABLE II
STEP RATIO AND TAP CHANGER FOR PARTIAL LOAD CONDITIONS

Partial load	Connected C	s_refined	k	Tap Changer
0.1pu	0.1pu	1.0011	95.09%	1-4×1.25%
0.2pu	0.2pu	1.0024	95.19%	1-4×1.25%
0.3pu	0.3pu	1.0040	95.35%	1-4×1.25%
0.4pu	0.4pu	1.0060	95.60%	1-4×1.25%
0.5pu	0.5pu	1.0085	95.93%	1-3×1.25%
0.6pu	0.6pu	1.0118	96.39%	1-3×1.25%
0.7pu	0.7pu	1.0163	97.01%	1-2×1.25%
0.8pu	0.8pu	1.0229	97.90%	1-2×1.25%
0.9pu	0.9pu	1.0333	99.26%	1
1.0pu	1.0pu	1.0526	101.72%	1+1×1.25%

If the converter works for partial load, and the tap changer is switched accordingly, then fault current ratio increases, but it remains close to the r_{pu}=1 if P_{part} is kept within a range from 0.3pu to 1.0pu. If P_{part} drops out of this range, the solution of (26) will go at least 3 times higher than the desired fault current ratio, as the Fig.6 shows. In addition, if we solve (26) numerically, it will become infinite when s_r=1 no matter the $s_{refined}$ increases or decreases (the green solid line with diamond in Fig.7). Although the fault current cannot soar to infinite in practice, it will still be quite large when DC faults happen. Thus it would not be a preferable working condition. It is also possible to analyze the relation of fault current ratio and k when using the *Solution 2*. Yet it will have similar result which would be repetitive, then it is not shown here.

IV. SIMULATION VERIFICATIONS

Detailed simulation has been done on PSCAD/EMTDC platform to validate the theory in previous sections. The Type 4 model of MMC model [13] [14] is used to build the LCL-VSC converter and a point-to-point test system. The schematic of the test system is as Fig. 8 and the upper level control loop in [11] is adopted. The parameters of LCL-VSC converters are listed in Table I. Assume that the range of the tap changer is ±5% with step size 1.25% of each tap [15]. It should be noticed that the voltages tabulated in Table I are all in line-to-line rms values. As the original s_r is higher than 1, there is no need to derate the converter under partial loads. For the conciseness, the desired $s_{refined}$ and its corresponding tap under each partial load are listed in Table II based on *Solution 1* only.

A. *Refine s to Decrease Power Loss*

It is assumed that the capacitor is divided into 10 banks, and specific capacitor banks are disconnected for different partial-load conditions. The tap changer of transformer is adjusted according to Table II. Active power P of 0.7pu, 0.6pu, 0.5pu and 0.4pu are chosen for the simulation, the results are shown in Fig. 9 with their counterparts that only disconnect the capacitor banks. The subscript 'or' represents the data with original s_r, 're' means those with refined $s_{refined}$ and all the data are absolute values for easy comparing.

It can be seen that the reactive power Q_1 remains almost zero before and after refining the step ratio s. This phenomenon occurs because the v_1 is clamped, but v_2 will be changed automatically by the converter according to modulation indices. In contrast of Q_1, the Q_2 has a negative correlation with the partial load, if we notice the ordinate of each sub-graph. This can be explained by (22): when the capacitor banks are disconnected from the grid, the parameter k_{1r} and k_{2r} can no longer be provided by (22) with the original step ratio s_r. Equation (21) reveals the demand of reactive power on the converter side. After refining the step ratio of LCL circuit, the reactive power can be compensated. If we observe the graphs for the all chosen partial-load conditions, it is obvious that although Q_2 cannot reduce strictly to zero, the reactive power transfer has been quartered or halved. However, it is foreseeable that if the partial load is further decreased, Q_{2re} will climb closely to Q_{2or}. Therefore, for an LCL-VSC converter, the minimum partial load should be within an range from 0.5pu to 0.9pu.

The reactive power cannot be zero majorly because of the nonlinear dependency of partial load and P_{part}; it is not easy to find the theoretical value of required capacitor under each partial-load condition (especially when the design parameters are selected randomly in the first step), thus (16) or (22) cannot be strictly guaranteed in practice. However, we can achieve this if we numerically design the relationship of required capacitor versus partial load then find the ideal parameters for an LCL circuit.

TABLE III
POWER LOSS WITH S_r AND $S_{refined}$ UNDER DIFFERENT PARTIAL LOADS (RECTIFIER)

	Power Loss [MW]		Δ Loss[MW]
P [pu]	s_r (Loss1)	s_refined (Loss2)	Loss1-Loss2
0.1	0.2551	0.2538	0.0013
0.2	0.7613	0.7525	0.0088
0.3	1.4271	1.3950	0.0321
0.4	2.1933	2.1216	0.0717
0.5	3.0244	2.9300	0.0944
0.6	3.9085	3.7160	0.1925
0.7	4.7728	4.5848	0.1880
0.8	5.6421	5.3873	0.2548
0.9	6.6978	6.5218	0.1760
1.0	7.4358	7.4358	0.0000

TABLE IV
POWER LOSS WITH S_r AND $S_{refined}$ UNDER DIFFERENT PARTIAL LOADS (INVERTER)

	Power Loss [MW]		Δ Loss[MW]
P [pu]	s_r (Loss3)	s_refined (Loss4)	Loss3-Loss4
-0.1	0.2944	0.2933	0.0011
-0.2	0.8550	0.8435	0.0115
-0.3	1.5843	1.5568	0.0275
-0.4	2.4216	2.3687	0.0529
-0.5	3.3435	3.2478	0.0957
-0.6	4.3421	4.1439	0.1982
-0.7	5.2715	5.1139	0.1576
-0.8	6.2758	6.0165	0.2593
-0.9	7.4481	7.2582	0.1899
-1.0	8.3091	8.3091	0.0000

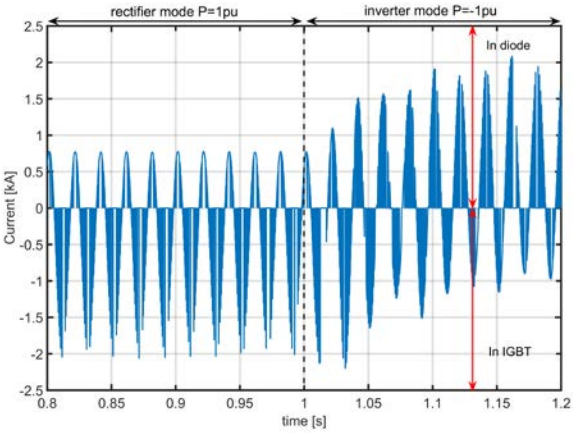

Fig. 10. Current in one sub-module of rectifier and inverter modes

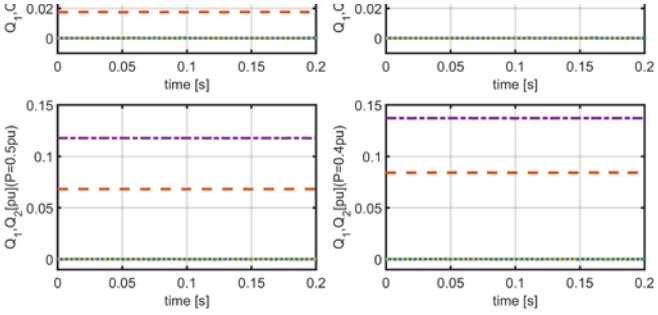

Fig. 9. Simulation of reactive power under different partial loads

To calculate the exact efficiency of a MMC converter is considerable complex, but the losses can be approximated [16]-[18]. In this paper, the estimation of power losses under different scenarios is achieved using the method described in [18]. The IGBT characteristics are of Mitsubishi CM1500HC-66R [19]. Table III and Table IV list the comparison of the power losses when converter working in rectifier and inverter modes respectively. The results show that proposed method can reduce the power

loss, therefore, increase the efficiency. In Table III and Table IV, the power losses from ±0.5pu to ±0.1pu are achieved by using *Solution 2*, which also show the effectiveness of tuning the transformer and the capacitor banks.

One should notice the unit of power loss is in MW order, which means a little reduction of it can have a considerable economic benefit. It is also predictable that this method can achieve similar or better performance when it is complemented with two/three-level converter, for the reason that these two types of converters have lower efficiency than MMC.

The different power losses in rectifier and inverter modes are because in every sub-module of MMC, the current goes through different paths, i.e. IGBT or diode, and they have different characteristics of resistance. Fig. 10 depicts the currents in one sub-module when converter transfers from rectifier mode (P=1pu) to inverter mode (P=-1pu) at 1s. We can observe that the current majorly goes through IGBTs in rectifier mode, while through diodes in inverter mode.

B. *Dynamics of LCL Converter During Load Change*

This section examines the dynamic behavior of the converter after changing the power reference using *Solution 1*. Assume the load requirement for a converter is decreased from 1pu to 0.5pu. Then the regulation is achieved by three procedures: 1) change the power reference of the converter; 2) disconnect capacitor banks of the LCL circuit; 3) adjust the tap of transformer. In order to verify the effects of these actions respectively, the simulation is divided into three parts: 1) change the reference from 1pu to 0.5pu at 0.2s; 2) disconnect the capacitors from 0.4s to 0.6s; 0.04s interval for disconnecting one bank; 3) adjust the tap from 0.95s to 1.45s.

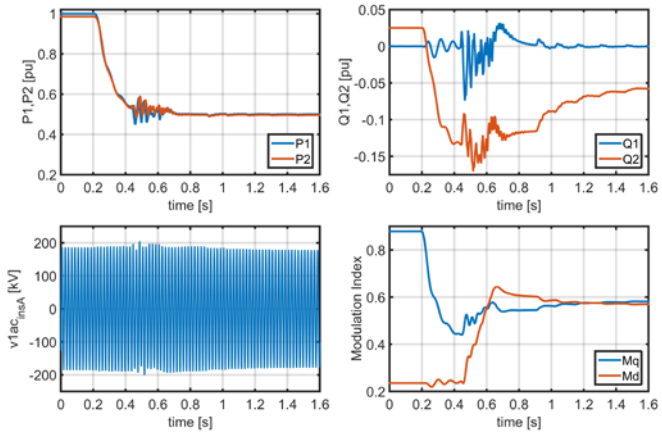

Fig. 11. Dynamics of LCL converter after changing power reference. Only the instantons voltage of phase A of v_{1ac} is shown.

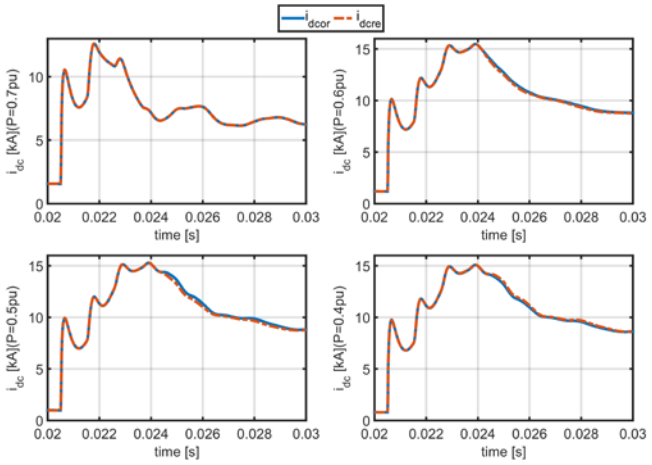

Fig. 12. Simulation of DC short-circuit current with refined step ratio

Fig. 11 informs that the converter can successfully re-stabilize. Although there are some fast transients during 0.4s to 0.7s, they are not significant. The step-by-step change of tap also arouses dynamic behavior, yet they are very smooth. The transformer links a strong system, so tapping the transformer does not cause fast transients in v_{1ac}. The three procedures cost 1.4s altogether as they are accomplished separately. This time can be shortened when all of them start at the same instant. Therefore, this method has good time response to cope with load change.

C. *Short-circuit Fault Current*

It has been analyzed that the fault current will be kept in an acceptable range when the converter does not operate at extremely low partial loads. In order to verify the theory, this simulation compares the DC short-circuit fault currents under different partial-load conditions. A pole-to-pole fault at 0.02s is implemented. A clarification is made here that the fault current ratio r is about the steady-state current after fault, and the transient peak value of the current depends on the nature of AC system and the fault instant, but the they are internally linked. Fig. 12 demonstrates the short-circuit currents under different partial load circumstances. Similarly, the subscript 'or' means the data with original s_r, 're' means those with refined $s_{refined}$.

In Fig. 12, the peak values of fault currents are same before and after applying this method. It is noticeable that under 0.7pu partial load, the transient peak value of fault current is lower than those of other conditions. As mentioned before, it is due to the fault instant and the nature of AC system. On the other hand, the steady state of fault currents under original and refined step ratio have good agreement. The conclusion can be made now that refining the step ratio by transformer tap changer has negligible influence on the LCL circuit's ability to restrain fault current. The *Solution 1* is applied in this simulation.

V. Conclusion

For the sake of high working efficiency, this paper presents an optimized design of LCL-VSC converter under partial-load conditions. The power balancing equation of LCL circuit is analyzed in depth, and the boundary of keeping zero reactive power transfer within LCL is derived correspondingly. The step ratio s can be modified theoretically for partial loads, and this can be achieved easily by using a transformer with tap changer. The leakage inductance and copper losses have been taken into account in this method, and they can be compensated based on the desired $s_{refined}$. The design procedures of LCL circuit are then proposed

based on the theory. The paper also proves that the original step ratio should be s>1, and the converter needs to be derated when s<1. Otherwise the converter would be physically impossible in low partial load.

The verification of this method was done in PSCAD/EMTDC environment. In order to achieve the best optimization, the range of partial load P_{part} of this type VSC converter should be from 0.5pu to 0.9pu. The results also show that refining the step ratio with a tap changeable transformer can improve the working efficiency of the LCL-VSC converter without sacrificing its capability of limiting fault current.

The application of LCL circuit cannot isolate DC fault feeding from AC side, but it is able to keep the DC fault current at a low level. This feature reduces the requirements of DC circuit breakers (DCCBs). With a lower power loss by applying the proposed method, the LCL-VSC converter will be a promising solution for future DC grids from both operating and protecting points of view.

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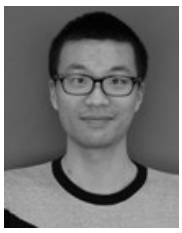

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