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Characterization and Compact Modeling of Nanometer CMOS Transistors at Deep-Cryogenic Temperatures

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***Abstract*—Cryogenic characterization and modeling of two nanometer bulk CMOS technologies (0.16-μm and 40-nm) are presented in this paper. Several devices from both technologies were extensively characterized at temperatures of 4 K and below. Based on a detailed understanding of the device physics at deep-cryogenic temperatures, a compact model based on MOS11 and PSP was developed. In addition to reproducing the device DC characteristics, the accuracy and validity of the compact models are demonstrated by comparing time- and frequency-domain simulations of complex circuits, such as a ring oscillator and a low-noise amplifier (LNA), with the measurements at 4 K.**

***Index Terms*—Cryogenic electronics, CMOS, cryogenic, cryo-CMOS, characterization, modeling, kink, 4 K, LNA.**

I. Introduction

CRYOGENIC electronics plays a fundamental role in several applications, such as spacecraft, high-energy physics experiments, metrology, superconductive astronomical detectors and, with the increased interest in quantum computing, the manipulation of quantum bits (qubits) [1]–[5]. Most qubits are placed in the coldest chamber of dilution refrigerators, where temperatures reach values in the range of 10-100 mK, in order to expose their quantum behavior and extend the lifetime of their quantum state. State-of-the-art quantum processors typically consist of a few qubits that are controlled and read out by general-purpose electronics operating at room-temperature [6]–[8]. Only a few components, such as the first amplification stages, operate at cryogenic temperatures (1-4 K) in order to reduce their noise level [9], [10]. Nonetheless, future quantum computers would require millions of qubits to run any algorithm with practical applications, such as the simulation of a complex molecule [11]. Thus, an enormous amount of room-temperature electronics and, consequently, an unpractical number of wires to connect such electronics to the qubits would be required. A viable alternative is to place the electronics much closer to the qubits [12]–[14]: a few circuits would operate at the qubit temperature (10-100 mK), while most of the electronics would be placed at 4 K, i.e. the lowest temperature at which existing dilution refrigerators can still provide a relatively large cooling power ($\approx$ 1 W). Among electronic technologies operating at those temperatures, only CMOS can provide the high level of integration required to reliably manipulate such a large number of qubits. However, although compact simulation models are crucial for the design of the high-performance circuits necessary for a large-scale quantum computer, the characterization and modeling of nanometer CMOS devices at cryogenic temperatures are not yet adequate. The use of nanometer CMOS nodes is particularly relevant to build low-power circuits for quantum-computing applications, since the handling of high-frequency and large-bandwidth signals is required for qubit control. As shown in Fig. 1, several CMOS technologies have been characterized at temperatures below 77 K [15]–[41], but only [24], [37] and [39] address quantum-computing needs, i.e. nanometer technologies (below 0.18 μm) necessary for high-speed circuits ($>$ 10 GHz), operating at 4 K or below where qubits can, in theory, still operate and the cooling power of state-of-the-art dilution refrigerator enables the placement of large integrated circuits. Furthermore, very few cryogenic models have been developed [29]–[39] with only [37] and [39] (of which this paper is an extension) recently focusing on the region of interest. In this paper,

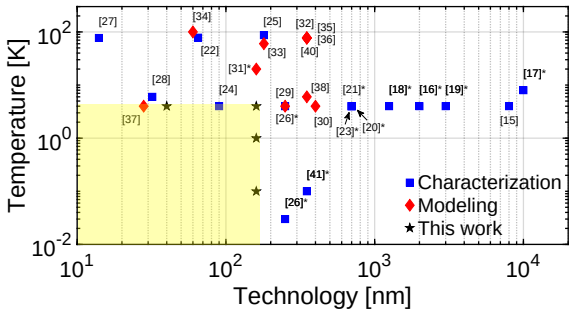

Fig. 1. Summary of CMOS technologies measured at cryogenic temperatures. The works on characterization are indicated by blue squares while attempts at modeling by red diamonds. The references with an asterisk showed kink.

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TABLE I
SUMMARY OF CHARACTERIZED DEVICES.

Technology	**SSMC 0.16 μm**		**ST 40 nm**	
Oxide	Thick	Thin	Thick	Thin
Nominal V_{DD} [V]	3.3	1.8	2.5	1.1
W/L [μm / μm]	2 / 1.61	2.32 / 1.6	1.6 / 1.35	1.2 / 0.4
	2 / 0.322	2.32 / 0.16	1.6 / 0.27	1.2 / 0.04
	0.4 / 1.61	0.232 / 1.6	0.32 / 1.35	0.12 / 0.4
	0.4 / 0.322	0.232 / 0.16	0.32 / 0.27	0.12 / 0.04

we present the characterization and SPICE modeling of two CMOS nanometer technologies (0.16-μm and 40-nm bulk CMOS) at 4 K, and for 0.16-μm devices also at 1 K and 100 mK [39]. Unlike prior works (see Fig. 1), we model, for the first time, the behavior of bulk CMOS devices at temperatures as low as 100 mK, and we validate the compact models at 4 K by comparing simulations and measurements of two complex circuits, namely a ring oscillator and a low-noise amplifier (LNA) for spin-qubit readout [42]. The paper is organized as follows: Section II describes the devices characterization; Section III discusses the cryogenic behavior and the related physics in detail; Section IV presents the modeling procedure and the resulting DC characteristics are compared to the measured ones; Section V presents the validation of the models with complex circuits and summarizes the effects of cryogenic cooling on technology parameters and on device figures of merit having an impact on future cryogenic-circuit designs; finally, conclusions are drawn in Section VI.

II. CHARACTERIZATION

Several transistors with different dimensions and different oxide thickness from both technologies (SSMC 0.16 μm, ST 40 nm) were tested at 4 K, as shown in Table I. Only a few 0.16-μm devices were cooled down to 1 K and 100 mK, namely one NMOS (W/L = 0.232/1.6) and two PMOS (W/L = 2.32/1.6 and W/L = 0.232/1.6), since other devices did not outlive the bonding required in the sub-Kelvin setup. An ST-500 probe station by Janis Research was used for 300 K and 4 K testing, while a CF-CS81 dilution refrigerator by Leiden Cryogenics was used for sub-Kelvin characterization. $I_D(V_{GS})$ and $I_D(V_{DS})$ characteristics are shown in Fig. 2, 3, 4, 5, Fig. 6, 7, 8, 9 and Fig. 10 for the two technologies.

As mentioned in Section I, mature CMOS processes have been characterized at cryogenic temperatures and the physics underlying several cryogenic effects has been explained. Our measurements closely match to previous observations for several aspects. A general increase in mobility ($\approx 2\times$), clearly visible in the long-channel devices of Fig. 3b-d and Fig. 7b-d, and threshold voltage ($\approx$ 30%) is observed. The former is due to an overall decrease in electron scattering, while the latter to an increase in ionization energy [43]. From 300 K to 4 K, the subthreshold slope (*SS*) improved by 3.8$\times$ for the 0.16-μm NMOS (Fig. 2) and 3.2$\times$ for the 40-nm NMOS (Fig. 6), thanks to the intrinsic temperature dependence of the diffusion current.

Furthermore, a jump in drain current, which is typically referred to as *kink*, is observed in the 0.16-μm thick-oxide short-channel NMOS in Fig. 5a-c. The voltage V_{DS} at which the kink occurs, $V_{DS-kink}$ is close to $V_{DD}/2$ and is bias

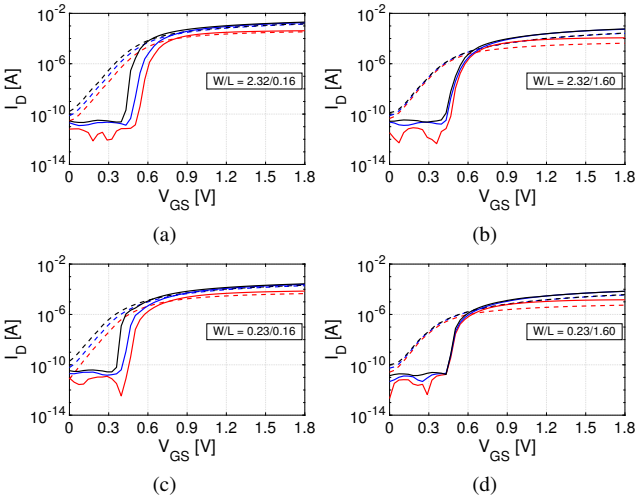

Fig. 2. Measured $I_D(V_{GS})$ characteristics of thin-oxide NMOS in 0.16-μm CMOS. V_{DS} = [0.1 V; 0.95 V; 1.8 V]. Solid line: 4 K; dashed line: 300 K.

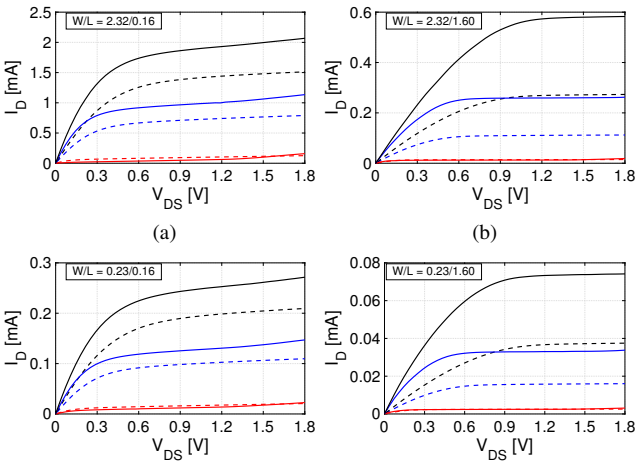

Fig. 3. Measured $I_D(V_{DS})$ characteristics of thin-oxide NMOS in 0.16-μm CMOS. V_{GS} = [0.68 V; 1.24 V; 1.8 V]. Solid line: 4 K; dashed line: 300 K.

dependent, moving to higher values for larger V_{GS}. The kink also causes a very steep subthreshold slope, as shown in Fig. 4a-c for $V_{DS} > 1.7$ V. This jump in current is not observed in all other PMOS and NMOS devices. Although no kink was measured in thin-oxide 0.16-μm NMOS transistors, an onset of the substrate-current body effect (SCBE), common in nanometer CMOS transistors, is present and occurring at a lower V_{DS} at 4 K as compared to 300 K (Fig. 3a-c).

In addition, when cooled down to 100 mK, the 0.16-μm devices showed proper operation, as shown in Fig. 10. In this case, mobility does not significantly change with respect to 4 K and the subthreshold slope improves by only 2.3$\times$ when reducing the temperature from 4 K to 100 mK.

Finally, few devices showed a difference in drain current in the subthreshold region when V_{GS} was swept from low to high or from high to low values. Such *hysteresis* will be discussed in Section III. For clarity, only the forward sweep is shown in Fig. 2, 3, 4, 5, Fig. 6, 7, 8, 9 and Fig. 10.

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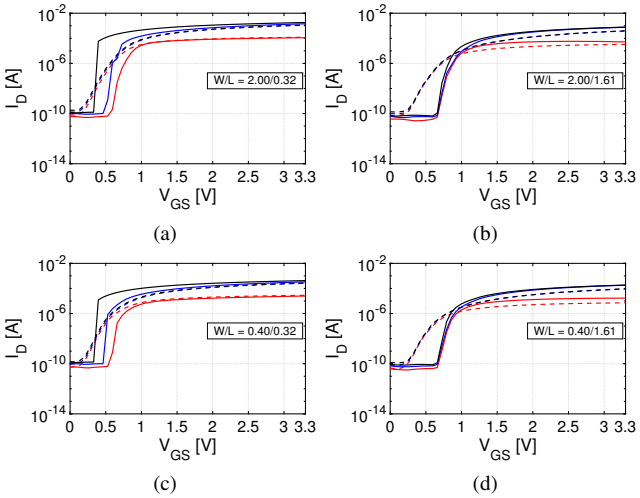

Fig. 4. Measured $I_D(V_{GS})$ characteristics of thick-oxide NMOS in 0.16-μm CMOS. V_{DS} = [0.1 V; 1.7 V; 3.3 V]. Solid line: 4 K; dashed line: 300 K.

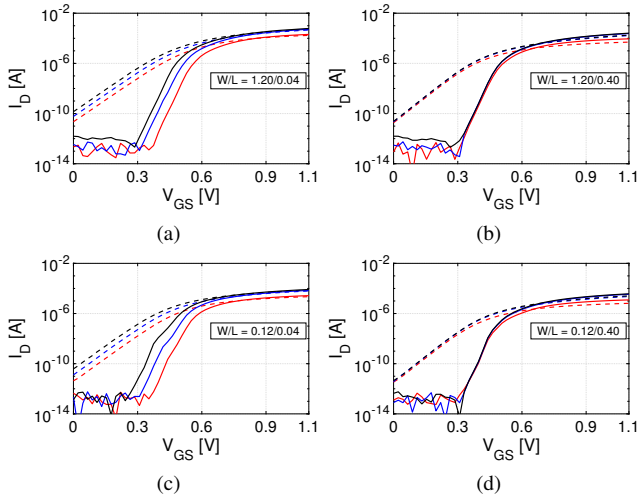

Fig. 6. Measured $I_D(V_{GS})$ characteristics of thin-oxide NMOS in 40-nm CMOS. V_{DS} = [0.1 V; 0.6 V; 1.1 V]. Solid line: 4 K; dashed line: 300 K.

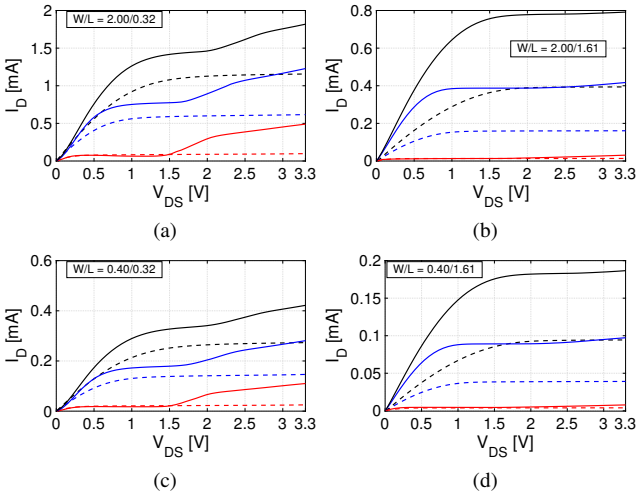

Fig. 5. Measured $I_D(V_{DS})$ characteristics of thick-oxide NMOS in 0.16-μm CMOS. V_{GS} = [1.05 V; 2.17 V; 3.3 V]. Solid line: 4 K; dashed line: 300 K.

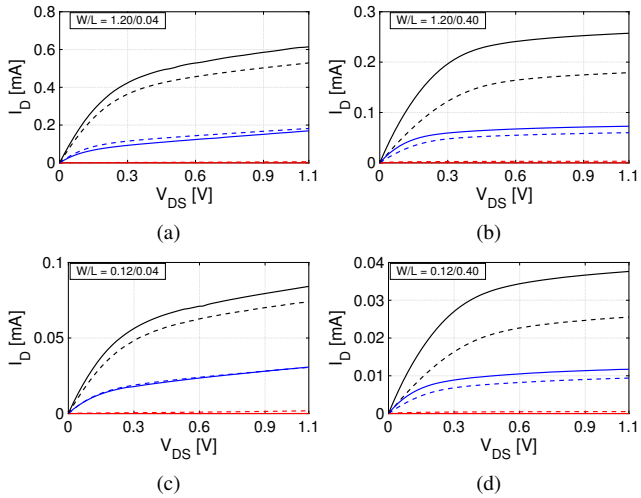

Fig. 7. Measured $I_D(V_{DS})$ characteristics of thin-oxide NMOS in 40-nm CMOS. V_{GS} = [0.43 V; 0.76 V; 1.1 V]. Solid line: 4 K; dashed line: 300 K.

III. Analysis of the Cryogenic Behavior

In this section, the differences between room-temperature and cryogenic behavior are discussed.

A. Kink Effect

For bulk CMOS transistors at 4 K, the kink (see Fig. 5a-c) was first explained in [18]. At large V_{DS}, the generation of electron-hole pairs due to impact ionization leads to a multiplication current, flowing in part to the drain and the rest to the bulk (I_{bulk} in Fig. 11c). At the same time, an increase in the substrate resistance R_{bulk} is observed due to carrier freeze-out, which appears at temperatures below 70 K and is exemplified by the large resistance of the n-well resistor in Fig. 11b. The multiplication current flowing through R_{bulk} causes the bulk potential to raise, thus producing a threshold voltage drop and, consequently, the current jump measured in Fig. 5a-c. Nonetheless, after reaching the kink, the current jump tends to flatten out as the drain-bulk-source lateral bipolar transistor starts conducting, with the bulk-source junction equivalent to the forward-biased base-emitter junction, thus diverting most of the drain ionization current and leading to a gradual saturation of I_{bulk}, as can be seen in the bulk current plot of Fig. 11c. Furthermore, the voltage at which the kink occurs, $V_{DS-kink}$, shifts to higher V_{DS} for larger gate voltages V_{GS}. This can be explained by considering that a higher V_{GS} leads to a larger surface scattering and, hence, to a more pronounced mobility degradation, which mitigates the impact ionization and, consequently, the value of V_{DS} where the kink occurs.

It is important to note that the kink is observed only in two thick-oxide NMOS transistors, namely W/L = 2/0.322 and W/L = 0.4/0.322 in the 0.16-μm CMOS technology. Prior works shown in Fig. 1 report the presence of the kink only in mature technologies, mostly for feature sizes larger than 0.35 μm and at temperatures below 100 K. The reason for

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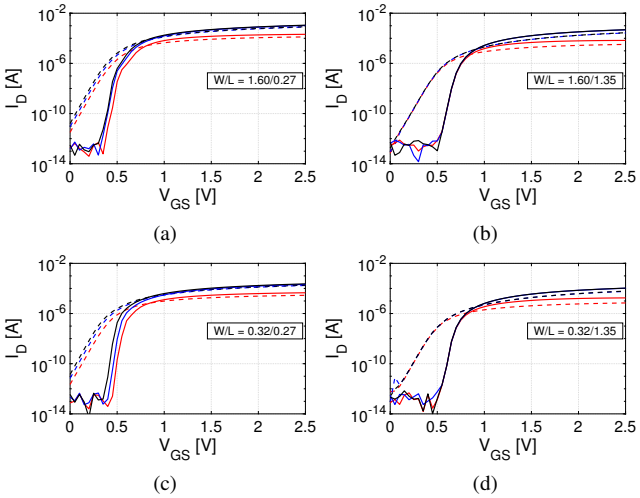

Fig. 8. Measured $I_D(V_{GS})$ characteristics of thick-oxide NMOS in 40-nm CMOS. V_{DS} = [0.1 V; 1.3 V; 2.5 V]. Solid line: 4 K; dashed line: 300 K.

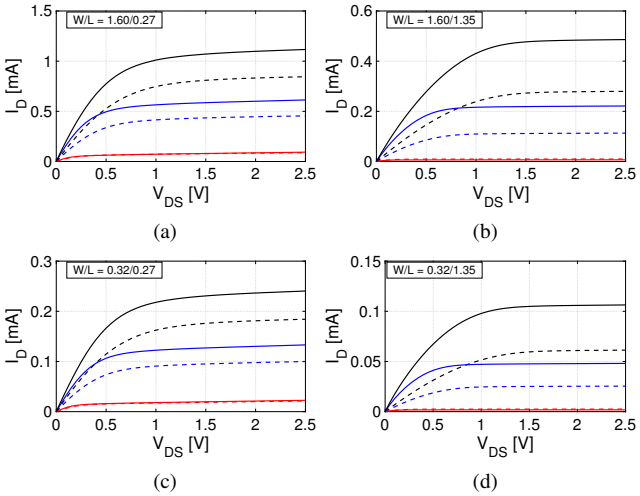

Fig. 9. Measured $I_D(V_{DS})$ characteristics of thick-oxide NMOS in 40-nm CMOS. V_{GS} = [0.85 V; 1.68 V; 2.5 V]. Solid line: 4 K; dashed line: 300 K.

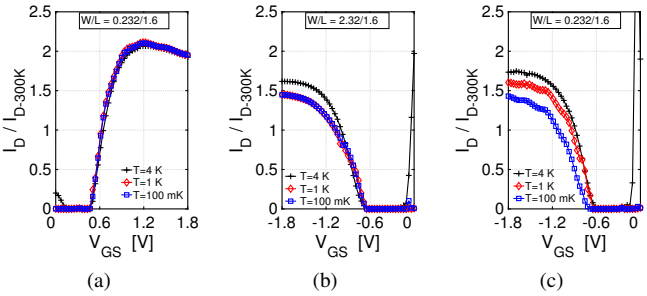

Fig. 10. Measured characteristics of the three devices tested at 1 K and 100 mK compared to 4 K; (a) NMOS, $V_{DS} = 1.8\ V$; (b)-(c) PMOS, $V_{DS} = -1.8\ V$. Every curve is normalized to 300 K to remove chip-to-chip spread since the 4 K measurements were done on a different chip placed in the probe station.

this technology dependence is strictly related to transistor scaling. Traditional scaling rules require thinner oxide thick-

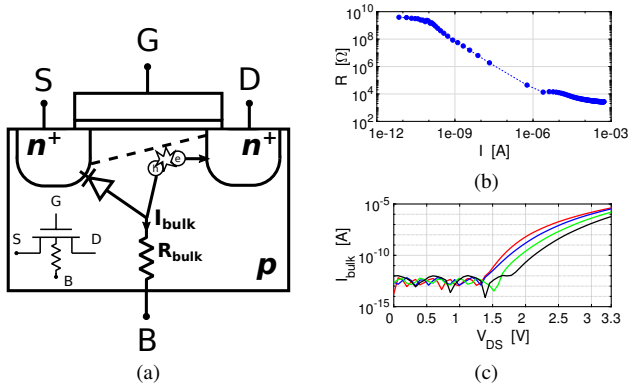

Fig. 11. (a) Cross-Section and schematic representation of the cause of kink effect at 4 K; (b) N-well resistance versus current at 4 K; the resistance value at 300 K is 3.5 kΩ; (c) $I_{bulk}(V_{DS})$ of thick-oxide NMOS, W/L = $2.32/0.322$ at 4 K.

ness to keep a constant vertical electric field. However, the vertical electric field in nanometer technologies has inevitably increased in spite of a proportional scaling of supply and gate insulator thickness, leading to higher mobility degradation (due to surface scattering, for example) that mitigates the impact ionization effect and, hence, the occurrence of the kink. Additionally, the substrate doping of nanometer technologies is considerably higher due to channel engineering, threshold-voltage control, lightly doped drain (LDD) [20], pocket and deep retrograde implants, which help to reduce the drastic increase of the bulk resistance and, hence, the kink effect. Finally, supply voltages below 1.2 V inevitably prevent the kink from occurring because carriers cannot acquire enough energy through impact ionization to overcome the silicon bandgap. All these effects combined explain why we observe the kink only in thick-oxide short-channel 0.16-μm NMOS devices. This type of transistor, in fact, closely resembles a 0.35-μm-CMOS device and does not yet "benefit" from the scaling consequences explained above. Long-channel devices (Fig. 5b-d) do not show a kink because the longitudinal electric field never reaches the required critical electric field to trigger impact ionization. Finally, no kink is observed in 0.16-μm thick-oxide PMOS because their intrinsic lower mobility suffices for the complete suppression of the kink.

B. Sub-Kelvin regime

Measurements at 100 mK* showed proper transistor operation, as mentioned in Section II. Fig. 10 shows the $I_D(V_{GS})$ characteristics at 4 K, 1 K and 100 mK of the three transistors listed in Section II normalized to the 300-K measurement to remove any chip-to-chip spread between the devices measured at 4 K in the probe station and those measured in the dilution refrigerator down to 100 mK. It can be observed that the three characteristics in Fig. 10 are almost overlapping for the three transistors, meaning that mobility and threshold voltage do not change significantly at temperatures below 4 K. For the PMOS, the current slightly diminishes below

*The temperature was set to 40 mK but because of self-heating in the transistors, the temperature was around 100 mK for most of the measurement time.

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4 K. The mobility degradation below 4 K is attributed to the strong contribution of carrier-to-carrier and neutral-impurity scattering, which increase at low temperature, as also observed in [44], [45]. Finally, the saturation in threshold voltage is most likely due to the fact that, once freeze-out is reached, the amount of ionized atoms does not significantly change and, hence, the threshold voltage V_T is not notably influenced.

C. Hysteresis

Although it has been a major concern in the past for several technologies operating at cryogenic temperatures [23], [46], [47], no significant hysteresis was observed in most of the tested devices, with the exception of those that showed a kink at 4 K and for the long-channel 0.16-μm PMOS at 100 mK.

For the thick-oxide NMOS (W/L = 2/0.16), hysteresis occurs in the subthreshold region, as can be observed in Fig. 12 where a voltage shift in V_{GS} of around 0.15 V is measured. This happens only for $V_{DS} > 1.7$ V, i.e. after the kink. This can be explained by considering that before V_{GS} overcomes the threshold voltage, negligible free charge is present at the surface, thus preventing significant impact ionization. As V_{GS} rises and the channel is being formed, the mechanism of avalanche due to impact ionization builds up as well. Once the channel is formed and the current is not negligible (at $\approx$ 0.4 V as shown in the forward-sweep curve in Fig. 12), the threshold voltage decreases due to the kink effect (see Section III-A), reaching the final value once the avalanche current is maximum, which happens when the channel is in strong inversion. When V_{GS} is swept in the other direction (red-circled line in Fig. 12), impact ionization is already occurring at large V_{GS} and, consequently, the threshold voltage V_T is already approximately 0.22 V. The V_{GS} must diminish below this value to completely turn off the transistor.

At sub-Kelvin temperature, a softer hysteresis can be seen in Fig. 13. However, although the temperature of the dilution refrigerator was set to 40 mK, the temperature of the sample varied between 40 mK and 100 mK due to self-heating. This could partially explain the presence of hysteresis in Fig. 13 as a measurement artifact. Further investigations are necessary though, to fully explain the cause of a possible hysteresis in the sub-Kelvin regime. In conclusion, we recognize that hysteresis is not a significant issue in nanometer nodes, since it emerged in very few tested devices.

D. Subthreshold Slope

The subthreshold slope is expected to become steeper with decreasing temperature due to the exponential dependence of I_D,

$$I_D \approx I_0 \cdot e^{\frac{q(V_{GS}-V_T)}{nk_BT}} \tag{1}$$

where I_0 is the saturation current, q the electron charge, k_B the Boltzmann constant and T the temperature. The expression of the subthreshold slope results, therefore:

$$SS(T) = \left[\frac{\partial \log(I_D)}{\partial V_{GS}}\right]^{-1} = \ln(10)\frac{nk_BT}{q} \tag{2}$$

From the Eq. 2, it can be concluded that the subthreshold slope should be linearly dependent on T. However, according

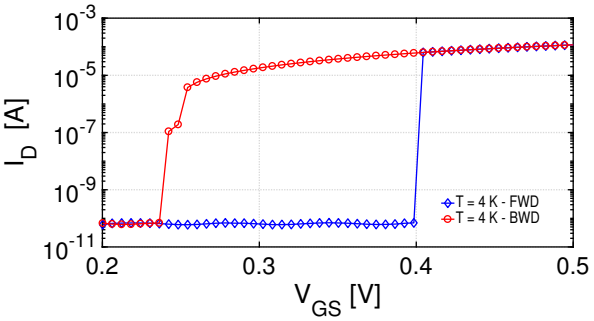

Fig. 12. Forward (FWD) and backward (BWD) sweep of $I_D(V_{GS})$ in subthreshold region for the thick-oxide NMOS (W/L = 2.32/0.16) at 4 K at $V_{DS} = 3.3\ V$. Hysteresis causes a shift of $\approx$ 0.15 V.

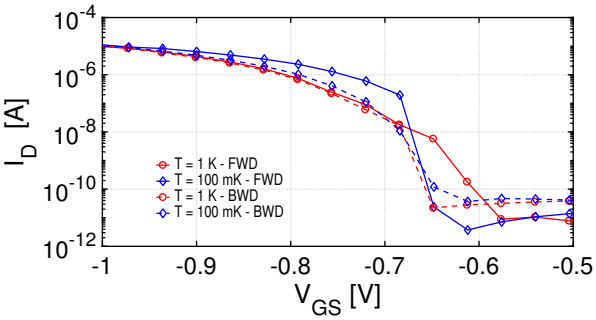

Fig. 13. Forward (FWD) and backward (BWD) sweep of $I_D(V_{GS})$ for the thin-oxide PMOS (2.32/1.6) at 1 K and 100 mK at $V_{DS} = -1.8\ V$.

to the literature [15], the subthreshold slope follows the proportionality with the temperature down to $\approx$ 77 K, as predicted by Eq. 2, but it becomes strongly sub-linear at lower temperatures. The sub-linear trend matches our observation of the NMOS SS (Fig. 2), which improves by only $\approx 3.8\times$ from 300 K to 4 K. This can be attributed to the factor n and its dependence on T. As a proxy for the subthreshold slope, n is

$$n = 1 + \frac{C_{dep}}{C_{ox}} + \frac{C_{it}}{C_{ox}} \tag{3}$$

where C_{dep}, C_{it} and C_{ox}, are the depletion, interface-states and oxide capacitances per device area, respectively. The temperature dependence of n can be explained by the non-negligible increase of interface states at cryogenic temperatures, as reported in [48]. By extracting the value of n from the measurements at temperature T^* as

$$\frac{SS(300\ K)}{SS(T^*)} = \frac{n_{300K}}{n_{T^*}} \cdot \frac{300\ K}{T^*}, \tag{4}$$

we obtain the plot of Fig. 14 for the 0.16-μm PMOS (W/L = 2.32/1.6). In the figure, we can observe a drastic increase of n below 1 K, which is in agreement with the theory in [48]. In conclusion, a summary of subthreshold slope and n of a PMOS (W/L = 2.32/1.6) versus temperature is shown in Fig. 14.

IV. Modeling

No commercial compact model can predict the behavior of CMOS at cryogenic temperatures and hence, commercial

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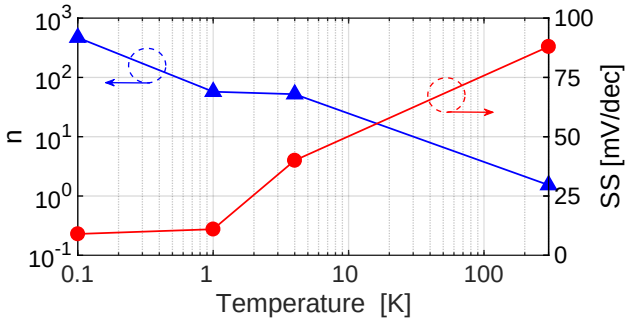

Fig. 14. Subthreshold slope (SS) and extracted ideality factor n of the PMOS (W/L = 2.32/1.6) across temperature.

models cannot be used for the design of circuits operating at cryogenic temperatures. To overcome that limitation, we propose a model for cryogenic CMOS devices based on existing compact models. Our modeling effort aims at demonstrating the capability of standard compact models to cover cryogenic operation without significant modifications. More specifically, we adopted MOS11 [49] and PSP [50] for the 0.16-μm and the 40-nm CMOS technology, respectively, since they were provided by the respective foundry for the standard temperature range. The development of PSP was inspired by MOS11 and therefore the modeling procedure could be mirrored, as will be presented below. Moreover, being MOS11 and PSP derived from surface-potential equations, they are possibly better suited to cover device behaviors in extreme conditions without trading off accuracy for model continuity.

As shown in Section II, the 40-nm CMOS technology did not show any specific cryogenic non-ideality. Therefore, the modeling procedure consisted in updating the parameters in the foundry-provided models with the new values extracted from the cryogenic characterization. On the contrary, some 0.16-μm transistors showed strong non-idealities, such as the kink, which are not included in standard models for bulk CMOS. As a consequence, the modeling of those devices required the addition of extra electrical components to capture semiconductor physics at 4 K. In particular, a non-linear resistor was added in series to the bulk of the transistor to emulate freeze-out of the substrate (see Fig. 11) and, consequently, generate the kink at the appropriate V_{DS}. This, in addition to the extracted parameters, enabled the modeling of the DC characteristics at every bias point.

A. Extraction and modeling procedure

To model the cryogenic behavior of the devices in Section II, we proceed in the following order: first, the temperature of the simulator was set to -200 °C in order to match the measured and simulated subthreshold slope. At the same time, the temperature-fitting parameters of the MOS11 model were zeroed to prevent the simulator from extrapolating meaningless values of mobility, V_T and other parameters at those temperatures. This was not necessary for the PSP. We then set the parameters related to the threshold voltage V_T (VFB for MOS11, DELVTO for PSP) and mobility μ (BETSQ for MOS11, FACTUO for PSP), since they have the largest influence on I_D,

TABLE II
LIST OF MODIFIED PARAMETERS FOR THE COMPACT MODEL AT 4 K.

MOS11 parameters for 0.16-μm CMOS					
BETSQR	VFBR	THESRR	SDIBLO	ALPR	KOR
THESATR	THERR	A1R	A2R	A3R	
PSP parameters for 40-nm CMOS					
FACTUO	DELVTO	THEMUO	THESATO	RSW1	CFL
ALPL	MUEO	FBET1			

as observed from the measurements. After this, the parameters that impact mobility degradation were modified; in particular, those related to surface scattering (THESRR for MOS11, THEMUO for PSP), and to velocity saturation (THESATR for MOS11, THESATO for PSP). This enabled us to match the curves at high V_{GS} where the characteristics are degraded by these effects. In combination to mobility degradation, impact ionization was enhanced through the parameters A1R, A2R and A3R for the 0.16-μm technology in order to reproduce the kink or the onset of SCBE, while this was not necessary for the 40-nm technology. At this point, the relative error between simulation and measurement is below 20% for most of the curves. The remaining parameters listed in Table II but not mentioned above were modified to fine-tune the models, to compensate for other second-order effects (e.g. channel-length modulation) and, hence, to reduce the mismatch further below 10% in almost all the bias regions.

During the whole procedure, the bulk contact of the thick-oxide 0.16-μm NMOS transistor was connected to a high-impedance non-linear resistor implemented as a look-up table. The data of such look-up table were extracted from the measurement of the n-well resistor in Fig. 11b and scaled by a constant coefficient at the end of the modeling procedure to tune the magnitude of the current jump and $V_{DS-kink}$. The final implemented resistor has an impedance of 100 kΩ at I_{bulk} = 1 nA.

The modeling of the devices at 100 mK followed the same procedure, proving that the models are scalable with temperature. It has to be noted that the parameters related to the dynamic behavior of the transistor were not modified and hysteresis was not modeled since the majority of the devices did not show this effect. Finally, although the extraction procedure described above has not yet been automated, we believe that, especially for the majority of the devices that do not show kink, the standard extraction procedure for the respective model can be adopted.

B. Modeling results

The results of this parameter-fitting procedure are shown in Fig. 15 and Fig. 16 where both 4 K and 100 mK measurements (dashed lines) and simulations based on the newly proposed models (solid lines) are superimposed. Good matching (relative error $<$ 10%) of simulations and experimental data is obtained at every bias point, in both weak and strong inversion, with a single set of parameters for each device. However, the accuracy of the model is limited in the moderate-inversion region, e.g. in Fig. 15f for V_{GS} = 0.6 V $\rightarrow$ 1 V, because both models employ a smoothing function to continuously merge the equations for weak and strong inversion, which was not modified in this work.

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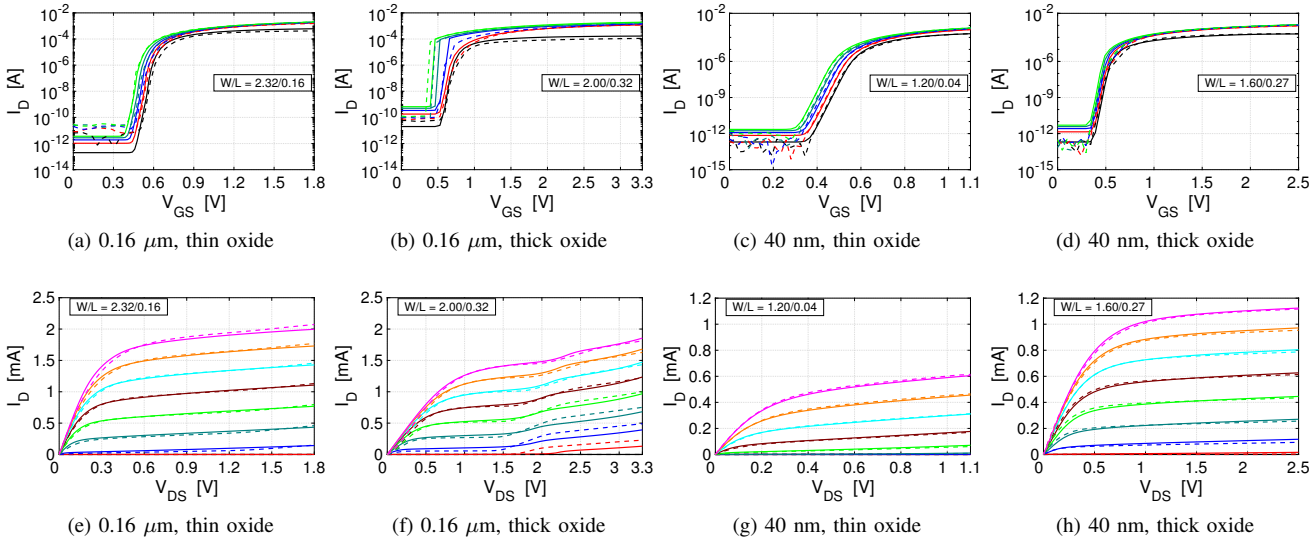
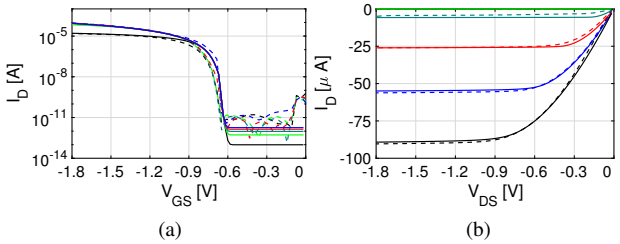


(a) 0.16 μm, thin oxide (b) 0.16 μm, thick oxide (c) 40 nm, thin oxide (d) 40 nm, thick oxide

(e) 0.16 μm, thin oxide (f) 0.16 μm, thick oxide (g) 40 nm, thin oxide (h) 40 nm, thick oxide

Fig. 15. Models (solid) and measurements (dashed) at 4 K; W/L in μm. (a,e) $I_D(V_{GS})$ and $I_D(V_{DS})$ of 0.16-μm thin-oxide NMOS; (b,f) $I_D(V_{GS})$ and $I_D(V_{DS})$ of 0.16-μm thick-oxide NMOS; (c,g) $I_D(V_{GS})$ and $I_D(V_{DS})$ of 40-nm thin-oxide NMOS; (d,h) $I_D(V_{GS})$ and $I_D(V_{DS})$ of 40-nm thick-oxide NMOS.



(a) (b)

Fig. 16. Models (solid) and measurement (dashed) of 0.16-μm thin-oxide PMOS (W/L = 2.32/1.6) at 100 mK. (a) $I_D(V_{GS})$, $V_{DS} = -1.8 \rightarrow -0.09$ V; (b) $I_D(V_{DS})$, $V_{GS} = -0.3 \rightarrow -1.8$ V.

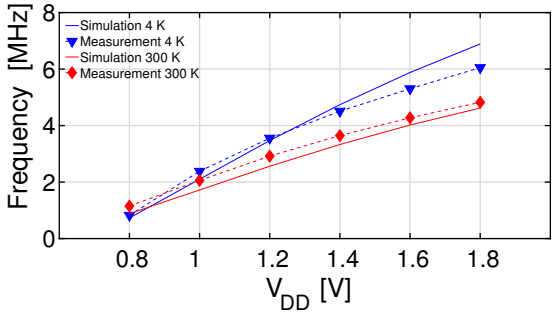


Fig. 17. Ring oscillator frequency versus supply voltage (V_{DD}) at 300 K and 4 K. Measurements (dotted lines) and simulations (solid lines) are compared with the compact model presented in Section IV.

V. Model Validation

A. Circuits at cryogenic temperature

A 2703-stages ring oscillator in 0.16-μm CMOS has been tested at 4 K. Its measured oscillation frequency is shown in Fig. 17 for both 300 K and 4 K for different supply voltages and compared to the simulation employing the proposed model. The higher driving capability reduces the gate delay by almost 30%. The simulation was performed on a different process corner with respect to the curves in Fig. 15, since the circuit was fabricated on a different die. The room-temperature measurements and simulation were firstly compared to calibrate the cryogenic model. After this calibration, the output frequency f_{osc} is in good agreement with simulation over a wide range of supply voltages. Faster saturation of the measured f_{osc} at high V_{DD} is observed at 4 K compared to simulation. This can be attributed to the increased poly depletion region, which leads to a smaller depletion capacitance in series with the thin-oxide and therefore a reduced effective gate-channel voltage (not included in our modeling procedure) [24]. This reduction in effective V_{GS} leads to I_D and, correspondingly, f_{osc} tapering off.

In order to further validate the model with a complex real-life circuit, a 0.16-μm-CMOS low-noise amplifier based on the noise-canceling topology [51] was designed using the cryogenic models developed in this work. A comprehensive description of the circuit and its design flow together with extensive experimental characterization have been reported in [42]. Here, we focus our attention on the accuracy of the presented model by comparing the measured frequency response of the amplifier to the simulation employing the developed cryogenic models (Fig. 18). Only a 3-dB error can be observed in the DC gain, while the 3-dB bandwidth matches within a 10% margin. The observed discrepancy is well within the margin due to process spread, which has not been modeled in this work due to lack of the required corner-lot samples. In conclusion, both experiments above confirm the effectiveness of the parameter extraction and the modeling procedure presented above.

B. Impact of cryogenic CMOS on circuit design

Device performance at 300 K and 4 K is compared and summarized in Table III for minimum-length devices for both technologies. The higher threshold voltage V_T combined

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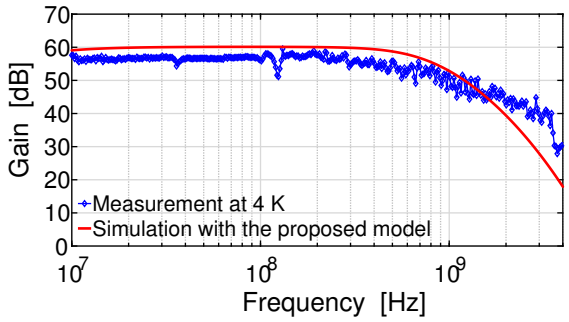

Fig. 18. Frequency response of the cryogenic LNA: comparison between measurement at 4 K and simulation with the proposed model. Reproduced from [42].

with a steeper SS is beneficial to minimize leakage currents. However, a high V_T reduces the voltage headroom available for circuits, especially when operating at low supply voltages. This may force the adoption of low-voltage circuit topologies typically showing a lower energy efficiency [52]. This can be particularly detrimental in cryogenic applications, such as quantum-computing controllers, because of the tight power budget imposed by the cooling capabilities of dilution refrigerators.

The effect of the higher V_T is partially compensated by the increase in mobility, which results in an overall increase of the maximum drain current (see I_{on} in Table III) and, consequently, in a faster switching speed (see Fig. 17). The larger driving current and lower leakage bring an improved I_{on}/I_{off} ratio (better than $100\times$ for 40 nm), which is advantageous for the implementation of high-energy-efficiency digital logic. Table III also shows the transconductance efficiency in terms of g_m/I_D ratio in both weak and strong inversion, extracted from the measurements shown in Fig. 2, 3, 4, 5, Fig. 6, 7, 8, 9. A significant improvement ($\approx 3\times$) is observed at 4 K in weak inversion while a slightly lower efficiency appears in strong inversion. This would lead to a major improvement in power efficiency for cryogenic circuits biased in weak inversion. Finally, a lower intrinsic gain is observed, due to the large increase in the channel-length modulation factor λ, in agreement to what was observed in [44].

VI. Conclusions

This work presents the extensive DC characterization of transistors fabricated in 0.16-μm and 40-nm CMOS technologies at deep-cryogenic temperatures (4 K, 1 K and 100 mK). A detailed understanding of the device physics at cryogenic temperatures was developed and captured in a compact model that was validated both via device DC characterization and through the design and testing of complex circuits.

It was demonstrated that nanometer bulk CMOS devices can operate reliably down to 100 mK and that, for the first time, their behavior can be modeled at such low temperature. Moreover, nanometer CMOS technologies are not affected by strong cryogenic non-idealities, such as kink, and several device figures of merit, such as I_{on}/I_{off} and g_m/I_D, significantly improve at 4 K, which is expected to enhance the performance of both analog and digital circuits at cryogenic temperatures.

Thus, the proposed models will enable the design and simulation of circuits in nanometer CMOS, which is a viable technology for the implementation of high-performance and power-efficient cryogenic circuits, as required in demanding applications such as quantum computing.

TABLE III
Comparison of Performance at 300 K and 4 K.

Technology		**0.16 μm**		**40 nm**	
Temperature		**4 K**	**300 K**	**4 K**	**300 K**
Device W/L	[$\mu m/\mu m$]	2.32 / 0.16		1.2 / 0.04	
V_T	[V]	0.55	0.40	0.50	0.38
SS	[mV/dec]	22.8	87.0	27.7	88.2
n	[-]	28.7	1.5	34.9	1.5
I_{on}	[A]	$2 \cdot 10^{-3}$	$1.5 \cdot 10^{-3}$	$6 \cdot 10^{-4}$	$5.3 \cdot 10^{-4}$
I_{off}[*]	[A]	$< 3 \cdot 10^{-11}$	$< 1.6 \cdot 10^{-10}$	$< 1.5 \cdot 10^{-12}$	$< 1.4 \cdot 10^{-10}$
I_{on}/I_{off}	[A/A]	$> 6.7 \cdot 10^{7}$	$> 9.4 \cdot 10^{6}$	$> 4.0 \cdot 10^{8}$	$> 3.8 \cdot 10^{6}$
Gate delay[†]	[ps]	30.60	38.30	-	-
λ[‡]	[V^{-1}]	3.3	0.6	4.0	1.3
		Weak Inversion			
g_m/I_D[§]	[V^{-1}]	70	27	92	27
Intrinsic gain = $g_m/(\lambda I_D)$	[V/V]	21.2	45.0	23.0	20.8
		Strong Inversion (at $V_{ov} = 0.2$ V)			
g_m/I_D	[V^{-1}]	6	9	9	10
Intrinsic gain = $g_m/(\lambda I_D)$	[V/V]	1.8	15.0	2.2	7.7

[*] I_{off} for 0.16-μm transistors is limited by leakage in the ESD of the samples and in 40 nm by the accuracy of the instrument.

[†] Gate delay is measured with V_{DD} of 1.1 V (40 nm), 1.8 V (0.16 μm).

[‡] λ is extracted at $V_{GS} = 0.65$ V (40 nm) and $V_{GS} = 0.68$ V (0.16 μm).

[§] The peak value for g_m/I_D is reported. At 4 K, this value is limited by the accuracy of the instrument in measuring small values of I_D.

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