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A 10kW Solar-Powered Bidirectional EV Charger Compatible with Chademo and COMBO

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Abstract— Charging electric vehicles (EVs) from photovoltaic panels (PV) provides a sustainable future for transportation. This paper presents the development of a 10kW EV charger that can be powered from both a PV array and the three-phase AC grid. The goal is to realize a high power density and high-efficiency three-port power converter that integrates the EV, PV, grid and meets the Chademo and CCS/Combo EV charging standards. The EV port is designed to be isolated and bidirectional, so that both charging and vehicle-to-Grid (V2G) can be implemented. As PV and EV are both DC by nature, the converter uses a central DC-link to exchange power between the EV and PV, thereby increasing efficiency. The use of silicon carbide devices and powdered alloy core inductors enables high switching frequency and power density. The closed-loop control allows four different power flows: PV→EV, EV→grid, grid→EV and PV→grid. Hence the converter operates as a PV inverter, a bidirectional EV charger and a combination of both. A 10kW prototype has been successfully tested, and its experimental waveforms and measured efficiency are presented. It has three times the power density and higher partial and peak load efficiency when compared to existing solutions.

Index Terms — Electric vehicle, charging, powered alloy core, photovoltaic systems (PV), silicon carbide (SiC)

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I. NOMENCLATURE

\( P_{\text{nom}} \) – Nominal power of the converter
\( V_{\text{ac}}, I_{\text{ac}}, P_{\text{ac}} \) – RMS voltage, current and nominal power of AC grid connection, respectively
\( V_{\text{pv}}, I_{\text{pv}}, P_{\text{pv}} \) – PV maximum power point voltage, current and power, respectively
\( \Delta I_{\text{in}}, \Delta I_{\text{in}(p-p)} \) – PV current ripple and in percentage, respectively (peak-peak)
\( \Delta V_{\text{pv}(p-p)} \) – PV voltage ripple (peak-peak)
\( V_{\text{ev}}, I_{\text{ev}}, P_{\text{ev}} \) – EV voltage, current and (dis)charging power, respectively
\( I_{\text{loss}} \) – Total losses in the power converter
\( V_{\text{dc}}, V_{\text{ac}} \) – Nominal and actual DC–link voltage
\( f_{\text{sw}} \) – Switching frequency
\( N_{i} \) – Number of interleaved stages
\( D \) – Duty cycle of the switch (for both IBC and IBFC)
\( d_{1} \) – Duty cycle of diode conduction in IBC
\( \Delta I_{L} \) – Inductor ripple current (peak-peak)
\( I_{L(\text{max})}, I_{L(\text{min})} \) – Maximum and minimum inductor current
\( N_{\text{on}} \) – Maximum number of switches that are simultaneously ON in IBC
\( A_{L} \) – Permeance of the core
\( A_{c}, V_{e} \) – Core area and volume of the core, respectively
\( l_{e} \) – Magnetic path length of the core
\( B_{\text{max}} \) – Maximum flux density in the core during operation
\( \Delta B \) – Peak-peak change in flux density of the core \( (B_{pk} = \Delta B / 2) \)
\( P_{L} \) – Total inductor/transformer losses
\( P_{\text{core}}, P_{\text{cu}} \) – Core losses and winding copper losses of inductor, respectively
\( P_{V} \) – Core losses of inductor per unit volume
\( R_{L} \) – Inductor winding resistance
\( f_{\text{eq}} \) – Equivalent frequency for modified Steinmetz equation
\( I_{L} \) – Inductor winding current
\( C_{\text{in}} \) – Input capacitance of the IBC
\( P_{S} \) – Total losses in the switch (conduction and switching losses)
\( P_{S,\text{con}}, P_{S,\text{sw}} \) – Conduction losses and switching losses of the switch, respectively
\( I_{DS} \) – Switch drain-source current
\( R_{DS(\text{on})} \) – Switch on-state resistance
\( V_{DS}, V_{DS(\text{max})} \) – Switch drain-source voltage and its maximum value, respectively
\( T_{j} \) – Semiconductor device junction temperature
\( T_{a} \) – Ambient temperature
\( V_{GS} \) – Switch gate voltage
\( R_{G} \) – Switch gate resistance
\( E_{\text{on}} \) – Turn-on energy of the switch
\( E_{\text{off}} \) – Turn-off energy of the switch
\( I_{D} \) – Diode current
\( P_{D} \) – Total losses in the diode (conduction and switching losses)
\( P_{D,\text{con}}, P_{D,\text{sw}} \) – Diode conduction losses and turn-off losses, respectively
\( V_{R,D} \) – Diode reverse voltage in OFF state
Electric vehicles (EVs) are considered to be the future mode of transportation. They are more efficient and have no emissions when compared to fossil fuel powered vehicles. However, EVs are currently charged from an electricity grid whose fuel mix is mainly dominated by fossil fuels [1]. In order to make EVs sustainable, it is essential to charge EVs from sustainable sources of electricity. Hence, the charging of EVs from photovoltaic (PV) panels is a sustainable proposition for the future [2]–[5].

At the same time, PV generation is characterized by both diurnal and seasonal variations. This necessitates a grid connection to ensure reliable power supply for charging the EVs. Workplaces like office buildings, factories and industrial area are ideal places to facilitate solar EV charging where the building rooftops and car parks can be installed with photovoltaic (PV) panels. There are several advantages to charging EVs from PV:

- **EV charging power demand on the grid is reduced as the charging power is locally generated by PV.**
- **EV battery can serve as an energy storage for the PV and reduces the negative impact of large-scale PV integration in the distribution network** [6].
- **Long parking time of EVs at workplaces results in low charging power requirements and enables implementing Vehicle-to-Grid (V2G) technology, where the EVs acts as a controllable generator** [7], [8].

**A. Literature review**

In order to charge EVs from PV, separate converters for the EV and PV that are connected to the AC grid can be used [9], [10]. Alternately, a single integrated converter that connects to the EV, PV and grid can be utilized [3]. A key
requirement of the EV charging standards is that the EV charger must be isolated from all power sources, namely PV and the grid [11]–[13].

Several studies have presented a three-port power converter for charging EV from PV. Direct DC charging of EV from PV using a ZVT-PWM buck converter interlinked on a 210V DC bus was presented in [14], [15]. A closed-loop control was developed, and a 2.4kW prototype is built that offers EV charging but not V2G. In [16], a DC nanogrid is used for charging EV from PV, fuel cells and the AC grid and 1.5kW DC/DC full-bridge LLC resonant converter is used a building block for the system. In [17], [18], a 3.3kW bidirectional three-port converter with 380V DC-link was made that integrates, EV, PV, and single-phase AC grid. The integrated converter showed an improved efficiency of 7-15% when compared to separate converters for EV, PV. Two DC/DC converters were used for charging an EV from PV via a 48V buffer battery in [19]. The 3.3kW system does not have bidirectional power flow, connection to the grid or isolation for the EV. In [20], a solar charging system for e-scooters is developed with single phase V2G/V2H functionally using 2x12V low voltage batteries. Buck and boost converters are used for the DC-DC power conversion and an H-bridge for the inverter operation.

In the above studies, the designs are not suited for three-phase high-power applications (>5kW). There is no consideration for the EV charging standards with respect to charging current ripple, EMI and/or isolation. Similarly, a review of several EV-PV topologies concluded that most designs neglected the EV isolation requirements [3].

In [21], [22], a high-frequency AC-link based on a multi-winding transformer was used for integrating EV, battery storage, and renewable energy sources. While the topology provides the benefit of isolation between all the ports and is applicable for high powers, it is not useful for EV-PV application because of two reasons. European regulations do not stipulate a need for isolation between the PV and the grid. Secondly, PV and EV are both DC by nature, so the AC-link will lead to unnecessary conversion steps.

A 10-kW, non-isolated, bidirectional converter to charge EV from PV is presented in [23]. A 575V DC-bus is used to integrate EV, PV and grid and the closed-loop control are designed to reduce PV intermittency. A symmetrically isolated 5kW Z-source converter was used for EV charging from PV in [24]. The performance was compared with transformer-less and high-frequency transformer-isolated topologies indicating the overall superiority of the Z-source converter. Similarly, a 3.3kW prototype of a solar EV charger based on the modified Z-source inverter with isolation is proposed in [25]. However, the Z-source topologies cannot be modularly scaled up for higher powers; require large passive components to make the impedance network and have a high ripple at the PV port reducing the efficiency of the maximum power point tracking (MPPT).

B. Contributions

This paper presents the development of a high power density, modular, V2G-enabled, integrated power converter for charging electric vehicles from photovoltaic panels and the AC grid. Fig. 1 shows the block diagram of the three-port converter for solar charging of EV with a central DC-link. There are three sub-converters inside: a unidirectional DC/DC converter for the PV, a bidirectional DC/AC inverter to connect to the AC grid and a bidirectional isolated DC/DC converter for EV. DC charging of EV is implemented here as opposed to AC charging as Chademo and Combined charging standard (CCS) facilitates smart charging, fast charging and V2G [12], [26], [27]. Smart charging can enable the EV charging to follow the PV generation, energy prices and regulation prices [28], [29].

The developed three-port architecture has three advantages. Firstly, since EV and PV are inherently DC by nature, an internal DC-link is used to exchange power between the three sub-converters. Secondly, the grid inverter is intrinsically bidirectional as it needs to feed PV power to the grid and draw EV charging power from the grid. Hence, by making the isolated DC/DC converter for EV bidirectional as well, V2G operation can be implemented. Thirdly, a single DC/AC inverter is sufficient to connect both PV, EV to the grid. This makes the converter cheaper and smaller. Typically, if an integrated converter is not used, two inverters would be needed, one each for PV and EV.
The critical aspects of the converter design are achieving high efficiency, high power density, modularity and low cost. The contributions of this work compared to earlier works are,

- Developing a high power bidirectional, isolated, three-port power converter for direct DC charging of an EV from PV and AC grid. It can be seen from the literature review that such a converter does not currently exist.
- The combined use of SiC devices, high switching frequency, interleaving and KoolMμ inductors has resulted in the developed converter to have much higher partial and peak load efficiency and three times the power density when compared to existing solutions.
- Designing a closed-loop control that enables four different power flows using the converter: PV→EV, PV→Grid, Grid→EV and EV→Grid (i.e., V2G).
- The developed converter is modularly built to be operated either as a DC V2G EV charger or as a solar powered DC V2G EV charger. Further, several DC V2G EV charger modules can be operated in parallel to scale up the power from 10kW up to 100kW for fast charging of EVs. State-of-the-art solar EV chargers do not exhibit such high levels of modularity.
- The converter is designed to be compatible with IEC, Chademo and CCS/Combo DC charging standard with respect to ripple, harmonic, voltage range and isolation requirements and charge/V2G operation has been tested using a Nissan Leaf EV. Currently developed solar EV chargers do not meet these criteria for commercial usability.

C. Paper organization

Section 3 describes the specifications of the EV-PV power converter and requirements from the EV charging standards. Section 4, 5, 6 provides the detailed design procedure and loss models for the isolated DC/DC converter for the PV, bidirectional DC/AC grid inverter and the DC/DC converter for the EV charging, respectively. Section 7 presents the closed loop control for each of the three sub-converters. Section 8 describes the experimental prototype developed and measured waveforms and efficiency of the three-port converters.

III. EV-PV POWER CONVERTER

A. Specifications

Table I shows the specifications of the three-phase, grid-connected EV-PV power converter. The voltage range, isolation and ripple requirements are compatible with the EV charging standards [11], [13]. A 10kWp PV array connected to the PV port is the primary power source. The internal DC-link voltage is rated at 750V. As the maximum EV current, $I_{ev}$, is 30A, power curtailment occurs at low EV voltages, as shown in Fig. 2. The critical operating point is

Fig. 1 – Block diagram of the grid connected bidirectional 10kW three-port EV-PV charger
when EV voltage, $V_{ev}$ is 333.3V, where both maximum power and maximum current has to be supplied to the EV battery.

The power difference between the EV charging demand, $P_{ev}$, PV power, $P_{pv}$ and the converter losses $P_{loss}$ is met by the grid power $P_{ac}$. For V2G operation, $P_{ev}$ is negative. The power balance equation is

$$P_{ac} = P_{ev} - P_{pv} + P_{loss}$$ (1)

B. Topology

Fig. 3 shows the topology of the three sub-converters in the EV-PV charger: an interleaved boost converter (IBC) for the PV, an interleaved bidirectional flyback converter (IBFC) for the EV and a three-phase voltage source inverter for the AC grid. The neutral of the AC grid is connected to the mid-point of the DC-link. The flyback converter is operated in a quasi-resonant mode to achieve soft switching, while the PV and grid converter are operated with hard switching.

C. Achieving high efficiency and high power density

The EV-PV power converter has four different power flows: PV→EV, PV→Grid, Grid→EV and EV→Grid. It is hence essential to ensure high efficiency for the four power flows. In particular, high partial-load efficiency is vital as smart charging is done by controlling the charging power below the rated power. Secondly, it is crucial that the converter has a high power density and occupies less space when installed at the parking lot. In order to achieve these

<table>
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<td><strong>Parameter</strong></td>
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<tr>
<td>PV MPPT Voltage, Current</td>
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<td>PV current ripple (pk-pk)</td>
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<td>PV voltage ripple (pk-pk)</td>
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<tr>
<td>EV voltage</td>
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<tr>
<td>EV current</td>
</tr>
<tr>
<td>Internal DC-link voltage</td>
</tr>
<tr>
<td>EV current ripple (rms)</td>
</tr>
<tr>
<td>EV voltage ripple (pk-pk)</td>
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Fig. 2 – Maximum power and current of the EV charger for different EV battery voltages
two objectives, three techniques are implemented: interleaving, use of silicon carbide devices and powdered alloy core inductors.

Interleaving is used in the both PV and EV DC/DC converters, with the use of three and four interleaved stages, respectively. Interleaving has four advantages:

1. Current through the switches and inductors in each leg is reduced by a factor of \((1/N_i)\), where \(N_i\) is the number of interleaved stages. Thus smaller inductors and lower-rated switches can be used.
2. The volume \(L_{vol}\) of an inductor is directly proportional to the energy it processes as given by \(L_{vol} \propto L I^2\). By interleaving, the total volume \(L_{vol(n)}\) of all the interleaving inductors reduces by a factor \(N_i\).
3. Effective frequency as seen at the input is increased by a factor of \(N_i\). This facilitates the operation of each leg at a lower frequency, thus lowering the switching losses.
4. As the currents in each leg are phase shifted by an angle of \(360^\circ/N\), the input current ripple is reduced by a factor of \((1/N_i)\) and the voltage ripple by \((1/N_i)^2\).

To achieve high power density, it is crucial to increase the switching frequency while still maintaining high efficiency. Silicon carbide (SiC) represents a revolution in power semiconductor technology, which can help realize high switching frequency [30], [31]. SiC MOSFETs exhibit very low switching losses while SiC schottky diodes have no reverse recovery and have very low turn-on voltage. SiC MOSFET of >1kV are now commercially available and can replace >1kV Si IGBTs in high power applications. In this paper, SiC MOSFETs and schottky diodes are used to reduce switching losses and hence achieve higher switching frequency.

Powdered alloy cores are different from ferrite cores as they have a distributed air gap and much higher saturation flux density (typically 2 to 3 times higher). This means that powdered cores can handle much higher currents without saturation, which is useful for high power applications. The main disadvantages of powdered cores, when compared to ferrites, are their higher core losses, higher cost and inductance variation [32]. So, if the switching frequency is not too
high, they could be excellent replacements for ferrites in higher power density applications. In this work, KoolMµ cores from Magnetics are extensively used in the grid inverter and solar converter [33], [34]. KoolMµ cores are chosen over other powdered cores due to the relatively lower core losses.

IV. DC/DC CONVERTER FOR PV

The DC/DC PV converter is built using an interleaved boost converter with three interleaved stages as shown in Fig. 3 [31], [35]. The detailed design of the converter and its comparison to an IGBT and ferrite based design are shown in [31]. SiC Schottky diodes (CREE C4D15120A), SiC MOSFETs (CREE C2M0080120D) and KoolMµ 40µ powdered alloy inductors are used in each leg. Each leg operates at a switching frequency, \( f_{sw} \) of 47kHz.

A. Operation of the interleaved boost converter

Operating waveforms of the IBC are shown in Fig. 4. The input PV current is shared equally between the three legs, and the average inductor current is given by \( I_{L(\text{avg})} = I_{PV}/3 \). When the switch is ON from 0 to \( (DT) \), the current in the inductor rises from \( I_{L(min)} \) to \( I_{L(max)} \) due to the positive PV voltage. When the switch is OFF, the inductor current decreases and flows through the diode. The voltage ratio of input and output voltage is the same as a normal boost converter for continuous conduction mode (CCM) and discontinuous conduction mode (DCM):

\[
\frac{V_{dc}}{V_{PV}} = \frac{d_1 + D}{d_1}
\]  

(2)

where \( D \) is the duty cycle of the switches and \( d_j \) is the period when current flows through the diode. In CCM, \( d_1 = 1 - D \).

The inductor ripple is vital in designing the PV converter as it directly translates to the input capacitor sizing, inductor size and the efficiency of the MPPT operation. The peak-to-peak inductor ripple \( \Delta I_L \) is:

\[
\Delta I_L = \frac{V_{PV}D}{f_{sw}L} = \frac{(V_{dc} - V_{PV})d_1}{f_{sw}L} = I_{L(max)} - I_{L(min)}
\]

(3)

where \( I_{L(max)}, I_{L(min)} \) are the maximum and minimum inductor current and \( L \) is the inductance, respectively. It can be seen from (3) that we either need to use a high switching frequency or a large inductor in order to have a low ripple. Both these methods have the drawback of increased switching losses, increased inductor losses and require a larger inductor core and heat sink.

The benefit of interleaving is that the maximum input current ripple \( \Delta I_{in} \) is \((1/N_i)\) of the maximum inductor ripple,

\[
\Delta I_{in}(D) = \frac{V_{PV}}{f_{sw}L} \left( \frac{N_{on} - N_iD}{1 - D} \right) \frac{1}{N_i} \left( N_iD - N_{on} + 1 \right)
\]

(4)

where \( N_{on} \) is the maximum number of switches that are simultaneously ON for the given duty cycle.

Fig. 5 shows the input ripple as a function of duty cycle for different numbers of interleaved stages. The peak input ripple occurs at \( D=(1/2N_i) \), and the input ripple is zero when \( D=(1/N_i) \). With three interleaved stages, the input current and voltage ripple reduce by a factor of three and nine, respectively.

B. Inductor design and losses

For the inductor design, the vital parameter is the maximum input ripple, \( \Delta I_{in(max)} \) cycles. The duty cycle for maximum input ripple can be determined from (4) by setting \( d(\Delta I_{in})/dD = 0 \) and solving for \( D \), where \( A_{int} \) takes odd integral values from 1 to \( 2N_i \):

\[
\Delta I_{in(max)} = \frac{V_{dc}}{4f_{sw}LN_i}, \quad @ \ D = \frac{A_{int}}{2N_i}
\]

(5)

For a three-leg IBC, maximum input ripple occurs at odd integral multiples of \( D=1/6 \) as seen in Fig. 5. It must be kept in mind that maximum ripple in inductor \( \Delta I_{L(max)} \) always occurs at \( D=0.5 \) irrespective of \( N_i \). The inductor is sized
at the point where the PV feeds maximum current \(I_{pv}=I_{pv(max)}=28.5\text{A}, V_{pv}=350\text{V}\), given by

\[
L = \frac{V_{dc}}{4f_{sw}N_{i}\left(\Delta I_{in(p-p)}\|I_{pv(max)}\right)} \tag{6}
\]

Using (6), the required inductance for 47kHz is 443\(\mu\text{H}\). The inductor is built using KoolM\(\mu\) E65 cores as they are suitable for PCB mounting and have large core area to reduce the core losses. The parameters of the 40\(\mu\) E65 core are: permeance \(A_{i}=230\ \text{nH/T}\) at zero DC bias, core area \(A_{c}=540\text{mm}^2\), magnetic path length \(l_{e}=147\text{mm}\) and core volume \(V_{e}=79400\text{mm}^3\). Table II shows the design of the KoolM\(\mu\) inductor considering the inductance variation due to soft saturation [32]. The skin depth for 47kHz is approximately 300\(\mu\text{m}\). Hence, litz wire of 1000x0.071mm is used in order to reduce the skin effect.

Fig. 4 – Waveforms of the IBC (top to bottom): Gate signal for S11; currents through the inductor \(L_{1}\), switch S11 and diode D11; phase shifted current through the inductors \(i_{L1}, i_{L2}, i_{L3}\) of each interleaved leg; net input current of the three legs in CCM operation.

Fig. 5 – Peak to peak input ripple \(\Delta I_{in}\) as a function of duty cycle (D) for different number of interleaved stages of IBC \((N)\) for \(V_{dc}=750\text{V}, f_{sw}=47\text{kHz}, L_{1}=443\mu\text{H}\).
Equations (7), (8) are used to determine the number of turns, $N$ and the maximum flux density in the core, $B_{\text{max}}$. While 47 turns are required for an inductance of 443µH, the bobbin can only accommodate a maximum of 42 turns. Therefore, the inductor is re-designed with 42 turns resulting in an inductance of $L=405\mu\text{H}$ at zero current and $L=355\mu\text{H}$ at maximum current, due to soft saturation. The smaller inductor will require a larger input capacitor to limit the input voltage ripple.

$$L = A_1N^2$$

(7)

$$B_{\text{max}} = \frac{A_2N_{L_{(\text{max})}}}{A_c}$$

(8)

The inductor losses, $P_L$, comprising of the copper losses, $P_{\text{cu}}$ and core losses, $P_{\text{core}}$ are estimated using the Modified Steinmetz Equation (MSE) [36]. For a boost converter, the equivalent frequency $f_{\text{eq}}$ for MSE is

$$P_L = P_{\text{core}} + P_{\text{cu}} = (Af_{\text{eq}}^{-1}B_{pk}^b)f_{\text{sw}}V_e + I_{L_{(\text{rms})}}^2R_L$$

(9)

$$f_{\text{eq}} = \frac{2}{\Delta B^2\pi^2}\int_0^T \left(\frac{dB}{dt}\right)^2 dt = \frac{2}{\pi^2} \left(\frac{D}{D_sT}\right)$$

(10)

where $\Delta B$ is the peak-peak change in flux density, $B_{pk} = \Delta B/2$ and measured value of $R_L$ is 28mΩ. MSE parameters are $A=120$, $b=2.09$, $a=1.46$ for the 40µ KoolMµ core, when $P_{\text{core}}$ is in mW/cm³, $f_{\text{sw}}$ in kHz, $B_{pk}$ in T and $V_e$ in V²/cm³ [37].

The inductor losses are shown in Table II, where 15.5W is lost per inductor at maximum input power. Since the skin depth at 47kHz in much higher than the litz diameter, the losses due to skin and proximity effect are not considered for the IBC.

The main advantage of the much lower core losses and saturation flux density of KoolMµ is that only a single core set is required per inductor. Using other powdered alloy core inductors will lead to much higher core losses while using ferrites will require two parallel E65 core sets. Secondly, the powder cores exhibit a gradual reduction in inductance under a fault condition, which makes the control of the converter easier and robust. Thirdly, powder cores have a distributed air gap which causes very low copper losses because of the fringing flux.

C. Sizing of input and output capacitor

When using an IBC, an input capacitor $C_{in}$ is sized to supply the ripple current, $\Delta I_{in}$:

$$C_{in} = \frac{1}{2} \left(\frac{T}{2N_i}\right) \left(\frac{V_{dc}}{8f_{\text{sw}}LN_i}\right) \left(\frac{1}{\Delta V_{in}}\right) \text{ @ } D = \frac{A_{\text{int}}}{2N_i}$$

(11)

Here, an input capacitor of 10µF is used which results in a maximum voltage ripple of $\Delta V_{in}=0.32V$. A LC filter ($L_{in}=47\mu\text{H}$, $C_{in}=10\mu\text{F}$) is used between the input capacitor and PV to further reduce this ripple voltage. A 470nF film capacitor is connected close to the output of each interleaved leg to filter the high frequency output ripple.

D. Converter loss estimation

The IBC operates in CCM and DCM depending on the PV voltage and current. The conduction losses in the diode ($P_{D,\text{con}}$, $P_{D,\text{sw}}$) and the conduction and switching losses in the MOSFET ($P_{S,\text{con}}$, $P_{S,\text{sw}}$) are estimated as:

$$P_S = P_{S,\text{con}} + P_{S,\text{sw}}$$

(12)

$$P_{S,\text{con}} = I_{DS_{(\text{rms})}}^2 R_{D\text{so}(on)}(T_j)\text{Va}$$

(13)

$$P_{S,\text{sw}} = f_{\text{sw}}(E_{on}(v_{DS_{(\text{off})}},T_j) + E_{\text{off}}(v_{DS_{(\text{on})}},R_{D\text{so}},T_j))$$

(14)

$$P_D = P_{D,\text{con}} + P_{D,\text{sw}} = I_{\text{avg}} U_{D0}(T_j) + I_{DS_{(\text{rms})}}^2 R_{D\text{(on)}}(T_j) + f_{\text{sw}} E_{D\text{ch}}$$

(15)

$$P_{\text{loss}} = 3(P_D + P_S + P_L) + P_{\text{filter}} + P_{\text{ctrl}}$$

(16)

where $P_S$, $P_D$ are the total switch and diode losses, $I_{DS}$,$I_D$ are the switch and diode current; $R_{D\text{so}(on)}$, $R_D$ are the on-state resistance of the MOSFET and diode; $E_{on}$, $E_{\text{off}}$ are the switch turn-on and turn-off energy; $E_{D\text{ch}}$ is loss due to the energy stored in the diode parasitic capacitance; $U_{D0}$ is the on-state voltage of diode. As indicated in the equations above, the
switch and diode parameters themselves are a function of the junction temperature $T_J$, the gate resistance $R_G$, gate voltage $V_{GS}$, blocking voltage of the device $V_{DS}$ and the device current $I_{DS}/I_D$ for the specific operating conditions [35].

$P_{\text{filter}}$ is the total losses in the filters namely, the input common mode filter (4mΩ resistance), fuse, input LC filter (11mΩ for $L_{\text{fin}}$, 13mΩ ESR for $C_{\text{fin}}$) and the output capacitor ($C_{\text{fdc}}$ with tanδ=0.03). $P_{\text{ctrl}}$ is the power consumed in the control and protection circuitry: three 20mΩ shunt resistors added to the MOSFET source for current control; gate drive, power supply and control ICs; and in the extra diode (VS-40EPS) added at the output of the IBC to protect against reverse currents. Reverse recovery losses due to the schottky diode are neglected as they are extremely small in SiC devices. The turn-on and turn-off gate resistance are 9.4Ω and 4.7Ω, respectively and $V_{GS}=20V$. The ambient and junction temperature are assumed to be 25ºC and 100ºC respectively.

The total converter losses and split up of losses within the converter for different PV voltages and power is shown in Fig. 6(a),(b), respectively. The worst case operating point is when $V_{PV}=350V$, $P_{PV}=10kW$ with losses of 160.4W. The

<table>
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<th>Inductance (µH) $L$</th>
<th>Avg. Inductor current (A) $I_L$</th>
<th>Inductor ripple (p-p) (A) $\Delta I_L$</th>
<th>Core Loss (W) $P_{core}$</th>
<th>Copper loss (W) $P_{cu}$</th>
<th>Total inductor loss (W) $P_L$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_{405}$</td>
<td>9.52</td>
<td>11.03</td>
<td>11.75</td>
<td>3.77</td>
<td>15.53</td>
</tr>
<tr>
<td>$L_{\text{least}}$</td>
<td>355</td>
<td></td>
<td>11.75</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Fig. 6 – (a) Total losses of the IBC as a function of input PV voltage and PV power. (b) Split up of losses for 10kW PV input for 350V and 700V PV voltage. (C) Estimated efficiency of IBC as a function of PV power for different voltages. Also shown is the efficiency of the three phase inverter as a function of power.
key observation is the low switching and conduction losses in the MOSFET of 33W and 16W, respectively. On other hand, the three 40µ powdered core inductors together have a relatively higher loss of 46.5W. The higher losses are the disadvantage of the powdered alloy core, with the benefit of needing lesser number core sets with respect to ferrites. It’s a trade-off between power density and losses. Fig. 6(c) shows the efficiency of the IBC for different PV voltages. The peak efficiency is 99.29% at 10kW,700V PV input.

For comparison, the same converter is designed using ferrite cores and silicon IGBT operating at 19kHz in [31]. The net converter volume was 2.5 times higher, owing to the 3x larger inductors, and bigger heat sinks to dissipate the IGBT switching losses. Thus, the comparison shows that the use of SiC devices and powdered alloy cores can help achieve high power density and high efficiency.

V. DC/AC GRID INVERTER

The DC/AC stage uses a standard three-phase inverter with three legs and six switches and operates from the 750V DC-link [38]–[40]. The converter is operated with sinusoidal PWM with \( f_s = 47\text{kHz} \). The inverter is designed to both draw and feed current to the grid up to 16A. Since the converter is operated with hard switching, SiC C2M0025120D MOSFETs with a lower \( R_{ds(on)} \) are used, along with its body diode. The gate resistances are 15.1Ω for turn-on, 5.1Ω for turn-off.

At the inverter input, six 470µF electrolytic capacitors, connected two in series form the DC-link. Three LCL filter, one per phase are used at the inverter output for filtering out the harmonics as shown in Fig. 3 [41], [42]. It’s composed of \( L_{abc}=23\text{6}μ\text{H} \) (E65 40µ KoolMµ, N=32, \( R_1=11\text{mΩ} \)); \( L_{fabc}=140\text{μH} \) (E42 N87, N=36, \( R_1=21\text{mΩ} \)) and a capacitor \( C_f=8\text{μF} \). Detailed control using sinusoidal PWM and loss modelling of the three phase inverter are well studied in literature and hence not presented again in this paper [38]–[42]. The estimated converter efficiency including the losses in the switches, filters and control circuitry (based on section III.D) is shown in Fig. 6(c) with a peak value of 98.05%.

VI. ISOLATED BIDIRECTIONAL DC/DC CONVERTER FOR EV

The bidirectional, isolated DC/DC converter for the EV is composed of four interleaved flyback converters (Fig. 3). MOSFETs and anti-parallel diodes are used on both sides of the transformer for bidirectional operation. Each 2.5kW flyback module has a three-winding transformer (1:1:1 turns ratio) with two series-connected windings on the DC-link side (primary) and a third winding on the EV battery side (secondary), as shown in Fig. 3. For \( I_{ev}=30\text{A} \), the corresponding output secondary current in each 2.5kW unit is \( I_{ev(m)}=7.5\text{A} \).

The secondary side voltage ranges between 50-500V while the primary voltage is \( V_{dc}=750\text{V} \). This difference in primary and secondary voltages leads to high secondary side currents (up to 30A). Therefore, two MOSFETs are connected in parallel at the secondary side to reduce the conduction losses. The flyback uses C4D15120A diodes and C2M0080120D MOSFETs with 20Ω turn-on and 10Ω turn-off gate resistance.

The main reason for picking the flyback for the EV converter is two-fold. Firstly, the topology provides isolation as required by EV the charging standards. Secondly, the flyback as implemented here can realize bidirectional operation with just four switches (two on the DC-link side and two in parallel on EV side). With other topologies, like a dual active bridge or a resonant converter, we would need 8 switches (or more in parallel for higher current).

A. Operation of interleaved bidirectional flyback in quasi-resonance

The flyback converter is operated in quasi-resonant (QR) mode for both charging and V2G operation, and this has four main advantages. Firstly, it enables valley switching of the MOSFET which results in reduced turn-on losses due to zero voltage (ZVS) or low voltage switching (LVS). The resonant capacitor \( (C_{z1}, C_{z2}, C_{z3}) \) absorbs the turn-off energy, and hence the turn-off losses are nearly zero. Third, the noise at turn off \( (dV/dt) \) is reduced by the resonance capacitor. Finally, the quasi-resonant operation is on the borderline between DCM and CCM and has lower RMS
currents than DCM. Fig. 7 shows the QR operating waveforms when in charge mode.

$0 < t < DT$: When MOSFETs $S_{21}$, $S_{22}$ are turned on simultaneously, the currents $i_{L1A}, i_{L2A}$ rise from zero to its peak value $I_{L1A(pk)}$ and energy is stored in the flyback transformer

$$I_{L1A(pk)} = \frac{(V_{dc}/2)D}{(L_{1A} + M)f_{sw}}$$

where $M = k \sqrt{L_{1A}L_{2A}}$ is the mutual inductance, $D$ the duty cycle and $f_{sw}$ the switching frequency.

$DT < t < (D+D_1)T$: When the switch is turned off, the energy stored in the flyback transformer is delivered to the load. The secondary side diode $D_{23}$ conducts for a time interval, $D_1/f_{sw}$, till the inductor current $i_{L3A}$ goes to zero. Due to the much lower on-state voltage of the SiC shottky diode, the MOSFET body diode does not conduct the load current.

The peak current in the secondary inductor, $I_{L3A(pk)} = 2I_{L1A(pk)}$, assuming $k=1$:

$$I_{L3A(pk)} = \frac{V_{ev}D_1}{L_{3A}f_{sw}} = 2I_{L1A(pk)}$$

$$I_{L3A(pk)} = \frac{(V_{dc}/2)D}{(L_{3A} + M)f_{sw}} = 2I_{L1A(pk)}$$

The power transferred $P_{ev}$ can be related to the peak inductor currents and energy stored in the inductor $E_L$:

$$E_L = \frac{P_{ev}}{f_{sw}} = 2 \left( \frac{1}{2} L_{1A}I_{L1A(pk)}^2 \right) + M I_{L1A(pk)}I_{L2A(pk)} = \frac{1}{2} L_{3A}I_{L3A(pk)}^2$$
\[ I_{L1A(pk)} = \frac{P_{ev}}{\sqrt{2L1A f_{sw}}} = \frac{1}{2} \frac{(V_{dc}/2)D}{L1A f_{sw}} = \frac{1}{2} \frac{V_{ev}D1}{L3A f_{sw}} \] (21)

When the secondary diodes are conducting, the voltage across the switch is the sum of the input voltage, \(V_{dc}/2\) and the reflected secondary voltage, \(V_{R0}\). Based on Table I, \(V_{R0} = V_{ev}\) and ranges from 50-500V. The maximum MOSFET drain-source voltage \(V_{ds(max)}\) is:

\[ V_{ds(max)} = \frac{V_{dc}}{2} + V_{R0(max)} + V_{trans} = 375 + 500 + V_{trans} \leq 1200V \] (22)

where \(V_{trans}\) is the turn-off voltage transient due to the leakage inductance of the transformer (Fig. 7). Split windings are hence used on the primary side to ensure that \(V_{ds(max)} < 1200V\).

\((D+\overline{D})T < t < T:\) As soon as the diode current reaches zero, the resonant capacitors \(C_{21}\), \(C_{22}\) begin to exchange energy with the primary inductors. This causes an LC oscillation on the MOSFET drain-source voltage with a period of \((2T_F)\), as shown in Fig. 7. The MOSFET is hence turned ON at the bottom of the valley when the voltage is at its lowest to reduce the turn-on losses:

\[ V_{ds(min)} = V_{valley} = \frac{V_{dc}}{2} - V_{ev} \] (23)

\[ T_F = \pi \frac{L1A C_{ds(net)}}{2} \] (24)

\[ C_{ds(net)} = C_{21} + C_{ds,S} + C_{DD} + C_{xmer} \] (25)

where \(C_{ds(net)}\) is the net drain-source capacitance due to the QR capacitor \(C_{21}\), \(C_{22}\) and due to the parasitic capacitance of the MOSFET \(C_{ds,S}\), schottky diode \(C_{DD}\) and the transformer windings \(C_{xmer}\). Depending on the difference \((V_{dc}/2 - V_{ev})\), valley switching results in either ZVS or LVS at turn-on. Therefore, the net switching losses are dramatically reduced and can be zero for LVS and ZVS, respectively. This is the primary benefit of the QR operation. The sizing of the resonant capacitor must be such that it is large enough to store the maximum turn-off energy of the MOSFET considering all the operating points.

From the above equations, the duty cycle \(D\) and frequency \(f_{sw}\) for this flyback can be calculated as:

\[ D = \frac{2}{(V_{dc}/2) \sqrt{P_{ev}L1A f_{sw}/2}} \] (26)

\[ f_{sw} = \frac{1}{T_F} \left(1 - D - \frac{(V_{dc}/2)}{V_{batt}}D\right) \] (27)

Hence, to increase the EV charging power, a larger duty cycle, a higher inductor peak current, and lower switching frequency are required, as shown in Fig. 8(a). The operating of the flyback in V2G mode is similar to the charge mode described above. The difference being that in the V2G mode, the two switches \(S_{23}\) are turned ON first and the diodes \(D_{21}\) and \(D_{22}\) conduct during the OFF period of the switch. Since there are four modules operating interleaved, the gate signals are phase shifted by 90°. The net output current, \(I_o\), is the sum of the output current \(I_{ev(m)}\) of each of the four interleaved modules, as shown in Fig. 7.

Table III shows the operating regions of the MOSFET for ZVS and LVS for the charge (CH) and V2G modes. \(V_{ev}\) ranges from 50-500V and is less than \((V_{dc}/2)=375V\) for the majority of the operating range. Hence, the converter operates in ZVS for a large part of V2G mode and in LVS for a large part of charge mode.

B. Flyback transformer design

The 2.5kW flyback transformer is essentially three coupled inductors on a common magnetic core. Since QR results in variable switching frequency, the limits are set between 30-350kHz. The required size of the inductor is determined by the maximum power to be handled at the lowest input voltage \((V_{ev}=50V, I_{ev(m)}=7.5A)\). From equations (17)-(26),
the required inductance can be estimated, and it was found to be $L_{1A}=78.42\,\mu\text{H}$:

$$L_{1A} = \frac{2(V_{dc}/2)^2D^2}{4P_{ev}f_{sw}}$$

(28)

The transformer is built using an Epcos E65 N87 core set [43]. The permanence of the core, $A_L$ varies with the air-gap length, $g$ according to (29) where $K_1=716$ and $K_2=(-0.762)$:

$$g = \frac{(A_L/K_1)^{1/K_2}}$$

Using (7), (29), the required number of turns $N=18$ when using 2mm spacers on the outer leg and $g=4\,\text{mm}$. The transformer design is shown in Table IV, where $L_{1A}, L_{2A}, L_{3A}=80.06\,\mu\text{H}$. 200x 0.071mm litz wire is used for the winding. The windings are built in seven parallel-connected layers to reduce the leakage inductance: Layer 1,3,5,7 for the two primary windings and Layer 2,4,6 for the secondary winding.

### C. Variable frequency QR and DCM operation

Fig. 8(a) shows the variable frequency QR operation of the IBFC. The switching frequency reduces as the EV charging power increases. The lowest switching frequency of 30kHz is observed when $V_{ev}=50\,\text{V}$, $I_{ev(m)}=7.5\,\text{A}$. At very

<table>
<thead>
<tr>
<th>Situation</th>
<th>CH</th>
<th>V2G</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{ev}\geq V_{dc}/2$</td>
<td>ZVS</td>
<td>0</td>
</tr>
<tr>
<td>$V_{ev}&lt; V_{dc}/2$</td>
<td>LVS</td>
<td>$V_{dc}/2-V_{ev}$</td>
</tr>
<tr>
<td>$V_{ev}= V_{dc}/2$</td>
<td>ZVS</td>
<td>0</td>
</tr>
</tbody>
</table>

TABLE III - LVS AND ZVS OPERATING REGIONS OF THE 2.5KW FLYBACK TRANSFORMER

<table>
<thead>
<tr>
<th>Transformer core, Air gap</th>
<th>$A_c, l, g$</th>
<th>Epcos E65 N87, 4mm net air gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>Turns</td>
<td>N</td>
<td>18:18:18</td>
</tr>
<tr>
<td>Parallel layers</td>
<td>2:2:3</td>
<td></td>
</tr>
<tr>
<td>Litz wire</td>
<td>200 x 0.071mm litz</td>
<td></td>
</tr>
<tr>
<td>Inductance</td>
<td>$L_{1A}, L_{2A}, L_{3A}$</td>
<td>80.06$\mu\text{H}$</td>
</tr>
<tr>
<td>Winding resistance</td>
<td>$R_L$</td>
<td>27.5m$\Omega$, 31.5m$\Omega$, 19m$\Omega$</td>
</tr>
</tbody>
</table>

TABLE IV - 2.5KW FLYBACK TRANSFORMER DESIGN

Fig. 8 – Variation of the (a) Switching frequency $f_{sw}$, (b) Duty cycle $D$, (c) Peak inductor current $I_{L3A(pk)}$ as a function of EV charging power for different EV voltages $V_{ev}$
low powers, the maximum switching frequency is restricted to 350kHz and the converter moves to DCM mode with valley skipping. The duty cycle and peak inductor current $I_{L1A(pk), L3A(pk)}$ increases as the charging power increases, as seen in Fig. 8(b) and Fig. 8(c), respectively. The maximum secondary inductor current $I_{L3A(pk)}=31.5A$ occurs at the crucial operating point of $V_{ev}=333V, I_{ev}=30A, I_{ev(m)}=7.5A$

D. Sizing of filter capacitors

Fig. 7 shows the flyback output current for one 2.5kW stage and the total output current for the 4 interleaved stages. The output ripple reduces by four times due to the interleaved operation. To keep the output voltage ripple within limits, the required output capacitance can be estimated:

$$\Delta V_{ev(p-p)} = \frac{\Delta Q}{C_{ev(net)}} = \frac{I_{ev}(1 - D_s)}{C_{ev(net)}} \left( \frac{T}{4} \right)$$  \hspace{1cm} (30)

For each 2.5kW IBFC, a capacitance of $C_b=3\mu F$ is used at the EV output side. The four IBFC stages are then connected in parallel and two $1.5\mu F$ capacitors, common-mode and differential mode filters are connected to the common output (not shown in Fig. 7).

E. IBFC losses and efficiency

The equations (9)-(10) for the inductor losses and (12)-(15) for the semiconductor losses are used for the loss estimation. The key losses in the IBFC occur in the inductor and semiconductor with minor losses in the capacitors and control circuitry. The estimated losses for one 2.5kW unit for different EV different powers and voltages can be seen in Fig. 9 and Fig. 10 for CH and V2G mode, respectively. In this design, the resonant capacitor, $C_{21}=C_{22}=C_{23}=470pF$. Based on the output capacitance of the MOSFET and diode at 400V, the corresponding value of $T_F=1.596\mu s$.

1) Flyback transformer losses

For the N87 ferrite core, the Steinmetz parameters are given by $A=47.66, b=2.63, a=1.4062 \quad \text{when} \quad P_{core} \quad \text{is in kW/m}^3$, $f_{sw}$ in kHz, $B_{pk}$ in mT and $V_e$ in m$^3$ [43]. Due to the same shape of flux density waveforms for both the boost and flyback converter, the same equivalent frequency $f_{eq}$ is applicable for both. A critical aspect of the flyback transformer losses are the AC copper losses $P_{cu}$ due to the high switching frequency between 30-350kHz. The losses due to skin and proximity effects are estimated based on [44].

Fig. 9(a) and Fig. 10(a) shows the estimated losses in the flyback transformer for CH and V2G modes, respectively. Typical for any flyback in QR, the core and copper losses increase with power due to higher flux swing in the core and higher RMS currents respectively. The relatively high copper losses at low powers are due to the skin and proximity effect due to the high switching frequency. There is no difference in flyback transformer losses between CH and V2G mode, as the same power is handled in both cases.

2) Semiconductor losses

The semiconductor losses are largely dominated by the occurrence of ZVS or LVS, as described in Table III. In case of QR, the turn-off energy is always stored in the quasi-resonant capacitor, and the turn-off losses are nearly zero. For ZVS, the turn-on losses are zero as well. In case of LVS, the turn on-losses are dominated by the energy stored in the QR capacitor on both the primary and secondary side. Hence Eqn. (14) is modified for IBFC for LVS to include the turn-on losses due to the discharging of the MOSFET side QR capacitor $E_{QR1}$ and charging of the diode side QR capacitor $E_{QR2}$:

$$P_{sw} = f_{sw}(E_{on(v_{DSJ}_{DS,RG,T})} + E_{onf(v_{DSJ}_{DS,RG,T})} + E_{QR1} + E_{QR2})$$

$$E_{QR1} + E_{QR2} = \frac{1}{2}C_{ds(nat)}(V_{dc}/2 - V_{ev})^2 + \frac{1}{2}C_{ds(nat)}\left\{ \left( \frac{V_{dc}}{2} + V_{ev} \right)^2 - (2V_{ev})^2 \right\}$$
In practice, the leakage inductance causes a significant part of $E_{QR}$ to be fed to the source/load. Hence, it is assumed here that only 25% of $E_{QR}$ is lost. Fig. 9(b) and Fig. 10(b) shows the total MOSFET and diode losses for CH and V2G mode, where ZVS occurs when $V_{ev}>375V$ for CH mode and when $V_{ev}<375V$ for V2G. For both modes, the semiconductor losses increase with increasing power owing to higher RMS currents. However, when LVS occurs, the switching losses dramatically increase at lower powers owing to the higher switching frequency, as seen in Fig. 8(a), Fig. 9(b), Fig. 10(b). Hence, the total semiconductor losses have a U-shaped curve when LVS occurs.

3) Total losses

Fig. 9(c) and Fig. 10(c) shows the total losses of a 2.5kW IBFC unit including the capacitor and the 2W power of the control circuit. The maximum losses of 44.9W occur at $V_{ev}=333V, P_{ev}=10kW$. The corresponding split-up of losses for CH and V2G modes for the 10kW IBFC is shown in Fig. 11(a). The diode conduction losses are high in CH mode, as there is only a single diode at the secondary and not two in parallel, like the MOSFET. The efficiency of the 10kW IBFC is shown in Fig. 11(b) and the peak efficiency is 98.8% ($V_{ev}=500V$, CH). The efficiency plot clearly reflects the occurrence of ZVS for CH and V2G mode, as shown in Table III. Commercial EVs typically have voltages in the range of 200-500V, hence the converter has a peak efficiency above 97.8% in this voltage range.
VII. CLOSED LOOP CONTROL

The converter is capable of four different power flows namely PV→EV, PV→Grid, Grid→EV and EV→Grid and this enabled by the closed-loop control. The closed-loop control is modularly organized into three control loops, one for each of the three converters (Fig. 12). The primary purpose of the control for the PV IBC, EV IBFC and grid inverter is MPPT, control of EV charging and power balance, respectively. The inverter uses the DC-link voltage to perform the power balance and PV, and EV converter implements power curtailment if the DC-link voltage is out of bounds.

A. PV converter

The IBC’s control has three control loops working in parallel to control the duty cycle $D$ as in Fig. 12(a):

$$D = D_{\text{max}} - d^*$$  \hspace{1cm} (33)

The control output $d^*$ is the maximum value as dictated by all the three loops (indicated by the diode) and the maximum duty cycle $D_{\text{max}}=62.5\%$. The first loop is for MPPT, that uses a microcontroller to continuously adjust the duty cycle by perturb-and-observe method [45]. The second and third loop are used to limit duty cycle if the PV current $I_{PV}$ is more than $I_{PV(max)}=32A$ or if the DC-link voltage is beyond $V_{dc(max)}=810V$.

B. DC/DC bidirectional EV charger

The IBFC control for the EV charging has four control loops acting in parallel, as seen in Fig. 12(b). The first loop controls the MOSFET on-time, $T_{on}$ based on the current reference, $I_{ev}^*$. The next two loops are used for curtailment of charging and V2G power if the minimum (700V) and maximum (810V) DC-link voltage are reached, respectively. The last loop is used to limit the on-time when the maximum battery voltage $V_{ev}$ is reached. The MOSFET off-time, $T_{off}$ is determined by the zero-current detection (ZCD) and QR valley detection circuit. The phase shift block is responsible for maintaining 90° phase shift between the interleaved modules. Depending on charge or V2G mode, the gate signals are provided to the appropriate MOSFETs.

C. DC/AC Grid inverter

The DC/AC inverter is responsible for maintaining the DC-link voltage at $V_{dc}^*=750V$ by controlling the grid current, $I_{AC}sin\theta$ that is either drawn (Rectifier mode, REC) or fed to the grid (inverter mode, INV). A PLL is used to estimate the voltage phase and maintain a high power factor, as shown in Fig. 12(b). There are two PI loops, the outer loop controls the DC-link voltage, while the fast inner loop is used to control the current.

![Fig. 11 – (a) Split up of losses for $V_{ev}=333V$, 10kW power for CH and V2G modes; (b) Efficiency of 10kW IBFC for CH and V2G mode](image-url)
D. Modular implementation

The control design is hence simple as it only requires an external voltage $V_{ev}^*$ and current set point for the EV, $I_{ev}^*$. If the inverter is disconnected suddenly, then both the PV and EV converters move to power curtailment mode and ensure safety. Secondly, no modifications in the control are needed if the bidirectional EV charger is used without the solar DC/DC converter.

The stability of the multi-loop control of the converter is addressed by three factors. Firstly, at any point in time, only one of the parallel loops is in operation for each of the PV and EV control. This is due to the parallel diodes in the control loop with one common point at the output which ensures that only one diode is forward biased at a given time. Secondly, a large energy buffer is created on the DC-link through the use of several electrolytic capacitors (6x 450V, 470μF). Since the DC-link voltage $V_{dc}$ is used by all the three controls (inverter, IBC, IBFC), a large energy buffer provides sufficient time for response during fast power variations. Finally, the stability of the control is tested individually and collectively by running several test cases at both low and high powers.

Fig. 12 – Schematic of the closed loop control: (a) PV converter, (b) EV charger and (c) Grid inverter
VIII. EXPERIMENTAL SETUP & VERIFICATION

A. Prototype of the EV-PV converter

Fig. 13 shows the prototype of the developed EV-PV converter with the PV IBC, EV IBFC, and the grid inverter. The converter is modularly built with the PV IBC and its controller on a separate PCB. Therefore, the converter can be used either as a solar-powered EV charger or as a bidirectional EV charger without solar. Due to the modular nature of the converter control, several bidirectional EV charger modules (i.e., flyback converter + inverter) can be operated in parallel by giving them a common current setpoint, $I_{ev*}$. By doing so, the charging power can be scaled up from 10kW to reach up to 100kW. Hence, the developed charger can be used for both Level 2 medium power charging and Level 3 fast charging.

The converter is 50x42x12cm with the control board placed at the back-side PCB. Based on cabinet dimensions, the power density of the PV converter, EV+Grid converters, and the complete EV-PV converter are 1380W/l, 555W/l and 396W/l, respectively. In order to make it commercially usable, the prototype is designed to be compatible with EN60950 for safety and EN55011 (class A), EN61000-4-2 to EN61000-4-6, EN61000-4-11 for Emission (Industrial).

B. Experimental waveforms and efficiency

Fig. 14 shows the operating waveforms of the PV IBC for CCM and DCM modes, where a PV emulator is used as input. During CCM, the inductor current $I_{L(1)}$ rises when the gate voltage $V_{GS(1)}$ is ON and then begins to fall once the gate is OFF, in Fig. 14(a). In DCM, the inductor current $I_{L(1)}$ goes to zero before the end of the switching cycle, causing the drain-source voltage $V_{ds(1)}$ to oscillate as it goes from $V_{ds(on)}$ to $V_{PV}$, in Fig. 14(b).
Fig. 14 – (a) Waveforms for the PV IBC for the phase shifted gate voltage $V_{GS}$, Inductor current $I_L$ and MOSFET drain-source voltage $V_{ds}$ for (a) CCM mode ($V_{PV}=700$ V, $I_{PV}=10$ A); (b) DCM mode ($V_{PV}=400$ V, $I_{PV}=10.75$ A)

Fig. 15 – Drain-source voltage $V_{ds}$ and gate voltage $V_{gs}$ for one phase of the IBFC for CH: (a) Quasi resonant operation LVS for $V_{e}=250$V, $I_{e}=5$A (b) Valley skipping and DCM operation at low powers for $V_{e}=100$V, $I_{e}=1$A

Fig. 16 – Waveforms of the AC current fed to the grid in the V2G mode for $P_{ev}=10$kW, $V_{ev}=402$V and the corresponding power and THD measurements
C. Comparison with conventional design

The developed three port converter is compared to a conventional solar EV charger that uses a 10kW solar inverter [46] and 10kW unidirectional EV charger [47], based on silicon IGBTs and ferrite cores. [46], [47] have the same specifications as listed in Table I, but use the AC grid to exchange power from the PV to EV, instead of DC. [46] uses a three-phase resonant topology while [47] uses an IBC with a three-phase inverter.

Firstly, for Grid→EV the developed converter has a much higher peak and a higher partial load efficiency than the resonant topology, as seen in Fig. 17. The high partial load efficiency makes it suitable for smart charging of EVs where the EV charging power is continuously varied [28]. Secondly, the power density of the developed charger (396W/l) is three times that of the two converters combined (134W/l). Thirdly, the proposed converter is bidirectional for V2G while the other is not.

D. Testing with a Nissan Leaf - Charging and V2G

Fig. 18(a) shows the testing of the converter to charge and discharge a V2G enabled Nissan Leaf EV using an outdoor cabinet. A Chademo charge controller that implements the CAN communication with the EV was used to...
provide the voltage $V_{ev}$ and current set points $I_{ev}$ to the power converter. Fig. 18(b) shows the 386V EV battery first being discharged (V2G) with a current and power of -23.5A, -9.07kW and then being charged with a current and power of 23.5A, 9.07kW, respectively. Due to the absence of PV panels at the test location, there was no PV power input.

IX. CONCLUSIONS

This paper presents the development of a 10kW, three-port, bidirectional converter for direct DC charging of EV from PV. The developed converter is compatible with CCS and Chademo EV charging standard and can operate with a PV array of wide voltage and power range. Interleaving of converters, Silicon carbide (SiC) devices, and powdered alloy core inductors are extensively used to increase the switching frequency, while keeping the converter losses within limits. This has helped to increase the power density by a factor of three when compared to conventional designs and reduce the voltage ripple at the EV, PV ports.

The converter is modularly designed with three sub-converters connected on a 750V central DC-link: interleaved boost converter for PV, a three-phase inverter for the AC grid and an interleaved flyback converter for EV. While the flyback is traditionally considered suitable only for low powers, this paper shows how the use of SiC devices in a QR mode flyback converter can achieve high efficiency even at high powers. Three closed loop controls were developed and tested for the three sub-converter which enables four power flows: PV$\rightarrow$EV, EV$\rightarrow$grid, grid$\rightarrow$EV and PV$\rightarrow$grid.

A 10kW prototype was built and tested and exhibits a peak efficiency of 95.2% for PV$\rightarrow$EV, 95.4% for Grid$\rightarrow$EV, 96.4% for PV$\rightarrow$Grid. The developed prototype has a much higher peak efficiency, higher partial load efficiency and three times higher power density than currently existing solutions based on AC power exchange. The charge and V2G operation at 10kW were tested with a Nissan Leaf EV with a Chademo charge controller.

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