Low-Power CMOS Smart Temperature Sensor With
a Batch-Calibrated Inaccuracy of ±0.25 °C (±3σ)
from −70 °C to 130 °C

Aita, AL; Pertijs, Michiel; Makinwa, Kofi; Huijsing, Johan H; Meijer, Gerard

DOI
10.1109/JSEN.2013.2244033

Publication date
2013

Document Version
Accepted author manuscript

Published in
IEEE Sensors Journal

Citation (APA)

Important note
To cite this publication, please use the final published version (if applicable). Please check the document version above.
A Low-Power CMOS Smart Temperature Sensor with a Batch-Calibrated Inaccuracy of ±0.25°C (±3σ) from −70°C to 130°C

André L. Aita, Member, IEEE, Michiel A. P. Pertjjs, Senior Member, IEEE, Kofi A. A. Makinwa, Fellow, IEEE, Johan H. Huijsing, Fellow, IEEE, and Gerard C. M. Meijer, Senior Member, IEEE

Abstract—In this paper, a low-power CMOS smart temperature sensor is presented. The temperature information extracted using substrate PNP transistors is digitized with a resolution of 0.03°C using a precision switched-capacitor (SC) incremental ΔΣ A/D converter. After batch calibration, an inaccuracy of ±0.25°C (±3σ) from −70°C to 130°C is obtained. This represents a two-fold improvement compared to the state-of-the-art. After individual calibration at room temperature, an inaccuracy better than ±0.1°C over the military temperature range is obtained, which is in-line with the state-of-the-art. This performance is achieved at a power consumption of 65μW during a measurement time of 100ms, by optimizing the power/inaccuracy trade-offs, and by employing a clock frequency proportional to absolute temperature (PTAT). The latter ensures accurate settling of the SC input stage at low temperatures, and reduces the effects of leakage currents at high temperatures.

Index Terms—smart temperature sensors, substrate PNP transistors, batch calibration, ΔΣ A/D conversion.

I. INTRODUCTION

SMART temperature sensors based on the substrate PNP transistors available in standard CMOS technology can achieve inaccuracies below ±0.1°C over the military range (−55°C to 125°C) [1][2]. To achieve this, such sensors require individual calibration and trimming. Although efficient methods of calibration and trimming have been devised [3][4], individual calibration is still a significant cost contributor, even if it is only done at room temperature. Significant cost reductions can be achieved by employing batch calibration, i.e. calibrating a limited number of samples from a production batch, obtaining an estimate of their average error, and then using this information to trim the entire batch.

In this work, a CMOS temperature sensor is presented that employs batch calibration to achieve an inaccuracy of ±0.25°C (±3σ) from −70°C to 130°C, which represents a two-fold improvement on the state-of-the-art [1][5]. Moreover, the sensor achieves an inaccuracy of ±0.1°C after individual calibration at room temperature, at par with the state-of-the-art [1], while consuming 3x less energy per measurement. While more energy-efficient temperature sensors have been reported [5][6], this is at the expense of somewhat lower accuracy.

This paper is organized as follows. Section II reviews the sensor’s operating principle, and discusses the main sources of inaccuracy. Section III describes the sensor front-end at the circuit level, detailing the approach taken to achieve the combination of high accuracy and low energy consumption. Section IV addresses innovative aspects of the incremental ΔΣ A/D converter, including a power-efficient implementation of its first integrator, and the use of a clock frequency proportional to absolute temperature (PTAT) to widen the sensor’s temperature range. Measurement results are presented and discussed in Section V, followed by conclusions.

II. SENSOR OPERATING PRINCIPLE

A. Sensor Block Diagram

Fig. 1 shows a block diagram of the sensor, which consists of a front-end circuit, a ΔΣ modulator and a decimation filter. In the front-end circuit, a substrate PNP transistor, either Qx or Qk, biased through its emitter with a current $I_{bias}$, generates a voltage $V_{BE}$ complementary to absolute temperature (CTAT), given by

$$V_{BE}(T) = \frac{kT}{q} \ln \left( \frac{I_c(T)}{I_{S}(T)} \right) + 1 \approx \frac{kT}{q} \ln \left( \frac{I_{bias}(T)}{I_S(T)} \right),$$

where $k$ is Boltzmann’s constant, $T$ the absolute temperature, $q$ the electron charge and $I_S$ is the transistor’s saturation current. The approximation is valid for $I_c=I_S=I_{bias}$ and if the ratio $I_c/I_S >> 1$. 
A voltage proportional to absolute temperature (PTAT) \( \Delta V_{BE}(T) = V_{BE,R} - V_{BE,L} \), is obtained by biasing two nominally equal PNP transistors \( Q_L \) and \( Q_R \) at a 1:m current ratio, i.e. \( m = I_{bias,R}/I_{bias,L} \). Provided the approximation in (1) is valid and mismatch errors in the bias currents and PNP transistors are negligible, this PTAT voltage, given by

\[
\Delta V_{BE}(T) \approx \frac{kT}{q} \ln(m),
\]

is intrinsically accurate. Ideally, it does not depend on any processing parameters [7] and, because of that, hardly suffers from process spread.

By adding to either \( V_{BE,L} \) or \( V_{BE,R} \) an amplified version of \( \Delta V_{BE} \), i.e. \( a \Delta V_{BE} \), a first-order temperature-independent reference voltage \( V_{REF} \) is obtained

\[
V_{REF} = a \Delta V_{BE} + V_{BE},
\]

where \( a \) is the scale factor required to compensate for the variation of \( V_{BE} \) with the temperature, about \(-2mV/°C\), with the variation of \( \Delta V_{BE} \) with the temperature, about +0.14mV/°C for \( m = 5 \). Exact values for \( a \) were obtained through simulations, taking into account the actual front-end biasing circuitry, and then determine an appropriate level of power consumption.

The temperature can thus be measured ratiometrically by comparing the scaled PTAT voltage \( a \Delta V_{BE} \) with the reference voltage \( V_{REF} \) [8], i.e., by evaluating the ratio

\[
\mu = \frac{V_{PTAT}}{V_{REF}} = \frac{a \Delta V_{BE}}{V_{BE}} + \frac{\alpha \Delta V_{BE}}{V_{BE}} = \frac{kT}{q} \alpha \ln(m) + \frac{\alpha V_{BE}}{q} = \frac{kT}{q} \alpha \ln(m) + \frac{\alpha V_{BE}}{q},
\]

which is also PTAT.

Whereas the front-end generates \( V_{BE} \) and \( \Delta V_{BE} \), the \( \Delta \Sigma \) modulator generates a bitstream \( bs \), whose average equals \( \mu \). This is achieved through charge balancing, i.e. by properly applying, every clock cycle, either \( a \Delta V_{BE} \) (when \( bs = 0 \)) or \( \alpha V_{BE} - V_{REF} \) (when \( bs = 1 \)) to the input of a loop-filter [1]. Because of the modulator’s feedback, the average at the input of the loop filter over time is zero, and the output bitstream \( bs \) will have the desired average \( \mu \) given by (4). After decimation, the temperature reading can then be determined as

\[
D_{out} = A \mu + B.
\]

where \( A = 600 \) and \( B = 273 \) are the gain and offset coefficients, respectively, for a direct result in degrees Celsius.

### B. Design Approach

In order to design a low-power high-accuracy sensor, the minimum amount of power needed to minimize the various error sources must be determined. To find how each error affects the temperature measurement, the sensitivity of the measured temperature (as given in (5)) to changes in \( V_{BE} \), \( \Delta V_{BE} \), \( \alpha \) [8] and \( m \) is calculated. These sensitivities are equal to:

\[
\frac{\partial V_{BE}}{\partial T} \approx 3 \frac{mV}{\alpha} \quad \frac{\partial \Delta V_{BE}}{\partial T} \approx 3 \frac{mV}{\alpha} \quad \frac{1}{\alpha} \approx 1 \quad \frac{1}{m} \approx 1 \quad \frac{1}{\alpha} \approx 1
\]

(6)

Allocating a maximum error margin of 0.01°C to each of the error sources, to arrive at an overall error below 0.1°C, a worst case variation of about 30µV in \( V_{BE} \), 2.0µV in \( \Delta V_{BE} \) for \( \alpha = 16 \), and a maximum relative error of about 0.0067% in \( \alpha \) and 0.01% in \( m \) are found (for \( \alpha = 16 \), \( T = 300\text{K} \)). The next step is to identify the accuracy-power tradeoffs in the interface circuitry, and then determine an appropriate level of power consumption.

### C. Process Spread of \( V_{BE} \)

While \( \Delta V_{BE} \) is insensitive to process spread, \( V_{BE} \) suffers strongly from process spread. Statistics about \( V_{BE} \) spread can be used to estimate the initial inaccuracy (without any correction) of \( V_{BE} \), and so of the sensor. Typically, this spread results in errors of several degrees and so the sensor must be trimmed. The success of this approach, though, will depend on the identification and reduction of the main sources of \( V_{BE} \) spread, discussed as follows.

#### 1) Spread due to the Saturation Current \( I_S \)

The spread of the saturation current \( I_S \) of a PNP transistor is the main cause of \( V_{BE} \) spread. In order to see how this affects \( V_{BE} \), a deviation \( \Delta I_S \) from the nominal value \( I_S \) is introduced in the equation for \( V_{BE} \) given in (1), resulting in

\[
V_{BE} = \frac{kT}{q} \ln \left( \frac{I_{bias}}{I_S + \Delta I_S} \right)
\]

(7)

This shows that the effect of the spread of \( I_S \) on \( V_{BE} \) is PTAT, if \( \Delta I_S/I_S \) is assumed temperature independent. Thus, the spread of \( I_S \) causes the function \( V_{BE}(T) \) to rotate around a fixed point at 0K. Because this PTAT error has only one degree of freedom, it can be trimmed based on a calibration at only one temperature, e.g. room temperature [7].

However, the assumption that \( \Delta I_S/I_S \) is temperature independent is not necessarily true. Mechanical stress due to
packaging may introduce a temperature-dependency to this ratio. Luckily, vertical PNP transistors are relatively insensitive to stress [7], which is why the temperature dependency of $\Delta I/I_s$ will be neglected in this work.

2) Spread due to the Current Gain $\beta$

Because the PNP transistors are biased via their emitters, the collector current is given by

$$I_c = \frac{\beta}{1 + \beta} I_{\text{bias}} \tag{8}$$

where $\beta$ is the forward current gain. Substituting (8) in (1) results in

$$V_{BE} = \frac{kT}{q} \ln \left( \frac{\beta + \Delta \beta}{1 + (\beta + \Delta \beta)} \right) \frac{I_{\text{bias}}}{I_s} \tag{9}$$

which reveals that $V_{BE}$ depends also on $\beta$ and, because of that, is sensitive to any process-spread on $\beta$. To see how this affects $V_{BE}$, a deviation $\Delta \beta$ from the nominal value $\beta$ is introduced in (9), i.e.

$$V_{BE} = \frac{kT}{q} \ln \left( \frac{\beta + \Delta \beta}{1 + (\beta + \Delta \beta)} \right) \frac{I_{\text{bias}}}{I_s} \tag{10}$$

This shows that $V_{BE}$ is modified by an error term that is proportional not only to $\Delta \beta/\beta$, but also to the factor $1/(1+\beta)$. Because $\beta$ is typically highly temperature dependent, the spread in $\beta$ will cause a non-PTAT error in $V_{BE}$. This adds to the PTAT error due to the spread of $I_s$, resulting in an overall error with more than one degree of freedom. Depending on the magnitude of $\Delta \beta/\beta$, a single-temperature calibration may therefore be insufficient.

Equation (10) also shows that transistors with larger $\beta$ are less sensitive to $\beta$ spread. Unfortunately, vertical PNP transistors in CMOS technology tend to have a small $\beta$. In the 0.7µm CMOS technology we used, $\beta$ is approximately 22. If $\Delta \beta/\beta$ is assumed to be about 20%, a $V_{BE}$ variation of about ±0.25mV results, which translates into a temperature error of about ±0.1°C. This shows that the effect of $\beta$ spread in $V_{BE}$ needs to be reduced if an accuracy of ±0.1°C is to be obtained using a single-temperature calibration. This need is even more acute in deeper sub-micron CMOS technology, where much lower values of $\beta$ are found [5][6]. A technique for making $V_{BE}$ less sensitive to spread of $\beta$ will be described in Section III-B.

3) Spread due to biasing current

The bias current, $I_{\text{bias}}$ in (9), also affects the accuracy of $V_{BE}$. Generally, this bias current is derived from a bias voltage using a bias resistor. As will be discussed in the following section, if a PTAT bias voltage is used, its contribution to process spread of $I_{\text{bias}}$ can be made negligible. The bias resistor, however, will inevitably be subject to process spread. Provided the temperature dependency of this resistor is insensitive to process variations, the effect of this on $V_{BE}$ is identical to that of the spread of $I_s$, i.e. it gives rise to a PTAT error in $V_{BE}$. Both errors can thus be corrected by a single PTAT trim.

III. SENSOR FRONT-END

The sensor front-end, as shown in Fig. 2, is composed of a core that in effect generates $V_{BE}$ and $\Delta V_{BE}$, as described in Section II, and of a bias circuit that generates the PTAT biasing as needed in the core.

In the core, Dynamic Element Matching (DEM) of current sources is used to provide an accurate current ratio $m$ [9]. Every $\Delta V_{BE}$ cycle, a different unit current source is used to bias the transistor $Q_h$ while the $m$ remaining ones are used to bias $Q_R$. By alternating the unit current source, over $(1+m)\Delta V_{BE}$ cycles, errors due to current-source mismatch are averaged out, so a more accurate $1/m$ ratio and thus $\Delta V_{BE}$ voltage is obtained [1]. The value of the ratio $m$ and the bias current level, though, are subject to accuracy and power consumption constraints, as will be discussed below.

A. Current Ratio and Bias Current

When the PNP bias current is reduced so as to lower the front-end power consumption while keeping $(1+m)$ current sources for DEM, the approximation for $V_{BE}$ as given in (1) is no longer accurate once the assumption of $I_c/I_s >> 1$ no longer applies. In this case, $V_{BE}$ is better approximated as (assuming for now $I_c=I_{\text{bias}}$)

$$V_{BE} = V_r \ln \left( \frac{I_{\text{bias}}}{I_s} + 1 \right) \tag{11}$$

which results in a $\Delta V_{BE}$ given by

$$\Delta V_{BE} = V_r \ln \left( \frac{m I_{\text{bias}} + I_s}{I_{\text{bias}} + I_s} \right) \tag{12}$$

if the mismatch in the current sources and PNP transistors is negligible (i.e. $I_{\text{bias}}=I_{s,R}$). The result in (12) shows that, regardless of how accurately $m$ is established, the presence of the saturation current $I_s$ will still cause a certain error in the value of $\Delta V_{BE}$.

Though the magnitude of $I_s$ can be reduced by reducing the emitter area of the PNP transistors, this is at the expense of poorer matching. The transistors also need to work in a region with neither low nor high injection effects and the region must have a constant current gain $\beta$[8].

The worst case relative error in the current ratio $m$ is given by

$$\frac{\Delta m}{m} = \frac{m I_{\text{bias}} + I_{s,\text{max}} - m I_{\text{bias}}}{m I_{\text{bias}} - I_{\text{bias}}} \tag{13}$$

where $I_{s,\text{max}}$ is the largest saturation current (i.e. at the highest temperature). According to (13), for a given $m$, a sufficiently high $I_{\text{bias}}$ has to be chosen to keep the error below a given level.
However, it is more important to evaluate the error contribution due to the saturation current against the total bias current of the core, i.e., $I_{sat}$ and $I_{total}$. Fig. 3 shows the simulated error contribution versus $I_{total}$ for $m=2, 5$ and 10. The results show that, for a given maximum error contribution, the required bias current can be reduced by reducing the current ratio $m$. However, as the resulting reduced sensitivity of $V_{BE}$, this comes at the expense of more stringent offset and noise requirements on the A/D converter. As a compromise, $m$ was set to 5. In addition, in order to limit the error contribution to below 0.02°C, $I_{bias}$ was set to 400nA, giving a total bias current of about 2.3 µA. Because the bias current is PTAT, the value of 400nA (at $T=140°C$) translates to a nominal bias current of approximately 250nA at $T=30°C$.

![Fig. 2. Circuit diagram of the sensor front-end: biasing circuit and core](image)

**Fig. 2.** Temperature error versus the total bias current $I_{total}$ for $m=2, 5$ and 10. Results obtained for $I_{bias}=110pA$ (estimated for PNPs with emitter area $A_e=225µm^2$ at $T=140°C$ [10]).

**B. PTAT biasing - Bias Circuit**

A PTAT bias current [11] was chosen to bias the two PNPs $Q_1$ and $Q_2$ in the core. Compared to other types of bias currents, a PTAT current can be made relatively insensitive to process spread, as it is generated from a process-insensitive PTAT PTAT voltage. Thus, only the spread of the resistor $R_1$ (Fig. 2) causes significant spread of the currents [8]. Additionally, a PTAT current partially cancels the curvature of $V_{BE}$ [12].

The bias circuit is built around a chopped opamp and two PNP transistors $Q_1$ and $Q_2$ biased at a $1:p$ current ratio (Fig. 2).

Ignoring resistor $R_2$ for now, the opamp forces the PTAT difference $\Delta V_{BE,b}$ between the base-emitter voltages of these transistors to appear across resistor $R_1$, resulting in a PTAT unit bias current of $\Delta V_{BE,b}/R_1$.

Resistor $R_2$ has been added to implement a $\beta$-compensation scheme [1]. The voltage drop across $R_2$ due to the base current of $Q_2$ makes the bias current proportional to $(1+\beta)/\beta$ for $R_2=R_1/\beta$, so that it gives rise to a PTAT collector current when copied to the emitters of $Q_1$ and $Q_2$ in the core. Thus, errors in $V_{BE}$ due to the spread of the PNPs’ finite current gain $\beta$ are minimized.

As in the core, $Q_1$ and $Q_2$ are biased at a 1:5 current ratio ($p=5$), but with a unit bias current of only 125nA (half of that used in the core). Though a greater current ratio $\rho$ would produce a greater $\Delta V_{BE,b}$, which is less sensitive to the opamp’s offset, $p=5$ is a better trade-off, reducing power dissipation at the expense of a small contribution to the sensor’s inaccuracy (smaller than 0.03°C).

Mismatches between the (1+$p$) current sources in the bias circuit give rise to an error in $\Delta V_{BE,b}$, and hence in the PTAT bias current of the core. This, in turn, increases the spread of $V_{BE}$ and thus the batch-calibrated inaccuracy of the sensor. Since the sensor is about an order-of-magnitude less sensitive to errors in $V_{BE}$ than it is to errors in $\Delta V_{BE}$, the matching requirement for the current sources in the bias circuit is much more relaxed than that for the current sources in the core. It can be shown that matching better than 0.15% is sufficient to reduce those errors to less than 0.01°C. While DEM could be applied, a careful inter-digitated common-centroid layout was found to be sufficient to achieve this level of matching. The current sources of the core were included in this matched layout, to minimize the spread associated with current-source mismatch between the bias circuit and the core.

**C. Trimming Approach**

In order to correct for the process spread of $V_{BE}$, the same $(1+m=6$ current sources of the core are used to digitally adjust the bias current of the PNP transistors when generating $V_{BE}$ between $I_{bias}$ and $mI_{bias}$ (digital control in Fig. 2). Five of the six current sources are used to coarse trim the bias current. Because the sensor is designed to normally operate with two unit currents, there is one coarse step down and three up, which gives a near-balanced trimming capability due to the logarithmic dependency of $V_{BE}$ on $I_{bias}$. To fine trim the sensor, the bitstream method [13] is used. The sixth current source is switched on and off, generating a bias current between 0 and $I_{bias}$ depending on the output of a digital modulator. For a nominal bias current of 250nA, an 8-bit modulator was used to obtain 1nA trimming resolution.

**IV. INCREMENTAL SC ΔΣ ANALOG-TO-DIGITAL CONVERTER**

The ratio-metric measurement of $\alphaDV_{BE}$ with respect to $V_{REF}$ has been implemented using a second-order switched-capacitor (SC) incremental ΔΣ modulator. It is based on the design presented in [1], but differs from this design in two important
aspects detailed below: a more power-efficient first integrator and a new temperature-dependent clocking scheme are employed.

A. Operating Principle

Fig. 4 shows a simplified circuit diagram of the modulator. It translates the output voltage of the front-end circuit $V_{\Delta \Sigma}$, which is either $\Delta V_{BE}$ (when $bs=0$) or $-V_{BE}$ (when $bs=1$), into a bitstream bs whose average value $\mu$ equals the desired ratiometric function given by (4), as explained in Section II. A decimation filter (not shown), is used to decimate and scale this bitstream according to (5) to produce a digital output.

The modulator is operated using a two-phase non-overlapping clock. During phase $\phi_1$, $V_{\Delta \Sigma}$ is sampled on capacitors $C_s$, while during phase $\phi_2$, the associated charge is transferred to the integration capacitors $C_{int}$. When $bs=0$ and $V_{\Delta \Sigma}=\Delta V_{BE}$, all $\alpha$ capacitors $C_s$ are used, whereas when $bs=1$ and $V_{\Delta \Sigma}=-V_{BE}$, only a single capacitor $C_s$ is used. This implements the relative gain $\alpha$ as needed in (3). It is worth mentioning that the value of $\alpha=16$ for $m=5$ establishes a reference voltage $V_{REF}$ that is slightly dependent on the temperature, which yields further compensation of the curvature of $V_{REF}$ [12], in addition to the PTAT biasing. Because of the modulator’s feedback, the average charge integrated over time is zero, i.e.

$$(1-\mu)\alpha C_s \Delta V_{BE} + \mu C_s (-V_{BE}) = 0 \quad (14)$$

which results, when solved for $\mu$, in the expression given by (4).

The size of the sampling capacitors ($C_s=2.5pF$) was a trade-off between settling time, on one hand, and $kT/C$ noise and most importantly charge injection error on the other.

To ensure that the modulator does not introduce any significant errors, several precision techniques are applied [1][8]. Offset errors are reduced below 2$\mu$V (which corresponds to 0.01°C) by means of a combination of correlated double sampling (CDS) [14] in the first integrator and system-level chopping. Errors in the factor $\alpha$ due to capacitor mismatch are mitigated by applying dynamic element matching techniques, i.e. by dynamically interchanging the sampling capacitors $C_{S, i=1,2,...,\alpha}$ (Fig. 4), so as to average out gain errors. Because the same integration capacitor $C_{int}$ is used, regardless of the cycle, it does not affect $\alpha$.

B. Modulator Implementation – First Integrator

The first integrator is built around a fully-differential gain-boosted telescopic-cascode opamp (shown in Fig. 5). Compared to the folded-cascode topology employed in earlier work [1], a notable power saving is achieved, since the telescopic topology only needs half the supply current of the folded version for the same transconductance and maximum output current. This comes at the expense of reduced output swing [15]. This can be accommodated thanks to the modulator’s input feed-forward topology, which minimizes the output swing [1]. Since the integrator’s CDS scheme requires unity-gain feedback, the opamp was designed to operate with identical input and output common-mode levels. Gain-boosting [16] was used to achieve a DC gain higher than a 100dB over all process corners and operating conditions, so as to ensure negligible sampling errors. Nominally, the DC gain of the first integrator is 135dB, with a GBW of 200kHz. Including the boosting amplifiers, the opamp draws a total supply current of 4.5$\mu$A.

C. PTAT Clock Frequency

Because of the PTAT biasing used in the front-end, the time needed for the modulator to settle is temperature dependent. Since the modulator’s sampling capacitors (capacitors $C_s$ in Fig. 4) are indeed the front-end’s output load, charging these capacitors will take longer at low temperatures. This is shown in Fig. 6, where $V_{\Delta \Sigma}$ is the sampled voltage (either $V_{BE}$ or $\alpha \Delta V_{BE}$).

As a result, the use of a constant sampling clock frequency is sub-optimal in terms of settling time. A clock frequency optimized for accurate settling at high temperatures leads to errors at low temperatures due to incomplete settling. Conversely, a clock frequency optimized for accurate settling at low temperatures leads to a settling time that is over-
designed, and hence less power-efficient, at high temperatures. Moreover, it will lead to increased errors due to leakage at the high end of the temperature range. 

To accommodate accurate settling at both ends of the temperature range without these issues, the sensor uses a sampling clock with a temperature-dependent frequency. At low temperatures, the frequency is lower than its nominal value, allowing more time for settling, while at high temperatures, it is higher, reducing leakage errors by shortening the sampling period.

A nominal clock frequency of 11kHz was chosen to ensure accurate settling at 30°C. To find the optimal temperature dependency of the clock frequency, it is important to account for the fact that the settling consists of a slewing phase and an exponential settling phase [17]. Taking the temperature dependence of these phases into account, an optimal frequency of about 70% of the nominal frequency is found at –55°C, and about 140% of the nominal frequency at 125°C. This leads to a frequency variation of about 1kHz/20°C, as shown in Table I. Because this temperature dependence is roughly proportional to absolute temperature, we refer to this as a PTAT clock frequency.

![Fig. 6. Simulated slewing-time dependence on temperature (for a VBE cycle, i.e. VAE=VBE) for a fixed clock frequency f=10kHz.](image)

TABLE I

<table>
<thead>
<tr>
<th>System (PTAT) Clock Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature (°C)</td>
</tr>
<tr>
<td>Clock frequency (kHz)</td>
</tr>
</tbody>
</table>

V. MEASUREMENT RESULTS

The temperature sensor was fabricated in a standard 0.7μm CMOS process and encapsulated in a ceramic DIL package. A chip micrograph of the sensor is shown in Fig. 7. The die size is 4.5 mm², including bondpads. The chip contains all required circuitry, except for the clock generator and decimation filter of the ∆Σ ADC, which were implemented off chip for flexibility.

Measurements have been made on 20 samples from one batch. These samples were mounted, together with a precision platinum thermometer calibrated to 0.01mK, on an aluminum block that provided thermal stability. This block, in turn, was placed in a climate chamber to vary temperature.
In addition, Fig. 10 presents the same result as that of Fig. 9, but without correction for systematic non-linearity. As expected, the inaccuracy of ±0.15°C for the same temperature range is slightly worse, but it shows the well-defined and systematic curvature behavior of the samples, as well as a small systematic error due to leakage at 125°C.

Fig. 10. Measured temperature error without compensation for systematic non-linearity and leakage, after trimming based on an individual calibration at 30°C (20 samples with average and ±3σ limits).

C. PTAT Clock Frequency versus Fixed Clock Frequency

Measurement results comparing the sensor performance using the PTAT clock frequency (center frequency $f_{\text{nom}}=11$kHz) and a fixed (11kHz) clock frequency are shown in Fig. 11. As expected, the PTAT clock leads to the same performance as a fixed clock in the middle of the temperature range, but it delivers superior performance at the temperature extremes: up to 50% less batch-calibrated inaccuracy at −55°C.

Fig. 11. Measured temperature error using a PTAT clock frequency (nominal frequency $f_{\text{nom}}=11$kHz) and fixed clock frequency ($f=11$kHz, dashed lines) (20 samples with average and ±3σ limits).

D. Measurement at 150°C

The 20 samples were also tested up to 150°C. At these temperatures, the PTAT clock frequency cannot compensate completely for the exponential rise in the leakage current. Therefore, clock frequencies higher than that defined by a PTAT characteristic were tested. The measured temperature errors, shown in Fig. 12, show a systematic non-linearity varying according to the clock frequency. For instance, at 150°C, a systematic error (on average) of −0.9°C, −0.5°C and 0°C is observed for clock frequencies of 20kHz, 25kHz and 35kHz, respectively. Because of the very systematic error behavior, the same non-linearity correction used to handle the third-order curvature can be used to compensate for leakage at 150°C. As shown, this extends the sensor’s operating range up to 150°C while maintaining ±0.25°C inaccuracy.

E. Benchmark

Table II summarizes the measured performance of the 20 samples and compares it with other designs.

Fig. 12. Measured temperature error (extended range, up to 150°C) after batch calibration, for three different clock frequencies at 150°C: 20kHz, 25kHz and 35kHz (20 samples with no third-order curvature nor leakage correction).
VI. CONCLUSION

This paper has presented the theory, design and implementation of a CMOS smart temperature sensor based on substrate PNP transistors and an incremental SC $\Delta \Sigma$ A/D converter. Without individual calibration, this sensor achieves an inaccuracy of $\pm0.25^\circ\text{C} (\pm3\sigma)$ from $-70^\circ\text{C}$ to $130^\circ\text{C}$, twice as good as that of the best ones reported up to now, while consuming only 6.5µW during a measurement time of 100ms. This is accomplished by optimizing the power/inaccuracy tradeoffs and by incorporating several circuit techniques, discussed throughout the paper. After an individual calibration at room temperature, the sensor achieves an inaccuracy of $\pm0.1^\circ\text{C} (\pm3\sigma)$ over the military range, which matches the state-of-the-art, while consuming 3x less energy per measurement.

REFERENCES


[6] K. Souri and K. A. A. Makinwa, “A 0.12 mm² 7.4 µW Micropower Temperature Sensor With an Inaccuracy of $\pm0.2^\circ\text{C} (3\sigma)$ From $-30^\circ\text{C}$ to $125^\circ\text{C}$,” IEEE J. Solid-State Circuits, vol. 46, no. 17, pp. 1693–1700, Jul. 2011.


Michiel A. P. Pertijs (S’99–M’06–SM’10) received the M.Sc. and Ph.D. degrees in electrical engineering (both cum laude) from Delft University of Technology, Delft, The Netherlands, in 2000 and 2005, respectively. From 2000 to 2005, he was a researcher with the Electronic Instrumentation Laboratory of Delft University of Technology, working on high-accuracy CMOS smart temperature sensors. From 2005 to 2008, he was with National Semiconductor, Delft, where he designed precision operational amplifiers and instrumentation amplifiers. From 2008 to 2009, he was a Senior Researcher at IMEC / Holst Centre, Eindhoven, The Netherlands. In 2009, he joined the Electronic Instrumentation Laboratory of Delft University of Technology as an Assistant Professor, working on sensor interface circuits and energy-efficient sensor systems. He has authored or co-authored one book, eight patents, and over 45 technical papers. His research interests include analog and mixed-signal electronics and smart sensors.

Dr. Pertijs is a member of the technical program committees of the International Solid-State Circuits Conference (ISSCC), the European Solid-State Circuits Conference (ESSCIRC), the IEEE Sensors Conference, and the IEEE PRIME Conference. He received the ISSCC 2005 Jack Kilby Award for Outstanding Student Paper, the IEEE Journal of Solid-State Circuits 2005 Best Paper Award, and the 2006 Simon Stevin Gezel Award from the Dutch Technology Foundation STW.

Kofi A. A. Makinwa (M’97–SM’05–F’11) received the B.Sc. and M.Sc. degrees from Obafemi Awolowo University, Nigeria in
1985 and 1988 respectively. In 1989, he received the M.E.E. degree from the Philips International Institute, The Netherlands and in 2004, the Ph.D. degree from Delft University of Technology, The Netherlands.

From 1989 to 1999, he was a Research Scientist with Philips Research Laboratories, Eindhoven, The Netherlands, where he worked on interactive displays and on front-ends for optical and magnetic recording systems. In 1999, he joined Delft University of Technology, where he is now an Antoni van Leeuwenhoek Professor in the Faculty of Electrical Engineering, Computer Science and Mathematics. His main research interests are in the design of precision analog circuitry, sigma-delta modulators, smart sensors and sensor interfaces. This has resulted in 3 books, 16 patents and over 150 technical papers.

Kofi Makinwa is on the program committees of the European Solid-State Circuits Conference (ESSCIRC) and the Advances in Analog Circuit Design (AACD) workshop. He has also served on the program committee of the International Solid-State Circuits Conference (ISSCC), as a guest editor of the Journal of Solid-State Circuits (JSSC) and as a distinguished lecturer of the IEEE Solid-State Circuits Society (2008 to 2011). He is a co-recipient of several best paper awards; from the JSSC, ISSCC, Transducers and ESSCIRC, among others. In 2005, he received a Veni Award from the Netherlands Organization for Scientific Research and the Simon Stevin Gezel Award from the Dutch Technology Foundation. He is an alumnus of the Young Academy of the Royal Netherlands Academy of Arts and Sciences and an elected member of the IEEE Solid-State Circuits Society AdCom, the society’s governing board.

Johan H. Huijsing was born on May 21, 1938. He received the M.Sc. degree in EE from the Delft University of Technology, the Netherlands in 1969, and the Ph.D. degree from this University in 1981.

He has been an assistant and associate professor in Electronic Instrumentation at the Faculty of EE of the Delft University of Technology since 1969. He became a full professor in the chair of Electronic Instrumentation since 1990, and professor-emeritus since 2003. From 1982 through 1983 he was a senior scientist at Philips Research Labs, in Sunnyvale, California, USA. From 1983 until 2005 he was a consultant for Philips Semiconductors, Sunnyvale, California, USA, and since 1998 also a consultant for Maxim, Sunnyvale, California, USA.

The research work of Johan Huijsing is focused on operational amplifiers, analog-to-digital converters and integrated smart sensors. He has supervised 30 PhD students. He is author or co-author of more than 300 scientific papers, 40 US patents and 15 books.

In 1992 he initiated the international Workshop on Advances in Analog Circuit Design. He co-organized it yearly until 2003. He has been a member of the program committee of the European Solid-State Circuits Conference from 1992 until 2002. He was chairman of the Dutch STW Platform on Sensor Technology and of the biannual national Workshop on Sensor Technology from 1991 until 2002. He is Fellow of IEEE, and was awarded the title of Simon Stevin Meester by the Dutch Technology Foundation.

Gerard C.M. Meijer received his M.Sc. and Ph.D. degrees in Electrical Engineering from the Delft University of Technology, Delft, The Netherlands, in 1972 and 1982, respectively.

Since 1972 he has been a member of the Research and teaching staff of Delft University of Technology, where he is a professor, engaged in research and teaching on Analogue Electronics and Electronic Instrumentation. Since 1984, he has been consultant for industrial companies and research institutes. In 1996 he co-founded the company SensArt, where he is consultant in the field of sensor systems. In 1999 the Dutch Technology Foundation STW awarded him with the honorary degree “Simon StevinMeester” and in 2001 he was awarded the Anthony van Leeuwenhoek chair at TU Delft.

In addition to many journal and conference papers, Meijer is also author and editor of books in the field of sensor systems, published by IOP, Kluwer, Springer and Wiley.
### TABLE II

**Performance Summary and Comparison.** Accuracy FOM (energy × error × %²) line calculated mostly with data from [18].

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Non-trimmed inaccuracy</td>
<td>±0.25°C</td>
<td>±0.5°C</td>
<td>±0.5°C</td>
<td>±1°C max</td>
</tr>
<tr>
<td>(±3σ, batch calibrated)</td>
<td>−70°C to 130°C</td>
<td>−55°C to 125°C</td>
<td>−30°C to 125°C</td>
<td>−40°C to 125°C</td>
</tr>
<tr>
<td>Trimmed inaccuracy</td>
<td>±0.1°C</td>
<td>±0.1°C</td>
<td>±0.2°C</td>
<td></td>
</tr>
<tr>
<td>(±3σ, single trim at 30°C)</td>
<td>−55°C to 125°C</td>
<td>−55°C to 125°C</td>
<td>−30°C to 125°C</td>
<td></td>
</tr>
<tr>
<td>Resolution</td>
<td>0.025°C</td>
<td>0.01°C</td>
<td>0.015°C</td>
<td>0.0625°C</td>
</tr>
<tr>
<td></td>
<td>10 conv./s</td>
<td>10 conv./s</td>
<td>10 conv./s</td>
<td>3.3 conv./s</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>2.5V to 5.5V</td>
<td>2.5V to 5.5V</td>
<td>1.6V to 2V</td>
<td>2.7V to 5.5V</td>
</tr>
<tr>
<td>Supply sensitivity (at 30°C)</td>
<td>0.05°C/ÇV</td>
<td>0.03°C/ÇV</td>
<td>0.1°C/ÇV</td>
<td>–</td>
</tr>
<tr>
<td>Front-end current</td>
<td>5µA</td>
<td>37µA</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Supply current (cont. operation)</td>
<td>25µA</td>
<td>75µA</td>
<td>4.6µA</td>
<td>50µA</td>
</tr>
<tr>
<td>Accuracy FOM (nJ%²)</td>
<td>76</td>
<td>231</td>
<td>49</td>
<td>44k</td>
</tr>
<tr>
<td>Technology</td>
<td>0.7 µm, CMOS</td>
<td>0.7 µm, CMOS</td>
<td>0.16 µm, CMOS</td>
<td>–</td>
</tr>
<tr>
<td>Chip area</td>
<td>4.5mm²</td>
<td>4.3mm²</td>
<td>0.12mm²</td>
<td>–</td>
</tr>
<tr>
<td># of measured samples</td>
<td>20</td>
<td>24 samples,</td>
<td>19</td>
<td>–</td>
</tr>
<tr>
<td># of trimming points</td>
<td>1-point trim</td>
<td>1-point trim</td>
<td>1-point trim</td>
<td>–</td>
</tr>
</tbody>
</table>