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A 0.25 mm$^2$-Resistor-Based Temperature Sensor With an Inaccuracy of 0.12 °C (3σ) From −55 °C to 125 °C

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Abstract—This paper describes a compact, energy efficient, resistor-based temperature sensor that can operate over a wide temperature range (−55 °C–125 °C). The sensor is based on a Wheatstone bridge (WhB) made from silicided poly-silicon and non-silicided poly-silicon resistors. To achieve both area and energy efficiencies, the current output of the WhB is digitized by a continuous-time zoom analog-to-digital converter (ADC). Implemented in a standard 180-nm CMOS technology, the sensor consumes 52 μA from a 1.8-V supply and achieves a resolution of 280 μK rms in a 5-ms conversion time. This corresponds to a state-of-the-art resolution figure-of-merit (FoM) of 40 fJ · K$^2$. After a first-order fit, the sensor achieves an inaccuracy of ±0.12 °C (3σ) from −55 °C to 125 °C.

Index Terms—Continuous-time delta–sigma modulator (CTΔΣM), energy efficiency, non-linearity correction, smart sensors, temperature sensor.

I. INTRODUCTION

TO STABILIZE their outputs over temperature, frequency references based on MEMS or XTAL resonators usually employ temperature compensation schemes [1]–[6]. In order not to degrade the reference’s jitter performance, such schemes require high-resolution temperature sensors [1]. These should also be highly energy efficient, so as not to impact the reference’s overall energy consumption, and be as compact as possible.

Temperature sensors based on dual-MEMS resonators have demonstrated superb stability, resolution, and energy efficiency [1]. However, their fabrication in a non-CMOS process results in the increased complexity and cost. In standard CMOS technologies, temperature sensors based on bipolar junction transistors (BJTs) [7]–[9], MOSFETs [10], [11], resistors [2]–[6], [12]–[15], and even electrothermal filters [16], [17] can be made. In terms of their resolution figure-of-merit (FoM) [18], however, the energy efficiency of resistor-based sensors is currently about two orders of magnitude less than that of other types of CMOS temperature sensors [19]. They can also achieve high (sub-mK) resolution and areas as low as 0.1 mm$^2$ [14], [15].

Depending on their choice of reference, two classes of resistor-based temperature sensors can be identified: RC-based sensors [2]–[4], [6], [14], which use a frequency reference to digitize a temperature-dependent RC time constant; and dual-resistor-based sensors [5], [12], [15], which digitize the resistance of a sensing resistor with respect to another resistor. As discussed in [20], RC-based sensors can achieve better stability and accuracy, because on-chip MIM capacitors are more stable and spread less than on-chip resistors. However, they require the availability of an equally accurate and stable (external) frequency reference. On the other hand, dual-resistor-based sensors can be used in a standalone manner and can be more energy efficient, as their sensitivity can be boosted by using resistors with complementary temperature coefficients (TCs.) In both cases, good accuracy (about 0.1 °C over the industrial temperature range) can be achieved after a two-point calibration [6], [12]. This paper will focus on the design of an area-efficient temperature sensor that employs silicided and non-silicided poly resistors in a Wheatstone bridge (WhB) configuration.

According to a recent survey [21], bridge-to-digital converters (BDCs) based on the combination of an instrumentation amplifier and an analog-to-digital converter (ADC) [22], [23] can achieve excellent energy efficiency, resolution, and accuracy. However, they occupy the significant area (>0.7 mm$^2$). Voltage-controlled oscillator (VCO)-based BDCs [24] can be very compact (0.06 mm$^2$ in 40-nm CMOS), at the expense of energy efficiency. A compact BDC based on a hybrid flash/SAR ADC occupies only 0.044 mm$^2$ in 65-nm CMOS [15]. However, this was achieved at the expense of resolution (0.12 °C rms).

Rather than reading out its open-circuit voltage, an alternative way of reading out a bridge is to measure its short-circuit output current. Current-readout BDCs based on continuous-time delta–sigma modulators (CTΔΣMs) are quite energy efficient, achieving resolution FoMs of 650 [5] and 49 fJ · K$^2$ [12], respectively. However, the latter occupies the significant area: 0.72 mm$^2$ in a 180-nm technology, mainly due to the area of the CTΔΣM’s integrating capacitors.

In this paper, a multi-bit CTΔΣM is proposed to replace the single-bit CTΔΣM used in [12]. Its multi-bit digital-to-analog converter (DAC) compensates the output current of the bridge more accurately, thus reducing the swing at the input of the modulator’s loop filter. As a result, both the size of the required integration capacitors as well as the ADC’s power dissipation can be significantly reduced.

The rest of this paper is organized as follows. Section II discusses the design of a zoom ADC based on a multi-
Measurement results and a comparison with the state-of-the-art are given in Section IV, and finally, conclusions are drawn.

\[ \text{WhB and in the DAC can be modeled as follows [5]:} \]

**II. ARCHITECTURE DESIGN**

**A. Wheatstone Bridge Readout and CTΔΣM**

As shown in Fig. 1, the sensor consists of a WhB made from two types of resistors with positive and negative TCs: \( R_p(T) \) and \( R_n(T) \). For high sensitivity and stability, \( R_p \) and \( R_n \) are silicided-p-poly and non-silicidned n-poly resistors, respectively [12]. A parallel resistor DAC (also made from \( R_n \)-type resistors) can then be used to cancel the bridge’s temperature-dependent output current \( I_{\text{err}}(T) \). As shown in Fig. 2, the DAC forms part of a CTΔΣM, which drives the average value of \( I_{\text{err}}(T) \) to zero by switching the DAC’s resistors either to \( V_{DD} \) or GND and thus effectively balancing the bridge [5].

The temperature dependence of the various resistors in the WhB and in the DAC can be modeled as follows [5]:

\[
\begin{align*}
R_p(T) &= R_p(T_0) \cdot (1 + T C_{p1} \cdot \Delta T + T C_{p2} \cdot \Delta T^2) \\
R_n(T) &= R_n(T_0) \cdot (1 + T C_{n1} \cdot \Delta T + T C_{n2} \cdot \Delta T^2) \\
R_{DAC}(T) &= R_{DAC}(T_0) \cdot (1 + T C_{n1} \cdot \Delta T + T C_{n2} \cdot \Delta T^2).
\end{align*}
\]

Here, \( R_p(T_0), R_n(T_0), \) and \( R_{DAC}(T_0) \) are the resistances at a reference temperature \( T_0 \), while \( T C_{p1} \) and \( T C_{n1} \) are their first-order TCs, \( T C_{p2} \) and \( T C_{n2} \) are their second-order TCs, and \( \Delta T \) is the temperature with respect to \( T_0 \). Noting that the active integrator virtually shorts the bridge’s output terminals to \( V_{DD}/2 \) while the modulator ensures that the integrator’s average input current \( I_{\text{err}} \) is 0, the bitstream average \( \mu_{\text{ADC}} \) can be expressed as

\[
\mu_{\text{ADC}} = \frac{I_{\text{sig}}(T)}{I_{\text{DAC}}(T)} = \frac{1/R_p(T) - 1/R_n(T)}{1/R_{DAC}(T)}
\]

\[
= \frac{R_{DAC}(T_0) \cdot (1 + T C_{n1} \cdot \Delta T + T C_{n2} \cdot \Delta T^2)}{R_p(T_0) \cdot (1 + T C_{p1} \cdot \Delta T + T C_{p2} \cdot \Delta T^2)}
\]

\[
= \frac{R_{DAC}(T_0) \cdot f_{\text{pa}}(\Delta T)}{R_p(T_0) \cdot f_{\text{pa}}(\Delta T) - R_{DAC}(T_0)}.
\]

Within a batch, the function \( f_{\text{pa}} \) only depends on the resistors’ TCs and so will be a constant but non-linear function of temperature. The ratio \( R_{DAC}/R_p \) involves different types of resistors and so will spread significantly, while the ratio \( R_{DAC}/R_n \) involves the same type of resistors and so should spread less. As such, (2) implies that a two-point trim will be needed to fully compensate for the effects of spread.

**B. Temperature Sensing Resolution**

With a sinc1 filter, the temperature sensing resolution of a balanced WhB can be expressed as [20]

\[
\Delta T_{\text{WhB}} = \frac{2}{V_{DD} \cdot (T C_{p1} - T C_{n1})} \cdot \sqrt{\frac{2kTR_{\text{conv}}}{t_{\text{conv}}}}
\]

where \( R = R_p = R_n \) is the bridge resistance and \( t_{\text{conv}} \) is the conversion time.

Since \( R_{DAC} \) is switched between \( V_{DD} \) and GND, it can be modeled by two resistors, \( R_{DAC1} \) and \( R_{DAC2} \) as shown in Fig. 3. In order to balance the bridge, their resistances must satisfy

\[
R_{DAC} = R_{DAC1}/R_{DAC2}
\]

\[
R_p/R_{DAC1} = R_{DAC}/R_{DAC2} = R_n/R_{DAC2}.
\]

From (4), \( R_{DAC1} \) can be expressed as

\[
R_{DAC1} = \frac{2}{1/R_n - 1/R_p + 1/R_{DAC}}
\]

and the first-order TC of \( R_{DAC2} \) can be calculated as

\[
T C_{p1,\text{new}} = \frac{T C_{p1}}{1 + R_p^2 / R_{DAC1}^2} + \frac{T C_{p1}}{1 + R_{DAC1}^2 / R_p^2}
\]

which is always less than \( T C_{p1} \). The TC of \( R_{n,\text{new}} \) is not affected since it consists of two resistors of the same type. Thus, (2) can be updated as

\[
\Delta T_{\text{WhB}} = \frac{2}{V_{DD} \cdot (T C_{p1,\text{new}} - T C_{n1})} \cdot \sqrt{\frac{2kTR_{\text{new}}}{t_{\text{conv}}}}
\]
where $R_{\text{new}} = R_{p,\text{new}} = R_{n,\text{new}}$. Therefore, the presence of the resistive DAC (RDAC) decreases the bridge’s sensitivity and thus its temperature sensing resolution.

C. From Single-Bit CTΔΣM to Multi-Bit CTΔΣM

The first stage of the CTΔΣM is basically an active-RC integrator, as shown in Fig. 4(a), where the WhB is modeled by a source resistor driven by a temperature-dependent voltage $V_{in}(T)$. In [12], the sensor’s energy efficiency and chip area were limited by the large variation in $I_{\text{sig}}$ over process, voltage, and temperature (PVT). This had to be compensated by the output current $I_{DAC}$ of a 1-bit DAC, resulting in an even larger error current $I_{\text{err}}$ flowing into the first integrator, as shown in Fig. 4(b). In consequence, the first integrator dissipated about half of the sensor’s power, while its integration capacitors occupied 60% of the sensor’s area.

A multi-bit resistor DAC ($N > 1$) can be used to reduce the magnitude of $I_{\text{err}}$ [Fig. 4(c)]. Since most of $I_{\text{sig}}$ will then be compensated by $I_{DAC}$, the first integrator’s supply current, as well as the size of its integration capacitors, can be significantly reduced.

D. Integrator Nonlinearity and Noise in Multi-Bit CTΔΣMs

Nonlinearity is a key challenge in multi-bit ΔΣMs. For CTΔΣ Ms with RDACs, the two major contributors are RDAC mismatch and the non-linearity of the first integrator. RDAC mismatch can be sufficiently suppressed by careful layout and dynamic element matching (DEM). The non-linearity of the first integrator, however, is more problematic.

In multi-bit CTΔΣMs, integrator nonlinearity increases in-band noise (IBN) [25], which, in our case, will degrade the sensor’s resolution. This can be understood intuitively by considering Fig. 5(a), in which the nonlinearity of the first integrator is modeled by $f_s(x)$. This can then be shifted to the input of the modulator and to the output of the DAC, as shown in Fig. 5(b). The resulting non-linear DAC will then cause quantization noise folding and raise IBN. Being signal dependent, it cannot be mitigated by DEM. Increasing the linearity of the first stage would help, but this usually comes at the expense of higher power dissipation.

E. Zoom CTΔΣM

During the fine conversion of a zoom ΔΣM, however, only two levels of its multi-bit DAC will be used [8], [26]. As a result, the DAC will still appear to be perfectly linear even in the presence of integrator non-linearity, and so, no quantization noise folding will occur [27].

The proposed zoom CTΔΣM digitizes the temperature-dependent ratio $X = I_{\text{sig}}/(2I_{DAC})$ in two steps, as illustrated in Fig. 6, for the case of a first-order modulator. First, a coarse SAR conversion determines the integer part $n$ of $X$. Then, the fractional part $\mu$ is determined by a fine $\Delta E$ conversion. Compared to the complexity of conventional multi-bit ΔΣMs, a zoom ADC only requires a single-bit comparator, a reset switch for the first integrator and some logic.
During the coarse conversion, the first integrator is used as a pre-amplifier for the comparator [8]. Each step of the SAR conversion then consists of choosing a DAC code, resetting the first integrator and then integrating the resulting error current for one clock cycle. The polarity of the result is detected by the comparator and used to determine the next DAC code to test. To absorb small errors from the SAR conversion and ensure that \( \mu \) lies in the modulator’s stable input range, over-ranging is used. This is implemented by switching the DAC between the codes \( n - 1 \) and \( n + 1 \) during the delta–sigma phase [Fig. 6(b)]. Since this range is significantly smaller than the full range of the DAC, the linearity and power dissipation of the first integrator can be significantly relaxed.

III. CIRCUIT IMPLEMENTATION

A. Wheatstone Bridge and RDAC

In contrast to previous WhB sensors [5], [12], [15], this sensor is designed to operate over the military temperature range (\(-55 \, ^\circ\text{C}–125 \, ^\circ\text{C}\)). As a result, the bridge is unbalanced at room temperature (RT, about 25 \(^\circ\text{C}\)), with \( R_p = 100 \, \text{k}\Omega \) and \( R_b = 80 \, \text{k}\Omega \). With a 1.8-V supply, this results in \( |I_{\text{sig}}| < 7 \, \mu\text{A} \) over PVT, which requires a minimum DAC resistance of 120 k\( \Omega \). Given \( t_{\text{conv}} = 5 \, \text{ms} \), \( T_{\text{CP1}} = 0.29\%/\text{C}, \) \( T_{\text{CN1}} = 0.15\%/\text{C}, \) and \( V_{\text{DD}} = 1.8 \, \text{V} \), then from (5)–(7) \( \Delta T_{\text{WhB}} \) is 125 \( \mu\text{K} \) (rms) at RT.

Since the minimum width of the process is fixed, there is a tradeoff between the number of DAC bits and the minimum possible DAC area. To ensure that the areas of the DAC and the integrating caps \( C_{\text{int}} \) are roughly equal, a 3-bit DAC was chosen, with unit elements of 960 k\( \Omega \). As in [8], an extra half-LSB unit element is used at the end of the coarse conversion to determine the optimal choice of the references used in the fine conversion [8].

B. Zoom-Based CT\( \Delta \Sigma \)M

Fig. 7 shows the circuit diagram of the zoom CT\( \Delta \Sigma \)M. To achieve high resolution in a reasonable conversion time, a second-order modulator was chosen with a feed-forward architecture to reduce the swing at the output of the first integrator, and thus further reduce the size of \( C_{\text{int}} \). As in [6], the loop is stabilized by a zero realized by the inclusion of \( R_{\text{ff}} \) in the feedback path of the second integrator.

Since its non-linearity will not increase IBN, the first integrator was optimized mainly for noise. It consists of an energy-efficient current-reuse operational transconductance amplifier (OTA) rather than the two-stage opamp used in [12]. High-V\( \text{t} \) input transistors are used to achieve a reasonable output swing (~0.9 V at RT) [9], as shown in Fig. 8(a).

To improve the modulator’s stability, the pole of the OTA-based integrator is compensated by inserter \( R_{\text{com}} = 1/g_{\text{in}} \) in series with \( C_{\text{int}} \). To suppress its offset and \( 1/f \) noise while avoiding quantization-noise fold back, the OTA is choppered at the CT\( \Delta \Sigma \)M’s sampling frequency (\( f_s = 500 \, \text{kHz} \)) [28]. It achieves over 80-dB gain, a gain-bandwidth product (GBW) product of ~20 MHz and consumes 22 \( \mu\text{W} \) at RT, which is about 60\% of the power dissipated by the bridge.

As shown in Fig. 8(b), the second stage is based on a source-degenerated cascaded telescopic OTA. It has a dc gain of 80 \( \text{dB} \) and dissipates 3 \( \mu\text{W} \) at RT.

For flexibility, the SAR and data weighted averaging (DWA) logic are implemented off-chip. Since the SAR conversion only involves 3 bits, its duration and power overhead are negligible, and the energy efficiency of the bridge readout is basically defined by the fine conversion. Simulations show that if implemented on-chip, the SAR and DWA logic would consume less than 1 \( \mu\text{W} \) and less than 0.01 mm\(^2\) area which are negligible compared to the other circuit blocks.

From simulations, the first-stage OTA’s contribution to the modulator’s total input-referred noise power is ~30\% of that of the WhB/DAC resistors. To decimate the bit-stream output of the second-order modulator, a sinc\(^2\) filter is adopted, whose effective noise bandwidth is 1.33 times that of the sinc filter assumed in earlier calculations. These two factors will reduce the sensor’s resolution to about 165 \( \mu\text{K} \) (rms) with \( t_{\text{conv}} = 5 \, \text{ms} \).

C. NonLinearity Analysis

Although the nonlinearity of the first integrator does not impact the IBN of a zoom ADC, it does impact its integral nonlinearity (INL). The main source of non-linearity is the signal dependent \( g_m \) of the current-reuse OTA, which can be modeled by the addition of a third-order term \( g_{\text{m3}} \) [Fig. 9(a)]. The simulated non-linearity in \( I_{\text{err}} \) is then as shown in Fig. 9(b).

The OTA’s non-linearity will cause errors in the bitstream average \( \mu \) obtained after the fine conversion. These will be a
weighted average of the associated errors in the two possible values of the first integrator’s input current \( I_{\text{err}} \). When \( \mu = 0 \), however, the bitstream output \( bs \) will toggle between +1 and −1 with equal probability, and since \( I_{\text{err}}(bs = +1) = -I_{\text{err}}(bs = -1) \), the resulting error in \( \mu \) will be 0. This will also be the case at the extremes of the modulator’s input range, because the bridge’s output current \( I_{\text{sig}} \) will then be exactly cancelled by \( I_{\text{DAC}} \), and so \( I_{\text{err}} = 0 \). Apart from these three cases, the error of the fine ADC will be non-zero. As shown in Fig. 10, the result is a sinusoidal error curve centered on \( \mu = 0 \).

Choosing the range of the fine conversion to be exactly equal to two steps of the coarse conversion (two LSB over-ranging) means that there are two different ways to convert a given input current, each corresponding to a different coarse code \( n \). Ideally, the zoom ADC’s output \( X \) would be the same in both cases. In the presence of OTA non-linearity, however, there will be an error in \( \mu \), which will be of opposite polarity in the two cases. As shown in Fig. 11, this means that at the coarse code transitions, i.e., when \( \mu = \pm 0.5 \), the error in \( X \) will abruptly change polarity. Simulations show that the jumps in \( X \) at RT can be as large as 0.1 °C, which is significantly larger than the sensor’s expected resolution.

### D. Segment Averaging

Noting that the errors associated with the two possible \( n/\mu \) combinations are of opposite polarity, they can be mitigated by simply averaging the values of \( X \) obtained from two such conversions, as shown in Fig. 12(a). Simulations show that this approach can reduce the error by about 8\( \times \), to about \( \pm 5 \) mK. This approach translates to considerable power savings since without this segment averaging technique, the bias current of the first integrator’s OTA would have to be increased by about 2\( \times \) to obtain similar linearity.

Although the stable input range of a second-order \( \Delta \Sigma \)M corresponds to \(-1 < \mu < 1\) for dc input signals [29], its quantization noise becomes quite large when \( |\mu| \sim 1 \). To avoid degrading the sensor’s resolution in such cases, segment averaging is disabled when \( 1 - |\mu| < 0.05 \). As shown in Fig. 12(b), this will have little effect on the sensor’s linearity, since the nonlinearity is anyway quite small in these cases, and the transitions are blurred by the presence of thermal noise. The associated timing diagram is shown in Fig. 13.
IV. MEASUREMENT RESULTS

The sensor is realized in a standard 180-nm CMOS process, with a dimension of $615 \, \mu m \times 410 \, \mu m$ (Fig. 14). At RT, it draws $52 \, \mu A$ from a 1.8-V supply, with over half of this dissipated in the WhB and the DAC. About 15% of the active area is occupied by the WhB, 30% by the DAC resistors, and another 30% by the integration capacitors of the first stage. For supply voltages varying from 1.6 to 2.0 V, the sensor’s supply sensitivity is $0.02 ^\circ C/V$. An off-chip sinc² filter is used to decimate the sensor’s bitstream output.

A. Temperature Characteristic, NonLinearity Correction, and Calibration

Using a temperature-controlled oven (Vötsch VT7004), 19 chips from the same batch were characterized from $-55 ^\circ C$ to $125 ^\circ C$ (in 10 °C steps) in ceramic dual inline (DIL) packages. The reference sensor was a calibrated Pt-100 RTD. To minimize the effects of oven drift, both the Pt-100 and the chips were placed inside a cavity in a large block of aluminum.

Fig. 15 shows the sensors’ output versus temperature. Due to the spread in $R_p$ and $R_n$, its sensitivity is about 16% less than that in the typical–typical (TT) corner, which in turns results in less resolution: $\sim 200 \, \mu K$ (rms) with $t_{conv} = 5$ ms. Over temperature, the output of the zoom ADC varies from about 0–3.2 over temperature, which is still within its designed full-scale range of $-4–4$. Without any calibration, the sensor has a spread of about 15 °C.

An individual first-order fit is applied to remove the process spread, i.e., the spread of $R_{DAC}(T_0)/R_p(T_0)$ and $R_{DAC}(T_0)/R_n(T_0)$ in (2). The residual error is then determined by the term $f_{pm}(T - T_0)$ in (2), which turns out to be quite systematic (Fig. 16). Despite the reduction of bridge sensitivity due to the process spread, the residual error agrees well with simulations made in the TT corner (maximum error $< 0.3 ^\circ C$). As in [4], [6], and [12], this error can then be removed by a fixed polynomial.

Without segment averaging, the $3\sigma$ inaccuracy is 0.2 °C after the systematic nonlinearity is removed by a fixed fifth-order polynomial [Fig. 17(a)]. As discussed in Section III-C, the jumps around $-35 ^\circ C$, $5 ^\circ C$, and $55 ^\circ C$ (when the fine code $\mu = \pm 0.5$) are caused by the non-linearity of the first stage. With segment averaging enabled (Threshold $= 0.05$), the inaccuracy can be reduced to 0.12 °C ($3\sigma$) within the military temperature range [Fig. 17(b)]. The 1.6× improvement in accuracy is less than the $8\times$ factor shown in Fig. 12, indicating that the majority of the error is due to the spread of the sensing resistors rather than to the nonlinearity of the ADC.

A simple offset trim results in an inaccuracy of 6.7 °C ($3\sigma$). By exploiting the correlation between the zero and first-order
coefficients of the individual first-order fit [6], this can be reduced to 1 °C, as shown in Fig. 18. Compared to the 0.2 °C inaccuracy achieved in an RC-based sensor [6], the extra inaccuracy of this design is probably due to the fact that the non-silicided n-poly resistors in the WhB spread more than the MIM capacitors of an RC filter.

B. Resolution and FoM

With different DEM algorithms, the power spectral densities of the sensor’s output bitstream are shown in Fig. 19. Compared to barrel-shifting DEM, DWA is more complex, but it preserves the sensor’s noise floor. Applying segment averaging of 2.5-ms/segment results in tones at multiples of 200 Hz but not a raised noise floor. For a fixed conversions time of 5 ms (Nyquist frequency of 100 Hz), the tones will be located at the notches of the sinc² decimation filter, and thus have no effect on the sensor’s resolution. The 1/f noise corner is at about 20 Hz, which is mainly due to the non-silicided poly resistor [6].

The sensor’s noise can be converted to temperature via the RT sensitivity obtained in Section IV-B. With a 5-ms decimation filter, the sensor’s output is shown in Fig. 20(a) over a 20-s period. A significant temperature drift can be seen (~3μm °C), which is mainly due to the temperature fluctuations in the oven.

In order to accurately estimate the sensor’s resolution, this drift must be suppressed. One way of doing this is to take the difference between successive samples of the sensor’s decimated output, and then compute a two-sample Allan deviation [6]. However, the differencing operation will also suppress the sensor’s non-negligible 1/f noise (Fig. 19).

To avoid this, the standard deviation can be computed over a shorter interval (1 s), during which the temperature drift (~140 μK, or ~40 μK rms) will be negligible compared to the sensor’s noise. The 20 s of data were divided into 20 intervals of 1 s, and the average standard deviation obtained from the 20 intervals.

As shown in Fig. 21, in a 20-s interval, the standard deviation is indeed limited by drift. Computing the two-sample Allan deviation [13] suppresses this drift and results in an estimated resolution of 260 μK rms with $T_{\text{conv}} = 5$ ms. Computing the standard deviation over a 1-s interval results in a more realistic estimate of 290 μK rms, which corresponds to a 40-fJ · K² resolution FoM. Compared to the 200 μK rms predicted in Section IV-A, the reduced resolution is mainly due to the sensor’s 1/f noise.

C. Comparison to Previous Work

The performance of the sensor is summarized in Table I and compared to other high-resolution temperature sensors. It achieves a state-of-the-art resolution FoM of 40 fJ · K², which defines the state-of-the-art in CMOS temperature sensors, and is equal to that of the MEMS-based sensor in [1]. It also has a small active area of 0.25 mm², which is 3× smaller than [12] and is close to that of precision BJT-based sensors [9]. Packaged in ceramic, the sensor achieves a temperature sensing range from -55 °C to 125 °C, and an inaccuracy of ±0.12 °C (3σ) after a first-order fit followed by a systematic nonlinearity removal.
TABLE I

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<th>[12]</th>
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<th>[4]</th>
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<td>3σ Inaccuracy (°C)</td>
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<td>0.32</td>
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<td>0.06</td>
</tr>
<tr>
<td>Power (μW)</td>
<td>94</td>
<td>180</td>
<td>65</td>
<td>31</td>
<td>160</td>
<td>68</td>
<td>13000</td>
<td>7</td>
</tr>
<tr>
<td>Conversion time (ms)</td>
<td>5</td>
<td>10</td>
<td>0.1</td>
<td>32</td>
<td>5</td>
<td>1</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>Resolution (mK)</td>
<td>0.29</td>
<td>0.16</td>
<td>10</td>
<td>2.8</td>
<td>0.41</td>
<td>2.8</td>
<td>0.02</td>
<td>15</td>
</tr>
<tr>
<td>Resolution FoM (fJ·K²)</td>
<td>40</td>
<td>49</td>
<td>650</td>
<td>8000</td>
<td>130</td>
<td>530</td>
<td>40</td>
<td>7300</td>
</tr>
</tbody>
</table>

ᵃ 1st order fit. ᵇ 1-point trim with 1st order fit. ⁴ min-max. ⁵ Energy / Conversion × Resolution².

V. CONCLUSION

A compact, energy-efficient, resistor-based temperature sensor for the temperature compensation of MEMS/XTAL oscillators has been implemented in a standard 180-nm CMOS technology. It is based on a WhB made from silicided poly-silicon and non-silicided poly-silicon thermistors, whose output current is digitized by a continuous-time zoom ADC. Compared to a 1-bit predecessor, the sensor achieves 3× smaller area as well as higher energy efficiency. The non-linearity of the zoom ADC is significantly mitigated by a segment averaging technique. These results demonstrate that zoom ADCs are suitable for reading WhB sensors with high energy efficiency and small chip area.

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