A ±4-A High-Side Current Sensor With 0.9% Gain Error From −40 °C to 85 °C Using an Analog Temperature Compensation Technique

Xu, Long; Huijsing, Johan H; Makinwa, Kofi

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Abstract—This paper presents a fully integrated shunt-based current sensor that supports a 25-V input common-mode range while operating from a single 1.5-V supply. It uses a high-voltage beyond-the-rails ADC to directly digitize the voltage across an on-chip shunt resistor. To compensate for the shunt’s large temperature coefficient of resistance (ΔR/ΔT = 0.335%/°C), the ADC employs a proportional-to-absolute-temperature voltage reference. This analog compensation scheme obviates the need for the explicit temperature sensor and calibration logic required by digital compensation schemes. The sensor achieves 1.5-μA rms noise over a 2-ms conversion time while drawing only 10.9 μA from a 1.5-V supply. Over a ±4-A range, and after a one-point trim, the sensor exhibits a 0.9% (maximum) gain error from −40 °C to 85 °C and a 0.05% gain error at room temperature.

Index Terms—Beyond-the-rails, current sensing, high-side, high-voltage (HV) interface circuit, metal shunt resistor, proportional-to-absolute-temperature (PTAT) voltage reference, temperature compensation, temperature sensor, ΔΣ ADC.

I. INTRODUCTION

Accurate current sensing is critical in many applications including battery management, motor control, and over-current protection. Several types of current sensors exist: inductive sensors (e.g., Rogowski coils), magnetic field sensors (based on the Hall effect or fluxgates) [1]–[3] and shunt-resistor-based sensors [4], [5]. Inductive and magnetic sensors enable non-contact current measurements and are well suited to high-voltage (HV) applications (>100 V). However, inductive sensors can only sense ac current, and both types of sensors have a relatively complex and expensive. By comparison, shunt-resistor-based sensors are simple and low-cost and are widely used. As shown in Fig. 1, current can be sensed by either placing a small shunt resistor between the load and ground or between the battery and the load. The former configuration is referred to low-side current sensing, while the latter is referred to high-side current sensing.

Fig. 1. Low-side current sensing (left) and high-side current sensing (right).

High-side current sensing has two major advantages over low-side current sensing: it can detect high load current caused by accidental shorts, and it does not increase the resistance in the ground path. However, it does require interface circuits that can handle input common-mode (CM) voltages up to the battery voltage, which can be several tens of volts.

To accommodate such large voltages, high-side current sensors will typically employ precision HV instrumentation amplifiers (IAs) [6], [7] to shift the small voltage drop across the shunt V_s down to a low-voltage (LV) domain for further processing. In [6], the IA employs a current-feedback topology. To handle large CM voltages, its input stage is powered from the HV domain, resulting in a significant power consumption. In [7], the IA employs a chopped capacitively coupled topology. Its input capacitors block the large CM voltage, achieving a ±30-V input CM range (ICMR) without a separate HV supply. However, in both cases, an extra LV ADC is required to provide a digital output. To further reduce the system complexity, an HV beyond-the-rails ADC is proposed in [8], which achieves a wide (±30 V) ICMR while operating from a single 5-V supply.

To build fully integrated current sensors, shunt resistors can be realized by using the metal layers of a CMOS process [4], [5], [9]. However, the resulting shunt will then have a large temperature coefficient of resistance (TCR) of 0.335%/°C, and so a temperature compensation scheme (TCS) is required to achieve good accuracy. In [4] and [5], a digital TCS is proposed that achieves state-of-the-art gain error (0.3%) over the industrial temperature range. However, it requires a temperature sensor whose output is used to perform a polynomial-based correction on
Fig. 2. Block diagram of the current sensor in [5].

Fig. 3. System-level architecture of the proposed current sensor.

Fig. 4. Cross section of metal shunt $R_S$ (top) and its chip photograph (bottom). (a) Cross-section of $R_S$, (b) Chip photo of $R_S$.

the ADC’s output via calibration logic (Fig. 2), which leads to increased complexity and power consumption.

In this paper, a fully integrated high-side current sensor [10] is presented that supports a 25-V ICMR while operating from a single 1.5-V supply. A beyond-the-rails ADC is used to directly digitize the shunt voltage, thus obviating the need for HV IAs. In addition, an analog TCS obviates the need for extra temperature sensor and calibration logic. As a result, the sensor is 10× more energy efficient than [5], while achieving a 0.9% (maximum) gain error from $-40^\circ C$ to $85^\circ C$ and a 0.05% gain error at room temperature.

The rest of this paper is organized as follows. Section II briefly introduces the system-level architecture of the sensor. Sections III and IV describe the detailed circuit implementation of the beyond-the-rails ADC and the reference generator, respectively. Experimental results are presented in Section V, and Section VI provides the conclusion.

II. System-Level Architecture

Fig. 3 shows the system-level architecture of the proposed current sensor. It consists of an on-chip metal shunt resistor, a beyond-the-rails ADC, and a proportional-to-absolute-

temperature (PTAT) reference voltage generator (RVG). The RVG generates a PTAT voltage $V_{PTAT}$ that substantially compensates for the TCR of $R_S$, which, serendipitously, is itself almost exactly PTAT.

A. Shunt Implementation

Fig. 4 shows the cross section of the shunt $R_S$. It consists of four metal layers M2–M5 connected in parallel and is similar to the ones described in [4] and [5]. The oxide separating the metal layers from the substrate provides galvanic isolation. To facilitate the TCS, temperature-sensing NPN transistors are located underneath the shunt to ensure good thermal coupling. This is further enhanced by using thermal vias to connect the dummy M1 layer around NPNs to the shunt.

As reported in [5], a metal shunt exhibits about 0.1% drift during a long-term (24 days) measurement at high current levels ($\pm 5$ A) and high ambient temperature ($85^\circ C$). This is caused by electromigration and can be mitigated by reducing the current density [11], [12]. Hence, the metal shunt in this design ($880 \mu m \times 450 \mu m$) is 20% wider than the one in [4] for the same resistance (10 m$\Omega$). In addition, the total sensor system was designed for a maximum sensing current of 4 A, which represents a further 20% reduction in current density compared to the 5-A sensor reported in [4]. To minimize the parasitic resistance between the shunt and the outside world, each side of the metal shunt is directly connected to the test PCB via 18 short (<1 mm) bond wires. (Each bonding wire has a parasitic resistance of roughly 300 m$\Omega$.)

B. Analog Temperature Compensation Scheme

As shown in Fig. 3, instead of a bandgap voltage, a PTAT voltage $V_{PTAT} (= kV \times T_A)$ is employed as the ADC’s
reference. Since the metal shunt’s temperature dependence is almost perfectly PTAT ($R_S \approx k_R \times T_A$, $T_A$ is absolute temperature) over the industrial temperature range (Fig. 5), the shunt’s 1st-order temperature dependence is corrected at the ADC’s output $D_{out}$ in a ratiometric manner

$$D_{out} \approx \frac{I_S \times R_S}{V_{PTAT}} \approx \frac{I_S \times k_R \times T_A}{k_V \times T_A} \approx \frac{I_S \times k_R}{k_V}. \quad (1)$$

To verify the effectiveness of the analog TCS, $D_{out}$ is simulated over the industrial temperature range with a fixed (1 A) input current. As shown in Fig. 6, $D_{out}$ varies by nearly ±20% when a bandgap voltage is used as the reference. This drops to ±0.5% when a PTAT reference is used. The residual error is mainly due to the non-linear components of the shunt’s TCR.

To evaluate the effect of the thermal gradient between the shunt and the NPNs used to generate the PTAT reference, $D_{out}$ is also simulated for the case when there is a 4 °C difference between them. As shown in Fig. 7, the variation of $D_{out}$ over temperature still remains within ±0.5%. This shows that unlike [4] and [5], the proposed TCS makes the sensor relatively insensitive to on-chip thermal gradients.

### III. Circuit Implementation of the Beyond-the-Rails ADC

In this design, an HV beyond-the-rails ADC with wide ICMR [8] is utilized to directly digitize shunt voltage $V_S$ in the presence of large CM voltages (Fig. 3). It eliminates the need for an HV IA, and thus reduces the power consumption and chip area of the HV interface circuit.

#### A. ΔΣ ADC

Fig. 8 shows the schematic of the beyond-the-rails ADC. It consists of a 2nd-order single-bit switched-capacitor (SC) ΔΣ modulator that employs a feed-forward topology. Its bitstream $\mu I$ is decimated by a $sinc^2$ filter to generate the digital output $D_{out}$. For flexibility, the decimation filter is implemented off-chip. Since the ADC’s full-scale input range is only ±40 mV (±4 A×10 mΩ), the swing in the loop filter is quite small and so its integrators can be realized with energy-efficient current-reuse amplifiers [13], as shown in Fig. 9.

Shunt voltage $V_S$ ($V_{ip} - V_{in}$) is sampled onto input capacitors $C_{S1}$ (2.5 pF) by an HV input chopper $C_{HV}$. In this way, the ADC’s active blocks are isolated from input CM voltages, and so can be powered from an LV supply. In a similar manner, a reference voltage $V_{PTAT}$ is sampled onto feedback capacitors $C_{S2}$ (2.5 pF) with the help of an LV chopper whose polarity is determined by the modulator’s bitstream. To obtain wide ICMR and good matching, HV fringe capacitors with a breakdown voltage of 70 V are employed to implement both $C_{S1}$ and $C_{S2}$.  

![Fig. 5. PTAT reference $V_{PTAT}$ and resistance of $R_S$ over temperature.](image-url)  

![Fig. 6. Simulated $D_{out}$ variation over temperature when a bandgap reference (top) and a PTAT reference (bottom) are applied to the ADC.](image-url)  

![Fig. 7. Simulated $D_{out}$ variation over temperature with PTAT reference including 4 °C thermal difference.](image-url)  

![Fig. 8. Schematic of the beyond-the-rails ADC.](image-url)
To achieve low offset and 1/f noise, a correlated double sampling (CDS) scheme is implemented in the 1st stage with the help of switches $S_1$ and $S_2$. While most of the 1st integrator’s offset is cancelled by CDS, the charge injection mismatch of $S_1$ and $S_2$ will cause some residual offset. To reduce this, the entire ADC is chopped at low frequency (CHL) as shown in Fig. 10. The required polarity inversion is usually achieved by placing an extra pair of choppers around the ADC [4], [5], [8]; one ($CH_{SYS, IN}$) is at its analog input and the other ($CH_{SYS, OUT}$) at its bitstream output. Since the ADC already has an input chopper ($CH_{HV}$), the function of two choppers $CH_{SYS, IN}$ and $CH_{HV}$ can be emulated by swapping the clock signals $1_L$ and $2_L$ applied to $CH_{HV}$, as shown in Fig. 6. This chopping scheme does not cancel the residual offset due to the charge injection mismatch of $CH_{HV}$. However, with proper timing, this mismatched charge will flow into the low-impedance shunt, and so causes negligible offset.

B. HV Input Chopper

The HV input chopper $CH_{HV}$ [7], [8] is a key building block of the beyond-the-rails ADC since it must accurately sample $V_S$ even in the presence of large CM voltages. A simplified schematic of $CH_{HV}$ is shown in Fig. 11. It is driven by two non-overlapping clocks $\Phi_{1L}$ and $\Phi_{2L}$, which are generated by 1.5-V logic. They are capacitively coupled to the gates of four sampling switches $M_1$–$M_4$ via a level shifter composed of two HV capacitors $C_{1}$–$C_{2}$ and a latch $M_{5}$–$M_{6}$. Due to the cross-coupled sampling scheme, $M_1$–$M_4$ can share one set of coupling capacitors. Compared to the HV switch proposed in [14], this design is $3 \times$ smaller, occupying only 0.01 mm$^2$.

In [7], the reference node of the level shifter (the source terminals of $M_{5}$–$M_{6}$) is tied to one of the input terminals (e.g., $V_{ip}$) such that the coupled clock is always superimposed on $V_{ip}$. If $V_{ip}$ is higher than $V_{in}$, the gate–source voltages ($V_{GS}$) of $M_2$ and $M_4$ will still be slightly positive ($\approx V_{ip} - V_{in}$) when they are supposed to be OFF. This results in a certain leakage current, especially at high temperature. Moreover, the bodies of $M_1$–$M_4$ are tied to their sources, which in turn create parasitic diodes between $CH_{HV}$’s input and output terminals and also add extra leakage current.

As discussed in [4], the leakage current of the switches in $CH_{HV}$ can degrade the accuracy of bidirectional
current sensing. To prevent this, a minimum selector MS$_{1-2}$ is inserted between input terminals $V_{ip}$, $V_{in}$ to select the lowest input voltage. Its output (node A) is tied to the reference of the clock-level shifter such that the coupled clocks are always superimposed on $V_{min}$ (the lower of $V_{ip}$ and $V_{in}$). It ensures that $V_{GS}$ of M$_{1-4}$ will always be equal or less than 0 when they are OFF. In addition, the body of each switch is also connected to node A which prevents forward biasing of their parasitic diodes.

To reduce their leakage current, both the sampling switches M$_{1-4}$ and the latch M$_{5-6}$ are high-$V_{th}$ NMOS devices, while the minimum selector M$_{S1-2}$ is made from low-$V_{th}$ devices to extend its operational range. All of them are isolated by a semi-floating HV n-well (HVNW), which forms two back-to-back connected parasitic diodes D$_{P1}$ and D$_{P2}$ with the local p-well (LPW) and the P-substrate (PSUB), respectively (Fig. 12). The LPW is connected to one of the input terminals via the minimum selector. If the input CM voltage rises, D$_{P1}$ will ensure that the potential of the HVNW will follow. In this case, D$_{P2}$ will be reverse-biased and so its breakdown voltage determines the upper limit of the ADC’s ICMR. When the input CM voltage drops below ground, the HV PNP connected to the HVNW will turn on, and the potential of the HVNW will be clamped at $V_{dd}$ (1.5–2 V). This ensures that D$_{P2}$ is always reversed-biased to prevent potential latch-up. Meantime, D$_{P1}$ is reverse-biased and so its breakdown voltage sets the lower limit of ICMR. In the chosen technology, the breakdown voltages of D$_{P1}$ and D$_{P2}$ are 30 and 70 V, respectively. As such, the ADC has an ICMR from −30 to 70 V. In the actual implementation, however, the ADC’s ICMR is limited to 0–25 V by the ESD diodes at its input terminals.

Fig. 13 shows the schematic of CH$_{HV}$ with extra protection circuits. Four diodes D$_{1-4}$ are added in parallel with M$_{1-4}$ to limit their drain–source voltages when a large input CM transient presents. In addition, a current mirror composed of M$_{7-9}$ and another coupling capacitor $C_3$ are added to protect M$_{1-4}$’s gates. When input CM voltage (source voltage of M$_{1-4}$) drops rapidly, the voltage at node A ($V_{min}$) will follow via the minimum selector, which turns on the transistor M$_{8}$. Then, the transistors M$_{7}$ and M$_{9}$ will mirror the operation of M$_{8}$ and lower the voltages at nodes B and C (gate voltage) to limit $V_{GS}$ of M$_{1-4}$. When the input CM voltage rises, $V_{min}$ also rises via the minimum selector, and the parasitic diodes D$_{BD1}$ and D$_{BD2}$ between M$_{5-6}$’s bodies and drains will limit the source–gate voltages ($V_{SG}$) less than the threshold voltage of these diodes.

IV. CIRCUIT IMPLEMENTATION OF THE PTAT REFERENCE VOLTAGE GENERATOR

Fig. 14 shows the schematic of the RVG. It consists of a bias circuit and a bipolar core. The bias circuit generates a PTAT current, which is then mirrored (1:4) to the bipolar core. Benefiting from the availability of vertical NPNs in the chosen process, the bias circuit is implemented without the extra low-offset amplifier required by PNP-based bias circuits [4], [5]. Two NPN transistors in the bipolar core are biased at a current density ratio of 7, and so their base–emitter voltage difference
\[ \Delta V_{BE} = \left(\frac{k}{q}\right) \times \ln(p) \times T_A \] is PTAT, and this is used as the ADC’s reference \( V_{PTAT} \).

Thanks to the analog TCS, a one-point trim will correct both spread in the shunt’s resistance as well as the spread in the absolute value of \( \Delta V_{BE} \) (due to the mismatch of NPNs). Hence, the NPNs do not require dynamic element matching, which represents a simplification over [4], [5]. Furthermore, the output of the PTAT reference (\( \sim 50 \text{ mV at room temperature} \)) is smaller than the bandgap reference (\( \sim 100 \text{ mV} \)) used in [4] and [5], resulting in less swing in the loop filter, and thus relaxing its settling requirement. Last but certainly not least, designing a PTAT reference is a lot simpler than designing a bandgap reference.

The two current sources in the bipolar core are chopped to suppress their 1/f noise. To avoid potential intermodulation between the chopping ripple and the ADC’s quantization noise, the chopping frequency is the same as the ADC’s sampling frequency. Compared to the analog compensation scheme described in [15], which uses a bandgap voltage followed by a reference buffer with a temperature-dependent gain, the proposed solution is much simpler and more power efficient.

V. EXPERIMENTAL RESULTS

The current sensor is implemented in a 0.18-μm HV BCD CMOS technology and occupies 1.4 mm\(^2\) (Fig. 15). It draws 10.9 μA from a 1.5-V supply at room temperature. The RVG, ADC, and digital clock generator consume 4, 5.2, and 1.7 μA, respectively. Fig. 16 shows the 2\(^{20}\)-point fast Fourier transform (FFT) output spectrum of the free-running ΔΣ modulator under different input currents. It is thermal-noise limited in a 1-kHz BW and does not exhibit idle tones. At a sampling frequency of 250 kHz, the ADC achieves a resolution of 1.5 μV\(_{\text{rms}}\) in a conversion time of 2 ms, which translates into a current-sensing resolution of 150 μA\(_{\text{rms}}\) (Fig. 17).

Similar to the previous simulation shown in Fig. 6, the sensor is also measured with a fixed 1-A input, the ADC’s output \( D_{\text{out}} \) varies 0.3% over the industrial temperature range (Fig. 18), which agrees well with the simulation results. To explore the effects of Joule’s heating in the shunt, \( \Delta V_{BE} \) was measured at different input currents (Fig. 19). It increases by 2.5 mV when input current changes from 0 to 4 A, which translates into a 15 °C temperature rise. Fig. 20 shows the transient measurement with a 4-A current step input. It can be seen that the gain error of \( D_{\text{out}} \) settles to 0.1% within 40 ms. (This latency is mainly caused by the limited slew rate of the Keithley 2400 SourceMeter used for the measurement.) The slower increase in die temperature (\( \Delta V_{BE} \)) is also shown.

The 10 sensors are characterized over a ±4-A range from −40 °C to 85 °C (Fig. 21). After a one-point trim (at +3 A and ~25 °C), the sensor’s gain error is only 0.05% at room temperature, increasing to 0.9% over the full temperature range. As discussed earlier, this large gain error over temperature is mainly caused by non-linear components.
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Fig. 19. Measured $\Delta V_{BE}$ versus input current.

Fig. 20. Transient measurement under a 4-A current step input.

Fig. 21. Measured current-sensing gain error at different ambient temperatures.

Fig. 22. Measured offset over ICMR without CHL (top) and with CHL (bottom).

Fig. 23. Measured histograms of offset and CMRR without CHL (top) and with CHL (bottom).

Fig. 24. Measured PSRR at dc.

of the shunt’s TCR, which are not cancelled out by the relatively linear PTAT reference. Over a 25-V ICMR, the ADC’s maximum offset is 6.4 μV (640 μA), dropping below 400 nV (40 μA) when CHL (a 250-Hz square wave) is enabled (Fig. 22). The offset varies by less than 700 nV over the full ICMR, corresponding to a CMRR of 151 dB, which improves to 158 dB after CHL (Fig. 23). Over a supply range from 1.5 to 2 V, the ADC’s offset varies less than 1 μV, corresponding to a dc PSRR of 113 dB. This improves to 125 dB when CHL is enabled (Fig. 24). The PSRR at high frequencies is
measured when the $\Delta \Sigma$ ADC is in free-running mode (CHL is disabled) and a 100-mV $p-p$ sinusoid is added to the 1.5-V supply. It remains above 95 dB up to 1 kHz (Fig. 25).

The performance of the sensor is summarized in Table I. Its energy efficiency, like that of a temperature sensor, can be expressed in terms of a resolution figure of merit (FOM) [16]. Compared with the other fully integrated current sensors [5], [17], [18], this design achieves 10× better energy efficiency, the lowest gain error at room temperature, and comparable gain error over the industrial temperature range.

VI. CONCLUSION

A fully integrated high-side current sensor has been implemented in a 0.18-μm HV BCD process. The shunt resistor is implemented with the on-chip metal layers of the CMOS process, which minimizes the required off-chip components. The beyond-the-rails ADC enables the direct digitization of the shunt voltage in the presence of large CM voltage and obviates the use of HV IAs, thus reducing the power and chip area of the HV interface circuit. To correct the error caused by the shunt resistance’s large temperature dependence, an analog TCS is realized by employing a PTAT voltage as the ADC’s reference. It eliminates the need for a temperature sensor and calibration logic and further simplifies the sensor architecture at the system level. As a result, the sensor achieves state-of-the-art power efficiency, as well as low gain error over the industrial temperature range.

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Long Xu (S’15) received the B.Eng degree in electronic engineering from Lanzhou University, Lanzhou, China, in 2010, and the M.Sc. degree in integrated-circuits design from the Institute of Electronics, Chinese Academy of Sciences, Beijing, China, in 2013. He is currently pursuing the Ph.D. degree with the Electronic Instrumentation Laboratory, Delft University of Technology, Delft, The Netherlands.

Since 2018, he has been as an Analog Design Engineer with Dialog Semiconductor B.V., ’s-Hertogenbosch, The Netherlands. His current research interests include sensor interface circuits and precision date converters.

Johan H. Huijsing (SM’81–F’97–LF’10) was born in 1938. He received the M.Sc. degree in electrical engineering and the Ph.D. degree from the Delft University of Technology, Delft, The Netherlands, in 1969 and 1981, respectively.

He has been an Assistant and an Associate Professor of electronic instrumentation with the Faculty of Electrical Engineering, Delft University of Technology, since 1969. In 1990, he joined the Chair of Electronic Instrumentation, as a Full Professor. He has been a Professor Emeritus since 2003. From 1982 to 1983, he was a Senior Scientist with Philips Research Labs., Sunnyvale, CA, USA. From 1983 to 2005, he was a Consultant with Philips Semiconductors, Sunnyvale, CA, USA. Since 1998, he has been a Consultant with Maxim, Sunnyvale, CA, USA. His research work is focused on operational amplifiers, analog-to-digital converters, and integrated smart sensors. He has supervised 30 Ph.D. students. He has authored or co-authored over 300 scientific papers, 40 U.S. patents, and 15 books. In 1992, he initiated the international Workshop on Advances in Analog Circuit Design. He co-organized it yearly until 2003.

Dr. Huijsing was a Program Committee Member of the European Solid-State Circuits Conference from 1992 to 2002. He was awarded the title of Simon Stevin Meester by the Dutch Technology Foundation. He was the Chairman of the Dutch STW Platform on Sensor Technology and the biannual national Workshop on Sensor Technology from 1991 to 2002.


From 1989 to 1999, he was a Research Scientist with Philips Research Laboratories, Eindhoven, The Netherlands, where he worked on interactive displays and digital recording systems. In 1999, he joined the Delft University of Technology, where he is currently an Antoni van Leeuwenhoek Professor and the Head of the Microelectronics Department. He has authored over 15 books and 250 technical papers, and holds 26 patents. His current research interests include the design of mixed-signal circuits, sensor interfaces, and smart sensors.

Dr. Makinwa is a member of the Royal Netherlands Academy of Arts and Sciences and the Editorial Board Member of the Proceedings of the IEEE. He is the Analog Subcommittee Chair of the International Solid-State Circuits Conference (ISSCC). He is also on the program committees of the VLSI Symposium, the European Solid-State Circuits Conference (ESSCIRC), and the Advances in Analog Circuit Design (AADC) workshop. He has served as a Guest Editor for the IEEE Journal of Solid-State Circuits (JSSC) and as a Distinguished Lecturer and an Elected AdCom Member for the IEEE Solid-State Circuits Society. For his doctoral research, he received the 2005 Simon Stevin Gezel Award from the Dutch Technology Foundation. At the 60th anniversary of ISSCC, he was recognized as a top-10 contributor. He was a co-recipient of 15 best paper awards from the JSSC, ISSCC, VLSI, ESSCIRC, and Transducers, among others.