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DOI
10.1109/JSSC.2018.2832168

Publication date
2018

Document Version
Accepted author manuscript

Published in
IEEE Journal of Solid-State Circuits

Citation (APA)

Important note
To cite this publication, please use the final published version (if applicable). Please check the document version above.

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A 19.8 mW Eddy-Current Displacement Sensor Interface with Sub-Nanometer Resolution

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Abstract—This paper presents an eddy-current sensor (ECS) interface intended for sub-nanometer displacement sensing in high-tech applications. The interface employs a 126 MHz excitation frequency to mitigate the skin-effect, and achieve high resolution and stability. An efficient on-chip sensor-offset compensation scheme is introduced which removes sensor-offset proportional to the standoff distance. To assist in the ratiometric suppression of noise and drift of the excitation-oscillator, the ECS interface consists of a highly linear amplitude-demodulation scheme that employs passive capacitors for voltage-to-current conversion. Using a PCB-based pseudo-differential ECS, stability tests were performed which demonstrated a thermal drift of < 7.3 nm/°C and long-term drift of only 29.5 nm over a period of 60 hours. The interface achieves an effective noise floor of 13.4 pm/√Hz which corresponds to a displacement resolution of 0.6 nm in a 2 kHz noise-bandwidth. The ECS interface is fabricated in TSMC 0.18 µm CMOS technology and dissipates only 19.8 mW from a 1.8 V supply.

Index Terms—inductive, eddy-current, sensor, displacement, amplitude demodulation, oscillation, chopping.

I. INTRODUCTION

Sub-nanometer (sub-nm) displacement sensing is one of the most important requirements in advanced metrology and high-tech industries e.g. wafer scanners and relay mirror experiment (RME) [1]. Incremental sensors, such as linear encoders and interferometers, possess high resolution and therefore are frequently used in these applications. However they are bulky and costly. Absolute sensors, such as capacitive and inductive sensors, can compete with incremental sensors in these applications because the typical measurement range (Δx_{max}) is small: in the order of few micrometers.

Capacitive sensors [2], [3], though compact with high resolution, require electrical access to the target, which is often an issue. They are also sensitive to environmental conditions such as humidity, dirt etc. Eddy-current sensors (ECSs), on the other hand, are immune to these disadvantages, but their stability is limited by the skin-effect [4], [5]. Since eddy-current is induced deep within the target, the effective displacement sensed by an ECS is dependent on the skin-depth δ (= 1/√πµσf_{exc}), where µ is the magnetic permeability, σ is the electrical conductivity and f_{exc} is the excitation frequency of the ECS. Hence a change in skin-depth can be taken as an apparent displacement. For instance, a temperature change of 1 °C in a copper target can cause displacement errors of ≈ 100 nm when f_{exc} is 1 MHz. To attain sub-nm measurements, the temperature has to be controlled with an accuracy of 1 mK which is often not possible. A practical way to obviate this instability issue is to use a higher excitation frequency (f_{exc} > 100 MHz) in the ECS interface [5]–[7].

However, it is not trivial to increase the excitation frequency in present ECS interfaces. This is largely due to the: (a) use of large ECS coils (L > few µH); (b) large parasitic inductance (L_{par}) of the cable between the ECS coil and readout circuitry; and (c) high power dissipation in the readout circuitry [8], [9]. Large ECS coils typically have low stability and a low self-resonance frequency (SRF). The parasitic inductance L_{par} of...
Self-oscillation is found to be a power-efficient way to generate $I_{exc}$ and to excite ECS coils at a high $f_{exc}$ [16]. However, noise and drift of the front-end excitation-oscillator are important concerns. Ratiometric measurement helps in suppressing these because of their correlated-multiplicative (CM) nature. However, the efficacy of this suppression is limited by the presence of any non-linearity, e.g. due to $g_m$ stages, in the demodulator [4], [17]. It is also more difficult to attain high linearity (> 70 dB THD) at a high $f_{exc}$. The non-linearity of the demodulator is further exacerbated due to the presence of large input offsets caused by a large $x_{so}$ and $L_{par}$. To maintain the efficiency of ratiometric measurements in suppressing the noise and drift of the excitation-oscillator, linear amplitude-demodulation and on-chip sensor-offset compensation are indispensable.

In this work, we present an ECS interface with displacement resolution of 0.6 nm in a 2 kHz noise-bandwidth, with a power consumption of only 19.8 mW [18]. This is achieved by: (a) exciting ECS coils with a high $f_{exc}$ (= 126 MHz) to alleviate the performance degradation caused by the skin-effect; (b) utilizing capacitors for voltage-to-current (V2I) conversion to obviate the use of non-linear $g_m$ blocks in the demodulator and perform linear amplitude-demodulation; (c) introducing an on-chip sensor-offset-compensation scheme to remove the sensor-offset ($\propto x_{so}$), without degrading the efficacy of the ratiometric suppression of the excitation-oscillator’s noise and drift.

The paper is organized as follows. Section II discusses the architecture of the ECS interface, along with the proposed sensor-offset compensation scheme. Section III shows the circuit implementation of important blocks of the interface. Section IV discusses experimental results achieved from the ECS interface prototype. Section V summarizes the performance and concludes the paper.

II. ECS INTERFACE

A. Architecture Overview

Figure 3 depicts the detailed system architecture of the ECS interface. The interface consists of two channels: a sensor-channel and a reference channel. These process voltage amplitudes directly proportional to the sensor coil $L_{sen}$ ($= L_{so} \pm \Delta L(x)$) and the reference coil $L_{ref}$ ($= L_{so}$) respectively, where $L_{so}$ is the value of $L_{ref}$ and $L_{sen}$ at the nominal standoff $x_{so}$. The excitation of ECS coils is achieved with a PMOS-based self-oscillating front-end [16] which comprises of $L_{ref}$, $L_{sen}$ and a tank capacitance $C$. The excitation frequency generated by them is given by $f_{exc} = 1/2\pi \sqrt{(L_{sen} + L_{ref})/C}$. The voltage swings of the excitation-oscillator outputs $V_{sen}$ and $V_{ref}$ are controlled by a digitally programmable tail-current source $I_{ss,osc}$.

The excitation-oscillator outputs $V_{sen}$ and $V_{ref}$ are converted into currents $I_{sen}$ and $I_{ref}$ using capacitors $C_{in}$ and $C_{ref}$. The low input-impedance of the transimpedance amplifier (TIA) is exploited for this. A clock $f_{mix}$ synchronous to $I_{sen}$ and $I_{ref}$ (but in quadrature to $V_{sen}$ and $V_{ref}$) is generated using a fast continuous-time comparator. Currents $I_{sen}$ and $I_{ref}$ are demodulated to zero intermediate-frequency
(IF) using passive current-mixers $M_{ix1}$ and $M_{ix0}$ [19]. TIA amplify and filter demodulated currents $I_{mix1}$ and $I_{mix0}$ to generate baseband voltages $V_{o,sen}$ and $V_{o,ref}$. These voltages are digitized and a ratiometric readout $D_{out} = V_{o,sen}/V_{o,ref}$ is performed to suppress the drift and noise of the excitation-oscillator.

### B. Sensor-offset compensation

As shown in Fig. 1(b), the maximum sensor-inductance change $\Delta L_{max}$ is usually a small fraction of the standoff inductance $L_{so}$ $(\propto x_{so})$. Hence $I_{sen}$ consists of a large signal proportional to $L_{so}$ (and $x_{so}$), along with the useful displacement information in $\Delta L(x)$. This offset signal degrades the linearity of the demodulator and therefore must be compensated for before being amplified.

The proposed ECS interface leverages the anti-phase relationship between the sensor and reference coil voltages for sensor-offset-compensation. To mitigate sensor-offset, $V_{ref}$ is used to generate a compensation current $I_{soc}$ through capacitor $C_{soc} (= C_{in})$. This current is added to $I_{sen}$ at the input of $M_{ix1}$. The TIA output $V_{o,sen}$ then depends only on $\Delta L(x)$. The signal gain in the reference channel is scaled down by a factor $\beta (= \Delta x_{max}/x_{so})$ with $C_{ref} = \beta \cdot C_{in}$ so that the reference channel output $V_{o,ref}$ corresponds to only the maximum inductance change $\Delta L_{max}$ and not $L_{so}$. The modified ratiometric readout $D^*_{out}$ is given by,

$$D^*_{out} = \frac{V_{o,sen}}{V_{o,ref}} = \frac{|V_{sen}| - |V_{ref}|}{\beta \cdot |V_{ref}|} = \frac{\Delta L(x)}{\beta \cdot L_{so}} = \frac{\Delta x}{\Delta x_{max}} \quad (1)$$

where $V_{o,sen}$ and $V_{o,ref}$ are the output of the sensor and the reference channel respectively, $|V_{sen}|$ and $|V_{ref}|$ are the amplitudes of the two outputs of the oscillator. Due to the proposed sensor-offset-compensation technique, the sensor channel output $V_{o,sen}$ is proportional to $|V_{sen}| - |V_{ref}|$ i.e. $\Delta L(x)$ and does not depend on the standoff inductance $L_{so}$.

The choice of using $V_{ref}$ for the sensor-offset compensation is important. Current $I_{soc}$ generated from $V_{ref}$ using capacitor $C_{soc}$, contains all CM terms of the excitation oscillator and hence preserves the functionality of the ratiometric readout in suppressing them after sensor-offset compensation. This would not be possible if the compensation current is not generated from the excitation-oscillator itself. Figure 4 depicts the working principle of the sensor channel, with sensor-offset-compensation, for the case $L_{sen} > L_{ref}$ i.e when the target is farther from the nominal standoff position.

### III. Circuit Implementation

#### A. Front-end Excitation Oscillator

This section discusses the implementation of the excitation-oscillator of the ECS interface. As shown in Fig. 5, a PMOS-based cross-coupled LC oscillator structure is employed. Off-chip ECS coils $L_{sen}$ and $L_{ref}$ form a resonator along with the on-chip capacitor $C$. The voltage swing can be calculated as:

$$|V_i| = j \cdot 2\pi \cdot f_{exc} \cdot L_i \cdot I_{LC} \quad (2)$$

where $V_i$ is the excitation-oscillator output voltage corresponding to the ECS coil $L_i$, $f_{exc}$ is the excitation frequency.
generated by the LC resonator and \( I_{LC} \) is the resonance current flowing in the LC tank. \( I_{LC} \) can be so derived from the excitation-oscillator bias current \( I_{ss,osc} \), tank quality factor \( Q \) and switching efficiency \( \eta \) [20], [21]. The oscillator bias current \( I_{ss,osc} \) is digitally programmable to provide currents from 520 \( \mu \)A to 2.16 mA. The tail current source is cascaded to prevent modulation due to oscillator output swing. One important point to note is that the effective oscillator amplitude-noise also flows through both ECS coils (like \( I_{ILC} \)) and is suppressed with ratiometric measurement [4].

Since ECS coils are off-chip, care must be taken to minimize various parasitic elements between coils and interface circuitry. Figure 5(a) shows important parasitic components namely: electrostatic discharge (ESD), cell parasitic capacitance \( C_{p,esd} \), package-pin parasitic capacitance \( C_{p,pin} \), bond-wire inductance \( L_b \), and coil-to-pin interconnect parasitic inductance \( L_{ic} \). ESD cells with 1 KV HBM ESD protection and a small parasitic capacitance \( \approx 100 \) fF are chosen so that \( C_{p,esd} \) is much smaller than the tank capacitance \( C \approx 8 \) pF. A QFN package with a small \( L_b \approx 1.5 \) nH and \( C_{p,pin} \approx 0.3 \) pF is used. The matching between two \( L_{ic} \)s is attempted by connecting nodes \( V_{sen} \) and \( V_{ref} \) to pins of the package which are at same angles. One important concern is that \( L_b \) can make a high-frequency parasitic resonance loop along with \( C \) and \( C_{p,pin} \). Then, the front-end can start to oscillate at a frequency which is independent of sensor and reference coils. This is obviated by ensuring that the primary LC resonator has a higher \( Q \) than parasitic resonators. This also limits the lower bound of the excitation frequency [4].

Figure 5(b) illustrates the conceptual structure of the sensor-head. It consists of two coils \( L_{sen} \) and \( L_{ref} \) of identical geometry. The matching between the sensor and the reference coils is important for the efficacy of the sensor-offset-compensation technique. The coils are shielded from each other using a grounded middle layer to obviate mutual inductance. The thickness of the shield should be at least 6 times higher than the skin-depth at the excitation frequency, to prevent interaction between the two coils. The nominal value of \( L_{ref} \) is achieved by positioning a fixed reference target at a nominal standoff \( x_{so} \) from reference coil. The nominal standoff for the sensor coil is chosen to be same as \( x_{so} \). This approach has three important advantages: (a) the nominal inductance of both ECS coils is very close at \( x = x_{so} \) which helps in accurate sensor-offset compensation, (b) drift in ECS coils, e.g. due to thermal expansion, is suppressed by the ratiometric readout, and (c) the real reference quantity used in the system is the distance between the reference target and \( L_{ref} \). This is attractive because we are sensing displacement and using the reference same as the measurand makes the system inherently more stable [22].

B. Amplitude Demodulation

This section discusses the implementation of the amplitude-demodulation block in the ECS interface. Figure 6 depicts the details of demodulator in the sensor channel. The demodulation in the reference channel is identical to that of the sensor-channel, the only difference being \( C_{rref} = \beta * C_{rin} \). As explained in Section II, capacitor \( C_{rin} \) generates \( I_{soc} \) from \( V_{ref} \) to compensate for the sensor-offset. For this
reason, $I_{\text{sen}}$ and $I_{\text{soc}}$ are added at the input of $M_{\text{tx1}}$ where the impedance is low around $f_{\text{exc}}$ [19].

A synchronous clock $f_{\text{mix}} (= f_{\text{exc}})$ is used for the amplitude-demodulation. Direct down-conversion to zero IF is chosen to reduce the complexity of the demodulator. However, this puts additional constraints on the offset and flicker noise, which are dealt with in this work by employing chopping at various levels [23]. Downconversion mixers and amplifiers in both TIAs are chopped to mitigate their low frequency errors. Unbalanced inputs to the demodulator causes common-mode signals at $2f_{\text{exc}}$ at the virtual ground of the TIA. Capacitor $C_s$ provides low impedance and assists the TIA in suppressing this and higher harmonics of $f_{\text{exc}}$.

1) Capacitors for V2I: As shown in Fig. 6, the demodulation scheme uses passive capacitors ($C_{\text{in}}$ and $C_{\text{soc}}$) as V2I blocks. The effective transconductance gain can be calculated as the product of transfer gain of the V2I block and the downconversion mixer, and is given by,

$$G_{m,\text{eff}} = 2\pi \cdot f_{\text{exc}} \cdot C_{\text{in}} \cdot \frac{2}{\pi} = 4 \cdot f_{\text{exc}} \cdot C_{\text{in}}$$  (3)

With $f_{\text{exc}} = 126$ MHz and $C_{\text{in}} = 500$ fF, $G_{m,\text{eff}}$ evaluates to 252 $\mu$A/V. This is equivalent to a switched-capacitance-resistor value of $\approx 4 \, k\Omega$. An example, for $|V_{\text{sen}}| = 400$ mV and $\beta = 0.1$, the maximum current ($\propto \Delta x_{\text{max}}$) input to the TIA is calculated as 10 $\mu$A. Hence, for $\Delta x_{\text{max}} = 10 \, \mu$m and $\Delta x_{\text{min}} = 1 \, \mu$m, the minimum current to be detected by the TIA is 1 nA.

Employing capacitors as V2I has a number of advantages. Firstly, it improves the linearity and reduces power consumption of the demodulator. Passive resistors [24] can also be employed for this purpose however they degrade the quality factor of the LC resonator. Another issue with using resistors is that the common-mode voltage of the excitation-oscillator outputs is too low for the TIAs to function properly. Using capacitors as V2I also relaxes the mixer size due to the quadrature relationship between the switch resistance $R_{\text{sw}}$ and capacitive reactance ($\propto C_s$) (Fig. 6). This helps in reducing the parasitic capacitance ($C_p$ in Fig. 6) and improves noise performance of the demodulator. Capacitors also assist in increasing the excitation-frequency as they present higher transconductance-gain with frequency whereas more current and area has to be spent to improve the transconductance-gain of $g_m$ cells and resistors, respectively.

2) Downconversion Mixer: Current-driven passive mixers are attractive due their low flicker noise, and hence they are often employed for demodulation to zero IF [19], [25], [26]. The proposed sensor-offset compensation scheme further reduces the mixer’s noise contribution by removing the excess offset-current flowing through them [27]. Due to the high frequency operation of downconversion mixers, the charge injection of mixers $M_{\text{tx1}}$ and $M_{\text{tx2}}$ can cause significant residual offset. This is mitigated by a nested-chopping scheme operating at $f_{\text{mix}}/4096$ [28], [29].

However for mixers to work in current-mode, the mixer switch resistance $R_{\text{sw}}$ and TIA input impedance ($R_{\text{in,tia}}$) should be much smaller than the capacitive impedance at $f_{\text{exc}}$ ($R_{\text{sw}} + R_{\text{in,tia}} << \frac{1}{j \cdot 2 \pi \cdot f_{\text{exc}} \cdot C_p}$). A small $R_{\text{sw}}$ can be achieved by increasing the size of switching transistors. However this causes an increase in the parasitic capacitance $C_p$ which deteriorates the noise performance of the demodulator. Assuming the noise of the amplifier $A_v$ is the dominant source, the noise-figure NF of the demodulator can be evaluated as:

$$NF = \frac{C_{\text{in}} + C_p}{C_{\text{in}}}$$  (4)

In this work, mixers are sized to add total parasitic capacitance $C_p$ of only 50 $\Omega$ which degrades noise of TIA by only 10%. Sensor-offset compensation capacitor $C_{\text{soc}}$ does affect the noise of the sensor-channel TIA adversely, hence NF has a minimum value of 3 dB. As per simulations, the effective $R_{\text{sw}}$ is 150 $\Omega$ (increased 3 times due to nested-chopping) and the capacitive reactance at 126 MHz is $\approx 2.5 \, k\Omega$. The quadrature relationship between these two impedances further helps in defining currents predominantly by the capacitance.

3) Transimpedance amplifier: The TIA is one of the most important block in the proposed demodulation scheme. For capacitors to perform efficiently as V2I blocks, the TIA must present a low input impedance $R_{\text{in,tia}}$ within the bandwidth of the input. The impedance transformation property of current-driven mixers shifts this low impedance to the input of mixers around $f_{\text{exc}}$ [19]. The amplifier $A_v$ must possess high gain at low frequency to achieve this. Also, the negative feedback in the TIA should still be present at $2 \times f_{\text{exc}}$ because the input to the TIA consists predominantly of a baseband signal around DC and $2 \times f_{\text{exc}}$ ($f_{\text{mix1}}$ in Fig. 4). To ensure the proper functioning of capacitors as V2I, $A_v$ is designed for a $> 110$ dB DC gain and a $> 1$ GHz unity-gain-frequency $f_u$ ($\approx 8 \times f_{\text{mix}}$).

The schematic of the amplifier $A_v$ is shown in Fig. 7. The amplifier consists of a two-stage Miller-compensated amplifier. The first stage is a telescopic amplifier and the second stage $A_v2$ is a common-source (CS) stage. To achieve high DC gain without deteriorating high-frequency behavior of the amplifier, gain-boosting is employed in the telescopic amplifier [30]–[32]. Auxiliary (gain-boosting) amplifiers, for both PMOS and NMOS cascodes, are also realized as two-stage amplifiers to achieve sufficient gain. Auxiliary amplifiers consist of a folded-cascode amplifier followed by a CS amplifier, and they are Miller-compensated. Although the use of a differential signal path reduces charge-injection errors, unbalanced inputs to the TIA lead to common-mode signals at $2 \times f_{\text{mix}}$. These are suppressed by common-mode feedback (CMFB) circuitry and capacitor $C_s$. Two auxiliary amplifiers and the main amplifier have their own CMFB control.

The noise of the amplifier $A_v$ is the dominant source in the demodulator. The input-referred noise $v_{n,\text{in}}$ required from the amplifier in the TIA can be evaluated as,

$$v_{n,\text{in}} \leq \Delta v_{\text{sen,min}} \cdot NF$$  (5)

where $\Delta v_{\text{sen,min}}$ is the minimum detectable change in the amplitude of $V_{\text{sen}}$. For $|V_{\text{sen}}| = 400$ mV, $x_{\text{so}} = 100 \, \mu$m and $\Delta x_{\text{min}} = 1 \, \mu$m, $\Delta v_{\text{sen,min}} = 4 \, \mu$V. Hence $v_{n,\text{in}} < 2 \, \mu$V is required from the amplifier in the TIA.
for \( NF = 3 \, \text{dB} \). For a bandwidth of 2 kHz, the amplifier \( A_v \) should possess an effective input thermal noise floor smaller than \( 45 \, \text{nV}/\sqrt{\text{Hz}} \).

Low-frequency errors of the amplifier are very important for the zero IF demodulation scheme. We have mitigated them using chopping technique in this work. As shown in Fig. 7, both the amplifier \( A_v \) and auxiliary amplifiers are chopped to mitigate their offset and low-frequency noise. Choppers are always placed at low impedance nodes to reduce their residual offsets, caused by self-mixing. PSS simulations show that the amplifier achieves a 113 dB DC gain over a 3-dB bandwidth \( \approx 4 \, \text{kHz} \). The amplifier is not unity-gain compensated.

### C. Quadrature Clock Generation

This section illustrates the implementation of the quadrature clock comparator needed for the generation of the clock which has a \( \pi/2 \) radian phase lead compared to the excitation-oscillator outputs. The design of a comparator, that is fast enough, is very important because any excess phase difference over \( \pi/2 \) radians attenuates the effective input signal to the TIA and degrades the input SNR to the TIA. This attenuation is proportional to \( \cos(\Delta \phi) \) where \( \Delta \phi \) is the phase difference between the ideal quadrature-clock phase and the phase of the comparator output. As an example, at \( f_{\text{exc}} = 200 \, \text{MHz} \), a 500 ps excess delay translates to \( \Delta \phi = 36 ^\circ \) causing the signal to be attenuated by 20 %. For this reason, a fast continuous-time comparator has been designed.

Figure 8 shows the schematic of the continuous-time comparator designed for the interface. The comparator consists of 3 stages: (1) quadrature generation stage, (2) self-biased preamplifier, and (3) regenerative latch. The quadrature generation stage provides a low input impedance so that capacitors \( C_{\text{comp}} (= 200 \, \mu \text{F}) \) generate currents proportional to input voltages \( V_{\text{sen}} \) and \( V_{\text{ref}} \). These currents, in quadrature to the excitation-oscillator voltages, are converted into voltages \( V_{\text{op1}} \) and \( V_{\text{om1}} \) at low impedance nodes, resulting in smaller delay at the expense of a low voltage gain. The self-biased preamplifier stage [33] amplifies the output of the 1st stage and also sets the optimum amplifier-to-latch transfer point which desensitizes the effect of PVT variations on the comparator delay [34]. This is important for minimizing the delay due to the regeneration stage. At \( f_{\text{exc}} = 126 \, \text{MHz} \), \( 0.4 \, \text{ns} \) delay of the comparator causes \( 5 \% \) signal attenuation.
IV. EXPERIMENTAL RESULTS

To evaluate the usefulness of proposed concepts in precision displacement sensing, a microchip was fabricated. As shown in Fig. 9, the ECS interface occupies only \(1.18 \text{ mm}^2\) in TSMC 0.18 \(\mu\text{m}\) CMOS technology. The interface consumes 11 mA from a 1.8 V supply, which includes 2.2 mA consumed by two on-chip unity-gain output buffers used to drive an off-chip ADC. The analog output of the chip is digitized using an evaluation board of the 24-bit \(\Sigma\Delta\) ADC AD7779.

A. PCB-based ECS

A PCB-based sensor was used to evaluate the performance of the microchip and its usefulness in sensing displacement. Figure 10(a) depicts the structure of the PCB-based sensor. It consists of two flat coils, of identical geometry, implemented in the top and bottom layer of a custom four-layer PCB. Each coil consists of four, 35 \(\mu\text{m}\) thick, turns with a 200 \(\mu\text{m}\) pitch and an 8 mm outer diameter. The coils are shielded from each other by two ground planes to prevent mutual inductance. Their distance to the moving sensor target and fixed reference target is established by a number of precision 10 \(\mu\text{m}\) stainless-steel spacers. Spacers are positioned 3 mm away from the coils so as not to affect the sensitivity of coils.

Figure 10(b) illustrates the custom PCB designed for the characterization of the ECS interface. Nylon nuts and bolts are used to position sensor and reference targets with the help of stainless steel spacers with high stiffness. With a copper target and nominal standoff \(x_{so} = 105 \mu\text{m}\) (14 spacers minus coil thickness of 35 \(\mu\text{m}\)), the effective standoff inductance \(L_{so}\) is found to be \(\approx 100 \text{nH}\) (including \(L_{ic} \approx 20 \text{nH}\)) using an impedance analyzer. The coil used for the characterization of the ECS interface is similar to coil 3, annotated in Figure 10(b) (but underneath the copper target in the figure).

B. Transfer characteristic

Figure 11 shows the measured transfer characteristic obtained using the ECS interface and the PCB-based sensor, where \(D_{out} = V_{o,sen}/V_{o,ref} = \Delta x/\Delta x_{max} = \Delta L(x)/(\beta \times L_{ref})\) (Eqn. 1). To introduce a displacement \(\Delta x\), the number of spacers between the sensor target and the sensor coil is varied. This introduces an effective displacement of 10 \(\mu\text{m}\) with each spacer, around nominal standoff \(x_{so} = 105 \mu\text{m}\) (Fig. 5 and Fig. 10). The distance between the reference coil and reference target is kept fixed at 105 \(\mu\text{m}\).

The transfer characteristics is evaluated at three different values of \(I_{ss,osc}\), 1.2 mA, 1.52 mA and 1.84 mA, to evaluate the effectiveness of the ratiometric principle in suppressing the effect of the oscillator bias current \(I_{ss,osc}\). Output \(V_{o,sen}\) has a higher slope at higher \(I_{ss,osc}\) due to higher gain. Three \(V_{o,sen}\) curves meet at a single point where \(L_{sen} = L_{ref}\). The variation in \(V_{o,ref}\) is dominated by the improvement in the quality factor of the sensor-coil, in spite of a decrease in \(f_{exc}\), with higher \(x_{so}\). The ratiometric readout \(D_{out}\) (Eqn. 1) is well matched for three values of \(I_{ss,osc}\).

The presence of the null in \(D_{out}\) around the nominal \(x_{so} = 105 \mu\text{m}\) shows that the sensor-offset is indeed compensated by the ECS interface. The deviation of zero-crossing...
from $x_{so} = 105 \, \mu m$ is due to a small mismatch ($\approx 3 \, nH$) between $L_{sen}$ and $L_{ref}$, caused primarily by the difference in parasitic inductances. The maximum displacement range $\Delta x_{\text{max}}$ was found to be 10 $\mu m$ which matches closely to $\beta \cdot x_{so}$, with $\beta = 0.1$ and $x_{so} = 105 \, \mu m$. The limited output voltage range of the TIA manifests itself as the saturation of $D_{out}$ at larger displacements. The ratiometric readout $D_{out}$ for higher ($I_{ss,osc}$) saturates at smaller standoffs due to larger signal swing from the excitation-oscillator.

Due to pseudo-differential structure of the sensor, the excitation frequency $f_{exc}$ also undergoes change with the displacement. An excitation frequency deviation of $\Delta f_{exc} = 1.3 \, MHz$, around $f_{exc} = 126 \, MHz$, for a displacement change of $\Delta x_{\text{max}} = 10 \, \mu m$ was noticed. This confirms that the frequency output in the ECS is indeed less sensitive when compared to the output amplitude ($\Delta f_{exc}/f_{exc} \approx 1 \%$).

C. Noise characterization

To evaluate the noise performance of the ECS interface, fast Fourier transform (FFT) was used. Measured 2$^{17}$ point FFTs of two output voltages and $D_{out}$ are shown in Fig. 12, with $\Delta x_{\text{max}} = 10 \, \mu m$ (standoff distance = 115 $\mu m$). The noise spectrum in two output voltages was found to be dominated by the oscillator amplitude-noise. The suppression of the low-frequency amplitude-noise of the excitation oscillator, due to ratiometric readout $D_{out}$, is clearly noticeable. The spectral shaping is primarily due to the decimation filter of the off-chip $\Sigma \Delta$ ADC. Low-frequency noise was found be dominated by residual flicker noise from the tail-current source of the excitation-oscillator. In a 2 kHz noise-bandwidth, the calculated SNR was found to be 86.6 dB, which corresponds to a resolution of 14.1 bits over $\Delta x_{\text{max}} (= 10 \, \mu m)$. This corresponds to a displacement resolution of 0.6 nm and effective noise floor of $13.4 \, \mu m/\sqrt{Hz}$. For coil inductance = 100 nH, this corresponds to an inductance resolution of 0.58 pH. The signal bandwidth could not be directly measured because of practical difficulty of introducing $\mu m$ range single-tone vibration into the sensor target. However, the signal bandwidth in the ECS interface is limited by the bandwidth of the amplifier $A_v$ used in the TIA. Parasitic extracted PSS simulations reveal that the amplifier $A_v$ has 3-dB bandwidth of $\approx 4 \, kHz$.

Another experiment was also performed to evaluate the suppression efficacy of the ratiometric measurement. A 2 kHz frequency component was introduced in the oscillator bias current by switching on and off 80 $\mu A$ in parallel to a fixed current of 1.12 mA. The output spectrum of output voltages and $D_{out}$ is shown in Fig. 13. It can be noted that the signal tone at 2 kHz is suppressed by 34 dB by the ratiometric measurement. This shows that ratiometric measurement suppresses variation in $I_{ss,osc}$, which is instrumental in improving the noise and drift performance of the ECS interface. A 34 dB suppression also endorses the high linearity of the
demodulators, when compared to [4] which achieved $\approx 24$ dB of ratiometric suppression. A higher noise floor is also noticed in the spectrum which we feel is due to the inter-modulation effect of the switched-current source.

Using an LNA (SR560) and a low-noise spectrum analyzer (HP4395A), the output noise floor of the reference channel is found to be 136 nV/Hz. This would translate into a 92.9 dB SNR, if all of oscillators amplitude-noise was suppressed by the ratiometric readout. In practice, it is slightly less because of the finite input impedance of the demodulator which allows some of oscillator’s amplitude-noise to escape from the LC tank. This illustrates an important trade-off when using capacitors as V2I instead of a $g_{m}$ block.

### D. Stability characterization

Stability tests were performed on the ECS interface using the climate chamber ACS DY110C. The temperature and humidity were controlled using the software LabVIEW®. As shown in Fig. 14, the PCB-based ECS and the readout interface were placed inside a thick Aluminium box to ensure a highly stable environment. During the experiment, a high precision temperature sensor Pt100 was used to find the exact temperature of the PCB-based ECS inside the Aluminium box (Fig. 10). The Aluminium box, with the ECS and interface inside, was placed in the climate chamber, and precautions were taken to isolate mechanical vibrations of the climate chamber from coupling to the sensor.

For thermal stability characterization, humidity was kept fixed at 40 % and temperature was stepped from 20 °C to 40 °C, in steps of 5 °C, and then back to understand the hysteresis effects. Figure 15 shows the drift in $D_{out}$ caused by the change in temperature. A temperature change of 17.14 °C caused an effective displacement error of 124 nm ($\Delta x = \Delta D_{out} \times x_{max}$), which corresponds to a thermal drift of 7.24 nm/°C. This amount of thermal drift is very low because various applications requiring such a high displacement resolution have very well-controlled environments ($\Delta T < 10 - 20$ mK). The difference in plots for the two directions of the temperature change is attributed to the long-term drift (the experiment took $\approx 22$ hours to complete).

For long-term stability, temperature and humidity of the climate chamber were kept fixed at 25 °C and 40 % respectively. The experiment was carried out for 60 hours, during which data was captured once every 5 minutes for a duration of 1 second. Figure 16 shows the effect of long-term drift on $D_{out}$. After the 1st order fit, the effective drift was calculated as $\approx 29.5$ nm over 60 hours. The deviation from the linear behavior is attributed to mechanical vibrations of the climate chamber which were not attenuated enough by the vibration isolator. High precision applications such as wafer scanners are frequently calibrated between each run ($< 2$ minutes). Hence a long-term drift of 29.5 nm over 60 hours is quite benevolent.

### E. Performance comparison

Table I summarizes the performance of the ECS interface and compares it to the state-of-the-art from both academia and industry. The presented ECS interface achieves 0.6 nm in a 2 kHz noise-bandwidth. This is at least 30 x better than [9]. Despite a higher $f_{exc}$, better resolution and implementation in a sub-micron CMOS process, the interface dissipates similar power [4], [7]. Thermal drift is found to at least one order
better than the previous state-of-the-art [4]. Furthermore, it achieves an inductance resolution of 0.58 pH which outperforms that of precision LCR meters.

To compare the power-efficiency of ECS interfaces, a figure-of-merit ($FoM_{ECS}$) was introduced in [4],

$$FoM_{ECS} = \frac{P}{BW \cdot 2^{ENOB} \cdot f_{exc}} \tag{6}$$

where $P$ is the power consumption, $BW$ is the measurement bandwidth, $ENOB$ is effective-resolution of the interface (in bits) and $f_{exc}$ is the excitation frequency of the ECS interface. The presented ECS interface is at least four times better than the state-of-the-art, when it comes to power-efficiency.

V. Conclusion

An ECS interface for sub-nanometer displacement sensing is presented. The degradation of the stability due to the skin-effect is mitigated using a high excitation frequency ($> 100$ MHz). A small standoff distance, along with integrated read-out circuitry in close proximity to the ECS coils, is employed to improve the sensitivity of the system. Ratiometric measurement is found to be instrumental in suppressing the noise and drift of the excitation-oscillator. To assist this ratiometric suppression, a highly linear amplitude demodulation scheme is realized using a passive (capacitive) voltage-to-current conversion approach. Sensor-offset-compensation is found to be helpful in obviating the detrimental effect of sensor-offset on the linearity of the interface, particularly demodulator blocks.

At a nominal standoff of 105 $\mu$m, the ECS interface achieved a displacement resolution of 0.6 nm (in 2 kHz noise-bandwidth) within a 10 $\mu$m displacement range. The thermal drift was found to be $< 7.3$ nm/$^\circ$C, in the range of 20 $^\circ$C to 40 $^\circ$C. A 60-hour long-term stability experiment showed a drift of only 29.5 nm. What is more, all of this is achieved by consuming only 11 mA from a 1.8 V supply. By increasing $f_{exc}$, reducing the standoff distance and compensating sensor-offset, this is the only ECS interface to achieve sub-nanometer displacement resolution.

ACKNOWLEDGMENT

Authors would like to acknowledge Prof. Johan Huising, Zu-yao Chang, Lukasz Pakula and Hui Jiang for their help at various stages of this project. Authors would also like to thank ASML, MicroEpsilon and Catena Microelectronics for useful technical discussions. Lastly, authors would like to thank the Dutch Technology Foundation NWO for the financial support.

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