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Low-Cost Calibration Techniques for Smart Temperature Sensors

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***Abstract*—Smart temperature sensors generally need to be trimmed to obtain measurement errors below $\pm 2^{\circ}$C. The associated temperature calibration procedure is time consuming and therefore costly. This paper presents two, much faster, voltage calibration techniques. Both make use of the fact that a voltage proportional to absolute temperature (PTAT) can be accurately generated on chip. By measuring this voltage, the sensor's actual temperature can be determined, whereupon the sensor can be trimmed to correct for its dominant source of error: spread in the on-chip voltage reference. The first calibration technique consists of measuring the (small) PTAT voltage directly, while the second, more robust alternative does so indirectly, by using an external reference voltage and the on-chip ADC. Experimental results from a prototype fabricated in 0.7μm CMOS technology show that after calibration and trimming, these two techniques result in measurement errors ($\pm 3\sigma$) of $\pm 0.15^{\circ}$C and $\pm 0.25^{\circ}$C, respectively, in a range from -55°C to 125°C.**

***Index Terms*—temperature sensors, calibration, trimming, bipolar transistors.**

I. Introduction

SMART temperature sensors manufactured in standard CMOS technology are attractive because of their low cost and digital interfaces. Without trimming, however, the accuracy of commercially-available smart temperature sensors is relatively poor, resulting in measurement errors that typically exceed $\pm 2^{\circ}$C over the industrial temperature range (-55°C to 125°C) [1]. Higher accuracy is feasible, but typically requires a costly calibration procedure at multiple temperatures.

In [1], we have reported a CMOS smart temperature sensor that achieves errors of only $\pm 0.1^{\circ}$C over the industrial temperature range. Like most CMOS smart temperature sensors, this sensor uses the temperature-dependent characteristics of substrate bipolar transistors to sense temperature. Its high level of accuracy was achieved by using offset cancellation and dynamic element matching (DEM) techniques throughout the design, so as to make errors contributed by the sensor's interface circuitry negligible. As a result, only a single calibration at room temperature was needed. However, this is still a time-consuming temperature calibration.

In this paper, we present two faster alternatives to such a conventional temperature calibration [2]. These alternatives are based on the observation that the on-chip voltage reference is the dominant source of error in a smart temperature sensor based on bipolar transistors [1], [3]. Therefore, it should only be necessary to calibrate and correct this voltage reference, rather than the complete sensor, provided sufficient measures have been taken to make other circuit-related errors negligible by design. The voltage measurement associated with such a calibration can be performed much faster than an accurate temperature measurement, and does not require a temperature-stabilized environment. Therefore, such *voltage calibration* should result in significant cost savings in the production of accurate smart temperature sensors.

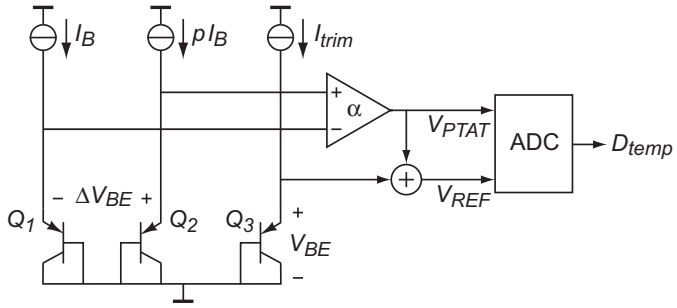

Fig. 1. Simplified circuit diagram of the CMOS smart temperature sensor.

This paper is organized as follows. The operating principle of smart temperature sensors is reviewed in section II, including the precision design techniques that can be applied to ensure that the on-chip voltage reference is the only dominant source of error. In section III, conventional calibration techniques for such sensors are reviewed. In sections IV and V, two implementations of the voltage calibration technique are discussed: the first is based on measuring an on-chip voltage, while the second is based on applying an external reference voltage to the chip. Both alternatives have been applied to the temperature sensor described in [1]. The experimental results are discussed in section VI. Section VII discusses the metrological traceability of the calibration techniques. The paper ends with conclusions.

II. Operating Principle

Fig. 1 shows a simplified circuit diagram of our smart temperature sensor [1]. A voltage proportional to absolute temperature (PTAT) is obtained from the difference in the base-emitter voltages of two bipolar transistors Q_1 and Q_2

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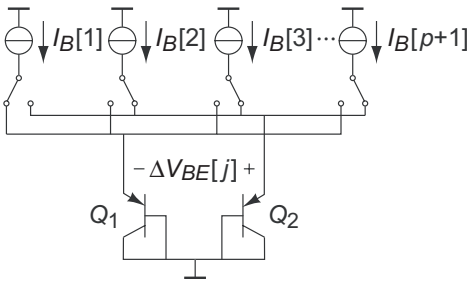

Fig. 2. Dynamic element matching of the bias-current sources to generate an accurate ΔV_{BE}.

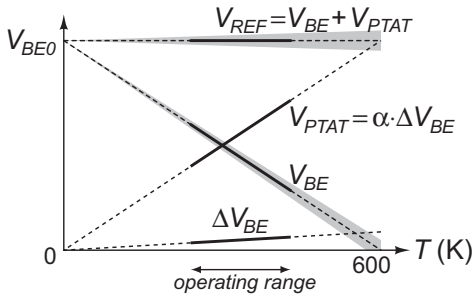

Fig. 3. Temperature dependency of the voltages in Fig. 1; the shaded areas indicate production spread.

biased at a $1:p$ current ratio:

$$\Delta V_{BE} = \frac{kT}{q}\ln\left(\frac{pI_B}{I_S}\right) - \frac{kT}{q}\ln\left(\frac{I_B}{I_S}\right) = \frac{kT}{q}\ln(p) \quad (1)$$

where k is Boltzmann's constant ($1.381\cdot10^{-23}\mathrm{J/K}$), q is the electron charge ($1.602\cdot10^{-19}\mathrm{C}$), T is the sensor's absolute temperature, I_B is the unit bias current used, and I_S is the saturation current of the two (identical) transistors. In CMOS technology, this voltage can be generated by using parasitic substrate pnp transistors [3]. Typically, an integer current ratio is used. In our design, we used $p=5$, which leads to a sensitivity of about $140\mu\mathrm{V/°C}$. Because ΔV_{BE} does not depend on any processing parameters, this voltage is intrinsically accurate, provided mismatch errors in the bipolar transistors and in the $1:p$ current ratio are eliminated.

Fig. 2 shows how such mismatch errors can be eliminated using DEM [3]. The two current sources I_B and pI_B in Fig. 1 are implemented using $p+1$ nominally identical current sources $I_B[j]$ ($1\le j\le p+1$), one of which is switched to transistor Q_1, while the other p are switched to transistor Q_2. Thus, $p+1$ voltages $\Delta V_{BE}[j]$ can be generated. As a result of the mismatch between the current sources, each of these voltages will be associated with an error:

$$\Delta V_{BE}[j] = \frac{kT}{q}\ln\left(\frac{\sum_{i\neq j} I_B[i]}{I_B[j]}\right) = \frac{kT}{q}\ln(p+\Delta p_j) \quad (2)$$

where Δp_j is the deviation in the current ratio from its ideal value p. In the *average* of these voltages, however, the error terms cancel, at least to first order. A small error proportional to $(\Delta p/p)^2$ remains, which is generally negligible. Using similar DEM techniques, errors associated with the mismatch between Q_1 and Q_2 can also be averaged out, resulting in an average ΔV_{BE} that is mismatch-error free.

A temperature-independent bandgap reference voltage V_{REF} is obtained by combining the base-emitter voltage V_{BE} of transistor Q_3 (Fig. 1) with a scaled version of ΔV_{BE}:

$$V_{REF} = V_{BE} + \alpha\Delta V_{BE} \quad (3)$$

where the scale factor α is chosen such that the negative temperature coefficient of V_{BE} of about $-2\mathrm{mV/°C}$ is compensated for by $\alpha\Delta V_{BE}$ (Fig. 3).

Finally, an ADC determines the ratio of ΔV_{BE} and V_{REF} to obtain a digital output proportional to temperature:

$$D_{temp} = \frac{\alpha\Delta V_{BE}}{V_{BE}+\alpha\Delta V_{BE}} = \frac{V_{PTAT}}{V_{REF}} \quad (4)$$

With appropriate scaling, this output can be directly interpreted as a temperature reading in degrees Celsius.

In this representation, V_{BE} is assumed to be a linear function of temperature. In practice, however, V_{BE} is slightly non-linear [4]. This so-called curvature means that V_{REF} exhibits a residual temperature dependence, and that D_{temp} exhibits a non-linearity that can amount to $2°\mathrm{C}$. This non-linearity is largely systematic, and can therefore be compensated for [1], [5].

An additional source of errors in this type of temperature sensors is amplifier offset. In particular, the offset voltage associated with amplifying ΔV_{BE} can easily dominate the overall error budget: typical offsets in CMOS technology are in the order of $1\mathrm{mV}$, which translates to a temperature error of several degrees, as a result of the relatively small sensitivity of ΔV_{BE}. Dynamic offset cancellation techniques can be used to reduce the offset voltage of CMOS amplifiers to levels well below $10\mu\mathrm{V}$, making the associated temperature error negligible [1], [6], [7].

Assuming DEM, offset cancellation, and curvature correction techniques are applied to eliminate mismatch-, offset-, and curvature-related errors, the sensor's dominant source of errors is the processing spread of V_{BE} (indicated by the shaded area in Fig. 3). This spread is reflected in the spread of V_{REF}, and hence in a device-to-device spread of the sensor's output. For a given device, this results in a systematic error that can amount to several degrees.

The spread of V_{BE} is mainly caused by variations in the saturation current of the bipolar transistor Q_3, and by variations in the nominal value of its bias current I_{trim}. Both can be traced back to the inevitable doping variations present in any low-cost CMOS process. Since the extrapolated value of V_{BE} at 0K, V_{BE0}, is essentially independent of these variations, only the slope of V_{BE} changes [8]. Therefore, the resulting temperature error has only one degree of freedom.

In our design [1], this error is corrected for by adjusting I_{trim} (Fig. 1) based on a room temperature calibration against a precision platinum thermometer. Thus, errors of less than $\pm0.1°\mathrm{C}$ over the military temperature range are obtained, confirming the validity of the assumption that the effect of V_{BE} spread on V_{REF} is the dominant source of error in the $0.7\mu\mathrm{m}$ CMOS technology used. This level of accuracy was maintained for a low-power version of the sensor [9], and even for a design using similar techniques in a state-

of-the-art $65\mathrm{nm}$ CMOS process [10], demonstrating that the assumption remains valid for different processing runs and different processes.

III. Conventional Calibration Techniques

Smart temperature sensors are usually calibrated by comparing them with a reference thermometer of known accuracy. To save production costs, this is typically done at only one temperature. The difference between a reading of the sensor and that of the reference thermometer is taken as an estimate of the measurement error of the sensor at the calibration temperature. The sensor is then trimmed to correct for this error, in our case by adjusting I_{trim} (Fig. 1). After this trimming procedure, no further corrections are applied to the sensor's readings by the user.

The required calibration procedure can be performed either at wafer-level, or after packaging. When calibrating at wafer-level, the temperature of a complete wafer, which may contain thousands of sensors, is stabilized and measured using a number of reference thermometers (e.g. thermistors or platinum resistors) mounted in the wafer chuck. A wafer prober then steps over the wafer, making contact to the bondpads of each of the sensor chips. It usually performs some electrical tests, takes a temperature reading from the chip, and trims the sensor to adjust its reading. The time required to stabilize the temperature of the whole wafer may be significant, but it is shared by many sensors.

An important limitation of wafer-level calibration lies in the fact that the subsequent dicing and packaging can introduce temperature errors (referred to as 'packaging shift'), which are mainly due to mechanical stress [11], [12]. When a chip is packaged in plastic without a stress-relieving cover layer, packaging shifts of up to $\pm 0.5°\mathrm{C}$ can occur, even when relatively stress-insensitive substrate pnp transistors are used [12]. Therefore, calibration and trimming have to take place after packaging if high accuracy is to be combined with low-cost packaging.

Calibration after packaging requires that every individual packaged sensor is brought to the same temperature as a reference thermometer. This typically means that the two are brought in good thermal contact by means of a thermally conducting medium, such as a liquid bath or a metal block [13], [14]. Some stabilization time will be needed, since the sensor will not be at the desired temperature when it enters the calibration setup. For uncertainties in the order of $\pm 0.1°\mathrm{C}$, this time will be much longer (more than ten minutes) than the time spent on electrical tests (seconds). Unlike the case of wafer-level calibration, however, the costs associated with this long stabilization time are now associated with a single sensor, or are at most shared by a small number of sensors calibrated together, and thus dominate the total production costs.

The techniques presented in the following sections can be used to calibrate individual sensors after packaging without the high costs associated with accurate temperature measurements.

IV. Calibration Based on ΔV_{BE} Measurement

The first alternative calibration technique is illustrated in Fig. 4. During calibration, an external voltmeter measures

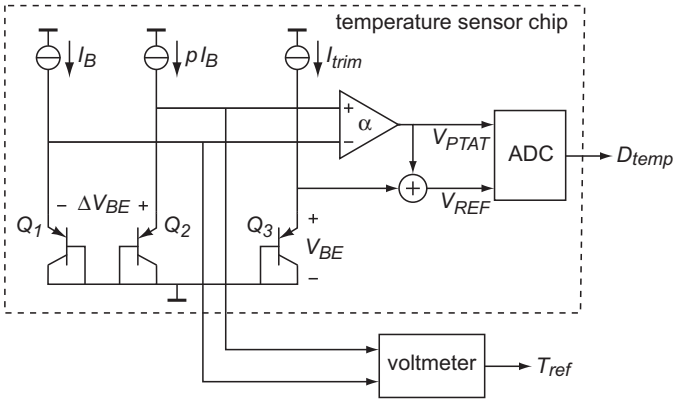

Fig. 4. Calibration by deriving the sensor's temperature from ΔV_{BE} measured using an external voltmeter.

ΔV_{BE} via two test pins. Given the intrinsic accuracy of ΔV_{BE}, the sensor's actual temperature can be accurately calculated from this measurement, and compared to the output of the sensor. The bias current I_{trim} is then adjusted to make the sensor's output equal to the calculated temperature.

Thus, the on-chip voltage reference is indirectly calibrated against that of the voltmeter. Temperature stabilization is no longer required, reducing the calibration time to that needed for the voltage measurement.

The accuracy that can be achieved with this calibration technique depends on a number of factors. First of all, it depends on how intrinsically accurate ΔV_{BE} really is, i.e. how much uncertainty is associated with eq. (1). This is determined, among other things, by the reverse Early effect, which introduces a multiplicative error in ΔV_{BE} [15], and modifies eq. (1) as follows:

$$\Delta V_{BE} = n\frac{kT}{q}\ln(p) \tag{5}$$

where the non-ideality factor n (which is also referred to as the effective emission coefficient) is assumed to be a process-dependent constant close to 1. Depending on the bias current levels used, the accuracy of ΔV_{BE} can also be affected by errors due to parasitic resistances in series with the base-emitter junction.

Results presented in [3] and [15] indicate that an uncertainty of $\pm 0.1°\mathrm{C}$ is feasible in spite of these errors. This does require, however, that the uncertainty in the on-chip $1:p$ current ratio be less than $\pm 0.01\%$. This can be achieved by dynamically matching the current sources and taking the average of the resulting ΔV_{BE} measurements (see Fig. 2).

The accuracy of the calibration is obviously also affected by the uncertainty due to the external voltmeter. With a typical sensitivity of ΔV_{BE} in the order of $100\mu\mathrm{V}/°\mathrm{C}$, this uncertainty has to be in the order of $\pm 10\mu\mathrm{V}$ to make the resulting temperature errors negligible, i.e. in the order of $\pm 0.1°\mathrm{C}$. This may be hard to implement in a noisy production environment.

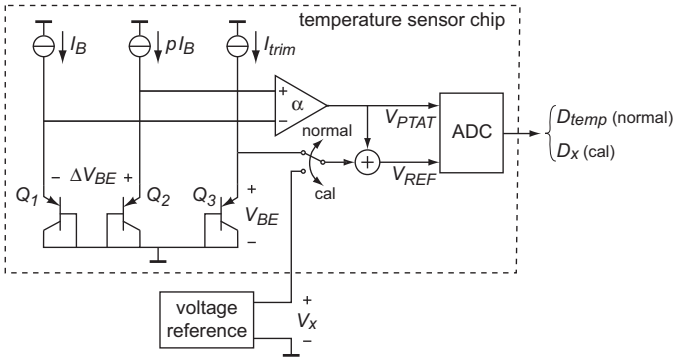

Fig. 5. Calibration by replacing V_{BE} by an external reference voltage V_x and deriving the sensor's temperature from the resulting output D_x.

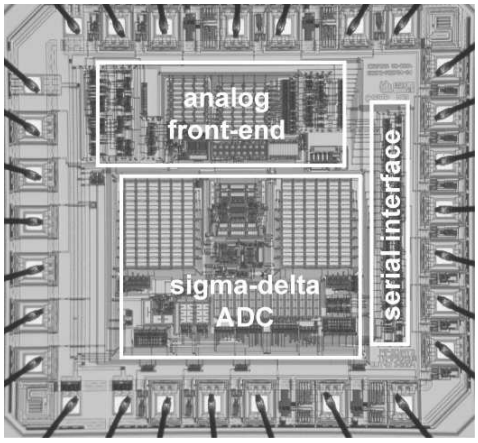

Fig. 6. Chip micrograph of the smart temperature sensor.

V. Calibration Based on an External Reference Voltage

A second calibration technique that does not require the accurate measurement of very small voltages is shown in Fig. 5. In a test mode, V_{BE} is replaced by an external reference voltage V_x. This voltage is nominally equal to V_{BE}, i.e. about $600\mathrm{mV}$, and is applied to the chip via a test pin. The resulting digital output of the sensor is then:

$$D_x = \frac{\alpha \Delta V_{BE}}{V_x + \alpha \Delta V_{BE}} \tag{6}$$

Since V_x is a known voltage, ΔV_{BE}, and hence the chip's temperature, can be calculated from this result. After that, I_{trim} is adjusted, as before, to null the error of the sensor. Implementation of this voltage reference calibration technique in a production environment is much easier than calibration based on ΔV_{BE} measurement, because a much larger uncertainty, in the order of $\pm 0.2\mathrm{mV}$ for $\pm 0.1°\mathrm{C}$ errors, is allowed in the external reference voltage. Moreover, the measurement is less sensitive to interference, because V_x can be generated by a low-impedance voltage source.

The accuracy of the calibration not only depends on accuracy the of V_x, but also on the intrinsic accuracy of ΔV_{BE}, and on the accuracy with which the sensor implements the transfer function given in eq. (6). The factors that limit the accuracy of ΔV_{BE} are the same as those discussed in section IV, while the accuracy of the transfer function depends on the accuracy of the ADC. Precision techniques such as dynamic offset cancellation and dynamic element matching will have to be applied to make the uncertainty due to the ADC negligible. In our precision temperature sensor, these techniques are already used to guarantee its accuracy over the military range after a single room-temperature trim [1].

VI. Experimental Results

A. Sensor Prototype

We have applied both a conventional calibration, as well as the two new calibration techniques to 24 samples of our smart temperature sensor. These sensors were fabricated in a $0.7\mu\mathrm{m}$ CMOS process and measure $4.5\mathrm{mm}^2$. They were mounted in 24-pin ceramic DIL packages.

A chip micrograph of the sensor is shown in Fig. 6. It consists of an analog front-end, which contains the substrate bipolar transistors and their biasing circuitry, a second-order sigma-delta ADC, and a serial digital interface. Dynamic element matching has been applied in the front-end to generate an accurate $1:5$ current ratio for generating ΔV_{BE}. In the switched-capacitor sigma-delta modulator, ratioed sampling capacitors are used to implement the amplification factor α. To obtain an accurately reproducible ratio, these capacitors are dynamically matched as well. Offset errors in the modulator are eliminated by a combination of correlated double sampling and chopping [1].

B. Calibration Against a Pt-100 Thermometer

Before applying the new calibration techniques, we calibrated 24 samples of our prototype using a conventional calibration procedure. A setup similar to the one described in [14] was used. The samples were mounted four at a time within a small cavity inside a large aluminum isothermal block. Two Pt-100 reference sensors were mounted in holes in the block, such that they were positioned just below the surface of the cavity. These sensors were calibrated with an standard uncertainty of $\pm 0.01°\mathrm{C}$ at the Dutch Metrology Institute NMI. Their resistance was measured using a Keithley 2002 multimeter, whose maximum measurement error of $\pm 3.3\mathrm{m}\Omega$ translates into a standard uncertainty of $\pm 0.005°\mathrm{C}$.

The aluminum block, in turn, was placed in a climate chamber at a temperature of $30°\mathrm{C}$. To ensure stability of the temperature in the block, the readings of the Pt-100 sensors were monitored in an automated setup until their variation as a function of time was less than $0.01°\mathrm{C}/\mathrm{min}$. When this condition was met, the difference between their readings, which is an indication of the unformity of the temperature in the block, was less than $\pm 0.01°\mathrm{C}$. The average of the Pt-100 readings was then taken as an estimate of the actual temperature of the devices under calibration, with an estimated combined standard uncertainty of $\pm 0.02°\mathrm{C}$.

The devices under calibration were then trimmed so as to null the difference between their readings and that of the Pt-100 sensors. This trimming consisted of adjusting the current

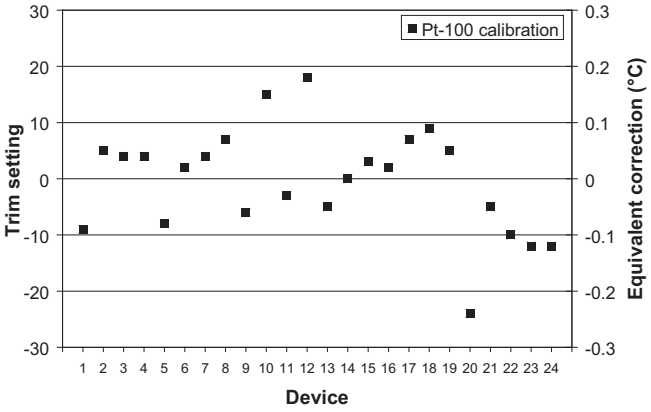

Fig. 7. Trim settings (and equivalent corrections) obtained by means of calibration against a Pt-100 reference thermometer.

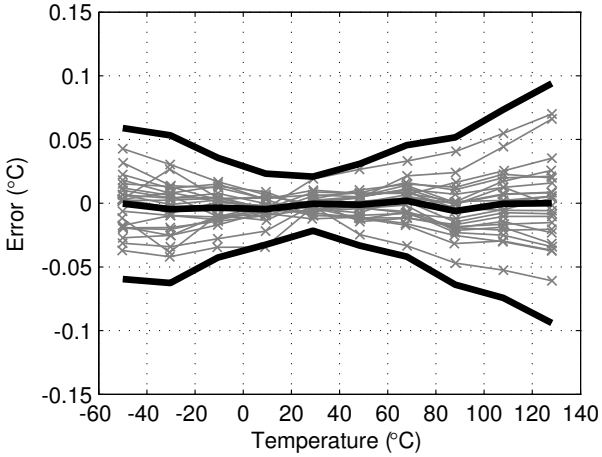

Fig. 8. Measured temperature error of 24 devices after trimming based on calibration using a Pt100 reference thermometer (bold lines indicate average and $\pm 3\sigma$ limits).

I_{trim} using the trimming technique described in [16], the digital part of which is implemented in an off-chip microcontroller so that the sensors can easily be re-trimmed based on the results of the other calibration techniques. The step size with which I_{trim} can be adjusted corresponds to a correction resolution of $0.01°$C. The standard uncertainty as a result of this finite resolution amounts to $\pm 0.003°$C. Fig. 7 shows the trim settings thus obtained for each of the 24 devices, along with the equivalent correction in °C.

After trimming, the measurement errors of the devices as a function of temperature were determined by means of a second comparison against the Pt-100 sensors. The temperature of the climate chamber was swept from $-55°$C to $125°$C in steps of $20°$C. For each temperature step, the same stabilization and measurement procedure was applied as described before. Fig. 8 shows the resulting measured temperature errors, with bold lines showing the average error, and the error interval with a coverage factor of 3 (i.e. three times the standard deviation around the average), which is associated with a level of confidence of 99.5%. This error interval is within $\pm 0.1°$C over the full range.

C. Calibration Based on ΔV_{BE} Measurement

Compared to the conventional calibration procedure described above, the new calibration techniques reduce the calibration time per sensor from more than 10 minutes to only a few seconds. This large improvement arises from the fact that a thermally-stable calibration environment is no longer needed.

In the case of ΔV_{BE}-based calibration, an estimate of the temperature of the device under calibration is obtained from a measurement of the difference in base-emitter voltages ΔV_{BE} of the bipolar transistors in the device's analog front-end (Fig. 4). This difference was measured using a Keithley 2002 multimeter, whose maximum voltage measurement error of $\pm 2.7\mu$V translates into a standard uncertainty of $\pm 0.011°$C. Several voltage measurements were averaged, corresponding to the dynamic element matching steps required to eliminate errors due to mismatch in the on-chip bias current sources, as described in Section II.

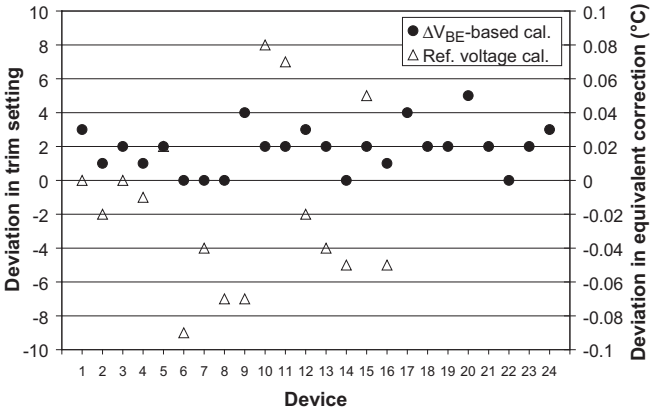

Fig. 9. Difference between trim settings (and equivalent corrections) obtained by means of the proposed calibration techniques and those obtained by means of calibration against a Pt-100 reference thermometer.

The devices were then, as before, trimmed to null the difference between their reading and their estimated temperature. So as to prevent temperature variations from affecting this procedure, the estimated temperature was compared to the average of a reading taken just before and one taken just after the ΔV_{BE} measurements.

Fig. 9 shows the difference between the trim settings thus obtained and those obtained using the calibration against a Pt-100 thermometer, along with the equivalent difference in correction in °C. The average of this difference is 1.9 trim steps (or $0.019°$C), and its standard deviation is 1.4 trim steps (or $0.014°$C).

The systematic difference can be attributed to second-order effects in the temperature dependency of ΔV_{BE} (see Section IV), most likely to an error in the estimate of the non-ideality factor n in eq. (5). Currently, the uncertainty in this factor, for instance due to batch-to-batch variations, is not yet known.

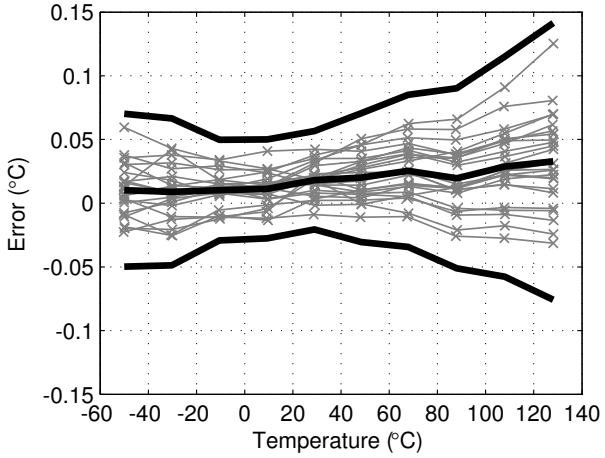

Fig. 10. Measured temperature error of 24 devices after trimming based on calibration using ΔV_{BE} measurement (bold lines indicate average and $\pm 3\sigma$ limits).

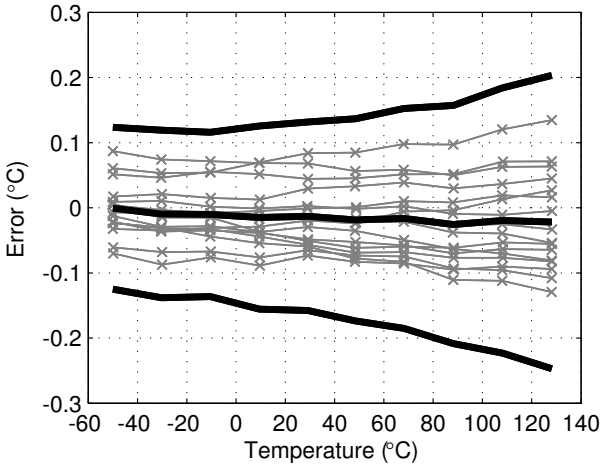

Fig. 11. Measured temperature error of 16 devices after voltage reference calibration (bold lines indicate average and $\pm 3\sigma$ limits).

Experimental results from several production batches will be needed to gather more information about this.

The compatibility between the two calibration techniques can be quantified by checking whether the differences in correction fall within the interval defined by the expanded uncertainty associated with the calibration techniques [14]. Taking the uncertainty of $\pm 0.011°\mathrm{C}$ due to the voltage measurement as an (optimistic) estimate of the standard uncertainty associated with the ΔV_{BE}-based calibration, and combining this with the standard uncertainty of $\pm 0.02°\mathrm{C}$ of the Pt-100-based calibration, gives a combined standard uncertainty of $\pm 0.023°\mathrm{C}$. Using a coverage factor of 2, 95% of the differences in correction should fall within the interval $\pm 0.046°\mathrm{C}$ if the calibrations are compatible. The results in Fig. 9 confirm that this is indeed the case.

After trimming, the measurement errors of the devices were determined by means of a comparison against the Pt-100 sensors, using the same procedure as before (Fig. 10). The ΔV_{BE}-based calibration and trimming introduced a small systematic error, which corresponds to the systematic difference in trim setting, as well as a slight increase in the device-to-device variation compared to the errors measured after the Pt-100-based calibration and trimming, leading to a $\pm 3\sigma$ error interval of less than $\pm 0.15°\mathrm{C}$ over the full temperature range.

D. Calibration Based on an External Reference Voltage

Finally, a calibration based on an external reference voltage was applied to 16 of the devices. An estimate of the temperature of the device under calibration was obtained by applying an external reference voltage of $600\mathrm{mV}$ to the chip, calculating ΔV_{BE} from the ADC's output D_x using eq. (6), and then calculating the temperature, as before, using eq. (5). The reference voltage was generated using a Keithley 2400 Sourcemeter, and measured back using a Keithley 2002 multimeter, whose maximum error of $\pm 9.7\mu\mathrm{V}$ translates into a standard uncertainty of $\pm 0.003°\mathrm{C}$.

As before, the devices were then trimmed based on this estimated temperature. As shown in Fig. 9, the trim settings thus obtained deviate more from those obtained using the Pt-100-based calibration than in the case of ΔV_{BE}-based calibration, with an average difference of -1.5 trim steps (or $-0.015°\mathrm{C}$), and a standard deviation of 5.0 trim steps (or $0.05°\mathrm{C}$).

These larger differences clearly cannot be accounted for based on the uncertainty due to the reference voltage only. An additional, more significant source of uncertainty was indentified in the ADC: a small parasitic interconnect capacitance introduced a gain error in eq. (6) that is not eliminated by dynamic element matching. Since this is a layout issue that can be solved, we expect that, in principle, the compatibility with the Pt-100-based calibration can be improved substantially in a re-design.

The larger differences in trim settings are reflected in larger measurement errors after trimming (Fig. 11), which were determined, as before, by means of a comparison over temperature against the Pt-100 sensors. In spite of the increased the device-to-device variation in the error, which leads to a $\pm 3\sigma$ error interval of around $\pm 0.25°\mathrm{C}$ at the high end of the temperature range, the errors still compare favorably to those of most commercial smart temperature sensors.

VII. Traceability

An important goal of a calibration procedure is to obtain information about how measurements made using a sensor relate to the 'standard' definition of the quantity being measured. That is, measurement results obtained from a properly calibrated sensor are *traceable*: they can be related to appropriate standards, generally international or national standards, through an unbroken chain of comparisons. In the case of a smart temperature sensor calibrated by means of a conventional comparison to a reference thermometer, this thermometer is the first step in a calibration hierarchy. A second step could be, for instance, the working standard in a calibration laboratory to which the reference thermometer was calibrated. This working standard, in turn, can be traced back via a number of further steps to the fixed points and

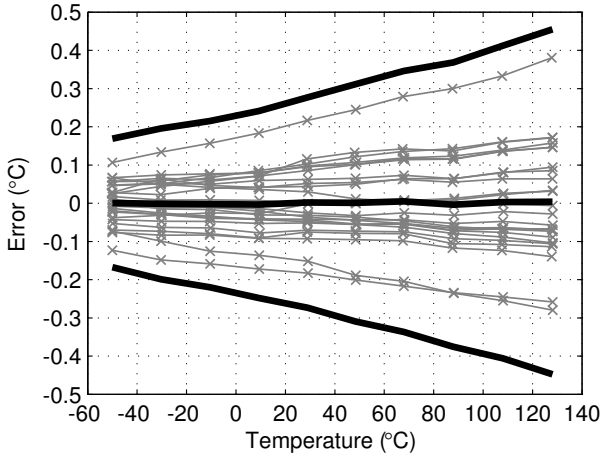

Fig. 12. Measured device-to-device variation in the temperature error of 24 uncalibrated devices from one production batch (bold lines indicate average and $\pm 3\sigma$ limits).

interpolation standards of the International Temperature Scale [13].

A problem of the calibration techniques presented in this paper is that they don't provide such traceability. As mentioned before, they essentially calibrate the internal voltage reference of a sensor under calibration, and thus provide at most traceability for this voltage reference, but not for temperature measurements performed with the sensor.

Such temperature traceability, however, can still be obtained in an *indirect* way. This would involve calibrating a small number of sensors from a production batch or a production process in the conventional way, even if the other sensors are calibrated using the proposed low-cost calibration techniques. This is done to characterize or monitor the performance and statistics of the production process. Assuming that the device-to-device variation between the sensors from a given production batch or process is limited, the calibration results of this limited number of samples are also applicable to the other sensors from the same batch or process, albeit with additional uncertainty due to the presence of device-to-device variation. Thus, the calibration results of these samples provide indirect traceability for all sensors.

The merit of the proposed voltage calibration techniques is that they provide, at very low cost, a substantial reduction in the uncertainty due to device-to-device variation, through calibration and trimming of the internal voltage reference. Fig. 12 shows the (untrimmed) device-to-device variation for our prototype, which corresponds to an error interval ($\pm 3\sigma$) of about $\pm 0.5°\text{C}$ over the military temperature range. The errors shown in the previous section are a factor of two smaller in the case of calibration based on an external reference voltage, and more than a factor of three smaller in the case of calibration based on ΔV_{BE} measurement.

Incidentally, the lack of direct traceability is not unique to the proposed voltage calibration techniques. For instance, conventional temperature calibration performed at wafer level, as is commonly done for commercial smart temperature sensors, does not provide direct traceability either. This is because the calibration procedure is performed before dicing and packaging, and therefore does not take the errors introduced by these production steps into account (the socalled packaging shift). Any statement regarding the accuracy of the final packaged sensors will be based on a combination of the calibration results and the uncertainty due to the packaging shift. Similarly, statements regarding the accuracy of sensors calibrated using the proposed voltage calibration techniques will be based on the results of temperature calibration of samples from a production batch and the known uncertainty (based on statistics) of the device-to-device variation after voltage calibration.

TABLE I
PERFORMANCE SUMMARY

Technology	0.7μm 2M-1P analog CMOS
Chip size	4.5mm^2
Supply voltage	2.5V – 5.5V
Supply current	75μA when operated continuously
Temperature range	$-55°\text{C}$ – $125°\text{C}$
Resolution	$0.01°\text{C}$ at 10 conversions/s $0.002°\text{C}$ at 1 conversion/s
Error interval ($\pm 3\sigma$)	$\pm 0.1°\text{C}$ trimmed based on Pt100 calibration $\pm 0.15°\text{C}$ trimmed based on ΔV_{BE} meas. $\pm 0.25°\text{C}$ trimmed based on ext. voltage ref. cal. $\pm 0.5°\text{C}$ untrimmed intra-batch variation

VIII. CONCLUSIONS

We have presented two calibration techniques for smart temperature sensors that are based on voltage measurements rather than on temperature measurements. These techniques significantly reduce the time needed for calibration, a major cost factor in the production of such sensors.

Experimental results from a prototype sensor, summarized in Table I, show that the first technique, direct measurement of ΔV_{BE} to determine the sensor's temperature during calibration, results in errors after calibration and trimming of $\pm 0.15°\text{C}$ ($\pm 3\sigma$) over the temperature range from $-55°\text{C}$ to $125°\text{C}$, only slightly larger than the errors of $\pm 0.1°\text{C}$ obtained with a conventional calibration against a Pt-100 thermometer. However, as a result of the small voltages involved, the implementation of this technique in a production environment may be difficult.

The second technique solves this problem by applying a larger external reference voltage to the chip during calibration. The chip's temperature is then determined by measuring ΔV_{BE} indirectly via the chip's ADC. A disadvantage of this approach is that any errors introduced by the ADC increase the uncertainty of the calibration. After calibration and trimming, we measured temperature errors of $\pm 0.25°\text{C}$ ($\pm 3\sigma$) over the temperature range from $-55°\text{C}$ to $125°\text{C}$. Even though this value is larger than that obtained with the first calibration technique, it still compares favorably with the specifications of current commercial temperature sensors [1], implying that this technique is suitable for production calibration of such sensors.

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