Towards a Full-Flexible and Fast-Prototyping TOF-PET Block Detector Based on TDC-on-FPGA

Venialgo Araujo, Esteban; Lusardi, Nicola; Garzetti, Fabio; Geraci, Angelo; Brunner, Stefan; Schaart, Dennis; Charbon, Edoardo

DOI
10.1109/TRPMS.2018.2874358

Publication date
2018

Document Version
Accepted author manuscript

Published in
IEEE Transactions on Radiation and Plasma Medical Sciences

Citation (APA)

Important note
To cite this publication, please use the final published version (if applicable). Please check the document version above.

Copyright
Other than for strictly personal use, it is not permitted to download, forward or distribute the text or part of it, without the consent of the author(s) and/or copyright holder(s), unless the work is under an open content license such as Creative Commons.

Takedown policy
Please contact us and provide details if you believe this document breaches copyrights. We will remove access to the work immediately and investigate your claim.
Towards a Full-Flexible and Fast-Prototyping TOF-PET Block Detector Based on TDC-on-FPGA

Esteban Venialgo, Nicola Lusardi, Fabio Garzetti, Angelo Geraci, Stefan E Brunner, Dennis R Schaart, and Edoardo Charbon

Abstract—Typically, a time-of-flight (TOF) PET block detector is built using application-specific integrated circuits (ASICs), since they integrate a high number of channels at a reasonable power consumption and into a small area. However, ASICs’ flexibility is limited and prototyping times are long because a semiconductor fabrication process is required in every design iteration.

Alternatively, fast terminal (FT) silicon photomultipliers (SiPMs) require a simplified analog front-end in order to achieve time-of-flight (TOF) accuracy. In addition, field-programmable gate arrays (FPGAs) can allocate time-to-digital converters (TDCs) as well as complex digital readout logics.

In this work, we propose building TOF-PET block detectors based on FPGAs, FT-SiPMs, and minimal amount of off-the-shelf components. In this way, TOF-PET accuracy is achieved with a full-flexible and fast prototyping solution. We evaluated the coincidence resolving time (CRT), performance degradations due to channel multiplexing, energy resolution, and scintillator pixel encoding performance of SiPM arrays utilizing the proposed approach. Experimental results show minimal timing degradations, when multiplexing FTs. Moreover, simulation results show a low reduction in the singles count rate of multiplexed channels at typical brain-PET radioactive doses.

I. INTRODUCTION

Since the introduction of the PET block detector in the 1980s, it was possible to build PET scanners in a modular approach [1]. One advantage of breaking out the detection area into many independent block detectors was the drastic increase in the count rate capability of the PET scanner [2], [3].

With the advent of time-of-flight (TOF) PET and PET/MRI imaging modalities, new technologies were introduced, e.g. silicon photomultipliers (SiPMs), in order to fulfill the new requirements, such as high timing resolution and magnetic field insensitivity. In addition to SiPMs, ASIC development appeared as a solution that integrates even more independent channels per PET block detector up to a single channel per scintillator pixel [4], [5]. This solution avoids utilizing scintillator pixel encoding circuits, which are usually difficult to calibrate on the edge of the block detector, and additionally allows to further increase the singles count rate. However, the main disadvantages of the ASIC approach are the lack of flexibility and long development and testing cycles.

1. Experimental setup description. (a) Obtained simulated energy spectrum (the energy resolution was set to 20% at 511 keV).

More recently, digital SiPMs appeared as an alternative photodetector utilized in combination with scintillators for gamma photon detection in PET [6]–[8]. These types of sensor
Fig. 2: Single count rate comparison for several channel multiplexing configurations and channel dead times. (a) Absolute single count rate with a channel dead time of 10 μs. (b) Absolute single count rate with a channel dead time of 1 μs. (c) Normalized singles count rate relative to the 64 channel case, with a channel dead time of 10 μs. (d) Normalized singles count rate relative to the 64 channel case, with a channel dead time of 1 μs.

represent a further step into system integration and ASIC development, since they integrate single-photon avalanche diode (SPAD) cells along with a comprehensive readout circuit into the same die. In addition, the analog readout is entirely removed by exploiting the intrinsic digital nature of SPADs when detecting light. Once the sensor is developed, it allows a direct system integration; however, its main drawbacks are the even longer development and testing cycles due to their high complexity.

In order to obtain accurate timing information from an analog SiPM, which features a relatively large output capacitance, specialized shaping circuits are required in order to keep a fast signal rise time. However, since the introduction of the fast terminal (FT) by SensL, a fast signal can be obtained without any specialized circuits [9]. Because the FT is integrated into the SiPM, the analog readout circuit can be simplified by removing the timing shaping circuits entirely and reducing it to few off-the-shelf components.

In PET instrumentation, time-to-digital converters (TDCs) replaced free-running fast sampling analog-to-digital converters (ADCs) for timestamping gamma-photon events [10]. Field-programmable gate arrays (FPGAs) can allocate TDCs as well as digital readout and interfacing logic in order to build a PET block detector. As an added benefit, FPGAs can be reprogrammed at any point in time of the development cycle in order to add or fix PET detector functionalities [11], [12].

In this work, we performed a series of experiments in order to demonstrate that fully-flexible and fast-prototyping TOF-PET block detectors can be built directly from off-the-shelf components without ASIC development. The prototype circuits are based on TDC-on-FPGA, off-the-shelf components, and FT J-series SiPMs from SensL [13]–[15].

II. SINGLE COUNT RATE AND CHANNEL MULTIPLEXING

When designing a PET scanner, the noise equivalent count rate (NECR) and the sensitivity are among the most important parameters under consideration [2], [3]. The NECR is reduced mainly by three factors: detector dead time, unrejected scatter events, and random coincidences.

The amount of unrejected random coincidences depends on the single count rate and the coincidence-window width. If the system-level coincidence resolving time (CRT) is smaller than the field-of-view (FOV) diameter in terms of time distance, which is 833 ps for a 250 mm diameter, the coincidence-window width is limited by the FOV diameter. Additionally, the coincidence-window width is extended beyond the FOV in terms of time by a factor that depends on the scanner
CRT, in order not to suppress valid events due to the timing measurement uncertainty.

The unrejected scattered events depend on energy resolution. Finally, the NECR sensitivity can be reduced significantly, depending on the injected radioactivity, which moreover depends on the specific PET application.

Incrementing the number of channels by subdividing the detector area into blocks drastically improves the NECR [2], [3]. However, implementing several channels within the same PET block detector might not increase the NECR significantly, because it also depends on the the injected radioactive dose and scanner geometry.

We performed a GATE/Geant4 simulation in order to study the impact of the channel multiplexing on the single count rate of a PET block detector [16]. We considered a brain-PET block detector case, which is described in Fig. 1a, because this application requires high NECR and sensitivity [17], [18].

For the simulation, a cylindrical phantom, which is 250 mm in diameter and 150 mm in length, was filled with $^{18}$F and water. The phantom radioactivity was varied from 0.1 to 1000 MBq. A PET block detector composed of $8 \times 8$ LYSO pixels of 3 mm pitch and 20 mm depth was simulated. In order to simulate a scanner inner bore diameter of 350 mm, the inner face of the PET block detector was placed 50 mm away from the external side of the cylindrical phantom. The obtained energy spectrum is depicted in Fig. 1b. In all the simulations, an energy resolution of 20% at 511 keV was assumed based on previous works [17].

For calculating the single count rate, all of the detected events were considered singles, as an example of extreme conditions for the instrumentation, without filtering events by an energy window.

In PET instrumentation, after detecting a gamma event an energy discrimination is applied in order to immediately discard Compton scattered gamma photons. For instance, if we select a low threshold of the energy-window around 300 keV, gamma events that generate multiple hits from Compton scattering within the scintillators and the energy of any individual hits lower than 300 keV are rejected. As a consequence, about 14 % of the events with inter-crystal scatter were rejected (see Fig. 1b). Therefore, in order to accept events with multiple hits, the PET detector module must be capable of detecting individual hits and combine them as a single gamma event.

As mentioned, the detector was composed of 64 LYSO pixels and we analyzed the single count rate for several scintillator pixel multiplexing cases (see Figs. 2a to 2d). In the following analysis, 64 channels refer to one independent measurement channel per LYSO pixel. Conversely, one channel means that the 64 LYSO pixels share a single measurement channel. We considered that the detector is composed of TDCs for gamma-photon timestamping and energy estimation [10]. Additionally, we assumed that the dominant dead time of the system is the time-of-conversion of the TDCs, which can be modeled as non-paralyzable. Furthermore, we chose 1 µs dead time as a reasonable time-of- conversion that can be achieved by a TDC on FPGA and 10 µs as a worse-case comparison point [10].

Figs. 2a and 2b show the absolute count rate of single events when sweeping the phantom activity for the 10 and 1 µs channel dead time cases, respectively. In addition, we calculated the relative singles count rate normalized with respect to the optimum case, which is 64 channels. Figs. 2c and 2d depict the relative singles count rate for the 10 and 1 µs channel dead time cases, respectively.

In previously reported injected doses utilized in brain-PET imaging, which were around 400 MBq, we observed a relative count rate loss of about 55 % and 12 % for the 10 and 1 µs channel dead time cases, respectively, in the case of 8 channels (see Figs. 2c and 2d) [17]. Therefore, we concluded that a reasonable number of channels per PET block detector is 8, if the channel dead time is 1µs, since the decrease in efficiency of the single count rate is low with respect to having 64 independent channels. An additional argument to favor 8 channels is that a row-wise readout circuitry can be implemented when choosing a $8 \times 8$ SiPM array, in order to achieve 8 independent measurement channels, as it is shown in the following sections.

III. TIMING RESOLUTION AND CHANNEL MULTIPLEXING

Previously, we demonstrated that state-of-the-art CRT can be achieved by PET detectors composed of TDC-on-FPGA and SiPMs equipped with FTs [10]. The case of having one timing channel per LYSO pixel requires many TDCs integrated on the FPGA. Additionally, an extensive analog front-end, which consumes a significant amount of power, is needed. To achieve a fully-flexible ASIC-less design channel multiplexing is necessary, in order to reduce power consumption and FPGA implementation complexity. We studied the timing impact of sharing the same measurement channel among several SiPM FTs. In all of the experiments presented in this work, which were performed at room temperature, the bias voltage of the SiPMs was 30 V. The utilized J-series SiPMs are characterized by a minimum and maximum breakdown voltage of 24.2 V and 24.7 V at 21°C, respectively [19].

A. Reference detector characterization

Firstly, we calibrated our reference detector that was composed of a SensL single SiPM evaluation board of a J-series 3 mm SiPM. We performed a coincidence measurement with two identical detectors in order to estimate the single detector resolution (SDR) (see Fig. 3), $3 \times 3 \times 5$ mm$^3$ LSO:Ce scintillators from Agile were glued on top of the SiPMs.

In comparison to our previous work [10], we utilized a newer version of the TDC on FPGA board that comprises an Artix7 system-on-module (SOM), digital-to-analog converters (DACs) for automatic threshold scanning, low-jitter comparators (ADCM607), and a high-speed USB 3.0 interface. This board, known as Panther, can allocate up to 16 TDC channels (see Figs. 4a 4b) [13]. The TDCs are implemented based on a tapped-delayed line (TDL) architecture achieving an LSB of 4.7 ps and a single-shot resolution of 12 ps $\sigma$ [14]. A full scale-range of 2.4 µs is obtained utilizing the mutt technique (see table 1) [15]. The total FPGA occupation per channel is 1200 SLICES, 54 kbit BRAM, and 1 DSP48E1. The 16 TDCs have a common stop signal connected to an internally
TABLE I: Panther board performance summary table.

<table>
<thead>
<tr>
<th>Feature</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of channels</td>
<td>16</td>
</tr>
<tr>
<td>Logic per channel</td>
<td>1200 Slices, 54kbit BRAM, 1 DSP48E1s</td>
</tr>
<tr>
<td>Channel latency</td>
<td>110 ns</td>
</tr>
<tr>
<td>Maximum channel rate</td>
<td>20 MHz</td>
</tr>
<tr>
<td>System-on-module</td>
<td>Artix7 Trenz</td>
</tr>
<tr>
<td>Single shot resolution</td>
<td>12 ps ($\sigma$)</td>
</tr>
<tr>
<td>full scale range</td>
<td>2.4 $\mu$s</td>
</tr>
</tbody>
</table>

generated clock, and the start signals are externally interfaced through a low-jitter comparator (see Fig. 4a).

We estimated the energy of the gamma event using the time-over-threshold (ToT) technique. For this reason, we connected two TDC channels per SiPM standard terminal (ST) in order to timestamp the falling and rising edges of the energy signal (see Fig. 3). The gamma-photon timemark estimation was performed by a single TDC connected to the FT after amplifying its signal with a metal-shielded case wideband amplifier of 30 dB gain and 2.5 GHz bandwidth (Minicircuits ZKL2R5).

As observed in Fig. 5c, we obtained a CRT of 122 ± 8.9 ps FWHM and the uncalibrated ToT spectra of both detectors are shown in Figs. 5a and 5b. In the latter measurements, we utilized one of these detectors as a reference with an SDR of 86.3 ps FWHM. The SDR is derived from the measured CRT of 122 ps by considering the two detectors with identical SDR.

B. Fast terminal multiplexing

Secondly, we built SiPM array test circuits in order to evaluate the impact of sharing FTs on the same TDC channel. The circuit was divided into three test structures: Single SiPM, row of SiPMs with Schottky diodes, and SiPM row without Schottky diodes (see Fig. 6).

In the first test structure, the single SiPM’s FT was connected to a surface-mount wideband amplifier (BGA2818) (see Figure 7). And, its ST was connected to a transimpedance amplifier (TIA) based on the OPA656 (see Figure 8). The single SiPM is the number 13 on the 4 $\times$ 4 SiPM array (see Figure 6). The hysteresis value ADCMP607 that connected the BGA2818 was kept as low as possible by removing its programming resistor, in order to achieve an accurate leading edge threshold.

In the second test structure, the FTs were connected in parallel through Schottky diodes in order to partially decouple their output capacitance (see Fig. 9) [20], [21]. In addition, an external bias voltage can be applied to the Schottky diodes that guarantees a faster signal transmission from the FTs to a second BGA2818 wideband amplifier [20], [21]. The STs were connected into a resistor divider chain, which is amplified by two additional TIAs, for scintillator pixel identification and energy estimation (see Figs. 8 and 10). The TIAs are called left and right amplifiers (see Fig. 10). This circuit connected the SiPMs 1, 2, 3, and 4 (see Figure 6 and 10).

The third test structure is similar to the second but the FTs were connected directly to a third wideband amplifier without any Schottky diodes. Also, two additional TIAs were connected in a second scintillator pixel encoding circuit (see Figure 6 and 10).
Firstly, we verified the performance of the single SiPM circuit in terms of timing, which is based on the BGA2818 instead of the bulky Minicircuits ZKL2R5. We attached a 3×3 mm$^3$ scintillator of LYSO Gen3 from Saint-Gobain to the SiPM 13 (see Figs. 6 and 11) and measured the CRT against the reference detector (see Figs. 12 and 11) [22]. In this measurement, only the single SiPM test circuit and reference detector signals were connected to the Panther board. The CRT threshold scan is depicted in Fig. 13 and no significant change was observed between the reference detector characterization and this measurement. We concluded that no timing degradation was detected between the timing channel based on the Minicircuits ZKL2R5 and that based on the BGA2818.

Secondly, we studied the timing resolution of the SiPM row that shares a single timing channel through Schottky diodes. This measurement was also performed against the reference detector. We connected the circuits of the corresponding SiPM row and the reference detector to the Panther board (see Fig. 6 and 4b). We attached the scintillator of 3×3 mm$^3$ scintillator of LYSO Gen3 to the SiPM 1 (see Figs. 6 and 11), aligned the reference detector, and disconnected the single SiPM test circuit (see Fig. 11). Consequently, in this SiPM row one out of four SiPMs has a scintillator; however, the four SiPMs of the row were biased and had the FTs connected. If non-uniformities, such as breakdown voltage variation, become significant, they can be compensated for by implementing an individual overvoltage-adjustment circuit based on ultra-low power DACs such as DAC088S085.

The minimum measured CRT was 128 ± 7.8 ps (see Fig. 14a) but at a lower threshold, which increases the sensitivity to threshold variations. The amplitude of the FT signal is slower in comparison to the single SiPM circuit because it is loaded with extra capacitance, which is partially decoupled by the
Schottky diodes, added by the row FTs. After subtracting the SDR of the reference detector in quadrature and assuming two identical detectors, we extrapolated a CRT* of 138 ps FWHM. In addition, we performed a Schottky bias scan at a fixed comparator threshold, which was 10 mV. The best of CRT performance was achieved when each Schottky diode was biased at 1.5 V, showing a current of 337 µA per diode (see Fig. 14b).

Last, we re-glued the 3×3×5 mm³ scintillator of LYSO Gen3 from the SiPM row with Schottky diodes to the SiPM row without Schottky diodes (SiPM 5). And, we reconnected the Panther board to that SiPM row. The result of the CRT threshold scan of this case is shown in Fig. 15. The measured CRT was 135 ± 10.3 ps and the extrapolated CRT* assuming identical detectors was 147 ps FWHM.

C. Timing signal waveforms

For comparing the output signals of the timing circuits, a source of ¹³⁷Cs was placed close to the detectors in order to obtain a maximum deposited energy of 662 keV, which is close to 511 keV. We re-glued the 3×3×5 mm³ scintillator of LYSO Gen3 onto the SiPMs 1, 5, and 13. An oscilloscope with 2.5 GS/s and 500MHz bandwidth was connected to the BGA2818 outputs. Since several amplitudes were measured from the detector, the oscilloscope’s trigger was set to the maximum measured amplitude.

Fig. 16 shows the captured waveforms of the array’s single SiPM amplified by the BGA2818 circuit and the reference detector amplified by the Minicircuits ZKL2R5. Although the gain of both amplifiers is the same, a lower amplitude is observed from the BGA2818 because of its lower saturated output power. Additionally, the saturated pulse is differentiated by the RC circuit created by the 50 Ω load and C₄ (see Fig. 7). However, accurate timing relies on the amplification of the beginning of the timing pulse, which is produced by the early photoelectrons, before reaching the saturated output power of the wideband amplifier [23].

Fig. 17 compares the captured waveforms of the three testing circuits of the SiPM array (SiPM row with Schottky diodes, SiPM row without Schottky diodes, and single SiPM). In addition, Fig. 18 compares the captured waveforms of the BGA2818 output that is connected to the Schottky row at several Schottky bias voltages. The difference of peak amplitudes was not observed between the SiPM rows with and without Schottky diodes. The tail length variations observed in Fig. 18 are related to the different speeds in which C₅ (in Fig. 9) is discharged that depends on the Schottky biasing.

D. LYSO pixel encoding

Since the TIAs’ output pulse polarity is negative, a DC voltage was added for connecting the TIAs to the Panther board (see Fig. 10), which required a positive input voltage. In order to test the scintillator pixel encoding circuit, the 3×3×5 mm³ LYSO Gen3 scintillator was glued on the SiPMs 1, 2, 3, and 4 (see Fig. 6). Then, we captured the corresponding
output waveforms of the left and right TIAs for each case, with an oscilloscope of 2 GS/s and 200MHz bandwidth.

Fig. 23 shows the captured waveforms and the ToT calculations that correspond to the left and right TIAs’ signals. In these experiments, we also utilized the $^{137}$Cs source and triggered the oscilloscope with the maximum amplitude of the FT. In a full PET module implementation, the DC voltage can be replaced by connecting STI$_N$ to the SiPM cathode, and biasing the anode to negative voltage. The DC voltage causes extra power consumption and $R_{dc}$ produces a slight impedance mismatch.

Additionally, we glued the $3\times3\times5$ mm$^3$ LYSO Gen3 scintillator on the SiPM 2, place the $^{22}$Na source close to the scintillator, and measured the time difference between $\text{ToT}_{\text{left}}$ and $\text{ToT}_{\text{right}}$ with the Panther board. The measured events were filtered by an energy window that captured the entire 511 keV photopeak. We also performed the same experiment on the SiPM 3 in order to verify the LYSO pixel identification. Fig. 21 shows the histograms that corresponds to the two previously explained experiments. Also, the falling edges of the right and left TIA pulses can be used for SiPM 3 and SiPM 2’s LYSO pixel identification, since in this architecture the individual fall and rising timestamps are available (see $t_{\text{fl}}$ and $t_{\text{fr}}$ in Figs. 23b and 23c).

### IV. Energy Resolution

In our previous work, we calculated the energy resolution of a PET detector composed of TDC-on-FPGA and J-series SiPMs [10]. We repeated a similar procedure but on the SiPM 1 (see Figs. 3 and 6). During the measurement the threshold level of the ADCMP607 was 800 mV, which did not allow...
to observe $^{241}$Am pulses (see Fig. 23). Therefore, the third calibration point was the 1274 keV photopeak of the $^{22}$Na source.

We calibrated the ToT values into gamma energy following two equations

\[ A_p = V_{th} \tau_d \exp\left(\frac{t_{tot}}{\tau_d}\right), \]  
\[ E_\gamma = -A_{p_{max}} \log\left(1 - \frac{A_p}{A_{p_{max}}} \right). \]

Equation (1) expresses the nonlinearity between area of the pulse and the measured ToT, assuming a single exponential SiPM output pulse. Equation (2) represents the SiPM cell saturation effect. In (1), $A_p$ is the area of ST pulse, $V_{th}$ is the threshold voltage of the comparator, $\tau_d$ is the single exponential decay constant, and $t_{tot}$ is the measured ToT. In (2), $E_\gamma$ is the absorbed gamma energy, and $A_{p_{max}}$ is the maximum pulse area (see Fig. 19). There are three unknown values, which are $V_{th}$, $\tau_d$, and $A_{p_{max}}$; therefore, we estimated them by measuring the spectra of three different photopeaks (see Figs. 20a and 20b). Later, we used the calibrated constant to convert the $t_{tot}$ values to its corresponding $E_\gamma$ by following (1) and (2). The calibrated spectra are shown in Fig. 20b were an energy resolution of 14 % is achieved. The ToT energy spectra of Fig. 20a have more dynamic range than Figs. 5a and 5b because the measurement was performed at a lower threshold.

**Fig. 17:** FTs captures of the SiPM 13, the Schottky row SiPM 1, and the non-Schottky row SiPM 5 amplified with BGA2818.

**Fig. 18:** FTs captures of the Schottky row SiPM 1 amplified with BGA2818 at several Schottky bias voltages.

**Fig. 19:** Energy calibration scheme.

**V. OUTLOOK**

We propose to use TDC-on-FPGA in combination with a simple analog front-end based on off-the-shelf components in order to build a PET block detector (see Figs. 22). The target application of this PET block detector is brain molecular imaging.

The detector is composed of an array of 8×8 SiPMs of 3 mm pitch and equipped with FTs. The board that allocates the SiPMs on the top layer is customized in order to host the small footprint Schottky diodes (SMS7621), in addition to small board-to-board connectors. The analog front-end allocates the fast comparators (ADCMP607), the wideband amplifiers (BGA2818), and the TIAs circuits based on the LT6230-10. The last board contains a small footprint FPGA (Artix7-100T-CSG324) and all the required circuitry to operate it.

The block detector has independent row circuitries, in order to realize 8 independent measurement channels. Each SiPM row also has a independent scintillator pixel encoding circuit that also improves the scintillator identification in order to avoid edge packing effects. The experimental results were measured with four SiPM FTs connected in parallel. However, in the proposed PET block detector, there are eight FTs per column. If the amplitude of the FTs is further reduced, this effect could be mitigated by choosing a wideband amplifier with a larger gain. The total number of required high-accuracy TDCs is 8 (for timing estimation) and the total number low resolution TDCs is 16 for ToT calculations.
A power consumption estimation is shown in Table II. In addition, Table II describes the required area of the components’ footprints relative to the detector size. Although we utilized the OPA656 as a transimpedance amplifier, we propose to use the LT6230-10 as a lower power consumption alternative. The Artix SOM expends 2.5 W when idle and around 4 W when the 16 TDC channels are operating at full capacity (see Table II). In addition, we included the comparator TLV320 for the scintillator pixel encoding and energy estimation ToT circuits because it has a lower power consumption than the ADCMP607 (see Table II). We kept the ADCMP607 for the timing channels because of its low jitter and programmable hysteresis feature.

The power consumption of a typical PET ASIC is about 25 mW per channel, which leads to a total power consumption of 1.6 W on the 64 channels [5]. In our design, we observe a power consumption, which is around 1 W for the analog front-end in addition to 2.5W-4W for the FPGA and all its required circuitry (see Table II). However, we also include an FPGA per block detector for data post-processing and communication [24]. Power consumption becomes critical in PET scanner implementations with reduced space for a cooling system, such as PET/MRI inserts [25]. Table III compares the proposed detector with respect to state-of-the-art ASICs for TOF-PET.

VI. CONCLUSIONS

We demonstrated that fully-flexible and fast prototyping TOF-PET block detectors can be built from off-the-shelf components, TDC-on-FPGA, and FT-SiPMs. We achieved a sub-120 ps CRT at a single SiPM level. A minimum degradation was observed when multiplexing the FTs with Schottky diodes. We obtained an energy resolution of 14 %, which is compatible for the targeted PET applications. In addition, we verified the LYSO pixel identification of a SiPM row composed of 4 elements.
Fig. 23: Oscilloscope captures of the scintillator pixel encoding circuit. Left and right transimpedance-amplifier outputs. (a) Scintillator glued on the SiPM 1 of the Schottky’s row. (b) Scintillator glued on the SiPM 2 of the Schottky’s row. (c) Scintillator glued on the SiPM 3 of the Schottky’s row. (d) Scintillator glued on the SiPM 4 of the Schottky’s row.

TABLE II: Detailed power consumption and area occupation description.

<table>
<thead>
<tr>
<th>Total devices</th>
<th>Power per device</th>
<th>Area per device</th>
<th>Total power</th>
<th>Total area</th>
</tr>
</thead>
<tbody>
<tr>
<td>BGA2818</td>
<td>8</td>
<td>65 mW</td>
<td>0.87 %</td>
<td>520 mW</td>
</tr>
<tr>
<td>OPA656</td>
<td>16</td>
<td>280 mW</td>
<td>1.01 %</td>
<td>4400 mW</td>
</tr>
<tr>
<td>LT6230-10</td>
<td>16</td>
<td>11 mW</td>
<td>1.56 %</td>
<td>176 mW</td>
</tr>
<tr>
<td>TLV320</td>
<td>16</td>
<td>1 &lt; mW</td>
<td>0.52 %</td>
<td>16 &lt; mW</td>
</tr>
<tr>
<td>ADCMP607</td>
<td>8</td>
<td>37.5 mW</td>
<td>1.56 %</td>
<td>300 mW</td>
</tr>
<tr>
<td>total analog power (a)</td>
<td>1</td>
<td>(2.54 \text{ W})</td>
<td>(40)</td>
<td>(2.54 \text{ W})</td>
</tr>
<tr>
<td>Artix7</td>
<td>1</td>
<td>(2.54 \text{ W})</td>
<td>(40)</td>
<td>(2.54 \text{ W})</td>
</tr>
</tbody>
</table>

\(a\) Power calculated with LT6230-10 instead of OPA656

TABLE III: ASICs for TOF-PET comparison table.

<table>
<thead>
<tr>
<th>Channels</th>
<th>Trigger</th>
<th>Hit Rate (per channel)</th>
<th>TDCs</th>
<th>Energy Estimation</th>
<th>Max. Throughput</th>
<th>Total Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>STiC3(c)</td>
<td>64</td>
<td>adjustable</td>
<td>40 kcps</td>
<td>50 ps LSB</td>
<td>ToT</td>
<td>160 Mbps</td>
</tr>
<tr>
<td>FlexTOT(b)</td>
<td>16</td>
<td>adjustable</td>
<td>&gt;1000 kcps</td>
<td>non-integrated</td>
<td>ToT</td>
<td>-</td>
</tr>
<tr>
<td>TOFPET2(c)</td>
<td>64</td>
<td>adjustable</td>
<td>600 kcps(^d)</td>
<td>31 ps LSB</td>
<td>ToT</td>
<td>3200 Mbps</td>
</tr>
<tr>
<td>Outlook design (f)</td>
<td>8</td>
<td>adjustable</td>
<td>&gt;1000 kcps</td>
<td>12 ps(^f)</td>
<td>ToT</td>
<td>3200 Mbps(^h)</td>
</tr>
</tbody>
</table>

\(a\) Values according to [5], [26].
\(b\) Values according to [27].
\(c\) Values according to [28].
\(d\) Simultaneous maximum rate in every channel is limited by the data throughput.
\(e\) This parameter depends on certain settings.
\(f\) It includes a scintillator pixel encoding circuit in order to allocate 64 SiPMs.
\(g\) The TDC’s single-shot resolution is specified as \(\sigma\).
\(h\) This parameter is limited by the FT600. It can be extended by using the GTP transceivers of the FPGA [24].
\(i\) The FPGA power consumption can be reduced further by optimizing the SOM circuitry (see table II).

The Schottky diode decoupling circuit avoids the signal amplitude reduction when connecting FTs in parallel. How-
ever, we did not observe a significant CRT degradation in the multiplexing circuit without Schottky diodes, which is 135 ± 10.3 ps FWHM with respect to the 128 ± 7.8 ps FWHM achieved without Schottky diodes.

We also concluded that the proposed block detector does not lose a significantly large amount of gamma events when the SiPM array shares the same measurement channel row-wise. This requires a measurement channel with a dead time of 1 μs, which it is already achieved by the Panther board.

REFERENCES


