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A 5800 μm² Resistor-based Temperature Sensor with a One-Point Trimmed Inaccuracy of ±1.2 °C (3σ) from −50 to 105 °C in 65 nm CMOS

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Abstract—This paper describes a compact resistor-based temperature sensor intended for the thermal monitoring of microprocessors and DRAMs. It consists of an RC poly-phase filter (PPF) that is read out by a frequency-locked loop (PLL) based on a dual zero-crossing (ZC) detection scheme. The sensor, fabricated in 65 nm CMOS, occupies 5800 μm² and achieves moderate accuracy (±1.2 °C (3σ) inaccuracy) over a wide temperature range (−50 to 105 °C) after a one-point trim. This is 2x better than previous compact resistor-based sensors. Operating from 0.85 to 1.3 V supplies, it consumes 32.5 μA and achieves 2.8 μm resolution in a 1 ms conversion time, which corresponds to a resolution FoM of 0.26 pJ·K².

Index Terms—CMOS temperature sensor, resistor-based temperature sensor, RC poly phase filter, frequency-locked loop (PLL), dual zero-crossing (ZC) detection, one-point trim.

I. INTRODUCTION

Compact temperature sensors are required for the thermal monitoring of microprocessors and DRAMs [1]-[4]. In microprocessors, they provide information about on-chip thermal gradients and hot spots, which helps to maintain performance and reliability [2]. In DRAMs, they control the self-refresh period, which, in turn, determines standby power [3]. To avoid wasting expensive die area, sensors intended for thermal monitoring in nanometer CMOS should be compact (< 0.01 mm²). They should also be fast enough (~1-ns conversion time) to track on-chip temperature gradients. Finally, to reduce calibration costs, they should only require a one-point trim to achieve moderate accuracy.

For thermal monitoring, resistor-based temperature sensors are attractive, because they can operate at low supply voltages and are highly energy efficient [4]-[8]. Of the available resistors in CMOS processes, silicided poly resistors are well suited for temperature sensing due to their relatively high temperature coefficient (TC ~ 0.3 %/K), low voltage dependency, and low 1/f noise [4]-[6]. In previous work, such resistors have been incorporated in Wheatstone bridges and read out by continuous-time ADCs, resulting in high energy-efficiency but large area (0.25 mm²) [6]. More compact sensors have been realized by incorporating resistors into Wien-Bridge filters (0.0068 mm²) [7], RC networks (0.01 mm²) [8], or poly-phase filters (0.007 mm²) [4]. However, these typically require two-point trimming to achieve inaccuracies below ±1 °C.

This paper presents a compact resistor-based temperature sensor in 65 nm CMOS. It is based on a poly-phase filter (PPF) whose temperature-dependent phase shift is digitized by a zero-crossing (ZC) detector and then read out by a frequency-locked loop (PLL). The PLL employs a dual zero-crossing detection scheme, which improves accuracy by reducing the impact of the ZC detector offset. As a result, the sensor requires only one-point trimming to achieve a 3σ inaccuracy of ±1.2 °C from −50 to 105 °C.

This paper is organized as follows. The sensor’s architecture is described in Section II, together with an analysis of its main error sources and the resulting circuit implementation. Section III presents measurement results. Finally, a conclusion is presented in Section IV.

II. PPF-BASED TEMPERATURE SENSOR

A. Sensor Architecture

A block diagram of the proposed sensor is shown in Fig. 1. As in [4], its temperature-sensing element is a PPF that incorporates a silicided poly resistor. The PPF is driven by an in-phase signal (P), generated by dividing the output frequency \( f_{\text{CCO}} \) of a current-controlled oscillator (CCO) by \( N \), while a quadrature-phase signal (Q) drives a digital phase/frequency detector (PFD). A ZC detector then detects the ZCs in the PPF’s output \( V_{\text{PPF}} \), which represent its temperature-dependent phase shift \( \phi_{\text{PPF}} \). Depending on the phase difference between the detector output \( V_0 \) and \( Q \), the PFD generates up or down pulses which are converted by a charge pump (CP) into current pulses that drive a loop filter (integration capacitor \( C_{\text{INT}} \)). The filter’s output then regulates the CCO frequency via the \( g_m \) stage. At steady state, the resulting PLL maintains \( \phi_{\text{PPF}} \) at −90°, and so \( f_{\text{CCO}} \) is locked to \( N \) times the center frequency (\( f_{\text{CCO}} = 1/2\pi R C \)) of the PPF.

B. Spread Analysis

Fig. 2 highlights the main error sources of the proposed sensor: resistor spread, ZC detector offset \( V_{\text{os}} \), and CP mismatch. From simulations, an inaccuracy of ±0.2 °C can be achieved with a 1000 μm² 70 kΩ resistor. The combined error of the other blocks should then be less than ±0.8 °C to obtain a worst-case total inaccuracy of ±1 °C.

The offset \( V_{\text{os}} \) causes phase errors in the detected ZCs of \( V_{\text{PPF}} \), which translate into temperature-sensing errors. As shown in Fig. 3(a),
Fig. 2. Main spread sources in the PPF-based temperature sensor.

Fig. 3. Single ZC detection scheme (a) Timing diagram (b) Calculated and simulated temperature error (one-point trimmed) versus $V_{OS}$.

Fig. 4. Dual ZC detection scheme (a) Timing diagram (b) Calculated and simulated temperature error (one-point trimmed) versus $V_{OS}$.

Fig. 5. Simulated temperature error (one-point trimmed) versus CP mismatch.

$V_{OS}$ either delays or advances the detected ZCs depending on its polarity. Single ZC detection, as in [4], will then cause a constant phase error, since the detected ZC will occur when $V_{PPF} = V_{OS}$. If $V_{OS}/V_{DD} = k$, the error in the rising edge $\Delta_{rise}$ can be expressed as

$$\Delta_{rise} = RC \cdot \ln(1+k).$$  \hspace{1cm} (1)

By using the TC of the silicided poly resistor, the resulting temperature error can be derived from this timing error. Fig. 3(b) shows the calculated and simulated temperature error versus $V_{OS}$ for an ideal FLL with single ZC detection after a one-point trimmed. The temperature error is still quite sensitive to $V_{OS} \approx 0.1 \degree C/mV$. However, this can be reduced by noting that while $V_{OS}$ delays the ZC of the rising edge of $V_{PPF}$, it simultaneously advances the ZC point of the falling edge, and vice-versa. This leads to the dual ZC detection scheme shown in Fig. 4(a). Since the error in the falling edge $\Delta_{fall} = RC \cdot \ln(1-k)$, the average error $\Delta_{total}$ in this case can be expressed as

$$\Delta_{total} = \Delta_{rise} + \Delta_{fall} = RC \cdot \ln(1-k^2),$$ \hspace{1cm} (2)

which is much smaller than $\Delta_{rise}$, since $k < 1$. There is some residual error, since $V_{OS}$ introduces slightly different errors in the rising and falling edges. Fig. 4(b) shows the calculated and simulated temperature errors versus $V_{OS}$ for an ideal FLL with a dual ZC detection scheme after a one-point trimmed. Compared to Fig. 3(b), the resulting temperature error is much smaller: less than ±0.5 \degree C for $V_{OS} = 15 mV$.

However, CP mismatch will still cause an error current to flow into $C_{INT}$, causing the FLL to output the wrong frequency. This leads to a constant phase error between $V_O$ and $Q$, and consequently to a temperature error. Fig. 5 shows simulation results with CP mismatch only. They show that it needs to be $< 1.6 \%$ to ensure $< \pm 0.3 \degree C$ error.

C. Circuit Implementation

Fig. 6 shows the block diagram of the proposed PPF-based temperature sensor with dual ZC detection scheme. The PPF consists of two silicided P-poly resistors ($R = 70 k\Omega$) and two MIM capacitors ($C = 0.5 pF$). When the PPF sensor is driven by $F_{CCO}/4$, the locked $F_{CCO}$ varies from 15.3 to 23.8 MHz as the temperature changes from −50 to 105 \degree C. From post-layout simulations, the parasitic capacitance at each PPF output node is $< 10 fF$. This translates into a small (and systematic) temperature-sensing error of about 0.5 mK.

The dual ZC detection scheme employs a dual-edge triggered PFD (DE-PFD), comprising a rising-edge triggered PFD (RE-PFD), a falling-edge triggered PFD (FE-PFD), and a pulse merging circuit.
Both the RE-PFD and FE-PFD are standard edge-triggered PFDs. Their output signals are combined in a pulse merging circuit, implemented with OR gates. Compared to a single ZC detection scheme, the output rate of a dual ZC detection scheme is 2× higher. As a result, even without the extra startup circuitry of [4], the average lock-time after a power-on reset is halved: from ~9.8 μs (56 cycles) to ~4.8 μs (26 cycles).

The CCO is a 9-stage ring oscillator, with a gain of 1 MHz/μA. Its delay cells consist of two inverters, which employ cross-coupled transmission gates to attenuate common-mode signals, and thus enable pseudo-differential operation. A single-ended output buffer employs a level shifter for rail-to-rail operation and an inverter-based latch for 50 % duty cycle. The loop filter uses a large g_m (100 μS) and small C_INT (1.6 pF) to achieve a loop bandwidth of 160 kHz, which is wide enough to effectively reduce the phase noise of the CCO [5].

Fig. 7 (a) shows the ZC detector, which consists of a preamplifier and a cross-coupled latch. To save power, it is only turned on around the expected ZCs by an enable signal (EN), derived from V_T (divided by 2 and 90° shifted). From Monte Carlo simulations, V_OS ~ ±12.5 mV (3σ), which translates into a one-point trimmed temperature inaccuracy of ±0.42 °C (3σ) with a dual ZC detection scheme. The detector’s delay has a negligible effect on temperature inaccuracy. From Monte Carlo simulations, the delay variation of the rising and falling edges are 6.5 and 5.7 ns, respectively. These translate into inaccuracies of 26 and 25 mK, respectively. As shown in Fig. 7 (b), the CP current sources are cascaded, which ensures a current mismatch of less than the target ±1.6 % over PVT. In this work, an external resistor sets the CP bias current. However, the specifications of an on-chip bias circuit are quite relaxed, since a current variation of 4.5 % only translates into a temperature error of ~20 mK.

III. MEASUREMENT RESULTS

The prototype sensor is fabricated in the TSMC 65 nm CMOS process and occupies only 5800 μm² (Fig. 8). For flexibility, its digital backend (mainly a 16-bit counter) and bias current generation are implemented off-chip. In the chosen process, they would occupy an estimated area of 900 μm². Compared to [4], the resistance of silicided p-poly resistor in the PPF is 2× larger, which reduces its power consumption to 32.5 μW from a 1 V supply. Since the resistor only contributes about 15 % of the total input-referred noise, this has negligible impact on the sensor’s resolution. Compared to [4], the use of a cascaded charge pump and the omission of a startup path results in less supply sensitivity. At room temperature, the sensor achieves a supply sensitivity of 0.22 °C/V from 0.85 to 1.3 V, which is 2.3× better than [4]. 20 samples in a ceramic dual in-line package were measured in a temperature-controlled oven from −50 to 105 °C. To minimize the effects of oven drift, the prototypes were placed in good thermal contact with an aluminum block containing a reference sensor (platinum Pt-100 resistor sensor).

A. Temperature Inaccuracy and Resolution

The FLL output frequency varies from 15.3 to 23.8 MHz (0.22 %/°C), while its period changes from 42 to 65.4 ns (Fig. 9). As in [4], [6], after a 1st order fit to remove process spread, the non-linear temperature dependence in the FLL’s output period can be removed by a fixed 5th order polynomial. This non-linearity is mainly determined by the silicided poly resistor, allowing the coefficients of this polynomial to be obtained directly from TT-corner simulations. The sensor then achieves an untrimmed inaccuracy of ±5.2 °C (3σ), which improves to ±1.2 °C after a room temperature trim (Fig. 10a). It can be further improved to ±0.16 °C by a two-point trim (Fig. 10b), which is similar to [4], but is over a wider temperature range. The sensor’s temperature-sensing resolution is determined by measuring the accumulated jitter of the FLL’s output period. In Fig. 11 (a), the resolution is plotted versus the conversion time (T_CONV). Up to T_CONV ~ 0.2-ms, the accumulated jitter exhibits a 1/NT_CONV behavior due to thermal noise. For longer measurement times, the accumulated jitter is limited by 1/f noise. As shown in Fig. 11 (b), the accumulated jitter is 7.8 ns in a 1-ms period, which corresponds to a resolution of 2.8 mK, and a competitive resolution FoM of 0.26 pJ K².
This work presents a temperature sensor with compact size (5800 μm²) in 65 nm CMOS. The sensor employs a PPF for temperature sensing and an FLL with a dual ZC detection scheme. The PPF consists of MIM capacitors and silicided poly resistors, resulting in a small area with high TC and large-signal swing. The FLL incorporates a DE-PFD and cascode CP to improve its one-point trimmed inaccuracy to ±1.2 °C (3σ) from −50 to 105 °C. The design consumes 32.5 μW from a 1 V supply and achieves a resolution of 2.8 mK, which corresponds to a resolution FoM of 0.26 pJ·K. Due to its combination of compact area, moderate temperature inaccuracy, and competitive resolution FoM, the proposed PPF-based sensor is well suited for use in thermal monitoring applications in sub-100 nm CMOS.

**REFERENCES**


