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Abstract: Charging of electric vehicles (EVs) from solar energy provides a sustainable means to power EVs in the future. A comparison of topologies for a three-port converter to charge EVs directly from photovoltaic (PV) panels is presented in this study. The grid-connected EV charger has a nominal rating of 10 kW and is bidirectional, enabling vehicle-to-grid operation. The topologies are optimally designed considering different switching frequencies, silicon carbide devices, magnetic cores and number of interleaved stages. Nine topologies are compared using a comparison framework, and the best topology is chosen based on the number of components, converter efficiency, volume, controllability and current ripple. The analysis shows that the best topology is a three-port converter with a central direct current link with a 3-leg interleaved boost converter (IBC) for the PV, two-level inverter with sinusoidal modulation for the grid and a 4-phase interleaved flyback converter for the EV. The loss models built are experimentally verified using a 3-leg IBC.

1 Introduction

Electric vehicles (EVs) are considered as a clean mode of transportation as they have zero tail-pipe emissions. At the same time, the electricity grid in most countries is powered mostly by fossil fuels. This means that if EVs are charged from such a grid, the net emissions are not entirely zero. A truly sustainable way to charge EVs is to use electricity from photovoltaic (PV) panels or wind turbines [1, 2]. Fig. 1 shows a solar charging station for EVs at a workplace where the PV panels are installed on rooftops and as solar carports.

There are several advantages of charging EVs from PV:

(i) Reduced demand on the grid as the EV charging power is locally generated from PV [2].
(ii) The local use of PV energy partially/entirely averts the negative impact of distributed generation like reverse power flow and overvoltage problems [3, 4].
(iii) Long parking time of EVs facilitates the EV to support the grid via vehicle-to-grid (V2G) technology [5, 6].
(iv) Lower cost of EV charging and reduced impact of reduction in PV feed-in-tariffs [7].

At the same time, PV generation suffers from diurnal and seasonal variability. This necessitates an AC grid connection for the EV charging to feed excess PV power and to draw power to meet the EV charging demand. Hence, a solar powered EV charging system would require the EV, PV and AC grid and a three-port power converter (TPC) to connect them, as shown in Fig. 2. The benefit of using a single bidirectional TPC as against separate (on-board or off-board) unidirectional EV charger and a PV inverter exchanging power on the AC grid are manifold:

Fig. 1 *Solar powered charging station for EV at workplace*

(i) Since EV and PV are both direct current (DC), exchanging power on DC is more efficient than on AC [8].
(ii) An integrated converter will require only one DC/AC inverter stage instead of two separate inverters for the EV and PV, respectively [9].
(iii) If the EV charger is bidirectional, the EV battery can be used as energy storage for the PV. This can be realised by charging the EV battery from solar and then discharging the power to the grid [2].
(iv) An integrated solar EV charger with V2G can facilitate intelligent power management (PV → EV, EV ←→ Grid, PV → Grid) to dramatically reduce the net operating costs by providing grid support and using the EV battery as an energy buffer [10, 11].

The goal of this paper is to determine the optimal topology for a TPC that integrates the EV, PV and AC grid. Determining the optimal topology is crucial as it will ensure that the converter has high efficiency, high power density and low cost. The optimal topology is chosen based on the several indices: efficiency, converter volume, number of components, ripple, controllability and possibility for efficiency improvement.

1.1 Architecture for EV-PV power converter

Three system architectures are possible for the TPC:

(i) Architecture 1 – DC-link based: The first architecture is based on a DC-link (Fig. 2*a*), which acts as a high voltage energy buffer between the ports. There are three sub-converters with different control algorithms: the PV converter is responsible for maximum power point tracking (MPPT); the EV converter controls the EV (dis)charging power; and the inverter is responsible for the power balance with the AC grid. The advantage of this architecture is that it is simple and allows for DC interconnection of EV and PV, thus reducing the DC/AC conversion losses. The architecture is

modular, so additional converters can be interfaced on the central DC-link.

(ii) *Architecture 2 – Impedance-network based*: The second TPC architecture is based on an impedance network converter, like the Z-source converter (Fig. 2*b*) [1, 12, 13]. This architecture has an inherent variable voltage DC-link which is connected to an isolated DC–DC converter for the EV charging. The advantage is that it has a lower switch count and requires only two controllers. The disadvantage is the control complexity of the impedance network converters and that the architecture is not intrinsically modular.

(iii) *Architecture 3 – AC-link based*: The last architecture uses a three-winding, high-frequency transformer (HFT) to integrate the EV, PV and AC grid [14, 15]. The main advantage is the isolation of all three ports. However, isolation between PV panels and the grid is not required by European standards (IEC 61727). Besides, there is high complexity in the design of the HFT and converter control making it not modular. Finally, there are increased AC/DC conversion steps between the ports compared to the other two architectures. Therefore, this architecture is not considered in this work.

1.2 Literature review and contributions

Several topologies and system architecture for PV charging of EVs are reviewed in [16, 17]. It has three main conclusions on PV charging system for EV: grid-connected systems are more popular than off-grid systems; a TPC with a DC-link is the best system architecture; and that isolation of EV converter was neglected by most works even though it is required by the standards [18]. Four types of EV-PV system architecture are proposed in [16] based on whether an integrated power converter or two separate power converters are used for PV and EV; and if the PV and EV are interconnected on AC or DC.

The authors of [19–21] propose the power exchange over AC through the use of a separate PV inverter and AC EV charger (possibly with energy storage). The disadvantage of this approach is that PV and EV are fundamentally DC. So power exchange over AC causes additional losses and needs two inverters instead of one.

Hence an integrated converter with DC-link based power exchange between EV and PV is preferred [9, 22–26]. Charging of EV from PV using a 2.4 kW zero voltage transition pulse width modulation (PWM) buck converter connected to a 210 V DC bus was proposed in [9, 22]. The EV charger is unidirectional with no isolation, and there is high ripple due to the use of buck converter. The use of EV charging for mitigating solar intermittency was analysed in [23, 24]. A 10 kW bidirectional DC/DC converter with zero voltage switching (ZVS) quasi square-wave at 98% efficiency is used for EV charging (no isolation). A 575 V central DC-link interconnects PV and EV converters. A 3.3 kW TPC with boost converter for PV, H-bridge inverter for grid and interleaved buck converter for EV (with no isolation) interlinked on 380 V DC link is presented in [25]. 7–15% improved efficiency compared to AC power exchange is reported. A 5 kW TPC made of boost converter for PV, 1-phase H-bridge inverter for grid and buck converter for EV (with no isolation) interlinked on 400 V DC link is proposed in [26].

In the case of impedance network-based topologies, three topologies for EV-PV charging using an isolated DC/DC EV charger are compared in [1] namely, Z-source converter, transformer-less PV inverter and high-frequency isolated PV inverter. The 5 kW Z-source converter with 10 kW EV charger was chosen as the best topology. The quasi-Z-source converter with DC link was used for EV and battery charging in [12, 13]. The topology facilitated bidirectional operation but did not have any isolation for the battery.

Based on the above literature review, the contributions of this work compared to earlier works are:

(i) There is no existing research that quantitatively compares bidirectional EV-PV converter topologies considering efficiency, power density, component count, controllability and efficiency improvement. This paper addresses this research gap by comparing nine topologies on the above-listed indices. The topologies considered have isolation for the EV as required by the standards [18, 27] and will enable V2G operation.

(ii) Each topology is designed considering two switching frequencies (50, 100 kHz), 8 silicon carbide (SiC) MOSFETs, 13 SiC diodes, 17 inductor core materials of varied sizes, different modulation techniques and heatsink sizes. This ensures that each topology is itself designed optimally, so there is a fair comparison of topologies. Such detailed design and comparison of EV-PV topologies have not been done before.

(iii) Interleaving of converters (1–5 stages) is implemented for the appropriate topologies to reduce the ripple at the EV and PV port and increase power density. This is vital as a high ripple prevents MPPT operation at PV port [28]. The previous works did not consider the impact of ripple.

(iv) The paper focuses on the design of a three-phase, high power converter (10 kW) for charging EV from PV. The existing research in this domain is predominantly on single phase, low power applications (<5 kW).

1.3 Three-port converter specifications & topology

Table 1 shows the specifications of the 10 kW EV-PV power converter.

The converter is designed to operate with EV and PV with a wide voltage range, small ripple, high peak and partial load efficiency (>95%) and high power density. The rated power of 10 kW is chosen because EV fast chargers of ≥50 kW are typically built using modular 10 kW power modules. Secondly, 10 kW presents the right balance between PV generation and (Level 2) EV charging [2].

For architecture 1, the topologies investigated are: the interleaved boost converter (IBC) [29, 30], the coupled inductors IBC (CIIBC) [31, 32], the three-level boost converter (TLBC) [33, 34] for the PV port; the dual active bridge (DAB) [35, 36] and the interleaved bidirectional flyback converter (IBFC) [37, 38] for the

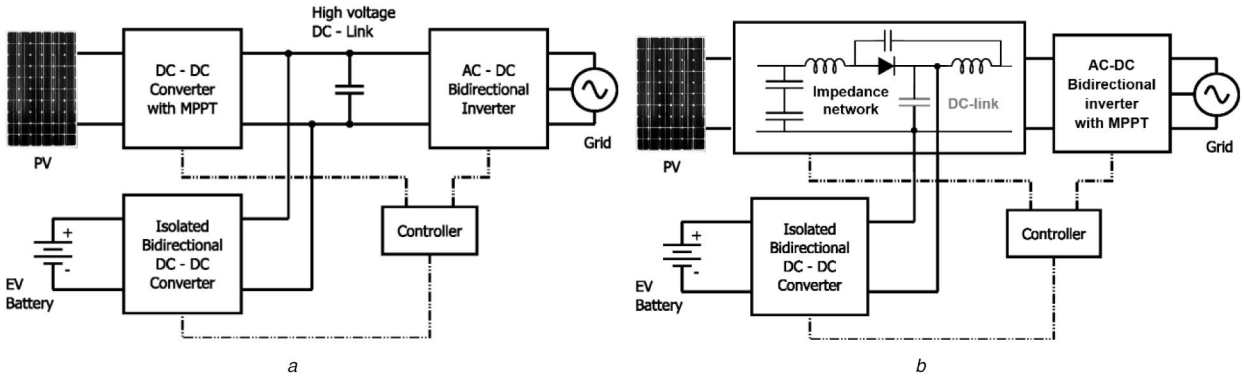


Fig. 2 *Block diagram of TPC*

(a) Architecture 1: DC-link and three converters for EV, PV, grid, ***(b)*** Architecture 2: Isolated EV converter connected to the internal DC link of an impedance network converter that uses an inverter to connect to AC grid

EV port, and the two-level converter (2LC) also known as voltage source inverter [39], three-level neutral point clamped converter (3LNPC) [40] and the three-level T-type converter (3LT2C) [41] for the grid port. For architecture 2, the quasi Z-source converter with the above EV port topologies is evaluated. This is further elaborated in Sections 4–6.

1.4 Outline of the paper

Section 2 presents the method used to design the three-port converter and estimate the converter losses. Section 3 presents the comparison framework used to compare the different topologies. Sections 4–6 provide the results of the converter design and comparison of the topology candidates for PV, EV and grid port, respectively. The Z-source converter-based design is analysed in Section 7. The choice of converter topology and the verification of the loss models are presented in Sections 8 and 9, respectively.

2 Design of converters and loss modelling

This section provides a method to optimally design a converter topology to achieve high efficiency and power density considering different design parameters: switching frequency, magnetic core, copper windings, semiconductor devices, capacitor and heat sinks. As shown in Fig. 3, this will require several iterations using an accurate loss model of the converter where the component selection and design are varied at every cycle. At the end of the iterations, the converter components, volume and efficiency of the optimised design are obtained.

Two different switching frequencies f_{sw} namely 50 and 100 kHz are considered. At a lower switching frequency, a larger inductor is required but the switching losses in the semiconductors are lower; and vice versa. The loss models presented below are built based on [30, 36, 42].

Table 1 Specifications of EV-PV converter

Parameter	Symbol	Value
nominal power	P_{nom}	10 kW
PV MPPT voltage	V_{pv}	350–700 V
PV MPPT current	I_{pv}	0–30 A
PV current ripple (pk–pk)	ΔI_{pv}	<10% of $I_{pv(max)}$
PV voltage ripple (pk–pk)	ΔV_{pv}	<0.5%
EV voltage	V_{ev}	200–500 V
EV current (bidirectional)	I_{ev}	−30 A to +30 A
internal DC-ink voltage	V_{dc}	750 V (for Arch. 1)
AC grid connection	—	400 V, 50 Hz, 16 A

2.1 Semiconductors

SiC MOSFETs and Schottky diodes are used in the design instead of silicon devices. This is due to the lower switching/conduction losses and practically zero reverse recovery of the diode. MOSFETs considered are CREE's C3M [0280090D, 0120090D, 0065090D] and C2M [0280120D, 0160120D, 0080120D, 0040120D, 0025120D]. The chosen CREE Schottky diodes are C3D [04065A, 08065A, 10065A]; C5D50065D and C4D [02120A, 05120A, 08120A, 10120A, 15120A, 20120A, 20120D, 30120D, 40120D]. The gate resistance is 2.5 Ω and the gate voltage is −5/20 V and −4/15 V for the C2M and C3M series, respectively.

To find the optimal switch and diode for each topology, the operating point with the highest semiconductor losses is considered. The SiC device which yields the lowest losses at that point is chosen. This method does not prioritise the losses over the entire operating range but minimises the maximum power dissipation, thereby reducing the heat sink size. A 25% margin is used in the device voltage rating to account for transient voltage spikes. The maximum semiconductor junction temperature is set to 100°C at an ambient temperature of ≤45°C. This ensures low heat-sink/junction temperature for a long lifetime of the converter.

The losses in the SiC MOSFETs P_{sw} consist of conduction losses $P_{sw,con}$ and the switching losses $P_{sw,on}$, $P_{sw,off}$. The losses depend on the drain-source current I_{DS}, on-state resistance R_{DSon}, junction temperature T_j, gate voltage V_{GS}, gate resistance R_{GS}, switching ON and OFF energies E_{on}, E_{off}, respectively; which are calculated for every operating point based on the datasheet.

$$P_{sw} = P_{sw,con} + P_{sw,on} + P_{sw,off} \tag{1}$$

$$P_{sw,con} = I^2_{DS,rms} R_{DS\,on}(I_{DS}, T_j, V_{GS}) \tag{2}$$

$$P_{sw,on} + P_{sw,off} = f_{sw}\{ E_{on}(V_{DS}, I_{DS}, T_j, R_{GS}) + E_{off}(V_{DS}, I_{DS}, T_j, R_{GS})\} \tag{3}$$

For specific soft-switching topologies like ZVS, the discharging of the MOSFET output capacitance C_{oss} before turn-on is also considered.

The conduction losses in the Schottky diode $P_{d,con}$ can be modelled as a forward voltage $U_{D,0}$ and a series resistor R_D and are obtained from the datasheets. When switching off a Schottky diode, there is a loss $P_{d,off}$ due to the switch-off energy $E_{D,ch}$ for charging the junction capacitance. Therefore, the total losses of a diode, P_D is the sum of the conduction losses, $P_{d,con}$ and switch-off losses $P_{d,off}$

$$P_D = P_{d,con} + P_{d,off} = \{I_{f,avg} U_{D,0}(T_j) + I_{f,rms} R_D(T_j)\} + V_R E_{D,ch}(V_R) f_{sw} \tag{4}$$

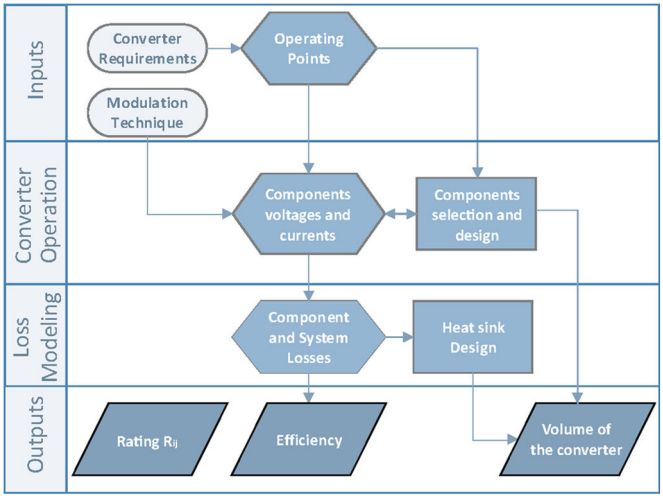


Fig. 3 *Method used to estimate rating R_{ij} of topologies*

2.2 Inductor and HFT design

The aim of the inductor design is to design an inductor that is low on losses and volume, to maximise efficiency and power density. Six inductor core sizes (E16, E25, E32, E42, E55, E65) and four inductor core materials (Magnetics *R,P*; FerroxCube *3C92, 3C96*) are used. The maximum core size is restricted to E65 to ensure easy printed circuit board (PCB) mounting. The inductor design follows an optimisation procedure:

(i) For the given topology and specifications, the inductor size and energy storage requirements are estimated.
(ii) Based on this, the minimum and the maximum number of turns and the corresponding air gap length are calculated, considering the core flux saturation limits.
(iii) The optimal Litz wire configuration is determined with a maximum current density of 4 A/mm^2 based on [43].
(iv) Then, the inductor copper (P_{cu}), core (P_{core}) and total losses (P_L) are calculated for every configuration.
(v) The optimal inductor is chosen based on the lowest index F_L that considers the inductor losses and total volume, V_L:

$$F_L = \frac{1}{2}\frac{P_L}{P_{L,max}} + \frac{1}{2}\frac{V_L}{V_{L,max}} \tag{5}$$

where $P_{L,max}$, $V_{L,max}$ are the highest losses and largest volume amongst all possible designs, respectively.

The core losses depend on the materials used, the magnetic flux in the core and the frequency. The Improved Generalized Steinmetz Equation [44] is used to estimate the core losses per unit volume, P_v

$$P_L = P_{core} + P_{cu} = V_e P_v + R_L I^2_{L(rms)} \tag{6}$$

where R_L is the winding resistance, $I_{L(rms)}$ the RMS inductor current and V_e the volume of the core.

A similar procedure is followed for the losses in the HFT after estimating the flux swing of the core. For the HFT, U cores from four materials (Matglas, MKM nano, Vitroperm, Hitachi Finemet) and 18 sizes (AMCC 4 to AMCC 250) are used. In the case of the LCL toroidal filters (L_{fconv}, L_{fg}, C_f) for the AC grid inverters, 21 powder alloy toroidal cores from Magnetics (KoolMμ 26,60,125; Xflux 26; MPP 14,26; Amoflux; High flux 26,125) are considered. The LCL filters are designed in such a way so as to limit the total harmonic distortion (THD) to less than 5% and the individual harmonics are limited as stipulated in [45]. The filter inductors are sized based on [46–48] and the losses estimated using the original Steinmetz equation. The final selection of both the HFT and toroid filter is based on (5).

2.3 Capacitors

Input and output capacitors (C_{in}, C_{out}) are used for filtering the current ripple. Capacitor design is given importance as the volume occupied can be significant even though the losses are relatively small. Epcos film capacitors of type B32776 {−450 to−1100} and B32796 {−250 to −40} are used in the design. The capacitors losses, P_{caps} depend on the equivalent series resistance (ESR) R_{ESR} and the series $N_{c,s}$ and paralleled $N_{c,p}$ connection of capacitors to increase the rated voltage and capacitance, respectively

$$\begin{aligned} P_{caps} &= R_{ESR,set} I^2_{cap,rms} \\ P_{caps} &= \frac{N_{c,s}}{N_{c,p}}\left(R_{ESR} + \frac{D_F}{2\pi f_{eq} C_r}\right) I^2_{cap,rms} \end{aligned} \tag{7}$$

where f_{eq} and $I_{cap,rms}$ are the equivalent frequency and RMS capacitor current, respectively, C_r is the rated capacitance and D_F is the dielectric factor. It is a requirement that the losses do not increase the capacitor temperature beyond 90°C at full load.

The optimum set of capacitors is selected similar to (5), which minimises the volume and PCB area based on the actual and maximum area (A_{set}, $A_{set,max}$) and volume (V_{set}, $V_{set,max}$) of the capacitor set

$$F_C = \frac{1}{2}\frac{A_{set}}{A_{set,max}} + \frac{1}{2}\frac{V_{set}}{V_{set,max}} \tag{8}$$

2.4 Heatsink

The heat sink size is computed from the losses in each semiconductor and the maximum allowed junction temperature. The cooling system performance index (C_{SPI}) method is used to find the heatsink volume [49]

$$V_S = \frac{1}{R_{th,Sa} C_{SPI}} = \frac{P_t}{(T_S - T_a) C_{SPI}} \tag{9}$$

where $R_{th,S-a}$ is the thermal resistance of the heatsink to the ambient and V_S, the volume of the heatsink. In this study, a $C_{SPI} = 10$ has been selected. The necessary $R_{th,Sa}$ is obtained via the heatsink temperature T_S, the ambient temperature T_a and the total losses in the power converter P_t. Hi-Flow 300P thermal pad with a performance of 0.94°C/W is used. The key is to ensure that the heatsink size is as small as possible to increase the power density.

3 Comparison framework

A comparison framework is used to find the optimal topology for the TPC based on nine criteria listed in Table 2 [50]. For each topology, the value of each criteria $V_{est,j}$ is estimated based on Section 2. Subsequently, each topology is given a rating (R_{ij}) from one to five for each criterion as, shown in Table 2, with one being the worst and five being the best. As seen in Table 2, $V_{0,j}$ and $V_{5,j}$ are the values of that criterion that corresponds to a rating of 0 and 5, respectively. For example, the number of switches for the grid port converter has a rating of $R_{ij} = 0$ when the number of switches is greater than $V_{0,j} = 20$ and a rating $R_{ij} = 5$ when it is less than $V_{5,j} = 6$. Further, for each topology i, linear scaling is used to estimate the rating R_{ij} for criterion j, when the value of that criterion $V_{est,j}$ lies between the values $V_{0,j}$ and $V_{5,j}$

$$R_{ij} = \frac{5(V_{est,j} - V_{0,j})}{(V_{5,j} - V_{0,j})} \tag{10}$$

So, if a grid topology has twelve switches, $V_{est,j} = 12$, then the corresponding rating based on linear scaling is $R_{ij} = 5(12–20)/(6–20) = 2.86$.

Since all the criteria do not have the same priority, a weight factor (W_j) is used to scale each criterion. The benefit of this step is that it offers the flexibility to adjust the weights for different requirements, such as those where efficiency is more important than the number of components or power density is more vital than controllability. Finally, the weight factor and the criterion rating are combined to estimate a total score ($T_{score,i}$) for each of the topologies using

$$T_{score,i} = \sum_{i=1}^{N_{cri}} W_j R_{ij} \tag{11}$$

where i refers to the topology, j the criterion and N_{cri} the total number of criteria (here, $N_{cri} = 9$). The converter with the highest score $T_{score,i}$ is the best suited for the given specification and application. Similarly, for qualitative ratings such as efficiency improvement and controllability, a score from 0 to 5 is given depending on how easy or difficult it is to achieve the same. The columns 'Criterion j', 'weight factor W_j' and 'criterion value

Table 2 Weight and rating scale for comparison framework of topology

Criterion	j	W_j	topology for port	value of criterion j for rating R_{ij} of 0 and 5, respectively	
				$V_{0,j}$	$V_{5,j}$
number of switches	1	4	PV	≥6	≤1
			EV	≥18	≤8
			grid	≥20	≤6
number of diodes	2	2	PV	≥6	≤1
			EV	≥18	≤2
			grid	≥20	≤6
number of core sets	3	3	all	≥6	≤1
number of capacitors	4	1	all	≥6	≤1
efficiency η, %	5	6	PV	$\eta \le 98.0$	$\eta \ge 99.5$
			EV	$\eta \le 97.25$	$\eta \ge 98.75$
			grid	$\eta \le 97.5$	$\eta \ge 99.0$
			qZSI	$\eta \le 95.5$	$\eta \ge 98.5$
converter volume V_C, dm^3	6	5	PV	$V_C \ge 0.6$	$V_C \le 0.3$
			EV	$V_C \ge 1.5$	$V_C \le 0.6$
			grid	$V_C \ge 0.9$	$V_C \le 0.4$
			qZSI	$V_C \ge 1.5$	$V_C \le 0.7$
EV current ripple, A	7	3	EV	≥55	0
efficiency improvement	8	2	all	difficult/not possible	very easy
controllability	9	3	all	very difficult	very easy

Table 3 Optimal design and score of PV port converters

Optimal design			IBC, 3 ph., 50 kHz		CIIBC, k = −0.9, 4 ph., 50 kHz		TLBC, 2 ph., 50 kHz	
MOSFET			C2M0040120D		C2M0080120D		C2M0025120D	
DIODE			C4D20120A		C4D15120A		C4D20120A	
inductance (per phase), magnetic core, turns, resistance			$L1$ = 874 µH, E65, *3C92*, 45 turns, 42 mΩ		$L1$ = 11.3 mH, E65, magnetics *R*, 29 turns, 34 mΩ		$L1$ = 328 µH, E65, *3C92*, 22 turns, 10 mΩ	
C_{in}, C_{out}, µF			0.688, 8.230		0.510, 2.258		0.511, 4.736	
criterion	j	W_j	$V_{est,j}$	R_{ij}	$V_{est,j}$	R_{ij}	$V_{est,j}$	R_{ij}
no. of switches	1	4	3	3	4	2	4	2
no. of diodes	2	2	3	3	4	2	4	2
no. of cores	3	3	3	3	2	4	2	4
no. of caps	4	1	2	4	2	4	3	3
efficiency, %	5	6	99.18	3.93	99.04	3.47	98.77	2.57
volume, dm^3	6	5	0.431	2.82	0.332	4.47	0.509	1.52
efficiency improv.	8	2	—	3	—	1	—	2
control	9	3	—	4	—	1	—	3
$T_{score,i} = \sum W_j R_{ij}$			86.68		76.17		63.02	

$V_{est,j}$', are shown later in Tables 3–6 when the scores for the various topologies are estimated and compared.

3.1 Number of components

A high number of components increases the complexity and cost of the system, and reduces reliability. The weights and ratings for different components are shown in Table 2. A rating of $R_{ij} = 5$ is obtained when the number of components is less than the value shown in column $V_{5,j}$. In the case of SiC switches, they have the highest costs and lead to a higher number of gate drive and control circuits; hence a bigger weight factor, $W_1 = 4$. On the other hand, diodes have a weight $W_2 = 2$ as they are uncontrolled elements. The number of magnetic cores adds to the cost, losses and volume of the converter and hence has a weight factor, $W_3 = 3$.

3.2 Efficiency and volume of the converter

Converter efficiency and volume, estimated in the previous section, are the most critical criterion and therefore have a weight of $W_5 = 6$ and $W_6 = 5$, respectively. The European efficiency is used for the PV and grid port [51]. Both inverting and rectifying efficiencies are equally considered for grid port. For the EV port, the average efficiency over the entire operating range shown in Table 1 is considered. Since several EV chargers will be installed in the parking lot, converter volume is a vital criterion. $V_{0,j}$ and $V_{5,j}$ values for the EV port are lower than the PV and, grid ports as the EV converter needs to have galvanic isolation, thus increasing the size and losses in the converter. The converter volume is estimated as the sum of the volumes of the heatsink, the inductors/HFT and the capacitors. In general, a converter with higher efficiency has lower losses and a smaller volume due to a smaller heatsink.

3.3 Current ripple in EV battery

The EV port topologies are compared based on the EV current ripple magnitude as it significantly affects the battery lifetime [52]. Hence, it has a weight of $W_7 = 3$.

3.4 Controllability and efficiency improvement

Controllability and efficiency improvement are qualitative criteria and hence the ratings R_{ij} are directly provided without an estimated value, $V_{est,j}$ Controllability addresses the control complexity of a

Table 4 Review of the analysed EV port converters

Optimal design			DAB (PSM-ZVS), 2 ph., 100 kHz		IBFC (QR), 4 phases, 50–200 kHz	
MOSFET			C2M0080120D primary		C2M0040120D	
—			C2M0025120D secondary		—	
DIODE			body diode		C4D15120A primary	
—			—		C4D20120A secondary	
leakage inductance: magnetic core, turns, resistance, air gap			L_{leak} = 125 μH, E65, *3C92*, 36 turns, 41 mΩ, 0.35 cm air gap		—	
HFT/inductor (per phase): magnetic core, turns, resistance, air gap			AMCC 50, vitrop. 500F, 40:20 turns, 17 mΩ: 90 mΩ, no air gap		$L_{m1} = L_{m2}$ = 454 μH, E65 core, magnetics *R*, 40 : 20 turns, 48 mΩ: 12 mΩ, 0.12 cm air gap	
C_{in}, μF			2.32		11.983	
criterion	*j*	W_j	$V_{est,j}$	R_{ij}	$V_{est,j}$	R_{ij}
switches	1	4	16	1	12	3
diodes	2	2	0	5	12	1.88
cores	3	3	3	3	4	2
caps.	4	1	1	5	1	5
eff., %	5	6	98.03	2.6	98.63	4.6
vol., dm^3	6	5	1.22	1.56	0.77	4.06
efficiency improvement	7	2	—	4	—	2
control	8	3	—	3	—	2
current ripple	9	3	53.13	0.17	28.21	2.44
$T_{score,i} = \sum W_j R_{ij}$			68.91		91.98	

Table 5 Review of the optimal configurations of the analysed grid port converters

Optimal design			2LC, SPWM, 50 kHz		3LNPC, SVPWM, 50 kHz		3LT2C, SVPWM, 50 kHz	
MOSFET			C2M0025120D		C2M0025120D		C2M0025120D	
DIODE, (T-DIODE)			C4D20120A		C5D50065D		C4D20120A, C5D50065D	
LCL filter parameters			$L_{f\,conv} = 480\,\mu H$, $L_{fg} = 16\,\mu H$, $C_f = 3.16\,\mu F$		$L_{fconv} = 214\,\mu H$, $L_{fg} = 6\,\mu H$, $C_f = 1.03\,\mu F$		$L_{fconv} = 214\,\mu H$, $L_{fg} = 6\,\mu H$, $C_f = 1.03\,\mu F$	
input capacitor, μF			40.26		36.39		36.39	
criterion	*j*	W_i	$V_{est,j}$	R_{ij}	$V_{est,j}$	R_{ij}	$V_{est,j}$	R_{ij}
switches	1	4	6	5	12	2.86	12	2.86
diodes	2	2	6	5	18	0.71	12	2.86
input caps.	4	1	3	3	8	0	8	0
efficiency, %	5	6	98.41	3.03	98.73	4.1	98.63	3.77
volume, dm^3	6	5	0.721	1.79	0.432	4.68	0.411	4.89
eff. impr.	8	2	—	3.5	—	1	—	1
control	9	3	—	5	—	3	—	2
$T_{score} = \sum W_j R_{ij}$			82.13		71.86		72.23	

Table 6 Review of the quasi Z-source inverter

Optimal design			qZSI, 50 kHz	
MOSFET			C2M0025120D	
DIODE (Dz)			C4D20120A, 3 in parallel	
impedance network inductance (*L*1, *L*2), capacitance (*C*1,*C*2,*Cz*1,*Cz*2)			*L*1 = *L*2 = 1083.35 μH (32 E65 core inductors of 542 μH); *C*1 = *C*2 = 0.952 μF, Cz1 = 37.7 μF, Cz2 = 37.7 μF (*C*1,*C*2,*Cz*1,*Cz*2 are made of 11 capacitors)	
542 μH inductor: core, turns, resist.			*3C92*, 35 turns, 25 mΩ	
LCL filter			$L_{fconv} = 214\,\mu H$, $L_{fg} = 6\,\mu H$, $C_f = 1.034$	
criterion	*j*	W_j	$V_{est,j}$ (PV, Grid)	R_{ij} (PV, Grid)
no. of switches	1	4	(0, 6)	(5, 5)
no. of diodes	2	2	(3, 6)	(3, 5)
no. of cores	3	3	(16,-)	(0, -)
no. of caps.	4	1	(11,0)	(0,5)
efficiency, %	5	6*2	97.58	3.47
Volume, dm3	6	5*2	4.37	0
eff. Impr.	8	2*2	—	1.5
control	9	3*2	—	3
$T_{score,i} = \sum W_j R_{ij}$			126.64	

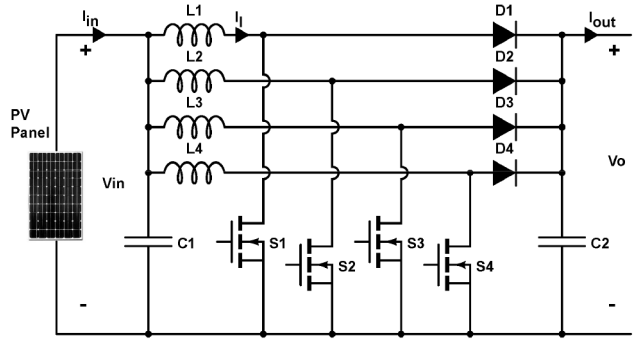


Fig. 4 *Structure of (top) four phases IBC. In the case of the four phases CIIBC, L1, L2 and L3, L4 are coupled*

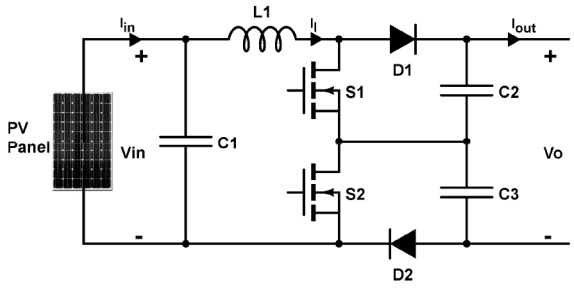


Fig. 5 *Structure of a single-phase TLBC*

given topology, and it has a weight of $W_8 = 3$. The converter efficiency can generally be increased by better modulation techniques, use of snubbers and circuitry to implement zero current switching (ZCS) and/or ZVS. Using a weight of $W_9 = 2$, the topologies are rated on how much efficiency improvements can be achieved and how easy it is to implement it.

In the next sections, nine topologies based on the DC-link and impedance architecture are designed based on the procedure in Section 2 and are compared based on the framework in Table 2. In the case of DC-link architecture, the topologies are split into the PV, EV and grid ports.

4 Architecture 1 – PV port candidates

4.1 Topologies

Figs. 4 and 5 show the three different topologies for the PV port for architecture 1: the IBC, CIIBC and TLBC. The PV converter must meet specifications in Table 1 and operate at the PV array at its MPPT. The IBC is based on interleaving the conventional boost converter, which reduces the current and conduction losses in each leg. It has reduced EMI and high efficiency at light load, at the expense of a higher component count. The CIIBC is a modified version of the IBC which reduces the number of inductors by using coupled inductors. This reduces the overall size and improves the regulation of power converters by enhancing current sharing. Direct and reverse coupling configurations can be used to reduce input ripple or inductor ripple (coupling coeff. $k = \pm 0.35$, ± 0.5, ± 0.9 considered). Lastly, the TLBC offers the advantages of a three-level topology with reduced voltage ratings and double switching frequency at the input current. However, the output current circulates through two diodes, increasing the losses.

4.2 Optimal configuration and comparison

The procedure from Section 2 is used to find the value $V_{\text{est},j}$ of each criterion enlisted in Section 3 for the PV topologies and their corresponding ratings. The configuration with the highest score for each of the three topologies is shown in the first 5 rows of Table 3: the 3 phases IBC, the 4 phases CIIBC with coupling factor −0.9 and the 2 phases TLBC, all of them switching at 50 kHz. The estimated efficiencies (for $V_{\text{PV}} = 500$ V) and volume for the converters are shown in Fig. 6. Topology configurations such as an IBC at 100 kHz or a 3-phase TLBC at 50 kHz are not shown in

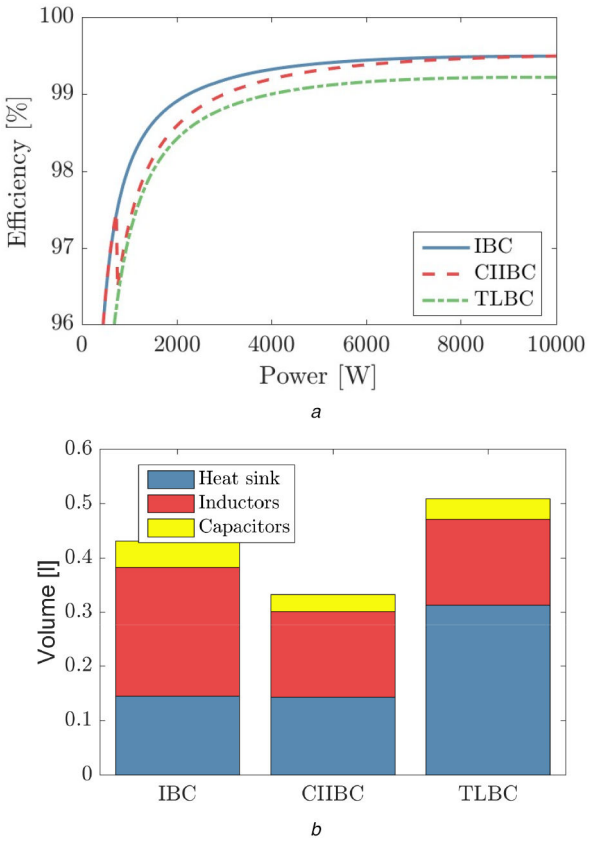


Fig. 6 *Comparison of the efficiency and volume of the PV port converter candidates:*
(a) Converter efficiency for $V_{\text{PV}} = 500$ V, ***(b)*** Volume of the converter

Table 3 as they have a much lower score than 86.68 and 63.02, respectively.

Table 3 shows that the IBC has a better rating for the number of components as it needs only 3 switches and diodes compared to 4 switches for the others. Fig. 6*a* shows how the highest efficiency of up to 99.5% and a European efficiency of 99.18 is achieved by the IBC as well. Based on Table 2, this results in an efficiency rating of $R_{ij} = 5(12–20)/(6–20) = 2.86$. The steep jumps in the efficiency of CIIBC are due to the inductor coupling and different conduction modes of the converter. The IBC and CIIBC have significantly lower losses over the operating range than the TLBC making the converters more efficient and smaller (due to a smaller heatsink). On the other hand, the CIIBC uses less number of cores than the IBC as it uses coupled inductors, and has lower losses than a TLBC, resulting in a lower converter volume (Fig. 6*b*) and a higher rating of 4.47. The trade-off is that the CIIBC is the most challenging converter amongst the three to control and efficiency improvements are difficult due to the coupled inductors, resulting in a much lower rating of 1 for criteria 8 and 9.

It hence can be seen that the three topologies have several trade-offs in their design and hence it becomes vital to provide weights for the criterion and estimate the overall score. From Table 3, it can be seen that the 3-phase IBC at 50 kHz frequency has the highest overall score of 86.6. It is hence the most optimal topology for the PV port.

5 Architecture 1 – EV port candidates

5.1 Topologies

Several DC–DC isolated topologies can be selected for the purpose of charging EV batteries for both for architectures 1 and 2. For this comparison, the DAB and the IBFC are the selected topologies (Figs. 7 and 8). Since isolated topologies have lower efficiency than non-isolated topologies, the DAB is operated in ZVS mode, and the IBFC is operated in quasi-resonance (QR), to reduce the switching losses.

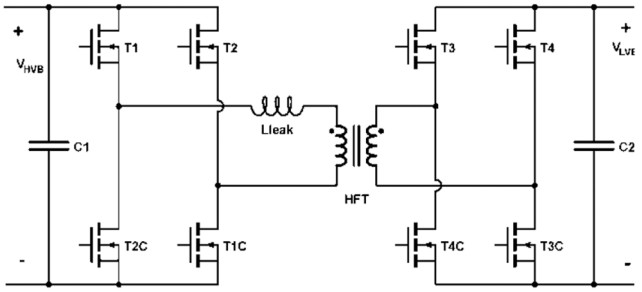


Fig. 7 *Structure of the DAB*

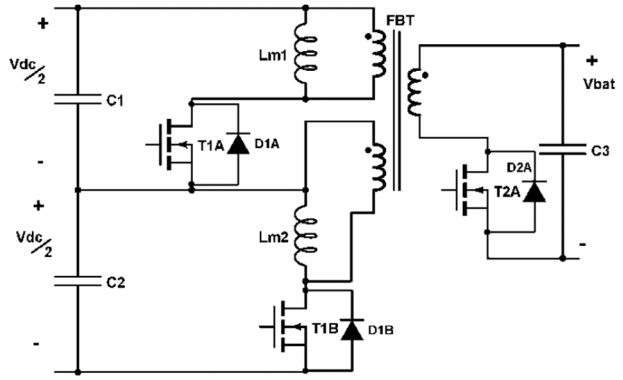


Fig. 8 *Structure of the IBFC with dual winding input*

The DAB consists of two full bridges connected via an HFT and is operated with phase-shift modulation (PSM) [35]. In each phase, a total of eight switches are necessary, and an external inductor is added if the transformer's leakage inductance is not enough. The DAB has inherent isolation, bidirectionality and ZVS possibility. It acts as an ideal current source, and the control is easy to implement. However, it has high current ripple both at the input and the output. To increase the range of the ZVS operation of DAB, the leakage inductance L_{leak} and turn ratio n have to be optimally sized.

On the other hand, the IBFC consists of two or more typical flyback converters in parallel, where the secondary diodes are replaced by a switch to add bidirectionality. The main advantage is the low number of switches and the lower current ripple if a high number of phases are interleaved. In Fig. 8, the flyback transformer has a split primary winding and must have a low leakage inductance to reduce the voltage stress on the switches. QR makes the converter operate with a variable frequency (in this case, 50–200 kHz) and reduces the energy lost due to the output capacitance.

5.2 Optimal configuration and comparison

The design has been performed based on Section 2, and the best topology configuration that was found is shown in Table 4: the 2 phases DAB at 100 kHz and the 4 phases IBFC in QR. The design shows how the use of SiC with QR and interleaving can help enable the use of a flyback topology for higher powers of 10 kW. In terms of the number of components, the IBFC is better as it needs a lower number of MOSFETs but at the same time needs a higher number of diodes. In terms of efficiency, their curves clearly show how the DAB and IBFC perform better at lower and higher output currents, respectively (Fig. 9*a*). The average efficiency for the entire operating range is between 98.03 and 98.57; while the average full load efficiency over the voltage range is between 97.04 and 98.63, respectively, for the DAB and IBFC. Hence, the IBFC performs much better than the DAB in spite of the higher switching frequency, resulting in a higher rating of 4.6.

In terms of size, the DAB has a bigger volume due to the external inductance and larger heatsink, resulting in a lower rating of 1.56 (Fig. 9*b*). Further, the output ripple is much lower for the IBFC by nearly a factor of two. On the other hand, the DAB due to its inherent ZVS and easy PSM gets a higher rating for efficiency improvements and control when compared to the IBFC. When all

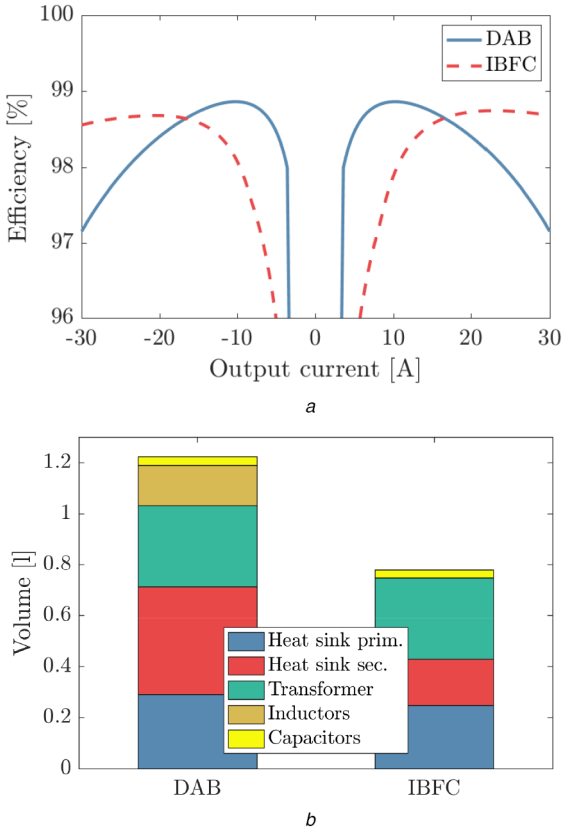


Fig. 9 *Comparison of the efficiency and volume of the EV port converter candidates:*
(a) Converter efficiency for $V_{\text{EV}} = 332$ V, ***(b)*** Volume of the converter

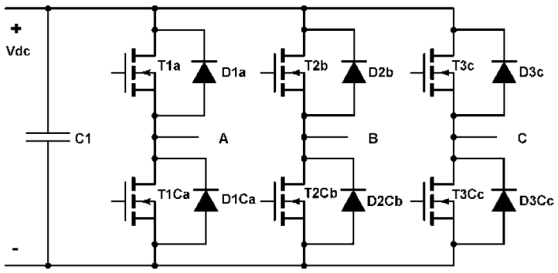


Fig. 10 *Structure of the 2LC*

these factors are combined together in Table 4, it is clear that the IBFC with a score of 91.98 is better topology than DAB with a score of 68.91.

6 Architecture 1 – grid port candidates

6.1 Topologies

The topologies considered for the TPC's grid port converter for architecture 1 are the 2LC, 3LNPC and 3LT2C (Figs. 10–12). Each topology is designed with different modulation techniques: sinusoidal PWM (SPWM), space vector PWM (SVPWM) [53] and near-state PWM (NSPWM) [54] for the 2LC; SVPWM and 2-Medium-1-Zero-Vector PWM (MZVPWM) [55] are applied to both the three-level topologies namely, 3LNPC and 3LT2C.

2LC in is the simplest two-level topology and consists of six switches with freewheeling diodes in anti-parallel. It is the most used DC–AC topology, due to the low number of components and the simple modulation technique. However, it has high THD and high switching losses. The three-level topologies clamp the neutral of the DC bus to the output: the 3LNPC2 clamps using diodes while the 3LT2C relies on MOSFETs with anti-parallel diodes. These topologies have lower output THD and lower output ripple, at the cost of increased components and the modulation

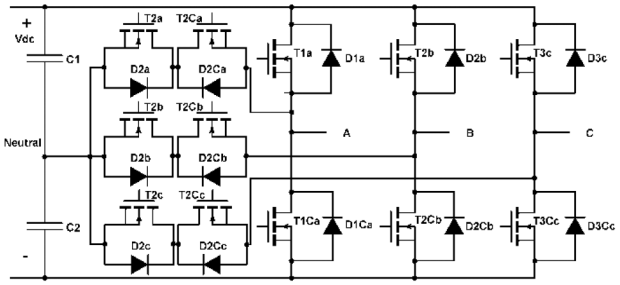


Fig. 11 *Structure of the 3LNPC*

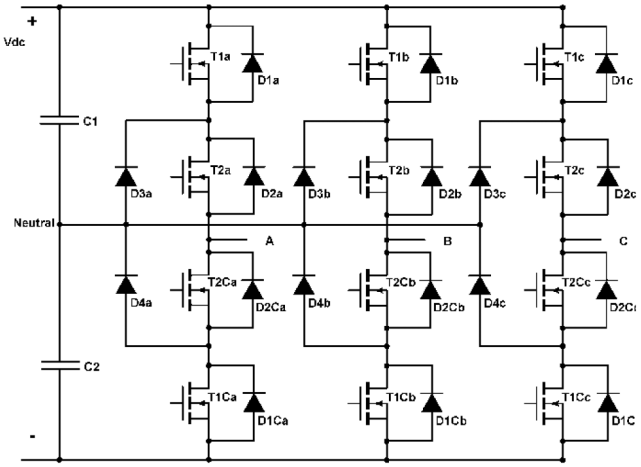


Fig. 12 *Structure of the 3LT2C*

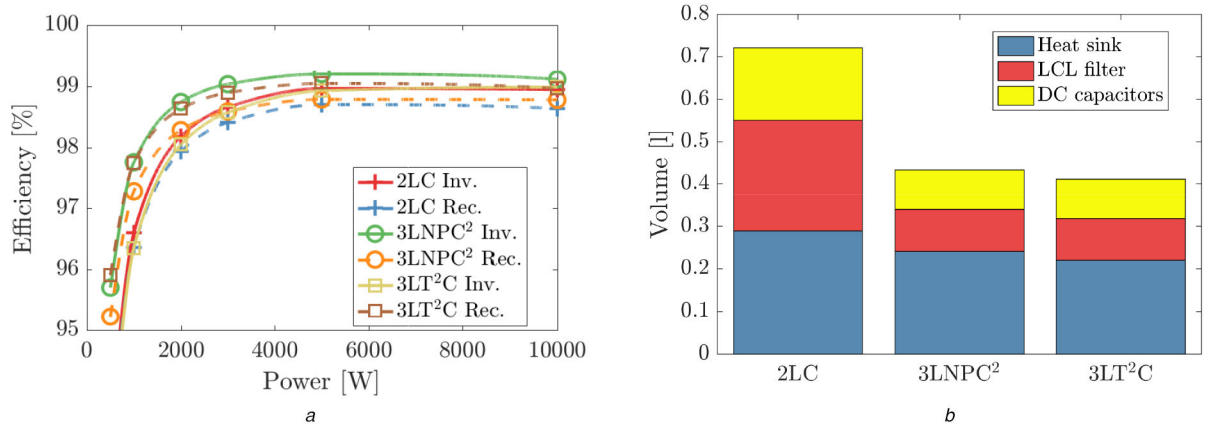


Fig. 13 *Comparison of the efficiency and volume of the grid port converter candidates:*
(a) Converter efficiency for rectifier and inverter mode, ***(b)*** Volume of the converter

complexity. The 3LT2C requires fewer components than the 3LNPC2 but requires higher voltage ratings.

6.2 Optimal configuration and comparison

The best topology configuration for grid port and the modulation strategies are estimated and shown in Table 5: 2LC with SPWM, 3LNPC with SVPWM and 3LT2C with SVPWM, all operating at 50 kHz. The grid topologies are not compared based on the number of cores and capacitors for the output LCL filter as they all require the same number of cores and capacitors but of different values, volume and losses. The converter losses and volume estimation include that of the LCL filter as well.

Fig. 13 shows the efficiency and volume of the grid port topologies. The results indicate a marginally higher efficiency over the operating range (98.73% for 3LNPC compared to 98.41% for 2LC) and much lower volume (0.411 dm^3 for 3LT2C compared to 0.721 dm^3 for 2LC) of the three-level topologies when compared to the 2LC two-level topology. The larger volume of the 2LC stems from the need for larger LCL filter and a bigger DC input capacitor, resulting in a lower rating of 1.79. At the same time, the 2LC has a higher overall score as it requires a lesser number of switches and diodes and has a simpler control getting the highest rating of 5 for all three criteria. Hence, when all the criteria are considered, the 2LC with SPWM is the optimal topology for the grid port with a score of 82.13 as compared to the scores of 71.86, 72.23 for 3LNPC, 3LT2C, respectively.

7 Architecture 2 – impedance-network based

7.1 Operation of quasi Z-source inverter (qZSI)

The qZSI [56, 57] in Fig. 14 is a topology derived from the traditional Z-source inverter (ZSI). It can be used to connect the PV and grid as shown in Fig. 2*b* for architecture 2. The qZSI inherits all the advantages of the ZSI namely lower component ratings and constant DC current from the source. It can realise buck/boost, inversion and power conditioning in a single stage. The qZSI boosts the input voltage by turning on all the switches in the triple bridge, known as the *shoot-through* state. When the converter is not in the *shoot-through* state, it is controlled like the 2LC, with

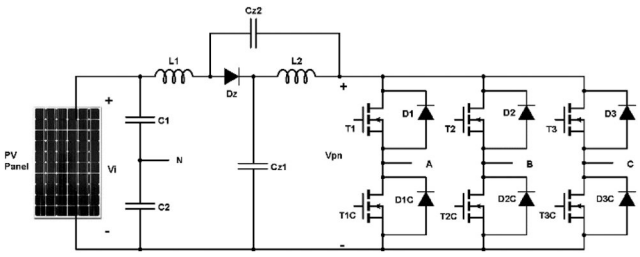
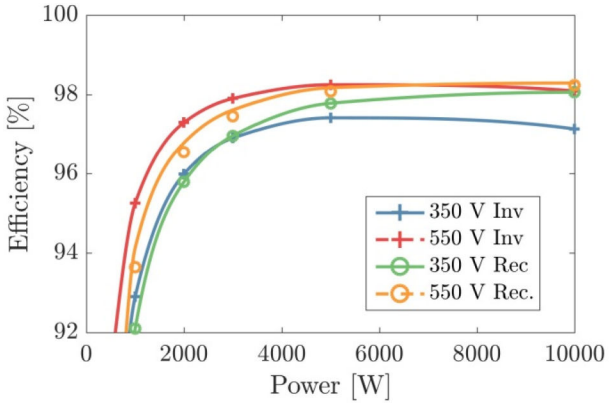
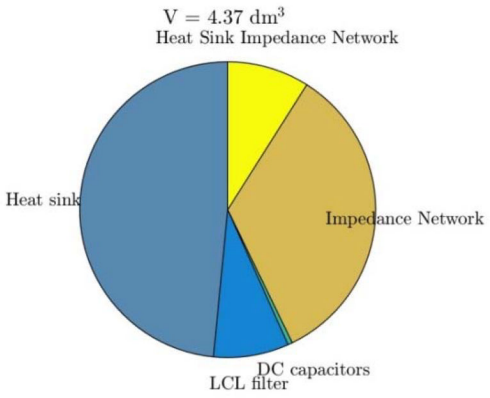


Fig. 14 *Structure of the qZSI*



a



b

Fig. 15 *qZSI*
(a) Efficiency for $V_{pv} = 230$ V, ***(b)*** Volume distribution of the components

SVPWM. The voltages across the capacitors are constant in steady-state, making the topology suitable for connecting to the EV port topologies. However, this voltage ranges between $\sqrt{2}\sqrt{3}V_{ph} = 563$ and 777 V, (the inverter voltage when maximum boost is required) increasing the complexity of designing the EV port converter.

7.2 Design and comparison of topology

Based on Sections 2 and 3, the optimal configuration of the qZSI is determined and is shown in Table 6. The rating R_{ij} for the number of components is estimated separately for the PV and grid part of the qZSI based on Table 2 while it is multiplied by two for the other parameters. The low component count of the Z-source converter results in a high rating for the number of switches and diodes. However, the main problem of the qZSI is the need for two big inductors of L1 = L2 = 1083 µH and four capacitors (C1, C2, Cz1, Cz2) for the impedance network if the ripple and current requirements have to be met.

Each inductor is composed of eight E65 core (configured in two parallel rows of four series inductors) which makes the converter have high losses and large volume. Further, the impedance network diodes have high currents equal to twice the input current, and so, three parallel diodes are needed. It must be noted that the core size is limited to E65 to make the design suitable for PCB mounting and manufacturing and the paralleling of diodes is possible as SiC diodes have a positive temperature coefficient.

The efficiency of the converter is quite high at 50 kHz as shown in Fig. 15*a*. However, most of the losses are concentrated in a small number of semiconductors in the inverter that are responsible for the shoot-through stage, resulting in a big heatsink. The large volume of the heatsink and impedance network can be seen in the volume distribution in Fig. 15*b*. It is for the same reason that the concentrated losses for the 100 kHz design were too high to be dissipated by the heatsinks considered. So, it can be seen that, while the qZSI appears to be a better topology as it requires one semiconductor stage less; it suffers from the disadvantage of the large volume of the impedance network and the concentrated losses in inverter semiconductor. This results in an overall low score of 126.64 as seen in Table 6.

8 Optimal topology for the TPC

In the case of the qZSI, it represents the combination of the PV and the grid converter of architecture 1. This means that the qZSI score must be compared to the summed score of the PV and grid port converters. The lowest and highest summed scores for PV and grid ports converters are 63.02 [TLBC] + 71.86 [3LNPC] = 134.88, and 86.68 [IBC] + 82.13 [2LC] = 168.61, respectively. On the other hand, the final score of the qZSI in Table 6 is 126.64, which is

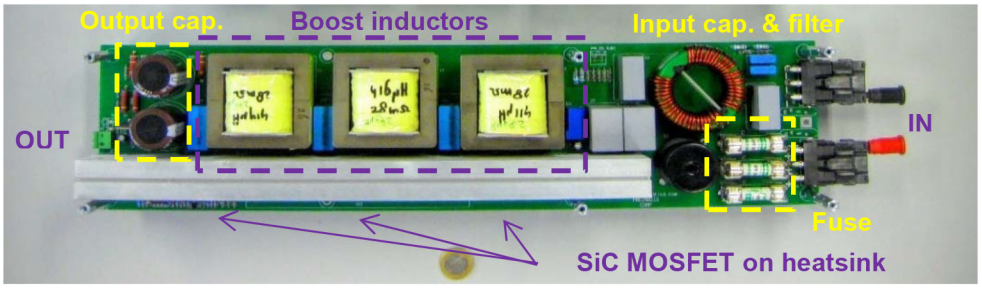


Fig. 16 *Practical setup of 3-phase IBC*

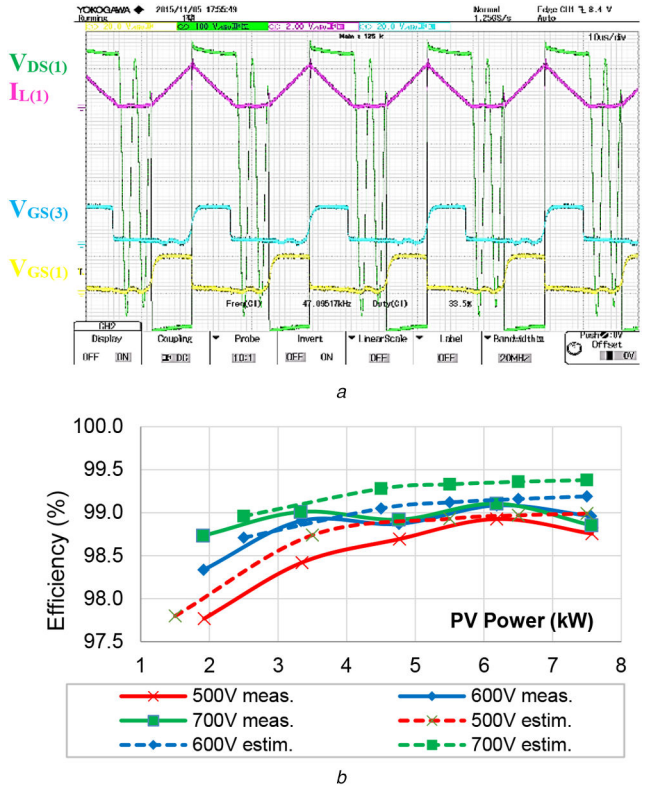


Fig. 17 *Experimental measurements of the 3-leg IBC prototype*
(a) Waveforms for the inductor current I_L, MOSFET drain-source voltage V_{ds} of one leg and the phase-shifted gate-source voltage VGS of the other two legs of the three-phase IBC in DCM, ***(b)*** Comparison of the estimated and measured efficiency of the 10 kW IBC for different input PV voltages at a fixed output voltage of 750 V

much lower than 168.1. Hence the qZSI and architecture 2 is not the preferred topology and architecture for the EV-PV converter.

For architecture 1, the highest scores for each of the three ports were obtained by the 3-leg IBC for the PV port, two-level inverter with sinusoidal modulation for the grid port and a 4-phase interleaved flyback converter for the EV port, with a net score of 86.86 + 91.98 + 82.13 = 260.97. This is hence the best design for the three-port EV-PV power converter with V2G.

It must be kept in mind that the topology scores $T_{score,i}$ are strongly influenced by the weight factors W_j. So, for the same converter specifications and design, the best topology would be different if the weights are adjusted based on the needs of the application. Secondly, instead of weight factors and score, the price of the various components (and their variability) can be used in the comparison framework alternatively to estimate the overall costs. This could be specifically useful when topologies have to be evaluated for a commercial prototype. This is, however, out of the scope of this paper.

9 Verification of loss models

Since the loss models mentioned in Section 2 play an essential role in the converter design and comparison, it is important to validate them experimentally. Hence, a 10 kW 3-phase IBC for the PV port was built based on the specifications in Table 1 and is shown in Fig. 16. The converter is operated at 47 kHz and uses C2M0080120D MOSFETs (with turn-on and turn-off gate resistance of 37.7 and 4.7 Ω), C4D15120A diodes and three 285 µH inductors. The inductors are built using KoolMµ 26 µ E-65 cores with 42 turns of 1000 × 0.071 mm Litz wire having a net resistance of 28 mΩ. The input capacitor is 10 µF, and a 470 nF metal film capacitor is connected at the output of each of interleaved legs. Two 470 µF, 450 V electrolytic capacitors are connected in series to form the DC link buffer. The efficiency and operation of the converter are both estimated using the loss models in Section 2 (ambient temperature of 25°C) and measured experimentally as shown in Fig. 17 using a PV simulator as input (Chroma 62150H-1000S). It can be seen that the estimated and measured efficiencies are close to each other, within 0.2%.

There are several reasons for the difference in efficiencies, which are the limitations of the loss model as well. First, the actual semiconductor junction temperature is different from that estimated by the model which directly affects the conduction and switching losses of the SiC devices. Secondly, the inductor core loss estimation does not consider the DC bias in the inductor current [58]. Thirdly, the loss model linearly extrapolates several values from the datasheet to account for differences between operating conditions and datasheet measurements for device voltage, current, gate resistance and junction temperature. These dependencies are not strictly linear but assumed to be such due to limited information in datasheets. Fourthly, when the IBC operates in discontinuous conduction mode (DCM), only a part of the turn-on energy is lost, and the rest is sent back to the source depending on the parasitic capacitance. This loss model assumes that all energy is lost in the switch during the turn-on process.

10 Conclusion

The paper presented a detailed design and comparison of topologies to find the optimal topology for a 10 kW, grid-connected bidirectional charger for EV that is powered by PV panels. The paper evaluated nine topologies, namely IBC, CIIBC, TLBC, DAB, IBFC, 2LC, 3LNPC, 3LT2C and the qZSI. The topologies were designed considering two switching frequencies (50, 100 kHz), 8 SiC MOSFETs, 13 SiC diodes, 17 core materials of different sizes, varied modulation techniques and a different number of interleaved phases. A multi-criteria framework was then used to quantitatively compare the topologies based on the number of components, efficiency, converter volume, controllability, efficiency improvement and current ripple.

From the evaluation, it was found that architecture 2 that uses the qZSI was not suitable for high power solar EV charging. This is due to the large impedance network and concentrated losses in the inverter semiconductor devices. The overall score was 126.64, and this was much lower than the combined score of 168.61 for the PV and grid ports of DC-link based architecture 1.

On the other hand, the DC-link based architecture 1 needed three converters, one for each of the EV, PV and grid ports. For the PV port, a three-phase IBC at 50 kHz was the best topology with a score of 86.68 mainly driven by its high efficiency, easy control and low component count compared to the CIIBC and TLBC. For the EV port, the four-phase IBFC had a score of 91.98 and was better than the DAB due to its high power density, lower number of switches and low current ripple. For the grid port, the 2LC at 50

kHz with SPWM scored better than the three-level topologies at 82.13, due to lower component count and simpler control while still maintaining a comparable efficiency. Further, the loss models used in the paper were experimentally validated using an IBC setup proving the validity of the approach.

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