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Beikmirza, Mohammadreza; Shen, Yiyu; de Vreede, Leo C.N.; Alavi, Morteza S.

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A Wideband Four-Way Doherty Bits-In RF-Out CMOS Transmitter

Mohammadreza Beikmirza, *Graduate Student Member, IEEE*, Yiyu Shen, *Member, IEEE* , Leo C. N. de Vreede, *Senior Member, IEEE*, and Morteza S. Alavi, *Member, IEEE*

***Abstract*— We present a wideband, 12-bit four-way Doherty Cartesian digital transmitter (DTX) featuring an innovative 50%-LO signed I/Q interleaved up-conversion technique that enables close to perfect orthogonal I/Q summation. The DTX incorporates a compact four-way lumped-element Doherty power combining network to enhance its average efficiency at deep power back-off (DPBO). It comprises a signed second-order hold (SOH) interpolation filter to suppress the sampling spectral replicas significantly. The proposed DTX is realized in a 40-nm bulk CMOS and delivers a peak output power of 27.54 dBm with drain and system efficiencies of 46.35% and 30.77%, respectively, at 5.3 GHz. At 12 dB DPBO, the realized DTX demonstrates a drain efficiency (DE) of 41.74%–39.27% in a 5.2–5.5 GHz band, respectively. Its intrinsic I/Q image, LO leakage, and C-IMD3/H_{3BB} for a 200 MHz tone spacing over a 4.8–6.2 GHz band are −64, −65, and −69 dBc, respectively, without calibration. Applying a simple memoryless 2 × 1-D digital pre-distortion, its error vector magnitude and adjacent channel leakage ratio are lower than −31 dB and −39 dBc, respectively, for a six-carrier "40 MHz 256-QAM OFDM" signal with 18 dBm average output power and a 41% average DE. The signed SOH functionality is verified employing a four-carrier "80 MHz 512-QAM OFDM" signal with spectral purity of better than −35 dBc, while its baseband sampling frequency is 675 MHz.**

***Index Terms*— 50%-LO clock distribution, 8-shape inductor/balun, current-mode class-D (CMCD), efficiency enhancement, in-phase/quadrature (I/Q) interleaving, radio frequency digital-to-analog converter (RF-DAC), sign-bit.**

I. Introduction

OVER the last few years, digital transmitters (DTXs) have increasingly gained popularity as they supercede the circuit building blocks of conventional analog-intensive TXs with radio frequency digital-to-analog converters (RF-DACs) [1]–[20]. These bits-in RF-out TXs feature digital interpolation filters and arrays of digital up-converters with their subsequent digital power amplifiers (DPAs). They offer several advantages: highly efficient operation, direct-digital synthesis (DDS) capability, frequency-agile operation, multi-mode/multi-band functionality, and nanoscale CMOS compatibility, enabling higher integration and reduced die area. Despite these benefits, next-generation DTXs must be augmented by circuit, system, and architectural innovations to satisfy the stringent requirements of modern communication standards. As a result, they must support spectrally efficient wideband modulation schemes, achieve low error vector magnitude (EVM), and meet TX spurious emission requirements. Generally, in-phase/quadrature (I/Q) DTXs are considered superior for wideband application over their polar counterparts due to their linear I/Q operation that avoids bandwidth expansion [21]–[23].

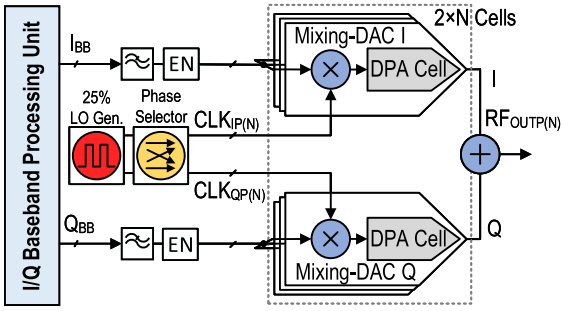

Fig. 1. Conventional 25%-LO I/Q DTX with its signed I/Q phase selector.

Nevertheless, I/Q DTXs can suffer from the interaction between their I and Q paths, especially at higher power levels, giving rise to an I/Q image, in-band nonlinearity, and spectral regrowth. As depicted in Fig. 1, the DTX in [24] uses 25% quadrature clocks and a signed I/Q phase selector to alleviate the I/Q interaction. However, the I/Q interaction predominately remains due to the analog I/Q summation that is prone to mismatch and excessive output parasitics. The design reported in [25] applies an I/Q power-cell sharing method based on time-division multiplexing. In this approach, the up-converted I/Q signals are digitally added together while sharing a single power-cell, coined as IQ-sharing architecture. Still, it requires 25%-LO, which is challenging to realize in the 5 GHz band due to its excessive power consumption of the LO clocks. Alternatively, Deng *et al.* [26] deploy 50% clocks while adopting the phase selector of [24]. Nonetheless, employing 50% quadrature clocks due to their inherent overlap causes a non-orthogonal operation and distortion, entailing sophisticated digital pre-distortion (DPD).

On the other hand, modern communication standards employ modulation schemes, such as 256-quadrature-amplitude modulation (QAM) orthogonal frequency-division multiplexing (OFDM). These modulation schemes feature a

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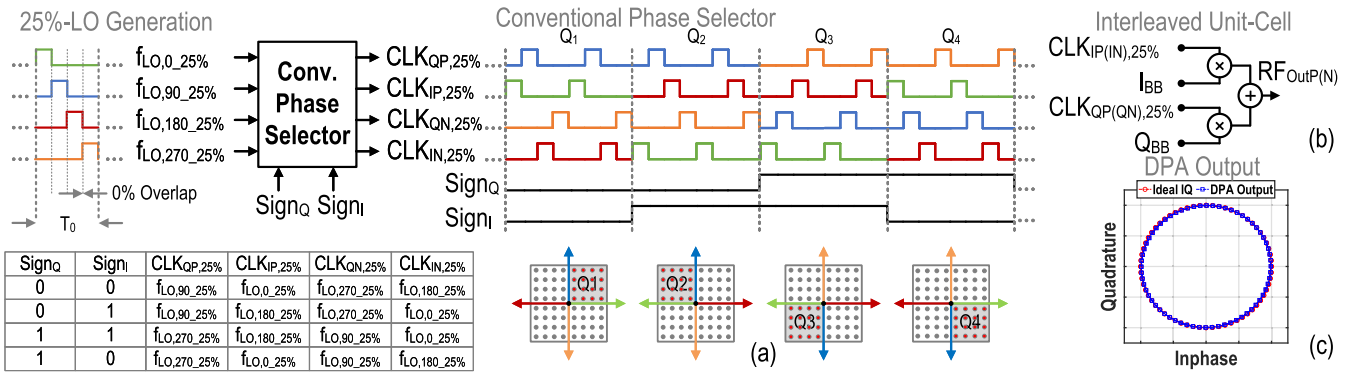
The authors are with the Department of Microelectronics, Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: m.r.beikmirza@tudelft.nl).



$Sign_Q$	$Sign_I$	$CLK_{QP,25\%}$	$CLK_{IP,25\%}$	$CLK_{QN,25\%}$	$CLK_{IN,25\%}$
0	0	$f_{LO,90\_25\%}$	$f_{LO,0\_25\%}$	$f_{LO,270\_25\%}$	$f_{LO,180\_25\%}$
0	1	$f_{LO,90\_25\%}$	$f_{LO,180\_25\%}$	$f_{LO,270\_25\%}$	$f_{LO,0\_25\%}$
1	1	$f_{LO,270\_25\%}$	$f_{LO,180\_25\%}$	$f_{LO,90\_25\%}$	$f_{LO,0\_25\%}$
1	0	$f_{LO,270\_25\%}$	$f_{LO,0\_25\%}$	$f_{LO,90\_25\%}$	$f_{LO,180\_25\%}$

Fig. 2. 25%-LO with conventional phase selector operation. (a) Resulting up-converting quadrature clock waveforms. (b) Idealized interleaved unit-cell. (c) Simulated single-sideband constellation diagram.

high peak-to-average-power ratio (PAPR) (e.g., >10 dB), which requires the DTX to operate in deep power back-off (DPBO), degrading its average efficiency. Many efficiency-enhancement techniques, such as out-phasing [27]–[29], envelop-tracking (ET) [30], and Doherty [31]–[37], are currently adopted in various DPA topologies to enhance their efficiency at DPBO. Two-way Doherty DPAs (DDPAs) are popular due to their less complicated baseband processing and handling large modulation bandwidth, but they typically enhance efficiency at 6 dB PBO. The N-way DDPA improves the efficiency at DPBO while maintaining the simplicity advantage of the DDPA configuration. However, it is incredibly challenging to implement an N-way DDPA since incorporating more DPA banks leads to excessive power combiner losses. In [31], a three-way DDPA architecture with decent overall linearity/efficiency performance has been reported.

Recently in [38], we have introduced a four-way DTX that achieves decent EVM, spectral purity, and efficiency at DPBO. It comprises a 50%-LO signed I/Q interleaved up-converter that facilitates close to perfect orthogonal I/Q summation. Moreover, it incorporates a push-pull low-loss four-way DDPA to enhance its average efficiency. This article elaborates on the system-/circuit-level design considerations and extensive measurement results. Section II introduces the proposed 50%-LO signed I/Q interleaving technique. Section III unveils the compact four-way DDPA. Section IV describes the TX architecture, while Section V demonstrates the measurement results. Section VI concludes this article.

II. 50%-LO Signed I/Q Interleaved Up-Converter

A. Conventional Phase Selector Operation

1) 25%-LO With Conventional Phase Selector Operation: Fig. 2 demonstrates the conventional phase selector operation concept with a 25%-LO clock [39]. Conventionally, to minimize the distortion due to the I/Q overlap, non-overlapping complementary quadrature clocks with a 25% duty cycle are required. In this context, the clock tree is typically implemented using a phase selector that operates directly on these narrow 25%-LO clocks ($f_{LO,0\_25\%}$, $f_{LO,90\_25\%}$, $f_{LO,180\_25\%}$, and $f_{LO,270\_25\%}$). Depending on the four states of the I/Q sign-bits, the related complementary clock pairs can be swapped [see Fig. 2(a)]. Note that, in this conventional approach, the Q sign-bit ($Sign_Q$) only acts on the QP/QN related clocks $CLK_{QP,25\%}/CLK_{QN,25\%}$, while the I sign-bit ($Sign_I$) only operates on the IP/IN related clocks $CLK_{IP,25\%}/CLK_{IN,25\%}$. For example, in the case of a transition from the first quadrant ($Sign_Q = 0$ and $Sign_I = 0$) to the fourth one ($Sign_Q = 1$ and $Sign_I = 0$), since the sign of Q is changed, the corresponding complementary clocks, $CLK_{QP,25\%}/CLK_{QN,25\%}$, are swapped [see table in Fig. 2]. These 25% phase-modulated LO clocks are then directly mixed with the up-sampled baseband data [see Fig. 2(b)], driving in the subsequent power cells to cover the targeted constellation quadrants. Fig. 2(c) shows the simulated single-sideband constellation diagram of the conventional phase selector, indicating correct sign-bit operation without compression due to non-overlapping 25%-LO quadrature clocks. Nonetheless, since this phase selector exploits 25% quadrature LO clocks, it entails practical limitations and causes various issues in the DTX clock trees. First, compared to using 50%-LO clocks, their rise/fall times in the clock tree must be very short, requiring faster buffers in the clock tree and consuming more dc power. Therefore, this approach is less attractive at higher frequencies. Second, compared to 50%-LO clocks, their 25% counterparts are not inherently symmetric and balanced, making them more prone to signal interference, dc offsets, and abrupt transient conditions (e.g., due to the changing sign-bits). These issues yield timing inaccuracies in practical implementations, which, in turn, gives rise to performance nonidealities, such as limited I/Q image rejection and unwanted spectral leakage spurs, especially at higher frequency bands [16], [40]–[42]. These TX spectral spurs increase the far-out spectral noise floor at receiver (RX) bands, which is detrimental. The single-sideband spectrum with 100 MHz tone-spacing and the power consumption breakdown at 2.4 GHz employing global 25%-LO clocks with conventional phase selector is presented in Fig. 3. Accordingly, its I/Q image is −59 dBc, while its digital circuit blocks consume 380.8 mW. The performance of this conventional arrangement will be compared to the proposed method in Section II-B.

2) 50%-LO With Conventional Phase Selector Operation: To address the issues mentioned above, Fig. 4(a) illustrates the resulting waveforms of applying the conventional phase

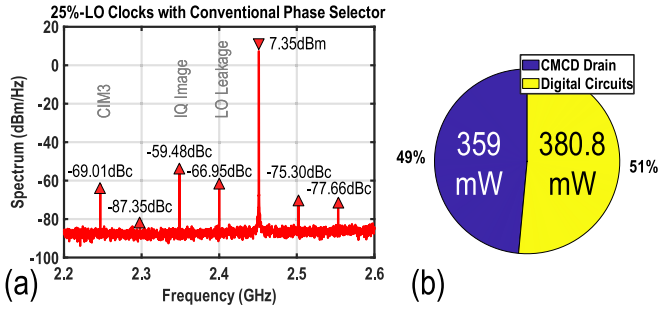


Fig. 3. (a) Single-sideband spectrum with 100 MHz tone-spacing at 2.4 GHz employing 25%-LO clocks with the conventional phase selector. (b) Power consumption breakdown.

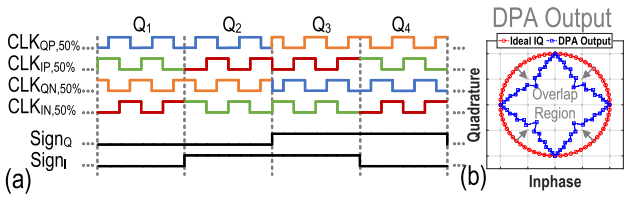


Fig. 4. (a) Resulting up-converting quadrature clock waveforms of 50%-LO with conventional phase selector operation. (b) Simulated single-sideband constellation diagram.

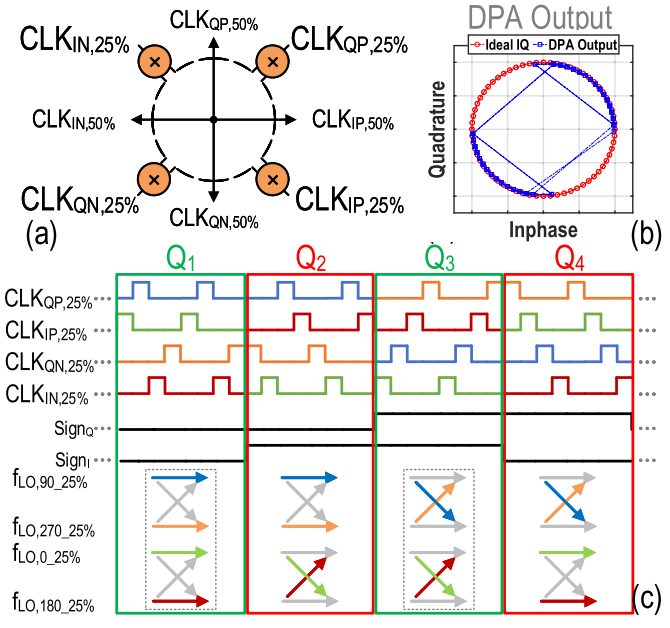


Fig. 5. (a) Possible implementation diagram of 25% clock generation by multiplying the adjacent 50%-LO clocks. (b) Simulated single-sideband constellation diagram. (c) Resulting 25% quadrature clock waveforms.

selector to 50% quadrature LO clocks. Accordingly, this setup leads to correct quadrant selection depicted in Fig. 4(b). However, it causes distortions due to an I/Q overlap, which significantly deteriorates the image-rejection ratio, in-band linearity, and close-in spectral purity [26], [43], [44]. To mitigate this issue, 25% quadrature LO clocks are required when both I and Q are active. Therefore, 25% complementary quadrature LO clocks are generated by multiplying the adjacent 50%-LO clocks together [see Fig. 5(a)]. However, after applying these 25%-LO clocks to the up-sampled baseband data, as shown in Fig. 5(b), it turns out that the sign-bit operation is still incorrect even when using these 25% non-overlapping clocks. Fig. 5(c) compares this latter case with the conventional phase selector using 25%-LO clocks. As illustrated, the resulting clock waveforms are correct in the first/third quadrant (alternate quadrant traverse). Nonetheless, the modified phase selector does not replicate the suitable clock waveforms in the second/fourth quadrant (adjacent quadrant traverse). The reason lies in the fact that both I and Q sign-bits change in an alternate quadrant traverse case, and thus, the clocks preserve their lead/lag phase relation. On the other hand, in an adjacent quadrant traverse condition, one of the I or Q sign-bits changes. Therefore, the clocks do not preserve their lead/lag phase relation. To tackle this issue, we propose a new 50%-LO signed I/Q interleaved up-converter.

B. Proposed 50%-LO Signed I/Q Interleaved Up-Converter

The proposed signed I/Q interleaved up-converter addresses this issue by exploiting global 50%-LO clocks, phase modulated by the sign-bits, along with a new single-sideband I/Q digital up-converter. In this method, the DTX quadrant selection (sign-mapping operation) is realized in two steps: 1) global 50% duty-cycle quadrature clock mapping and 2) local I/Q up-conversion and I/Q interleaving. The remainder of this section elaborates further on the details of these two steps and their design considerations.

1) Step 1: Global 50% Duty-Cycle Quadrature Clock Mapping: Fig. 6(a) illustrates a graphical representation of this step. The DTX clock tree uses 50% square-wave LO clocks ($f_{\mathrm{LO,0\_50\%}}$, $f_{\mathrm{LO,90\_50\%}}$, $f_{\mathrm{LO,180\_50\%}}$, and $f_{\mathrm{LO,270\_50\%}}$), and the conventional clock phase selector described above in Fig. 2 is replaced by the proposed sign-bit phase mapper. As illustrated, in the first step, based on the I/Q sign-bit states, the 50% quadrature clocks are swapped in a particular fashion that contrasts with the typical approach whose complementary clocks are swapped. The table in Fig. 6 summarizes the phase mapping relations for the proposed 50%-LO clocks. In this approach, the I sign-bit impacts both the I-related clock signals ($\mathrm{CLK_{IP,50\%}}$/$\mathrm{CLK_{IN,50\%}}$) operation and, more importantly, the Q-related clocks ($\mathrm{CLK_{QP,50\%}}$/$\mathrm{CLK_{QN,50\%}}$). Similarly, the Q sign-bit affects both Q-/I-related clocks. For example, in the transition from the first quadrant to the fourth one, in the first step, 50%-LO clocks of $\mathrm{CLK_{QP}}$/$\mathrm{CLK_{QN}}$ are swapped with $\mathrm{CLK_{IN}}$/$\mathrm{CLK_{IP}}$, respectively [see Fig. 6(b)]. The proposed 50%-LO quadrature sign-bit mapper scheme enables simple multiplication actions on the resulting clocks ($\mathrm{CLK_{QP,50\%}}$, $\mathrm{CLK_{IP,50\%}}$ $\mathrm{CLK_{QN,50\%}}$, and $\mathrm{CLK_{IN,50\%}}$) to adequately generate 25% up-converting LO clocks for the unit cells, which is described in the next step.

2) Step 2: Local I/Q Up-Conversion and I/Q Interleaving: To complete the up-conversion operation, the required 25%-LO clocks are generated by multiplying the appropriate pair of the phase-modulated 50%-LO quadrature clocks together. A possible implementation is illustrated in Fig. 6(c) showing the generation of the local 25%-LO clocks in each RF-DAC sub-cell ($\mathrm{CLK_{QP,25\%}}$, $\mathrm{CLK_{IP,25\%}}$, $\mathrm{CLK_{QN,25\%}}$, and $\mathrm{CLK_{IN,25\%}}$), by bit-wise multiplying of their corresponding

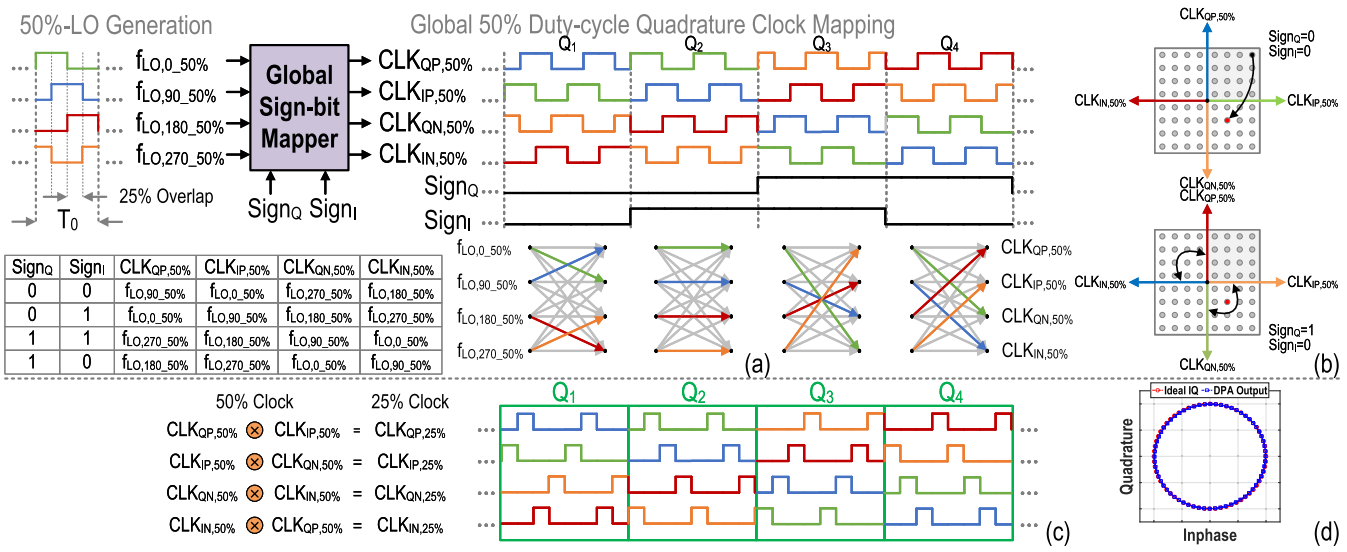


Fig. 6. Proposed global 50% duty-cycle quadrature clock mapping operation. (a) Resulting up-converting quadrature clock waveforms. (b) Example for the first quadrant to the fourth-quadrant transition. (c) Resulting 25% clocks generated by multiplying the adjacent 50%-LO clocks. (d) Simulated single-sideband constellation diagram.

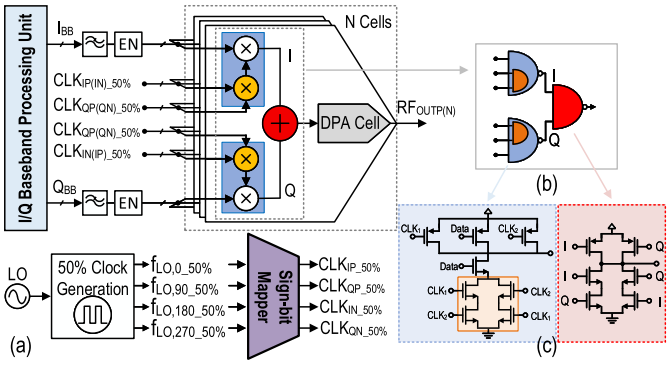


Fig. 7. (a) Schematic of the local 25%-LO clock generation, I/Q up-conversion, and interleaving. (b) NAND gate-based logical implementation circuitry. (c) Two-/three-input symmetrical NAND logic gates.

50% clocks ($CLK_{QP,50\%}$, $CLK_{IP,50\%}$, $CLK_{QN,50\%}$, and $CLK_{IN,50\%}$) with their clockwise adjacent clock ($CLK_{IP,50\%}$, $CLK_{QN,50\%}$, $CLK_{IN,50\%}$, and $CLK_{QP,50\%}$), respectively. Accordingly, as illustrated in Fig. 6(c), the resulting 25% clocks replicate the required clock waveforms in all quadrants. Fig. 7(a) conceptually shows how the 25%-LO clock signals are generated and multiplied with their baseband signals, i.e., I_{BB} and Q_{BB}, performing the up-conversion. The up-converted I/Q bitstreams are combined to fulfill I/Q interleaving. Fig. 6(d) presents the simulation results of the proposed 50%-LO signed I/Q interleaved up-converter concept showing accurate sign-bit operation without compression. It is worth mentioning that the local 25%-LO clock generation and up-conversion are performed using three-input NAND gates [see Fig. 7(b)]. As stated above, 50%-LO clocks are inherently symmetrical. Therefore, they will be less prone to electromagnetic (EM) couplings and interferences, especially when the clock lines are implemented symmetrically. In addition to these symmetrical conditions, the logic gates used for the sign-bit mapper, local I/Q up-conversion, and interleaving circuits are also fully symmetrical to their inputs. Most traditional logic gates do not have this feature. For example, a conventional NAND logic gate is inherently asymmetrical. Therefore, it does not offer precise symmetrical loading to the incoming phase-modulated clock lines. This arrangement jeopardizes the DTX operation due to interfering signals and leads to timing errors. A NAND gate circuitry comprising symmetrical logic gates is employed to address this issue, which provides symmetric input loading and transfer function [see Fig. 7(c)]. By making the clock tree and its loading fully symmetrical, the timing error is remarkably diminished. The single-sideband spectrum with 100 MHz tone-spacing and the power consumption breakdown at 2.4 GHz of the proposed global 50%-LO signed I/Q interleaved up-converter is presented in Fig. 8. Accordingly, the DPA's I/Q image is -67 dBc, while its digital circuit blocks consume 333.8 mW. Compared to Fig. 3, the I/Q image and dc power consumption are boosted by 8 dB, and 47 mW, respectively, at 2.4 GHz. Nevertheless, at higher operational frequencies, employing global 25%-LO clocks becomes impractical, leading to performance degradation. Consequently, the proposed technique facilitates high-frequency I/Q up-conversion by utilizing symmetrical, balanced, and matched 50% quadrature LO clocks in a two-step I/Q phase modulator. Using 50%-LO clocks has benefits that significantly enhance orthogonal summation and system efficiency (SE). Its advantages are given as follows.

1) It lowers the impact of the clock line EM couplings and parasitics.
2) It has more immunity to the duty-cycle distortion.
3) The LO signals in the clock trees are more robust to interfering signals due to their symmetrical operation and balanced loading.
4) It consumes less power.

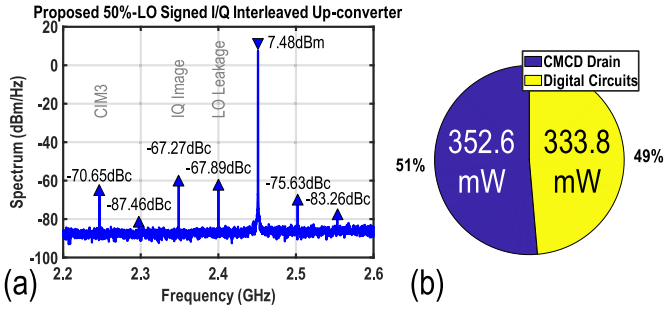


Fig. 8. (a) Single-sideband spectrum with 100 MHz tone-spacing at 2.4 GHz employing the proposed 50%-LO signed I/Q interleaving up-converter. (b) Power consumption breakdown.

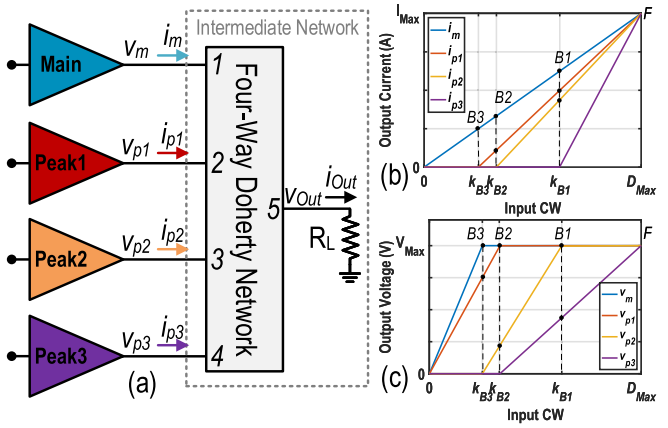


Fig. 9. (a) General four-way DPA with lossless power combining network. (b) and (c) Output current and voltage profiles versus input codeword.

5) It improves its in-band linearity and close-in/far-out spectral purity.

III. Doherty Power Combining Network

As mentioned in Section I, to obtain highly efficient operation at DPBO and generate relatively high average RF power in CMOS technology, a compact four-way DDPA is introduced. Its power combining network comprises four input ports and one RF output for the 50-Ω antenna connection. To facilitate the design of the four-way combiner, an approach similar to [45] has been adopted to design various types of four-way DDPA power combining networks. In this context, as shown in Fig. 9(a), first, the designated five-port power combiner is considered as a five-port black box. Next, its ports' current profiles are determined based on a given set of three free-to-choose peak efficiency power back-off points [i.e., k_{B1}, k_{B2}, and k_{B3} in Fig. 9(b)]. The power combining network is assumed to be lossless and reciprocal. Nevertheless, an intermediate network that includes the power combining network and the DDPA load, R_L, is hypothetically considered to reduce the five-port to four-port configuration. The intermediate network is still reciprocal but no longer lossless because of the 50-Ω lossy load component. The z-parameters can be expressed in terms of voltages and currents by solving (1), as shown at the bottom of the next page, where the subscripts m and pi (i = 1–3) represent the main and peak$i$ (i = 1–3) DPAs, respectively. The second subscripts F and Bi (i = 1–3) represent the full power and back-off points, which are related to its full power by factors of ${k_{B1}}^2$, ${k_{B2}}^2$, and ${k_{B3}}^2$, respectively. The next step is to determine all of the voltage and current variables at the output of each DPA to determine the z-parameters of the intermediate network uniquely. It is worth noting that different sets of boundary conditions result in various power combining networks. In this work, however, the output current of all DPAs at their maximum, i.e., I_{Max}, is considered to be equal, which occurs at full power (F). Due to this boundary condition, the proposed DTX comprises four identical DPA banks to implement the main and peaking power devices. Furthermore, the corresponding peaking DPAs are off before their corresponding back-off points and are active beyond their related back-off point. Thus, the following boundary conditions are considered.

$$\begin{aligned} i_{m,F} &= i_{p1,F} = i_{p2,F} = i_{p3,F} = I_{\text{Max}} \\ i_{p1,B3} &= i_{p2,B3} = i_{p2,B2} = i_{p3,B1} = i_{p3,B2} = i_{p3,B3} = 0. \end{aligned} \quad (2)$$

On the other hand, to maximize the efficiency at full power and the three other back-off points Bi (i = 1–3), the RF voltage amplitude at the output of the relevant devices (main, peak1, peak2, and peak3) has to be maximized at these points, as depicted in Fig. 9(c)

$$\begin{aligned} |v_{m,F}| &= |v_{m,B1}| = |v_{m,B2}| = |v_{m,B3}| = |v_{p1,F}| = |v_{p1,B1}| \\ &= |v_{p1,B2}| = |v_{p2,F}| = |v_{p2,B1}| = |v_{p3,F}| = V_{\text{Max}}. \end{aligned} \quad (3)$$

The output power of the four-way DPA, assuming a lossless power-combining network, can be expressed as a function of its voltage and current variables

$$P_{\text{out}} = \frac{1}{2}\text{Re}\left(v_m i_m^* + v_{p1} i_{p1}^* + v_{p2} i_{p2}^* + v_{p3} i_{p3}^*\right). \quad (4)$$

For the requirement of peak efficiency at the back-off points, the output power of the four-way DPA at the back-off point has a fixed ratio to its full power

$$\begin{aligned} k_{B1}^2 &= \frac{P_{\text{out},B1}}{P_{\text{out},F}} = \frac{\text{Re}\left(v_{m,B1} i_{m,B1}^*\right) + \text{Re}\left(\sum_{i=1}^{2} v_{pi,B1} i_{pi,B1}^*\right)}{\text{Re}\left(v_{m,F} i_{m,F}^*\right) + \text{Re}\left(\sum_{i=1}^{3} v_{pi,F} i_{pi,F}^*\right)} \\ &= \frac{\text{Re}\left(v_{m,B1} i_{m,B1}^* + v_{p1,B1} i_{p1,B1}^* + v_{p2,B1} i_{p2,B1}^*\right)}{\text{Re}\left(v_{m,F} i_{m,F}^* + v_{p1,F} i_{p1,F}^* + v_{p2,F} i_{p2,F}^* + v_{p3,F} i_{p3,F}^*\right)} \end{aligned} \quad (5)$$

$$k_{B2}^2 = \frac{P_{\text{out},B2}}{P_{\text{out},F}} = \frac{\text{Re}(v_{m,B2} i_{m,B2}^* + v_{p1,B2} i_{p1,B2}^*)}{P_{\text{out},F}} \quad (6)$$

$$k_{B3}^2 = \frac{\text{Re}\left(v_{m,B3} i_{m,B3}^*\right)}{P_{\text{out},F}}. \quad (7)$$

In addition, each DPA current is linearly related to its input code when the DPA is active. Consequently, the main DPA currents at back-off points Bi (i = 1–3) are

$$\begin{aligned} i_m &= \frac{I_{\text{Max}}}{D_{\text{Max}}}(D_{\text{in}}) \Longrightarrow \\ i_{m,B3} &= \frac{I_{\text{Max}}}{D_{\text{Max}}}(k_{B3} D_{\text{Max}}) = k_{B3} I_{\text{Max}} \\ i_{m,B2} &= k_{B2} I_{\text{Max}}, \quad \text{and } i_{m,B1} = k_{B1} I_{\text{Max}} \end{aligned} \quad (8)$$

where D_{Max} is the maximum input code of each DPA. Moreover, the peak1 DPA currents at back-off points $B2$ and $B1$ are

$$\begin{aligned} i_{P1} &= \frac{I_{\text{Max}}}{D_{\text{Max}}(1-k_{B3})}(D_{\text{in}} - k_{B3}D_{\text{Max}}) \Longrightarrow \\ i_{p1,B2} &= \frac{I_{\text{Max}}}{1-k_{B3}}(k_{B2} - k_{B3}) \\ i_{p1,B1} &= \frac{I_{\text{Max}}}{1-k_{B3}}(k_{B1} - k_{B3}). \end{aligned} \tag{9}$$

In addition, the peak2 DPA current at back-off point $B1$ is

$$\begin{aligned} i_{P2} &= \frac{I_{\text{Max}}}{D_{\text{Max}}(1-k_{B2})}(D_{\text{in}} - k_{B2}D_{\text{Max}}) \Longrightarrow \\ i_{p2,B2} &= \frac{I_{\text{Max}}}{1-k_{B2}}(k_{B1} - k_{B2}). \end{aligned} \tag{10}$$

Moreover, the current profile of peak3 DPA is represented as

$$i_{P3} = \frac{I_{\text{Max}}}{D_{\text{Max}}(1-k_{B1})}(D_{\text{in}} - k_{B1}D_{\text{Max}}). \tag{11}$$

To complete our set of equations, the reciprocal property of the intermediate network forces to have these relationships: $Z_{12} = Z_{21}$, $Z_{13} = Z_{31}$, $Z_{14} = Z_{41}$, $Z_{23} = Z_{32}$, $Z_{24} = Z_{42}$, and $Z_{34} = Z_{43}$. Afterward, the remaining unknown variables can be uniquely solved using the above independent equations for specific back-off levels k_{B1}, k_{B2}, and k_{B3}, and phase relations between main and peak DPAs. The z-parameters of the intermediate network will then be defined. Next, its s-parameters of the intermediate network can be obtained from the already known four-port z-parameter matrix. Therefore, the five-port s-parameters of the power combining network can be derived from its four-port s-parameters. Note that only the fifth port (which is connected to the load) needs to be reintroduced, and the remaining s-parameters are identical to those of the intermediate network. Since the power combining network is considered to be lossless, the s-parameters of $(N+1)$-port have the following properties:

$$\sum_{n=1}^{N+1} |s_{\text{np}}|^2 = 1 \quad \forall p \quad \text{and} \quad \sum_{n=1}^{N+1} s_{\text{np}} s_{\text{nq}}^* = 0 \quad \forall p \neq q \tag{12}$$

where N represents the power combining network number of ports excluding the load port. Using (12), the unknown variables are s_{5i} $(i = 1\text{–}5)$. The magnitude of s_{51} can be obtained

$$|s_{51}| = \sqrt{1 - |s_{11}|^2 - |s_{21}|^2 - |s_{31}|^2 - |s_{41}|^2}. \tag{13}$$

Thus, we can define $\angle s_{51} = \alpha$, and then, s_{5i} for $i = 2\text{–}5$ are defined as functions of α

$$\begin{aligned} & s_{11}s_{12}^* + s_{21}s_{22}^* + s_{31}s_{32}^* + s_{41}s_{42}^* + s_{51}s_{52}^* = 0 \Longrightarrow \\ s_{52} &= \frac{-1}{s_{51}^*}\left(s_{11}^* s_{12} + s_{21}^* s_{22} + s_{31}^* s_{32} + s_{41}^* s_{42}\right) \\ s_{53} &= \frac{-1}{s_{51}^*}\left(s_{11}^* s_{13} + s_{21}^* s_{23} + s_{31}^* s_{33} + s_{41}^* s_{43}\right) \\ s_{54} &= \frac{-1}{s_{51}^*}\left(s_{11}^* s_{14} + s_{21}^* s_{24} + s_{31}^* s_{34} + s_{41}^* s_{44}\right) \\ s_{55} &= \frac{-1}{s_{51}^*}\left(s_{11}^* s_{15} + s_{21}^* s_{25} + s_{31}^* s_{35} + s_{41}^* s_{45}\right). \end{aligned} \tag{14}$$

Consequently, the s-parameters of the power combiner are known and only depend on the variable α. The phase of α may yield the optimum power combiner topology. Subsequently, the passive network topology of the power combiner can be extracted from the z-/y-parameters of the five-port network (Z_C/Y_C). The general four-way power combiner topology is shown in Fig. 10(a). It is worth mentioning that different passive topologies can be achieved by solving the equations for various phase relations that differ in terms of simplicity, operational bandwidth, and passive efficiency. In some cases, the values of Z_C/Y_C may become complex and not pure imaginary numbers, which indicates that the network is not realizable by the $\lambda/4$ or $3\lambda/4$ transmission lines shown in Fig. 10(a). Since the four-way Doherty network is considered as a black box, thus, any network, whose z-/y-parameter is equal to the calculated z-/y-parameter, can be considered a feasible solution for the desired Doherty network. Fig. 10(c) and (d) depicts two possible arrangements for the four-way Doherty combiner based on $\lambda/4$-line impedance inverter. In this work, the structure in Fig. 10(d) is chosen [46] since, in contrast to the conventional Doherty parallel combiner, the selected configuration has the advantage of a relatively short RF path from the main DPA branch to the load. This arrangement directly improves the DPBO average efficiency [see Fig. 10(e)]. The z-parameter of this network is given as follows:

$$Z_T = \begin{bmatrix} 0 & j\dfrac{Z_{01}Z_{02}}{Z_{03}} & 0 & 0 & -jZ_{01} \\ j\dfrac{Z_{01}Z_{02}}{Z_{03}} & 0 & j\dfrac{Z_{02}}{Z_{05}} & 0 & 0 \\ 0 & j\dfrac{Z_{02}Z_{04}}{Z_{05}} & 0 & -jZ_{04} & 0 \\ 0 & 0 & -jZ_{04} & 0 & 0 \\ -jZ_{01} & 0 & 0 & 0 & 0 \end{bmatrix} \tag{15}$$

where Z_{0i} $(i = 1\text{–}4)$ are the characteristic impedance of the $\lambda/4$-line impedance inverters. Assuming $\alpha = 90°$, Z_C is

$$\begin{bmatrix} z_{11} & z_{12} & z_{13} & z_{14} \\ z_{21} & z_{22} & z_{23} & z_{24} \\ z_{31} & z_{32} & z_{33} & z_{34} \\ z_{41} & z_{42} & z_{43} & z_{44} \end{bmatrix} = \begin{bmatrix} i_{m,F} & i_{p1,F} & i_{p2,F} & i_{p3,F} \\ i_{m,B1} & i_{p1,B1} & i_{p2,B1} & i_{p3,B1} \\ i_{m,B2} & i_{p1,B2} & i_{p2,B2} & i_{p4,B2} \\ i_{m,B3} & i_{p1,B3} & i_{p2,B3} & i_{p4,B3} \end{bmatrix}^{-1} \begin{bmatrix} v_{m,F} & v_{p1,F} & v_{p2,F} & v_{p3,F} \\ v_{m,B1} & v_{p1,B1} & v_{p2,B1} & v_{p3,B1} \\ v_{m,B2} & v_{p1,B2} & v_{p2,B2} & v_{p3,B2} \\ v_{m,B3} & v_{p1,B3} & v_{p2,B3} & v_{p3,B3} \end{bmatrix} \tag{1}$$

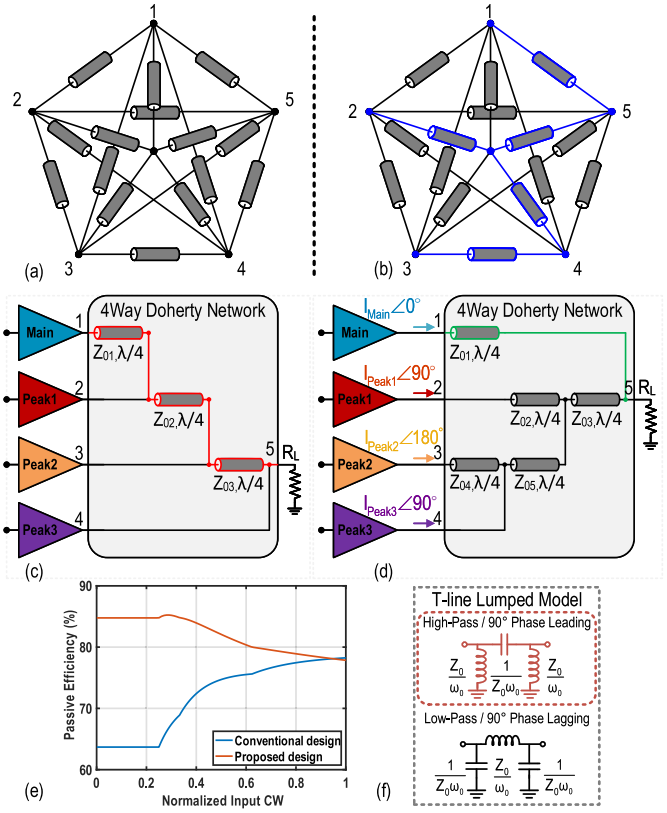


Fig. 10. (a) General topology of the Doherty power combiner. (b) Selected topology. (c) Conventional four-way Doherty parallel power combiner. (d) Proposed (on-chip) Doherty parallel combiner. (e) Simulated passive efficiency. (f) Lumped component model of the T-line.

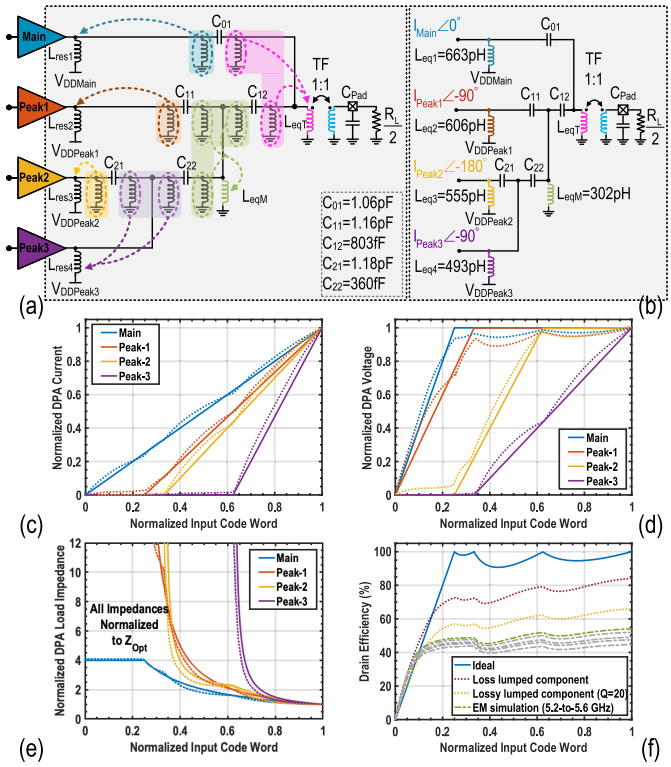


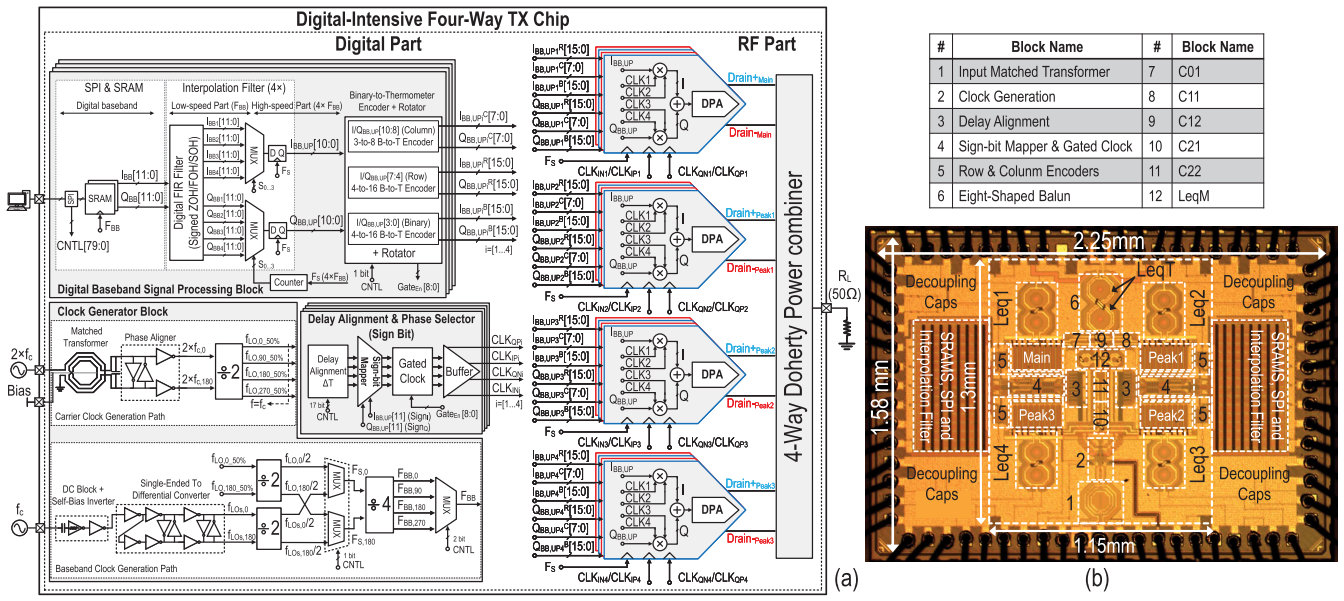
Fig. 11. (a) and (b) Implementation of the four-way Doherty output impedance matching network with consolidated on-chip lumped elements for transmission lines. (c)–(f) Theoretical and simulation (colored dotted lines) results of the proposed four-way Doherty output matching network at 5.4 GHz [EM simulation results of DE in other frequencies are plotted in gray dotted lines in (f)].

calculated as

$$Z_C = \begin{bmatrix} 0 & j17.319 & 0 & 0 & -j25 \\ j17.319 & 0 & j6.946 & 0 & 0 \\ 0 & j6.946 & 0 & -j22.37 & 0 \\ 0 & 0 & -j22.37 & 0 & 0 \\ -j25 & 0 & 0 & 0 & 0 \end{bmatrix}. \tag{16}$$

Solving (15) and (16), the characteristic impedance value of the associated transmission lines can be obtained. Note that Z_{02}, Z_{03}, Z_{04}, and Z_{05} have dependent relation. In our design, $Z_{01} = 25\text{-}\Omega$, $Z_{02} = 22.86\text{-}\Omega$, $Z_{03} = 33\text{-}\Omega$, $Z_{04} = 22.37\text{-}\Omega$, and $Z_{05} = 73.63\text{-}\Omega$. It should be emphasized that our proposed Doherty architecture contrasts with the approach in [31] since, in our work, the phase delay is digitally implemented using the quadrature clocks. Implementing such a transmission line of the DDPA occupies silicon area and exhibits excessive losses, resulting in a significant deviation of its passive efficiency from the theoretical performance. To make the power combiner more compact, the transmission lines can be replaced either with a lumped low- or high-pass π-networks, as shown in Fig. 10(f). Nevertheless, in this work, the $\lambda/4$ transmission lines are approximated by a lumped high-pass equivalent LC π-networks with a $-90°$ phase delay. These high-pass π-networks are equivalent to $3\lambda/4$ transmission lines that require different LO phase relations in the four identical DPA branches connected to the power combiner. Using the proper LO clocks' phases, the I/Q DPA banks' currents drive the four-way DPA combiner, yielding the desired active-load modulation and in-phase power summation.

Fig. 11(a) also shows that the DPAs require RF chokes for the dc feed and second-harmonic termination. Employing the high-pass LC networks facilitates consolidating shunt inductors directly at the output of the DPAs into four inductors L_{eq1}–L_{eq4} that resonate out the associated DPA output capacitance and also provide dc biasing and only one extra inductor L_{eqM}. Moreover, high-pass LC networks allow incorporating the output balun into the DPA power combining network, yielding an even more compact power combiner. Furthermore, the capacitor in the high-pass network acts as an ac-coupled capacitor providing dc voltage isolation to the other DPAs enabling the incorporation of different supply voltages for the individual DPAs [indicated as V_{DDMain}, V_{DDPeak1}, V_{DDPeak2}, and V_{DDPeak3} in Fig. 11(b)]. This technique can potentially improve the efficiency even at deeper power back-off regions. Fig. 11(d)–(f) demonstrates the theoretical and simulated results of the proposed four-way Doherty output matching network. As shown in Fig. 11(f), with loss-less passive components and real active power devices, the DTX achieves an average drain efficiency (DE) of 76% throughout the 12 dB PBO, while this value is 59.73% considering lossy inductors with a quality factor of $Q = 20$. The DTX delivers



#	Block Name	#	Block Name
1	Input Matched Transformer	7	C01
2	Clock Generation	8	C11
3	Delay Alignment	9	C12
4	Sign-bit Mapper & Gated Clock	10	C21
5	Row & Colunm Encoders	11	C22
6	Eight-Shaped Balun	12	LeqM

Fig. 12. (a) Detailed block diagram of the proposed four-way Doherty I/Q DTX. (b) Chip microphotograph.

an average DE of 49.73% incorporating EM simulation of the complete structure. The physical layout floorplan of the proposed four-way Doherty power combiner will be revealed and further discussed in Section IV.

IV. Implementation Details

An overview of the architecture is illustrated in Fig. 12(a). It comprises digital and RF parts. The digital part includes the digital baseband signal processing block, the LO and sampling clock generator block, the phase (sign-bit) selector block, and the digital I/Q interleave banks. In addition, the RF part consists of digital power cells and the four-way power combiner. In the remainder of this section, its building blocks will be sequentially disclosed, and their circuit design techniques will be described.

A. Clock Generation And Distribution

An off-chip single-ended clock operating at $2 \times f_C$ is applied to a matched on-chip transformer, which converts the unbalanced clock to its balanced counterpart. Fig. 13(a) exhibits the layout of the matched input transformer. A recursive design is performed to achieve matched wideband transformer with negligible amplitude and phase mismatch. The transformer outer diameter is 185 μm $\times$ 185 μm. The EM simulation results using Momentum are plotted versus frequency in Fig. 13(b)–(e), including the magnetic coupling factor K_m, primary and secondary inductances L_P and L_S, winding resistances R_P and R_S, and quality factors Q_P and Q_S. At 12 GHz, these parameters are $K_m = 0.389$, $L_P = 412$ pH, $L_S = 832$ pH, $R_P = 1.9$-Ω, $R_S = 6.9$-Ω, $Q_P = 16.8$, and $Q_S = 9.1$, respectively. The next stage has a large impedance. Thus, a parallel resistor of 250-Ω and a capacitor of 220 fF are added differentially to transform these differential loads into an optimum single-ended primary load, facilitating the matching condition. The EM simulation

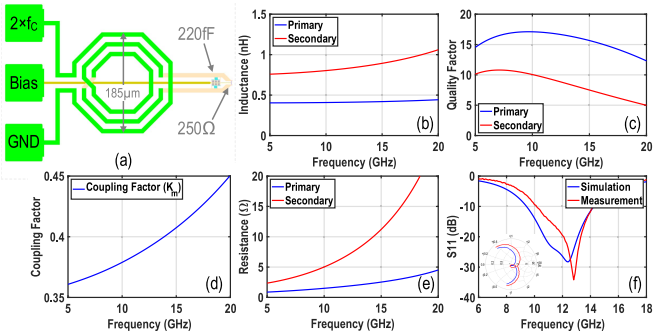


Fig. 13. (a) Layout of the input unbalanced-to-balanced transformer. (b)–(e) EM simulation results of the input balun. (f) Simulated versus measured S_{11}.

and measured s-parameters of Fig. 13(f) represent a good matching condition at the transformer input. Utilizing this matched transformer at the transmitter's input, the required power for the off-chip single-ended LO at 10.8 GHz is 5 dBm. Therefore, considering 27.54 dBm output power at this frequency, the LO-IN RF-Out power conversion gain is roughly 22 dB. Although the transformer's differential layout traces are completely symmetrical, a phase aligner comprising a back-to-back inverter pair is employed at the transformer output to prevent any misalignment. The phased aligned differential $2 \times f_C$ clocks, i.e., $2 \times f_{C,0}$ and $2 \times f_{C,180}$, are applied to a divide-by-2 circuit to generate the desired 50%-LO clocks at f_C with a relative phase difference in multiples of 90°. These complementary quadrature LO clocks are $f_{\mathrm{LO,0\_50\%}}$, $f_{\mathrm{LO,90\_50\%}}$, $f_{\mathrm{LO,0\_180\%}}$, and $f_{\mathrm{LO,270\_50\%}}$ in Fig. 12(a). The divide-by-2 circuit is implemented as a flip-flop-based frequency divider that consists of four C^{2}MOS latches arranged in a loop [24]. All other divide-by-2 circuits also utilize the same structure. The transistor sizing, however, is adjusted based on its operational frequency.

On the other hand, the master/baseband sampling clocks (F_S/F_{BB}) are generated by employing two different approaches. In the first method, these clocks can be created from the existing carrier clock by applying one of its complementary clock pairs (e.g., $f_{LO,0\_50\%}/f_{LO,180\_50\%}$ or $f_{LO,90\_50\%}/f_{LO,270\_50\%}$) to another divide-by-2 circuit. By utilizing this arrangement, the F_S clock operates at $f_C/2$, resulting in direct dependency of the baseband modulation bandwidth to its carrier operating frequency. In the second method, independent master/baseband clocks can be generated using another off-chip single-ended clock running at $2 \times F_S$. Using an active unbalanced-to-balanced converter and a subsequent divide-by-2 circuit, the F_S clock is generated. This master clock is then applied to a divide-by-4 circuit to generate the F_{BB} clock. The following block is a multiplexer to select the appropriate baseband clock. It is worth mentioning that, to mitigate the crosstalk mostly caused by capacitive coupling, ground lines were placed in-between the quadrature LO lines. In addition, to suppress the LO leakage, shielding is utilized to diminish the coupling from other routing lines, e.g., data routing, when multiple crossover lines occur.

B. Delay Alignment and the Phase (Sign-Bit) Selector

1) Delay Alignment: The required Doherty phase relations of the DPA branches are digitally implemented by appropriately swapping carrier quadrature clocks. To compensate for different design variations, such as the process/voltage/temperature (PVT), frequency, and load variations on Doherty phase relations, fine-tune phase aligners are adopted [17] and implemented, as shown in Fig. 14. Their controlling signals are static and come from a serial-to-parallel interface (SPI). A binary-to-thermometer encoder converts the 4-bit input binary code (CNTL⟨1:4⟩) to a 15-bit thermometer code where each bit is used as a delay control bit for a delay cell. The delay line can be bypassed or employed by the Enable bit. The absolute delay of each delay cell is controlled with a single bit by enabling or disabling NMOS and PMOS transistors in series with the supply/ground paths. The RF clock passes through 15 cascaded delay cells to arrive at the output, resulting in a total relative delay of 85 ps with a resolution of roughly 5.5 ps, which is more than enough to compensate for the variation mentioned above.

2) Phase selector: The following stage is the carrier clock phase selector. As demonstrated in Fig. 15, it is implemented as four NAND-gate-based multiplexers with its input selection control signals of $\text{Sign}_I = I_{BB,up}[11]$ and $\text{Sign}_Q = Q_{BB,up}[11]$ [see Fig. 12(a)]. As depicted in Fig. 12(b), four controlling signals of C_1, C_2, C_3, and C_4 are first generated by ANDing the corresponding I/Q sign-bits and subsequently applied to the phase mapper. Based on the four different states of the I/Q sign-bits, the 50% phase-modulated quadrature clocks fed to the DPA can adequately be swapped, and thus, the entire four-quadrant I/Q plane can be covered. To equalize the delays of the clocks, the NAND gates are implemented in a fully symmetric configuration [see Fig. 15(c)]. Moreover, due to employing 50%-LO clocks, a back-to-back inverter pair is employed to align further the phases of the complementary clock pairs.

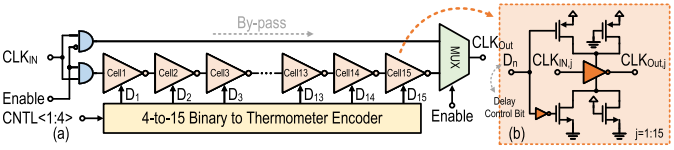


Fig. 14. (a) Schematic of the 4-bit fine-resolution delay line and (b) its delay-cells.

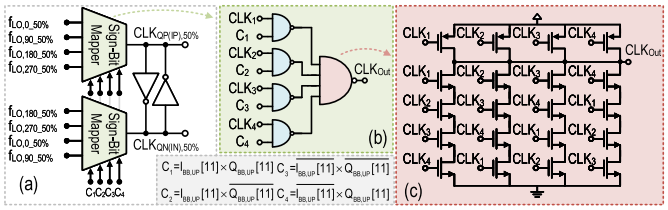


Fig. 15. (a) Schematic of the global 50%-LO quadrature clock mapper. (b) NAND gate-based multiplexer implementation circuitry. (c) Four-input symmetrical NAND logic gate.

C. 11-Bit I/Q DPA Floor Plan

The transmitter comprises four identical 12-bit resolution I/Q banks (including the sign-bit) that act as four I/Q RF-DACs. Fig. 17(a) depicts the implementation details and the floorplan of one of the I/Q banks. For each bank, the digital I/Q baseband data (I_{BB}/Q_{BB}[11:0]) are stored on a 4-K SRAM and clocked at F_{BB}, which are programed through the low-speed SPI interface. The 12-bit digital I/Q baseband signals passed through a "signed" zero-/first-/second-order hold (ZOH/FOH/SOH) FIR filter to up-sample by a factor of 4 ($F_S = 4 \times F_{BB}$) and low-pass filter the up-sampled I/Q baseband data, suppressing the sampling spectral replicas (SSRs) [22]. Fig. 16 unveils the detailed multiplexer implementation and the corresponding waveforms. The DFF at the input of the MUX is clocked at F_{BB} and re-times the output data of the digital FIR filter ($I/Q_{BB1}[i]$, $I/Q_{BB2}[i]$, $I/Q_{BB3}[i]$, and $I/Q_{BB4}[i]$, where $i = 0$–11). As illustrated in Fig. 16(b), the pulsewidth of the selection signals driving the transmission gates (S_0–S_3) are $1/F_S$, which are realized by bitwise ANDing of the proper F_{BB} clocks pairs [see Fig. 16(c)]. Accordingly, the multiplexer performs the $4 \times$ up-sampling and summing operation by generating three zeros and merely one sample of the input signal during one period of the baseband signal. The DFF at the output is clocked at F_S and re-times the up-sampled and interpolated I/Q data, resulting in ZOH function at F_S, and FOH/SOH suppression at multiples of F_{BB}. This FIR filter architecture contrasts with the approach in [22] since, in our work, it is implemented for signed baseband data. $I_{BB,UP}$[10:0], and $Q_{BB,UP}$[10:0] represent the interpolated un-signed binary digital codes that must be converted to corresponding thermometer codes to avoid nonmonotonic behavior and mid-code transition glitches. However, the pure thermometer-coded approach increases the complexity of the encoders, the chip area, interconnect parasitics, and power consumption. Thus, in this design, a segmented approach

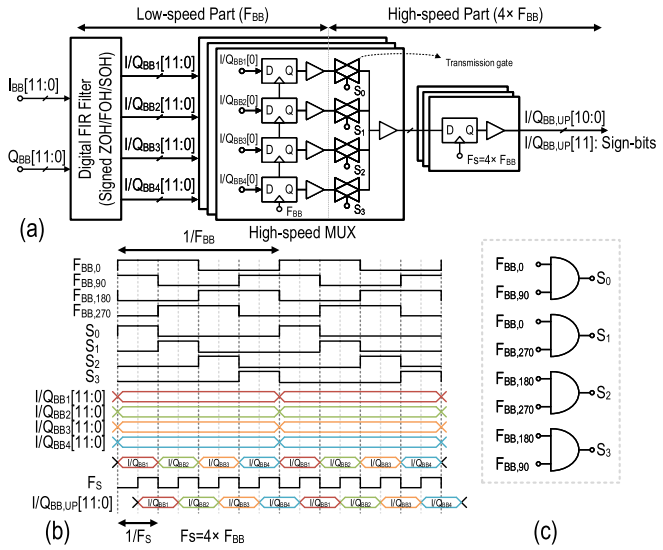


Fig. 16. Interpolation filter and its high-speed MUX. (a) Detailed implementation. (b) Corresponding waveforms. (c) Generating MUX selection signals from different phases of the F_{BB} clock [22].

with 4-bit ($I/Q_{BB,UP}[3:0]$) binary-weighted LSB and 7-bit ($I/Q_{BB,UP}[10:4]$) thermometer-coded MSB cells is adopted. Therefore, the I/Q bank implementation requires 128 MSB, with an aspect ratio of $W/L = 19.2$ μm/40 nm, which are realized as eight parallel cascoded transistors with an aspect ratio of $W/L = 2.4$ μm/40 nm and 16 LSB units with an aspect ratio of $W/L = 1.2$ μm/40 nm. Moreover, the 7-bit MSB ($I/Q_{BB,UP}[10:4]$) is split into 3-bit ($I/Q_{BB,UP}[10:8]$) for a column encoder and 4-bit ($I/Q_{BB,UP}[7:4]$) for a row encoder. Hence, the 128 MSB units of each part are arranged such that they comprise 16 rows ($I/Q_{BB,UPR}[15:0]$) and eight columns ($I/Q_{BB,UPC}[7:0]$). Furthermore, the LSB units comprise 16 small unit cells ($I/Q_{BB,UPB}[15:0]$) that occupy a column. In the I/Q RF-DACs floorplan, the "snake" traverse movements are performed among sub-cells to preserve continuity and improve the differential nonlinearities (DNLs). Fig. 17(d) presents the simulated transient voltage and current waveforms of the final stage. As can be seen, the waveforms are no longer ideal square waves or half-sinusoids due to device parasitic capacitance. However, the overlap between high voltage and high current is a small fraction of the whole period.

Instead of having two separate push-pull banks, an interdigitated push-pull layout is implemented. In other words, every other column of the I/Q RF-DAC matrix is dedicated to the in-phase arrays and their 180° out-of-phase counterparts. This technique reduces the overall I/Q RF-DAC core size for the same achievable output power resulting in a highly compact area, minimal mismatch, fewer parasitics, and power consumption leading to an improved overall DTX efficiency. To equalize the primary output traces, swapped/cross-coupled routings for the in-phase and out-of-phase drain lines are utilized. A data-aware clock gating technique [47], [48] is also employed to reduce LO distribution power in the back-off and enhance the SE at these levels.

The I/Q RF-DAC sub-cells comprise two parts: a pure digital logic section and a power-cell part [see Fig. 17(b)].

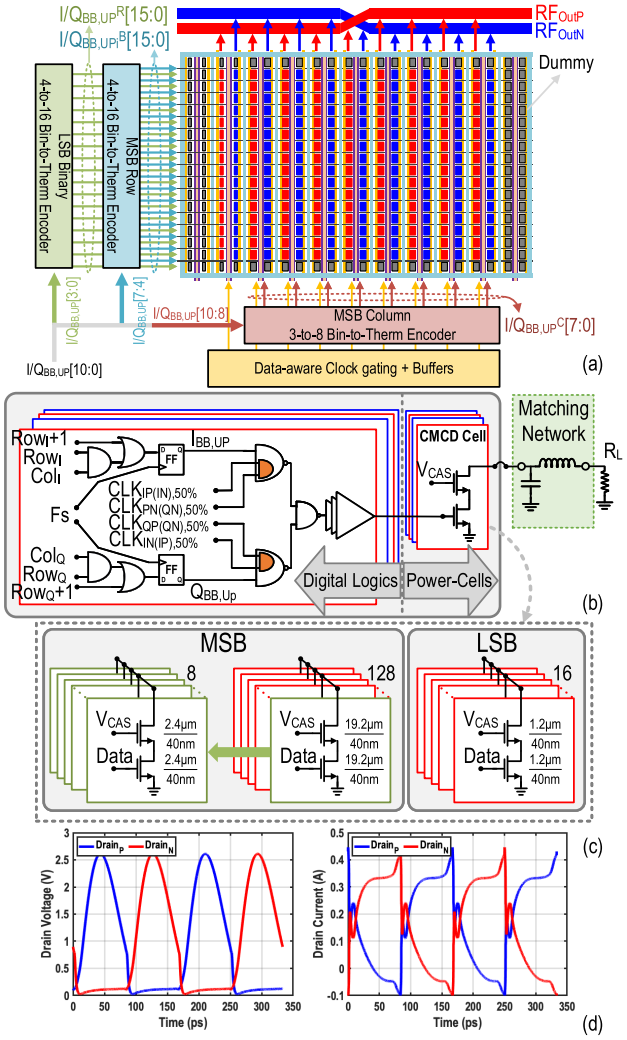


Fig. 17. (a) 11-bit I/Q DPA floor plan. (b) I/Q RF-DAC sub-cells. (c) MSB and LSB power cells aspect ratios. (d) Simulated transient voltage and current waveforms.

The logic part consists of a decoding logic and a time synchronizer flip-flop followed by an I/Q implicit mixing circuit. The AND–OR decoder determines whether the designated cell should be activated. The master/slave DFF is employed to synchronize all I/Q RF-DAC unit cells to the master clock (F_S), diminishing undesirable spectral impurity related to an early–late arrival of each unit cell's input data. Before the mixing operation, the designated 25%-LO generation is performed using a three-input NAND gate. Next, the synchronized digital data are up-converted by 25%-LO clocks using the bitwise AND operation. Subsequently, the up-converted I/Q bitstreams are combined by the subsequent NAND gate to fulfill I/Q interleaving and fed to the power cell inverter buffers. As stated previously, the orthogonal summing of the I and Q paths is achieved by employing the complementary quadrature 25%-LO clocks at this stage. As a result, the local 25% duty-cycle generation and up-conversion circuit are among the most crucial building blocks of the DPA chain. All critical digital logics are implemented based on symmetrical gates to equalize the delay from the input to the output and the fan-out

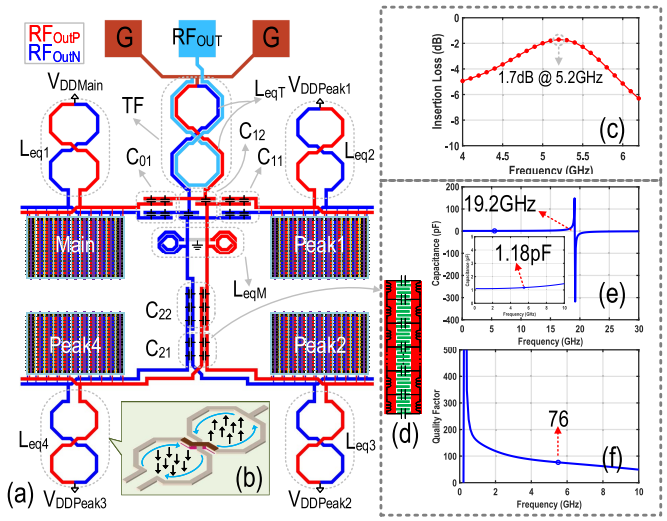


Fig. 18. (a) Physical layout implementation of the four-way Doherty DTX configuration. (b) 8-shaped inductor's EM fields. (c) Simulated insertion loss of the Doherty network. (d) Implemented distributed series ac-coupling capacitors. (e) EM simulation of the C_{21} capacitance. (f) Quality factor of the C_{21}.

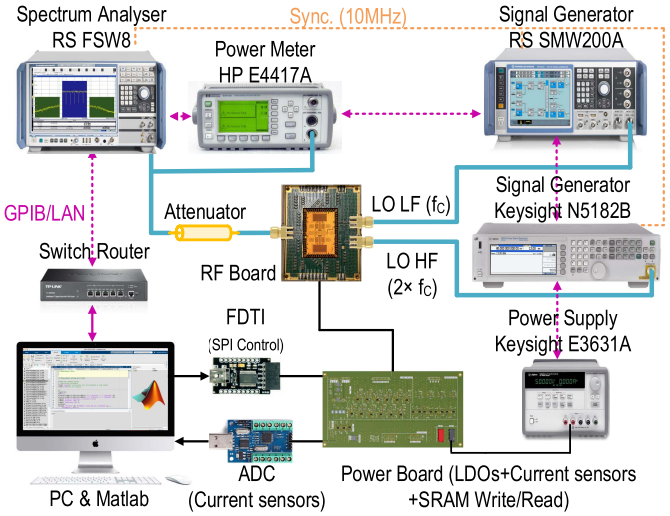


Fig. 19. Measurement setup.

for proceeding circuitry. The power cells are current-mode class-D (CMCD) PAs [49], [50] driven by three-stage digital buffers. Meanwhile, since, in the CMCD, the drain voltage can exceed two to three times the supply voltage, thus, a cascode topology is adopted in this design for preventing reliability violations.

D. Doherty Power Combiner Floor Plan

Fig. 18(a) illustrates the Doherty power combiner floor plan. Its layout can be so compact that the four-way combiner's inductors suffer from undesired magnetic couplings between the different Doherty branches. Consequently, 8-shaped inductors that offer self-cancellation of their EM field are implemented. As illustrated in Fig. 18(b), the inductors provide an opposite orientation of the magnetic flux for their coil loops to avoid unwanted magnetic coupling between the closely spaced DPAs. As depicted in Fig. 18(d), to bridge a physical distance between the DPA banks, the series ac-coupling capacitors (C_{01}, $C_{12}, \ldots, C_{22}$) are implemented as distributed capacitors. As illustrated, these distributed capacitors can be modeled by a series LC-network that provides the same susceptance at the fundamental frequency as the original floating capacitors in the high-pass sections. The EM simulation results of C_{21} are presented in Fig. 18(e) and (f). As depicted, the capacitance value is exactly 1.18 pF, as the originally designed C_{21} value in the high-pass section, while the self-resonance frequency of the LC-network occurs at 19.2 GHz, far enough from the designated operational bandwidth of the DTX. The quality factor of this capacitor is $Q = 76$ representing its broadband operation. As demonstrated in Fig. 18(c), the EM simulated insertion loss is approximately 1.7 dB at 5.2 GHz.

V. Experimental Results

The proposed DTX is designed and fabricated in the 40-nm bulk CMOS. Fig. 12(b) exhibits the chip micrograph, while the block names are specified in a table. The chip occupies an area of 2.25 mm × 1.58 mm with a core area of 1.3 mm × 1.15 mm, as shown in Fig. 12(b). Moreover, the SPI, the designated SRAMs, and the low-speed part of the interpolation filter are digitally synthesized and occupy an area of 2×0.67 mm × 0.38 mm, while decoupling capacitors and I/O pads occupy the remainder. The measurement setup is shown in Fig. 19. The I/Q data are generated in MATLAB and then applied to the DTX using four on-chip 4-K SRAMs (one SRAM for each I/Q DPA) running at $F_S = 675$ MHz. The power consumption of all blocks (except the SRAMs) is included in the reported SE.

A. Static Measurements

The DTX is first characterized by static measurements. The output power is measured using a power meter. Fig. 20(a) presents the measured output power, DE,[1] and SE[2] over a 4–6.2 GHz band under the static input condition of $I_{\mathrm{BB}} = Q_{\mathrm{BB}} = 2047$ for all DPAs. The proposed bits-in RF-out transmitter generates 27.54 dBm peak output power and 46.35% DE at 5.3 GHz with a supply voltage of 1 V dedicated to each DPA. It achieves a 3 dB bandwidth of 1.3 GHz in a 4.6–5.9 GHz band, while the 1 dB bandwidth is roughly 5–5.6 GHz, maintaining decent performance. To measure the DTX PBO performance, the corresponding $I_{\mathrm{BB}}/Q_{\mathrm{BB}}$ data are swept based on the current profile of the main and peak DPAs, as discussed in Section III. The measured drain and system efficiencies versus output power at different frequencies are presented in Fig. 20(b), yielding a DE of 37.35/35.47/33.49%, 40.33/38.11/36.95%, 43.49/41.06/40.6%, and 41.74/40.16/39.27% for 6/9/12 dB PBOs at 5.2/5.3/5.4/5.5 GHz, respectively. These results indicate that the realized compact four-way Doherty DTX maintains its decent drain and system efficiencies enhancement

[1] $\mathrm{DE}(\%) = 100 \times (P_{\mathrm{RF_{Out}}})/(P_{\mathrm{dc-Power\ Cells}})$.
[2] $\mathrm{SE}(\%) = 100 \times (P_{\mathrm{RF_{Out}}})/(P_{\mathrm{dc-Power\ Cells}} + P_{\mathrm{dc-All\ Blocks\ (Except\ SRAMS)}})$.

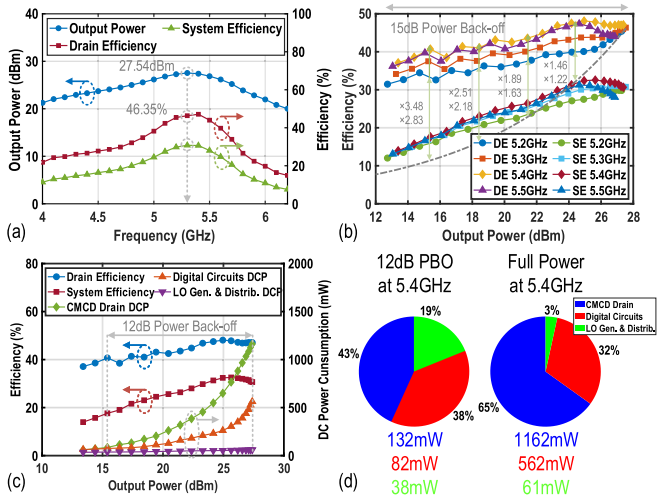


Fig. 20. Measured (a) peak output power, drain, and system efficiencies versus operational frequency, (b) drain and system efficiencies versus output power at different frequencies, (c) drain/system efficiencies, and the related dc power consumption versus power back-off at 5.4 GHz, and (d) power consumption breakdown at the full power and 12 dB back-off at 5.4 GHz frequency.

over DPBO. Fig. 20(c) demonstrates the drain/system efficiencies and the related dc power consumption versus power back-off at 5.4 GHz. Fig. 20(d) represents the power consumption breakdown at the full power and 12 dB back-off at 5.4 GHz frequency. As expected, the SE degrades more in lower codewords as it includes the power consumption of circuit blocks that do not scale with the output power. However, utilizing more effective clock gating mitigates this issue.

B. Single-Sideband Signal Measurements

The performance of the proposed DTX versus power back-off is measured with a single-sideband signal at 5.4 GHz with 200 MHz tone-spacing, and the output spectrum and corresponding I/Q image, LO leakage, and C-IMD3/H_{3BB} suppression are demonstrated in Fig. 21(a) and (b), respectively. Hence, the uncalibrated I/Q image, LO leakage, and C-IMD3/H_{3BB} preserve their approximate value of $-64/-65/-69$ dBc over the power back-off. In addition, the I/Q trajectory depicted in Fig. 21(c) shows that the proposed 50%-LO signed I/Q interleave up-converter retains its orthogonal summation enhancement over the output power back-off, and it demonstrates correct sign-bit operation without compression. Moreover, the single-sideband performance over the frequency band of 4.5–6 GHz dependent on tone-spacing of 10–140 MHz is presented in Fig. 21(d)–(f). The intrinsic LO leakage, I/Q image, and C-IMD3/H_{3BB} remain better than $-64/-60/-67$ dBc, respectively, without calibration while measuring five different samples of the proposed DTX.

C. Complex Modulated Signal Measurements

The DTX dynamic performance is also verified by employing OFDM signals with different modulation bandwidths.

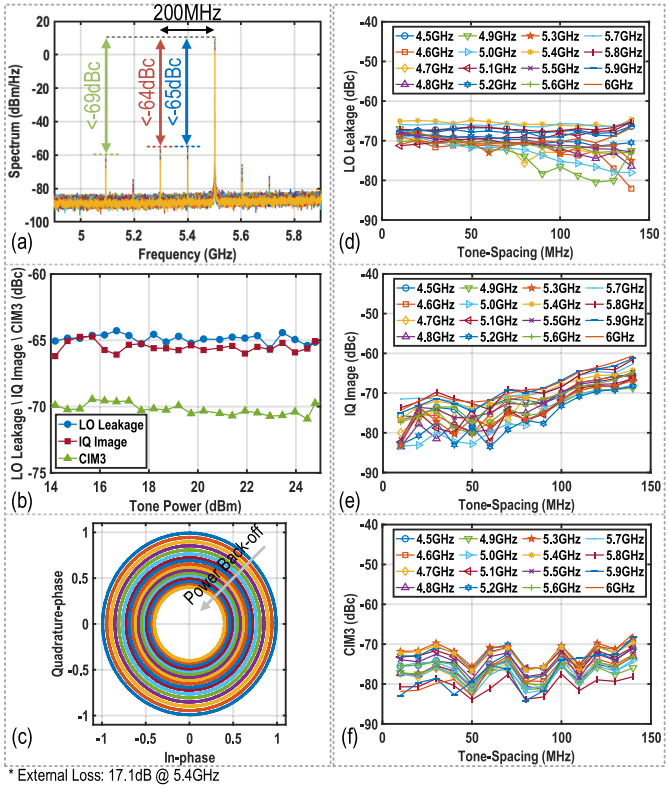


Fig. 21. Measured (a) output spectrum of a single-tone test with 200 MHz tone-spacing at 5.4 GHz versus power back-off, (b) its corresponding LO leakage, I/Q image, and C-IMD3/H_{3BB}, and (c) I/Q trajectory. (d)–(f) Measured single-sideband performance over frequency band versus tone-spacing.

A simple fixed memoryless 2 × 1-D DPD is employed for all complex modulated signals in this work. The effect of the I/Q image on the performance of the multi-carrier scenarios is demonstrated in Fig. 22. In the first scenario, a two-carrier "20 MHz 64-QAM OFDM" signal, located at -90 (CH1) and -50 MHz (CH2), respectively, away from $f_C = 5.4$ GHz, is applied to the DTX. Fig. 22(a) and (b) demonstrates the spectrum (blue) and its constellation diagrams with EVMs of -35.64 and -33.65 dB, respectively. In the second scenario, the TX signal is mirrored with respect to the carrier frequency, locating the channels at $+50$ (CH3) and $+90$ MHz (CH4), respectively, away from f_C. Fig. 22(a) and (c) shows the spectrum (red) and its constellation diagrams with EVMs of -33.44 and -34.94 dB, respectively. As illustrated, the channels' image component in the first scenario is located at the same position as the channels in the second scenario and vice versa. Therefore, when operating four channels simultaneously, large image components dramatically deteriorate the EVM of each channel. The spectrum (black) and its constellation diagrams of the four-channel scenario are presented in Fig. 22(a) and (d), exhibiting that the channels' EVM has not been degraded significantly due to the decent I/Q image performance of the DTX.

The spectral purity of a single-carrier "40 MHz 256-QAM OFDM" signal is measured at $f_C = 5.4$ GHz. The measured spectrum of the signal and its constellation diagram are depicted in Fig. 23(a) and (b). The DTX achieves an average

TABLE I

PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART WORKS

Specifications		This Work		ISSCC 2021 A. Zhang		ISSCC 2021 B. Yang		JSSC 2020 S.W. Yoo		JSSCC 2020 A. Bassat	RFIC 2020 J. Sheth	TMTT 2019 D. Jung	JSSC 2020 D. Jung	JSSC 2020 Y. Yin	ISSCC 2016 P. Filho	TMTT 2017 W. Gaber	JSSC 2018 M.Mehrpoo	CICC 2020 Y.Shen	
Technology		CMOS 40nm		CMOS 65nm		CMOS 40nm		CMOS 60nm		CMOS 28nm	CMOS 65nm	CMOS 55nm	SOI 45nm	CMOS 40nm	CMOS 28nm	CMOS 28nm	CMOS 40nm	CMOS 40nm	
Architecture		Quadrature 4-way Doherty / CMCD		Current-Mode SHS		Quadrature SFCPA /Hybrid Doherty		TI-Doherty /Class G		Polar	4-way Doherty	Analog Doherty	Hybrid Doherty	Switched Transformer	RQDAC	DDRM	DDRM	IQ-Mapping DDRM	
Die Area		3.55mm² (1.5mm² ‡)		7.1mm²		2.2mm²		3.36mm²		4mm² ¥1	3mm²	6mm²	6mm²	0.8mm²	0.22mm² ‡	1.53mm²	0.21mm² ‡	1.1mm² ‡	
Supply		1V		N/A		1.2/2.4V		2.5V		1.4V	0.55V	5.5V	1.2V	1.1V	0.9V	3.6V	2V	2.5V	
Frequency		5.4GHz		5.4GHz		2.4GHz		2.4GHz		5GHz	5.25GHz	5.8GHz	2.3GHz	1.5GHz	2.4GHz	1GHz	3GHz	2.4GHz	
1-dB Power BW		5-5.6GHz		5.3-6.05GHz		2.3-2.8GHz*		N/A		N/A	4.5-5.25GHz*	5.4-6.1GHz*	2.1-2.5GHz*	1.3-3.5GHz	N/A	N/A	N/A	0.5-2GHz*	
Peak P_{Out}		27.4dBm		27dBm (5.7GHz)		30.3dBm		30dBm		27dBm	6.5dBm	27.2dBm	22.4dBm	21.4dBm	3.5dBm**	21dBm**	9.2dBm**	14.1dBm** @2GHz	
Efficiency (Drain/System)	Peak	47.4% / 30.66%		40.1% / N/A	5.4GHz	41.3% / 36.5%		40.2% / N/A		37% / N/A	42% / 26%	N/A / 24.5%	38.5% / N/A	N/A / 31.3%	N/A	N/A / 33%**	NA / 5.7%†	NA / 7.56%	
	3dB PBO	47.68% / 31.63%		32%* / N/A		37.5% / 32.9%		37.9% / N/A		31%* / N/A	36% / 20%*	N/A / 22*%	33%* / N/A	N/A / 28%*	N/A	N/A	N/A	N/A	
	6dB PBO	43.49% / 26.34%		26.3% / N/A		36.1% / 29.1%		38.8% / N/A		24%* / N/A	28% / 14%	N/A / 13*%	25%* / N/A	N/A / 27.7%	N/A	N/A	N/A	N/A	
	9dB PBO	41.06% / 23.1%		29.2% / N/A		30.9% / 23.7%		36.3% / N/A		18% / N/A	23% / 15%*	N/A / 8*%	18.7% / N/A	N/A / 18%*	N/A	N/A	N/A	N/A	
	12dB PBO	40.6% / 18.1%		19.1% / N/A		26.2% / 18.6%		29.4% / N/A		14%* / N/A	20%* / 7%*	N/A	13%* / N/A	N/A / 16.6%	N/A	N/A	N/A	N/A	
Modulation		240MHz 6×256-QAM OFDM	320MHz 4×512-QAM OFDM	20MHz 256-QAM	80MHz 64-QAM OFDM	60MHz 256-QAM	40MHz 1024-QAM	10MHz 1024-QAM	10MHz 64-QAM OFDM	20MHz MCS7	160MHz MCS11	1.6MHz 16-QAM	80MHz 256-QAM	40MHz 64-QAM	20MHz 64-QAM LTE	20MHz 64-QAM	40MHz 64-QAM WLAN	113MHz 64-QAM	160MHz 256-QAM	320MHz 256-QAM
Average P_{Out}(dBm)		17.82	18.16	22	18	23.3	20.4	23.2	19.1	21.1	19.2	2.9	17	15.3	15.2	-3.87	12	0.1	NA	5.15
Average Efficiency		41.23%(DE) 22.17%(SE)	41.12%(DE) 20.52%(SE)	27.4% (DE)	28.1% (DE)	30.7% (DE)	22.6% (DE)	36.2% (DE)	30.3% (DE)	26% (PE)	21% (PE)	34% (DE)	5.3% (PAE)	24.7% (DE)	25.3% (PAE)	1.7%* (SE)	11% (SE)	NA	NA	
EVM		-32.28dB	-29.65dB	-33.5dB	-30.4dB	-31.9dB	-35.9dB	-44.5dB	-41.7dB	-28dB	-35dB	-20dB	-34.8dB	-32dB	-32.5dB	-36dB	-30.3dB	-27dB	-36dB	-32dB
PAPR		9.68dB	9.41dB	4.4dB	8.4dB	6.98dB	9.86dB	6.8dB	10.9dB	5.9dB	7.8dB	3.6dB	6.3dB§	7.1dB	6.2dB	7dB	8.73dB	6.2dB	8dB	8dB
LO Leakage / IQ image / CIM3		<-58 / -60 / -67dBc		N/A		N/A		N/A		N/A	N/A	N/A	N/A	N/A	-59 / -44 / -50dBc	-44 / -39 / -26dBc	N/A / -45 / -56dBc	-52 / -54 / -55*dBc	
Linearization		DPD		N/A		DPD		No		DPD	DPD	MGTR	AM-AM LUT	DPD	DPD	DPD	No	No	

* Estimated from reported figures and plots. ** Off-chip matching network. ‡Core area. ¥1 Area including Digital front end, DPLL, and LB/HB DTX. †Excluding LO generation. § Measured at 3.9dB additional PBO.

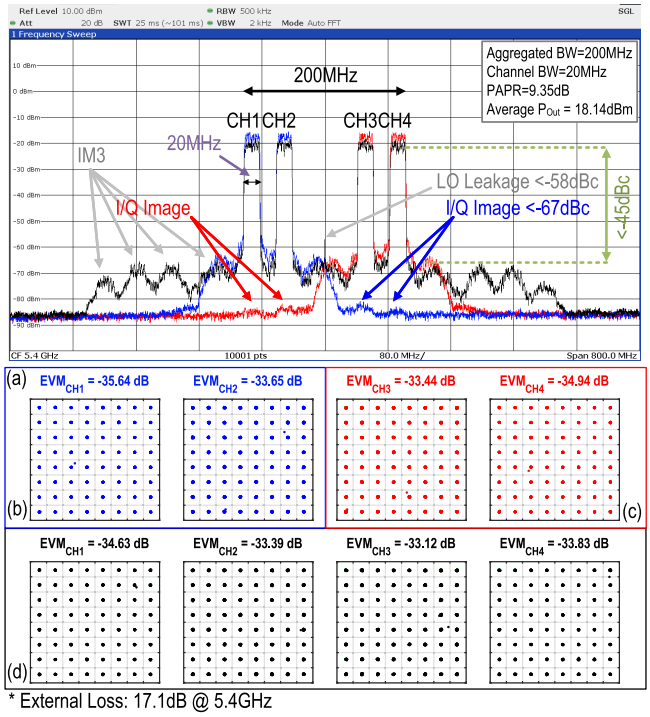


Fig. 22. Measured (a) output spectrum of two-/four-carrier 20 MHz 64-QAM OFDM scenarios and (b)–(d) corresponding constellation diagram and EVM.

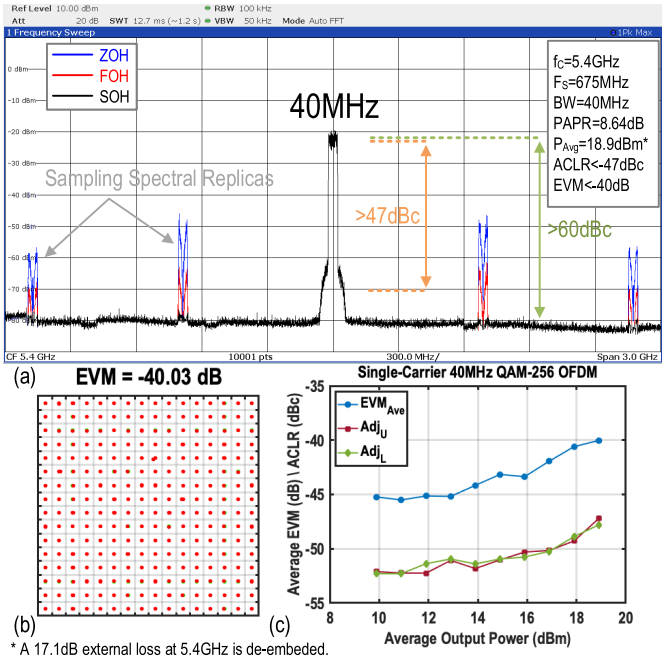


Fig. 23. Measured (a) spectrum of single-carrier 40 MHz 256-QAM OFDM signal and (b) constellation diagram and EVM. (c) ACLR and average EVM performances versus average output power.

output power of 18.9 dBm while maintaining the average drain and system efficiencies of 43.11% and 24.51%, respectively. Utilizing the abovementioned fixed memoryless 2 × 1-D DPD, the ACLR is better than −47 dBc, and the EVM is −40.03 dB. The ACLR and average EVM performances versus average output power are also exhibited in Fig. 23(c), reaching −45.14 dB EVM at 12 dBm average output power, while the ACLR is better than −51 dBc. These results indicate that the spectral purity and EVM of the proposed digital TX can meet the TX spectral emission requirements of the prevailing wireless communication standards.

A six-carrier "40 MHz 256-QAM OFDM" signal with an aggregated bandwidth of 240 MHz is applied to the DTX, and the performance is verified at $f_C = 5.4$ GHz using the simple fixed memoryless 2 × 1-D DPD. Fig. 24(a) exhibits the measured spectrum of the signal and its CH6 constellation diagram. Accordingly, the DTX delivers 17.82 dBm average power while achieving an ACLR of better than −39 dBc and

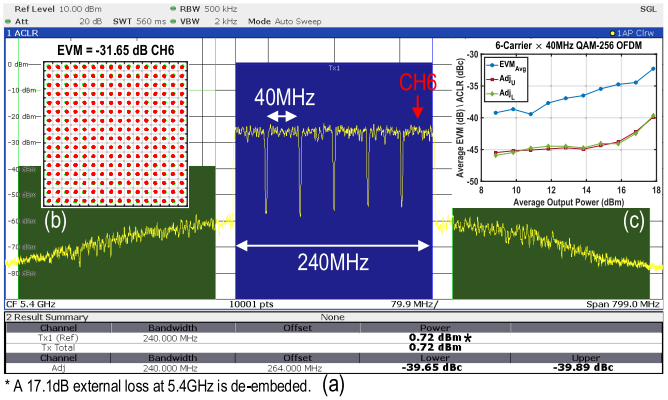


Fig. 24. Measured (a) spectrum of six-carrier 256-QAM OFDM signal and (b) worst channel constellation diagram and EVM. (c) ACLR and average EVM performances versus average output power.

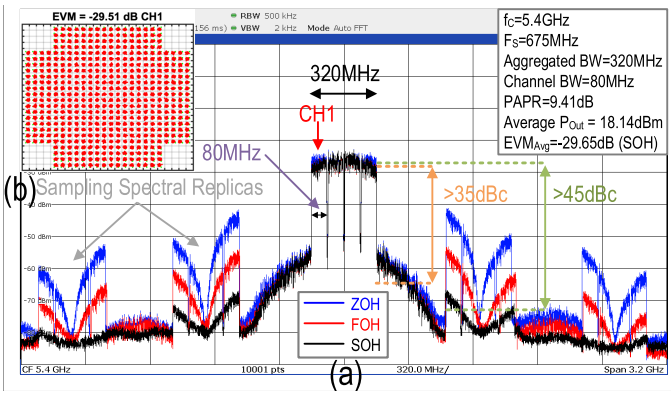


Fig. 25. (a) Measured suppression of SSRs using ZOH/FOH/SOH filters. (b) Worst channel constellation diagram and EVM using SOH filter.

an average EVM of −32.28 dB. The measured average drain and system efficiencies are 41.23% and 22.17%, respectively. The ACLR and average EVM performances versus average output power are also exhibited in Fig. 24(c), achieving −37.55 dB average EVM at 12 dBm average power, while the ACLR is better than −44 dBc.

The effectiveness of signed ZOH, FOH, and SOH filters on the suppression of SSRs is demonstrated in Fig. 25 where a four-carrier "80 MHz 512-QAM OFDM" signal with an aggregated bandwidth of 320 MHz and $F_S = 675$ MHz is applied to the DTX, and the interpolation filter order is varied. The SOH filter achieves suppression of more than 30 dB compared to ZOH for such a wideband signal.

The performance of our DTX is summarized and compared to that of the prior art in Table I. It indicates that the realized compact four-way Doherty DTX achieves excellent efficiency at 12 dB DPBO at 5.4 GHz while generating more than 27 dBm peak power. The I/Q DTX can also support wide modulation bandwidth with high average output power and decent average drain and system efficiencies. Moreover, our 50%-LO signed I/Q interleaved upconverter yields exceptional orthogonal I/Q summation compared to the other works.

VI. Conclusion

This article demonstrates a compact wideband digital I/Q transmitter realized in a 40-nm bulk CMOS. Introducing a 50%-LO signed I/Q interleaved up-converter and a compact four-way Doherty combiner, the proposed DTX achieves a spectrally pure operation, and simultaneously, it enhances its DPBO efficiency. The DTX generates more than 27.54 dBm with 46.35% DE in a 4–6.2 GHz band. Its EVM and ACLR performance are better than −31 and 39 dB, respectively, for a six-carrier "40 MHz 256-QAM OFDM" signal. The realized DTX can be reconfigured as a stand-alone DDS to support signals with a 320 MHz modulation bandwidth. Moreover, the proposed bits-in RF-out TX replicates the spectral purity performance of its state-of-the-art analog-intensive counterparts. Finally, it can perform as a high-power energy-efficient CMOS transmitter to target next-generation multi-band/multi-band applications requiring large modulation/aggregated bandwidth.

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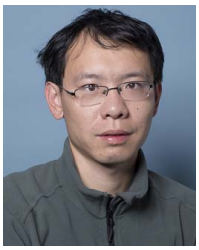
Mohammadreza Beikmirza (Graduate Student Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering from the Amirkabir University of Technology (Tehran Polytechnic), Tehran, Iran, in 2014 and 2016, respectively. He is currently pursuing the Ph.D. degree with the Delft University of Technology, Delft, The Netherlands.

His current research interests include digital-intensive transmitters and RF/monolithic microwave integrated circuits design.



Yiyu Shen (Member, IEEE) received the M.S. degrees in microelectronics from Tsinghua University, Beijing, China, and Katholieke Universiteit Leuven, Leuven, Belgium, in 2014. He is currently pursuing the Ph.D. degree in electrical engineering with the Delft University of Technology (TU Delft), Delft, The Netherlands.

His current research interests include power amplifiers and digital-assisted RF integrated circuits and systems.

Leo C. N. de Vreede (Senior Member, IEEE) received the Ph.D. degree *(cum laude)* from the Delft University of Technology, Delft, The Netherlands, in 1996.

In 1996, he was appointed as an Assistant Professor at the Delft University of Technology, working on the nonlinear distortion behavior of active devices. In 1999 and 2015, he was appointed, respectively, as an Associate Professor and a Full Professor at the Delft University of Technology, where he became responsible for the Electronic Research Laboratory (ERL/ELCA). During that period, he worked on solutions for improved linearity and RF performance at the device, circuit, and system levels. He is a Co-Founder/Advisor of Anteverta-mw, Eindhoven, The Netherlands, a company specialized in RF device characterization. He has (co)authored more than 120 IEEE refereed conference papers and journal articles. He holds several patents. His current interests include RF measurement systems, RF technology optimization, and (digital-intensive) energy-efficient/wideband circuit/system concepts for wireless applications.

Dr. de Vreede was a (co)recipient of the IEEE Microwave Prize in 2008 and a Mentor of the Else Kooi Prize Awarded Ph.D. Work in 2010 and the Dow Energy Dissertation Prize Awarded Ph.D. Work in 2011. He was a recipient of the TUD Entrepreneurial Scientist Award in 2015. He (co)guided several students who won (best) paper awards at the Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), Program for Research on Integrated Systems and Circuits (PRORISC), the European Solid-state Circuits and Devices Conference (ESSDERC), the International Microwave Symposium (IMS), the Radio-Frequency Integration Technology (RFIT), and the Radio Frequency Integrated Circuits Symposium (RFIC).

Morteza S. Alavi (Member, IEEE) received the B.Sc. degree in electrical engineering from Iran University of Science and Technology, Tehran, Iran, in 2003, the M.Sc. degree in electrical engineering from the University of Tehran, Tehran, in 2006, and the Ph.D. degree in electrical engineering from the Delft University of Technology (TU-Delft), Delft, The Netherlands, in 2014.

He was a Co-Founder and the CEO of DitIQ B.V., The Netherlands, a local company developing energy-efficient, wideband wireless transmitters for the next generation of the cellular network. Since September 2016, he has been an Assistant Professor with the ELCA Group, Delft University of Technology. He has coauthored *Radio-Frequency Digital-to-Analog Converter* (Elsevier, 2016). His main research interest is designing high-frequency and high-speed wireless/cellular communication and sensor systems, as well as in the field of wireline transceivers.

Dr. Alavi was the Best Paper Award Recipient of the 2011 IEEE International Symposium on Radio-Frequency Integrated Technology (RFIT). He was a recipient of the Best Student Paper Award (Second Place) of the 2013 Radio-Frequency Integrated Circuits (RFIC) Symposium. His Ph.D. student also won the Best Student Paper Award (First Place) of the 2017 RFIC Symposium held in Honolulu, HI, USA. He also serves as a Reviewer for the IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC), the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES (TMTT), IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS (TCAS-I), IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, and *ICEIE Transactions on Communications*.