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Design and Comparison of a 10kW Interleaved Boost Converter for PV Application Using Si and SiC Devices

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***Abstract*--** Grid connected PV inverters have a DC/DC converter connected to the PV for executing the maximum power point tracking (MPPT). The design of an interleaved boost converter (IBC) with three switching legs for 10kW PV inverter is presented in this paper. The paper shows how the use of SiC switches and powdered iron core inductors enables the operation of the converter at a higher switching frequency and increasing the converter power density. The IBC is designed using 1.2kV SiC MOSFET and Schottky diodes and KoolMμ powdered iron inductors. The design is compared with an IBC built with Si IGBT, fast recovery Si diodes and ferrite cores. The use of SiC devices reduces the switching loses drastically and there is no reverse recovery losses, resulting in improved efficiency. The higher frequency and higher saturation flux density of the powdered iron core enables the reduction in core size by three times. A 10kW prototype is built and tested for both the Si and SiC design and compared with theoretical estimations.

***Index Terms*—** Interleaved boost converter, powered iron core, photovoltaic systems (PV), silicon carbide (SiC).

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I. INTRODUCTION

THE use of photovoltaic (PV) panels for distributed electricity generation is becoming increasingly popular in the world. PV inverters are used to interface the PV panels with the AC grid and consist of a DC-DC converter and DC-AC inverter [1]–[9], as shown in Fig. 1. For low power inverters, a single phase connection is used. For high power inverters, a three phase inverter is used to connect to the 400V grid with a 16A or 32A connection. The DC-DC converter plays two important roles - it ensures that the PV panels operates at its maximum power point (MPPT) and does power curtailment when the input PV power is too high or the DC-link voltage is beyond its rated limits. The DC-AC inverter maintains the DC-link within the prescribed limits and feeds the power from the DC link to the AC grid.

As per European standards, galvanic isolation is not required in the current flow path from the PV to grid. The most important advantages of transformer-less PV converters when compared to the PV converters with galvanic isolation are higher efficiency and power density. However, the absence of isolation means that a high common mode voltage ripple on the PV side due to the power converter switching can lead to dangerously high capacitive leakage currents $I_{PV(leakage)}$ from the PV panel to earth [10], [11]:

$$I_{PV(leakage)} = C_{G.PV} \frac{dV_{PV(cm)}}{dt} \qquad (1)$$

where $C_{G.PV}$ is the parasitic capacitance to earth of the PV panels and $V_{PV(cm)}$ is the common mode voltage

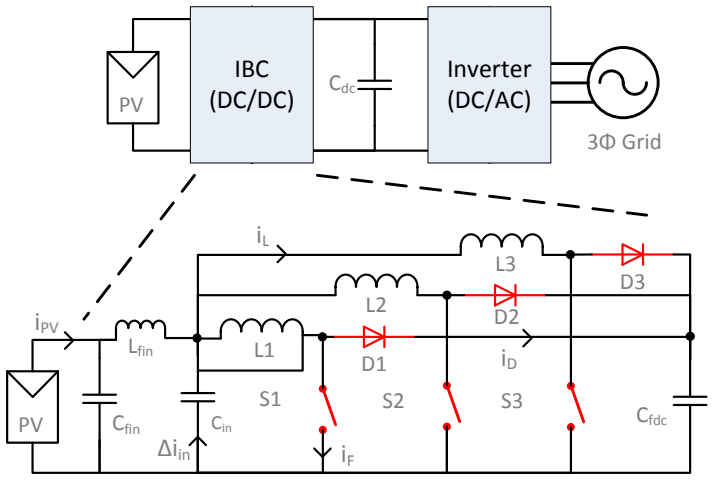

Fig. 1 – Topology of a three leg interleaved boost converter (IBC) with input PV side and DC buffer capacitors at the output side. Devices marked in red are 1.2kV SiC devices for 47kHz design and Si devices for the 19kHz design.

at PV terminals. With a three phase inverter, a 300Hz ripple exists on the DC link capacitor C_{dc} which in turn causes a 300Hz common mode voltage $V_{PV(cm)}$ at the PV side when using a non-isolated topology.

Fig. 1 shows the topology of an interleaved boost converter (IBC) which is used as the DC/DC pre-converter in PV inverter. It operates the PV at its MPPT and boost the PV voltage to the DC-link voltage. For a PV converter of high power rating of ≥10kW, interleaving has several advantages over a single leg boost converter as:

1. Current through the switches and inductors in each leg is reduced by a factor of $(1/N_i)$ where *Ni* is the number of interleaved stages. Thus a smaller inductor and lower rated switch can be used.
2. The volume L_{vol} of an inductor is directly proportional to the energy processed by it as given by $L_{vol} \propto LI^2$. By interleaving, the total volume $L_{vol(n)}$ of all the interleaving inductors reduces by a factor N_i,

$$L_{vol(n)} \propto N_i L\left(\frac{I^2}{N_i}\right) = \frac{LI^2}{N_i} \qquad (2)$$

3. Effective frequency as seen at the input is increased by a factor of N_i. This facilitates the operation of each leg at a lower frequency leading to lowering of switching losses
4. As the currents in each leg are phase shifted by an angle of $360^0/N$, the input current ripple and voltage ripple are reduced by a factor of $(1/N_i)$ and $(1/N_i)^2$ respectively. This reduces the input voltage ripple shown in (1)

To achieve high power density and efficiency, it is important to increase the switching frequency as well as the efficiency of the IBC. SiC represents a revolution in power semiconductor technology which can help realize this. SiC is a wide-bandgap material having much better conduction performance when compared to Si material [12]–[14]. SiC MOSFETs exhibit very low switching losses while SiC schottky diodes have no reverse recovery and have very low turn-on voltage.1.2kV SiC MOSFET are now available commercially and is opening a plethora of opportunities especially in high power three phase applications, where 1200V Si MOSFET were not widely available for high currents of the order of 30A.

The use of silicon carbide (SiC) devices for DC/DC converters for PV applications has been investigated in the past [15]–[19]. In [15], a two leg IBC of 2.5kW power for PV is designed with the use of SiC diodes and CoolMOS transistors. In [16], the IBC system design and efficiency from [15] are compared with those obtained using a comparable Si diode. The use of SiC diodes has been shown to reduce both the losses in the switch and

the diode due to lower conduction losses and extremely small reverse recovery charge that is negligible at low switching frequencies. The reduced losses necessitated a smaller heat sink and hence both a higher power density and efficiency was obtained. In [17], an all SiC switching cell is evaluated to show that up to 1.5% improvement in European efficiency can be obtained. In [20], the use of SiC switches in design of optimized filters for H5 and Conergy-NPC transformer-less PV inverters is presented.

In this paper, the design of an interleaved boost converter using Si and SiC devices for PV application is presented. It shows how the combined use of SiC switches and powdered iron core inductors enables the operation of the converter at a higher switching frequency and increasing the converter power density. Two cases are considered for the analysis:

1. Classical case - Silicon (Si) IGBT, Si diode and ferrite core inductors with switching frequency of 19kHz
2. Modern case - SiC switches, SiC schottky diodes and powdered iron core inductors with more than twice the switching frequency, i.e. 47kHz

The contributions of this work compared to earlier works are:

1. The earlier works have demonstrated the use of SiC MOSFETs in PV pre-converters for single phase low power applications of 3kW or less. The real use of SiC MOSFETs is however in high power (≥ 10kW) three phase applications as demonstrated in this work where >900V Si MOSFETs could never be used earlier due to their large on-state resistance, limited commercial availability and high cost.
2. The earlier works shown the realization of an improved IBC converters by changing a single component in the converter like diode and/or switch while using the same switching frequency and passive components. In this work, an improved IBC is designed considering the switch, diode, switching frequency and inductor core material in a holistic manner.
3. Powdered iron core inductors have not found extensive use in high frequency power electronics due to their high core losses. The authors have investigated the use of low loss powdered iron core material in this work, namely the KoolMμ core [21], [22]. A three time reduction in inductor size and better response to fault condition is hence possible.
4. The work has exhibited how the combined use of SiC devices and powered core inductors has provided a

2.5 increase in power density with less than 1% reduction in measured efficiency.

5. Full scale 10kW converter prototype including closed loop control for MPPT and power curtailment operation is built for both the Si and SiC design.

The specifications of the PV converter is shown in Table I and Table II. A detailed design procedure is presented for designing the components and estimating the losses in the converter. In both cases, the boost converter is operated with hard switching. Depending on the input current level, the boost converter operates in continuous conduction mode (CCM) or discontinuous conduction mode (DCM). Unlike [15], [16], the converter has only one mode of operation and does not use a bypass diode that bypasses the IBC. This is because the IBC is used as part of a three phase inverter and PV panel voltage is always less than the rated DC-link voltage of 750V. The DC link voltage is rated at 750V as it must be greater than the peak AC voltage for normal inverter operation:

$$V_{dc} > \sqrt{2}(V_{ac})(110\%) \qquad (3)$$

where V_{ac}=400V and 110% takes into account the variation in grid voltage due to distributed generation and loading on lines.

The switching frequencies were set at 19Hz and 47kHz respectively for two reasons. 19kHz was found to be optimal in terms of trade-off between IGBT losses and inductor losses and size. This optimization was done in a different study and out of scope of this paper. At higher frequencies than 19kHz, the IGBT switching losses increased dramatically while at lower frequency, the inductor size and losses increased thus lowering efficiency and power density. Secondly, 19kHz is at the edge of the audible frequency range for human being making the converter quiet in operation. 47kHz was chosen for the SiC version so that the number of parallel core sets required for the IBC can be reduced from three to one (as will be seen later). The second reason is that third harmonic injected in the grid must be below 150kHz as per the limits set in the standard EN55022. So with a frequency below 50kHz for each leg, the third harmonic of the interleaved converter is below 150kHz and hence there is no requirements for additional/larger filters in the inverter.

The structure of the paper is as follows – section 2 describes the basics of the IBC operation and elucidates the estimation of input and inductor ripple. Section 3 explains the calculation of inductor size and the design of inductor using ferrite and powdered iron core. Inductor core and copper losses are compared for the two designs

and the input capacitor is sized to limit the ripple on the PV. Section 4 explains the design of the closed loop control of the converter for MPPT and power curtailment operation. In section 5, loss models of the Si and SiC based IBC are built and the efficiency of the converter is estimated. In the last section, the experimental setup of the two converters is presented and are compared with the theoretical estimates.

II. BASICS OF INTERLEAVED BOOST CONVERTER

An interleaved boost converter has N_i number of interleaved switching legs that are connected in parallel. The gate signals for each leg are phase shifted by $360^0/ N_i$. The current through each leg is $(1/ N_i)$ of the input current. In this design, a three-leg interleaved boost converter is used as shown in Fig. 1.

The operation of the converter can be explained based on the waveforms shown in Fig. 2. When the switch is

TABLE I

SPECIFICATIONS OF PV CONVERTER

Parameter	Symbol	
Maximum PV input voltage	$V_{pv(max)}$	850V
Input MPPT Voltage	V_{pv}	350-700V
Input MPPT Current	I_{pv}	0 - 30A
Maximum Power	P_{pv}	10kWp
Output rating (DC link)	V_{dc}	750V, 14A
DC link capacitance	C_{DC}	470µF
Duty cycle	D	0.067 to 0.53
Interleaved stages	N_i	3
Input current ripple (peak-peak)	$\Delta I_{in(p\text{-}p)\%}$	10% of $I_{pv(max)}$
Input voltage ripple (peak-peak)	$\Delta V_{in(p\text{-}p)\%}$	0.5%

TABLE II

COMPONENT SELECTION FOR SI AND SIC CONVERTERS

	Classical Si design	Modern SiC design
Switching frequency (f_{sw})	19 kHz	47 kHz
Diode	Si IXYS 1kV Fast recovery diode, DSEI 30	SiC CREE Schottky diode C4D15120A
Switch	Si IGBT 900V APT25GP90BDQ1	SiC CREE MOSFET C2M0080120D
Inductor core	Ferrite, Epcos N87, E65 size	KoolMµ Powdered iron core E65 – 26µ,40µ,60µ

ON for the period from 0 to (*DT)*, the current in the inductor rises from $I_{L(min)}$ to $I_{L(max)}$ due to the positive PV voltage across it. The slope of the inductor current is given by (V_{PV}/L), where L is the inductance. When the switch is turned OFF, there is a negative voltage across the inductor and the inductor current decreases with a slope $(V_{dc} - V_{PV})/L$ and flows through the diode. The waveforms of the current through the switch $i_F(t)$ and diode $i_D(t)$ can be seen in Fig. 2.

The voltage ratio of input and output voltage is the same as a normal boost converter for CCM and DCM modes and is given by:

$$\frac{V_{dc}}{V_{PV}} = \frac{d_1 + D}{d_1} \tag{4}$$

where D is the duty cycle of the switches and d_1 is the period for which the switch is OFF and current flows through the diode. In CCM,

$$d_1 = 1 - D \tag{5}$$

A. Ripple in the inductor

The inductor ripple is vital in designing the PV converter as it directly translates to the input capacitor sizing and the voltage ripple on the PV given by (1). The peak-to-peak ripple in the inductor ΔI_L is dependent on the duty cycle of the converter as seen in Fig. 2 and is given by

$$\Delta I_L = \frac{V_{PV}}{f_{sw}L}(D) = \frac{(V_{dc} - V_{PV})d_1}{f_{sw}L} \tag{6}$$

$$\Delta I_L = I_{L(max)} - I_{L(min)} \tag{7}$$

$$I_{L(avg)} = \frac{I_{PV}}{N_i} \tag{8}$$

where $I_{L(avg)}$, $I_{L(max)}$, $I_{L(min)}$, is the average, maximum and minimum current through the inductor respectively. In Fig. 3, the input ripple as a function of duty cycle can be seen for N_i=1 with maximum ripple occurring at D=0.5.

In CCM,

$$I_{L(max)} = I_{L(avg)} + \frac{\Delta I_L}{2} \tag{9}$$

$$I_{L(min)} = I_{L(avg)} - \frac{\Delta I_L}{2} \tag{10}$$

In DCM,

$$d_1 = \frac{V_{PV}}{(V_{dc} - V_{PV})} \tag{11}$$

$$I_{L(min)} = 0 \qquad I_{L(max)=}\Delta I_L \tag{12}$$

In both CCM and DCM operating modes it is assumed that the currents are evenly shared between the switching legs. For three interleaved legs, the current through each inductor is $I_{L(avg)} = I_{PV}/3$. It can thus be seen from (6) that, in order to have a low ripple, we either need to use a high switching frequency or a large inductor.

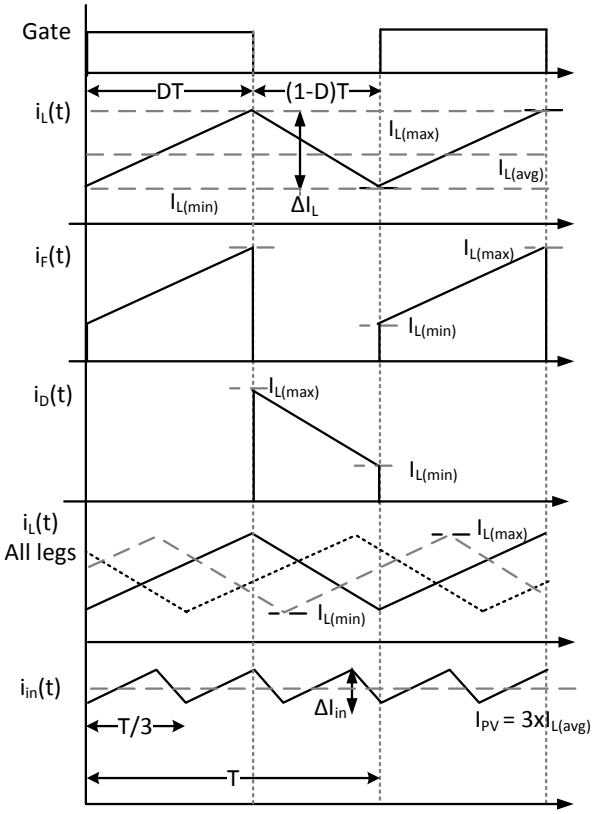

Fig. 2 – Waveforms of currents through the inductor, switch and diode in each interleaved leg and phase shifted currents of all three inductors. Maximum input current ripple is (1/Ni) of the inductor ripple.

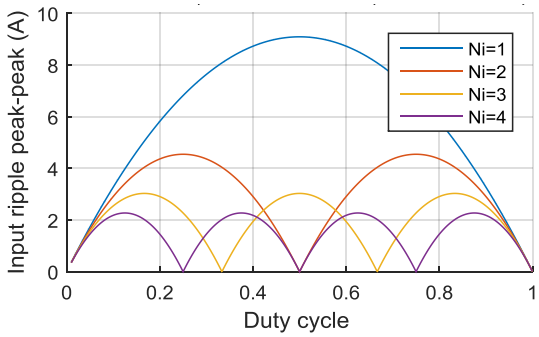

Fig. 3 – Magnitude of input ripple as a function of duty cycle for different number of interleaved stages. V_{dc}=750V, f_{sw}=47kHz, L=443µH

Both these methods have the drawbacks that they reduce the converter efficiency and power density due to increased switching losses, increased losses in inductor (core and copper losses) and requiring larger size of core material and/or heat sink. The benefit of interleaving is that the maximum input current ripple is *(1/ N_i)* of the maximum inductor ripple. This is elaborated in the next section.

B. Ripple in the input of IBC

The currents i_L in the three inductors *L1, L2 and L3* are phase shifted by 120º. The input ripple ΔI_{in} is then only a fraction of the ripple in each of the inductors. This can be mathematically shown for a general IBC as

$$\Delta I_{in}(D) = \frac{V_{PV}}{f_{sw}L}\left(\frac{N_{on} - N_i D}{1 - D}\right)\frac{1}{N_i}(N_i D - N_{on} + 1) \qquad (13)$$

where N_{on} is the maximum number of switches that are simultaneously ON for the given duty cycle. The expression (13) has been derived based on the work in [23]. When equation (13) is used for ripple estimation with N_i=2, it comprehends well with the results in [15].

In Fig. 3, the magnitude of input ripple as a function of duty cycle can be seen for different number of interleaved stages. The peak input ripple occurs at a duty cycle of *D=(1/2N_i)* and the input ripple is zero when *D=(1/N_i)*. The peak input ripple for N_i=1,2,3,4 are 9.1A, 4.55A, 3.03A and 2.275A respectively with V_{dc}=750V. It can be observed that the marginal reduction in ripple with increase in interleaved stages keeps reducing from 4.55A to 0.755A and there is no sizeable benefit when going beyond N_i=3.

For the inductor design, the vital parameter is the maximum input ripple considering all duty cycles. The duty cycle for maximum input ripple can be determined from (13) by setting $d(\Delta I_{in})/dD = 0$, and solving for D. Maximum input ripple $\Delta I_{in(\max)}$ is obtained at $D = A_{int}/2N_i$, where A_{int} takes odd integral values from 1 to $2N_i$

$$\Delta I_{in(\max)} = \frac{V_{\mathrm{dc}}}{4f_{sw}LN_i} \qquad @\ D = \frac{A_{int}}{2N_i} \qquad (14)$$

For a three leg IBC, maximum input ripple occurs at odd integral multiples of D=1/6 as seen in Fig. 3. It must kept in mind that maximum ripple in inductor $\Delta I_{L(\max)}$ always occurs at D=0.5 irrespective of number of interleaved legs.

III. DESIGN OF INTERLEAVED BOOST CONVERTER

A. Inductor size calculation

Inductors play the vital role of energy storage element in an IBC. The inductors in each leg must be identically designed to ensure proper current sharing between the legs. The size of the inductor is determined in such a way that the maximum input ripple $\Delta I_{in(\max)}$is within the prescribed limits. Maximum input ripple is set at the point where the PV feeds in maximum current, when I_{pv}=$I_{pv(max)}$=*10A.*

$$\Delta I_{in(\max)} = \Delta I_{in(\mathrm{p-p})\%} I_{PV(\max)} \quad (15)$$

$$L = \frac{V_{\mathrm{dc}}}{4 f_{sw} N_i \Delta I_{in(\max)}} \quad (16)$$

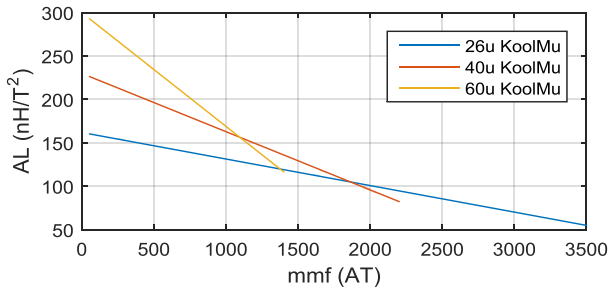

Fig. 4 – Permeance A_L of the Kool Mμ E65 core as a function of the ampere-turns. The permeance and inductance of the core reduces linearly with increase in current through the inductor.

As can be seen above, the required value of inductance is frequency dependent - a large switching frequency means a smaller inductor is required. Using (15) and (16), the inductor values obtained for the two design of 19kHz and 47kHz are 1.12mH and 443μH respectively. Three such inductors will be required for the converter. Ripple and inductor calculations are summarized in Table III.

B. Inductor design using ferrite and powdered iron core

In this section the inductor design for the two inductors is elaborated:

1. 19kHz, 1.12mH, ferrite core inductor using Epcos N87 material
2. 47kHz, 443μH, powdered iron core inductor using Kool Mμ core of permeability 60μ, 40μ and 26μ

Both inductors are implemented using E65 cores as they are easily suitable for PCB mounting and have large core area to reduce the core losses. The E65 core has the following parameters - Core area A_c of 540mm^2,

Magnetic path length l_e of 147mm and core volume V_e of 79400mm^3. Litz wire of 1000x0.071mm is used for the inductor design in order to reduce the skin effect at high frequencies. The skin depth for 19kHz and 47kHz is approximately 300µm and 472µm respectively. 1000x0.071mm litz has a diameter which is much lesser than the skin depth of either frequency.

The key differences in the material characteristics of ferrite and Kool Mµ cores are:

1. Powdered iron core have a 'fixed' distributed air gap. This is unlike the case of ferrite cores where the air gap and number of turns can be optimized to give the least inductor losses.
2. Powdered iron cores are typically characterized by high core losses with respect to ferrites. The authors looked extensively for different powdered iron cores so as to find a candidate with the least losses. Kool Mµ cores were hence chosen due to their very low lower core losses and temperature rise [22].
3. Kool Mµ cores have a high saturation flux density which is nearly twice as that of ferrite cores and with minimal reduction with increase in temperature. This means that a fewer number of parallel core sets are required leading to higher power density.
4. Kool Mµ cores have a soft saturation as shown in Fig. 4, where the permeance of the core varies with inductor current. This means that the inductance *L* linearly reduces with increase in inductor current i_L.This necessitates the oversizing of inductance so that there is sufficient inductance L_{least} at maximum input current, where L_0 is the inductance at zero current and *K* is the slope with which the inductance reduces with current through the inductor. This causes non-linear currents through the inductor [24].

$$L(t) = L_0 - K i_L(t) \qquad (17)$$

TABLE III

CALCULATION OF INPUT RIPPLE, INDUCTOR RIPPLE

Duty for maximum input ripple	$A_{int}/(2Ni)$	0.167, 0.5, 0.833	
Maximum current per leg	$I_{PV(max)}/N_i$	10 A	
Maximum input ripple (p-p)	$\Delta I_{in(\max)}$	3 A	
Maximum inductor ripple (p-p)	$\Delta I_{L(\max)}$	9 A	
Switching frequency	f_{sw}	19kHz	47kHz
Required inductor size	L	1.12mH	443µH

Ferrite cores are used for the 19kHz design as they are characterized by low losses and lower cost. As will be seen later, the 19kHz inductor requires three parallel E-core sets, hence it is vital to keep the cost and losses low. Kool Mμ on the other hand have a higher flux density, so a single E-core set is sufficient at higher frequency of 47kHz. At the same time, Kool Mμ cores are characterized by higher cost and losses, which is higher by a factor of three and five respectively when compared to ferrites (for 200mT flux density variation, 50kHz).

1) Inductor design using ferrite core

The material properties of Epcos N87 E65 ferrite core is mentioned in [25], [26]. It has a permeance of 7900nH and relative permeability of 1700. With the addition of an air-gap of length g, the permanence A_L varies according to (18) where K_1=716 and K_2=(- 0.762).

$$g = \left(\frac{A_L}{K_1}\right)^{\frac{1}{K_2}} \tag{18}$$

Based on A_L, the number of turns required to get inductance of 1.12mH can be calculated by (16) and (19).

$$L = A_L N^2 \tag{19}$$

$$B_{max} = \frac{A_L N I_{L(max)}}{N_p A_c} \tag{20}$$

Several combinations of N and g can give the same value of inductance. At every combination it must be checked if the maximum flux density B_{max} is below 380mT saturation flux density of the core. For the given operating currents stated in Table III, the core saturates if only a single core set is used. To prevent saturation, the number of parallel cores N_p required per inductor is three. In order to optimize the inductor design, the inductor losses, namely the core and copper losses have to be determined for various values of air gap g keeping the inductance L as a constant. The core losses P_{core} can be estimated for a boost converter inductor using the Modified Steinmetz Equation (MSE) [27]. It is more accurate than using the normal Steinmetz Equation (SE) as it is applicable for inductors carrying DC currents with a ripple. However, it must be remembered that MSE does not consider the effect of DC offset introduced during DCM and CCM mode of operation in boost converter.

$$SE \rightarrow \quad P_{core} = A\, f_{sw}^{a} B_{pk}^{b}\, V_e \tag{21}$$

$$MSE \rightarrow \quad P_{core} = \left(A f_{eq}^{a-1} B_{pk}^{b}\right) f_r\, V_e \tag{22}$$

$$f_{eq} = \frac{2}{\Delta B^2 \pi^2} \int_0^T \left(\frac{dB}{dt}\right)^2 dt \qquad (23)$$

For a boost converter, the equivalent frequency f_{eq} for MSE is

$$f_{eq} = \frac{2}{\Delta B^2 \pi^2} \left\{ \int_0^{DT} \left(\frac{dB}{dt}\right)^2 dt + \int_{DT}^{(D+d_1)T} \left(\frac{dB}{dt}\right)^2 dt \right\} \qquad (24)$$

$$f_{eq} = \frac{2}{\pi^2} \left(\frac{D + d_1}{D d_1 T}\right) \qquad (25)$$

where V_e is volume of core, A,a,b are the Steinmetz parameters, ΔB is the peak-peak change in flux density and $B_{pk} = \Delta B/2$. For the N87 ferrite core, the Steinmetz parameters are given by A=47.66, b=2.63, a=1.4062 [25] when P_{core} is in kW/m^3, f_{sw} in kHz, B_{pk} in mT and V_e in m^3.

The second part of the inductor losses are the copper losses P_{cu} which can be estimated by (26) based on the RMS inductor current $I_{L(rms)}$, mean turn length l_{MTL} and resistance per unit length of the litz wire R_{pu}. For the 1000x0.071mm litz wire, the measured R_l=4.74 mΩ/m. The total inductor losses P_L can hence be estimated as:

$$P_{cu} = I_{L(rms)}^2 R_L = I_{L(rms)}^2 (N l_{MTL} R_{pu}) \qquad (26)$$

$$P_L = N_p P_{core} + P_{cu} \qquad (27)$$

To optimize the inductor design, inductor losses can be estimated for different values of air gap as shown in Fig. 5, at the operating point with lowest input voltage of 350V and maximum power of 10kW. It can be observed that at N=27, the inductor losses are minimum with P_L=5.9W, as elaborated in Table IV. The corresponding air gap is g=1.55mm. The total inductor losses in the converter will be three times due to the use of three inductors in the IBC. The losses in the copper due to fringing flux in the air gap are not taken into account here. The inductors

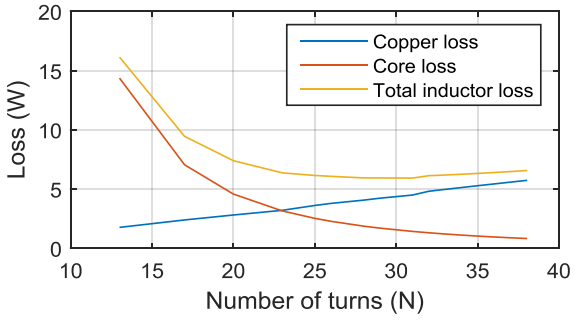

Fig. 5 – Ferrite core and copper loss estimation @ 350V, 10kW PV input, V_{dc}=750V with CCM operation at 19kHz frequency

design parameters are summarized in Table IV.

2) Inductor design using KoolMμ core

The design of the KoolMμ inductor for the 47kHz application is different from the ferrite design due to two main reasons – the core has a 'fixed' air gap and the inductance reduction due to soft saturation has to be compensated. To obtain different inductors, three different cores are considered - 60μ, 40μ and 26μ permeability. The design procedure is as follows [24]:

1. Equation (19) is used to determine the number of turns N for the given A_L. The 60μ, 40μ and 26μ core have a permeance of 300, 230 and 162 nH/T^2 at zero DC bias.
2. Using the ampere turns from step 1 namely ($NI_{L(avg)}$), the permanence A_L at the maximum inductor current is determined using the Fig. 4.
3. For the new compensated value of A_L, the number of turns N is again determined again using (19).

The Kool Mμ core is designed in such a way that it gives the required inductance of 443μH even at the highest inductor current of 9.5A, as shown in Table V. The corresponding inductance and number of turns obtained are

TABLE IV

INDUCTOR DESIGN PARAMETERS AND LOSS ESTIMATION

Frequency (kHz)	f_{sw}	19	47		
Cores per inductor	N_p	3	1		
Core		Ferrite	Kool Mμ		
			60μ	40μ	26μ
Inductance (μH)	L	1123	529	405	285
Inductance (μH)	L_{least}	1123	440	355	257
Number of turns	N	27	42	42	42
Air gap (mm)	g	1.55	-	-	-
Winding resistance (mΩ)	R_L	39.6	28	28	28
Peak flux variation (mT)	B_{pk}	113.4	90.1	78.6	65.5
Avg. Inductor current (A)	$I_{L(avg)}$	9.52	9.52	9.52	9.52
Inductor ripple (p-p) (A)	ΔI_L	8.76	9.06	11.03	15.02
Core Loss (W)	P_{core}	2.05	16.40	11.75	8.03
Copper loss (W)	P_{cu}	3.84	3.65	3.77	4.02
Total inductor loss (W)	P_L	5.9	20.06	15.53	12.05

shown in Table V, with *N* ranging from 43 to 56. However, the bobbin can only accommodate a maximum of 42 turns with 1000x0.071mm litz. Therefore the inductor is re-designed with 42 turns as shown in Table V and Table IV, resulting in an inductor of 529µH, 405µH and 285µH for the three cores.

The inductor losses are estimated in the same fashion as mention for the ferrites using (21) to (27). A=193, b=2.01, a=1.29 for 60µ core and A=120, b=2.09, a=1.46 for KoolMµ 40µ, 26µ powdered core when P_{core} is in mW/cm^3, f_{sw} in kHz, B_{pk} in T and V_e in cm^3 [28]. The core and copper losses are calculated and shown in Table V, where the losses range between 20W to 12W per inductor.

3) Ferrite Vs Kool Mµ inductor

The main advantage of the much higher switching frequency and saturation flux density of Kool Mµ is that only a single core set is required per inductor. This results in a three time reduction in inductor size compared to ferrite core, as shown in Fig. 6. This results in big reduction in converter volume due to size reduction of three inductors. Secondly, the powder cores exhibit gradual reduction in inductance with fault current, unlike ferrites that quickly saturate to zero inductance. This helps in making the protection and control of the converter easier and robust. Thirdly, powder cores have a distributed air gap which causes very low copper loses because of the fringing flux. Fringing flux causes extra losses at high frequency when using ferrite cores, especially if they have

TABLE V

INDUCTOR DESIGN USING KOOLMµ CORE

KoolMµ Core	**60µ**	**40µ**	**26µ**		**60µ**	**40µ**	**26µ**
A_L (nH/T^2)	300	230	162		300	230	162
N	43	47	56		42	42	42
L (µH)	554	508	508		529	405	285
L_{least} (µH)	461	444	457		440	355	257

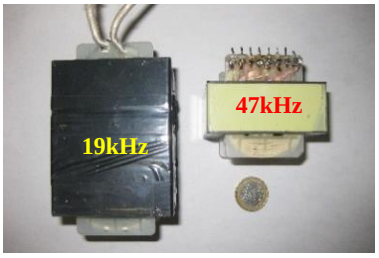

Fig. 6 – Reduction in size of inductor from 3xE65 cores (left) for 19kHz ferrite inductor to 1xE65 core sets for 47kHz KoolMµ inductor

a center gap instead of a gap in the outer legs. From the cost point of view for high volume purchases (~100-1000 pieces), it is interesting to note that even though the cost of one Kool Mμ core set (~6.5$) is much higher than a ferrite core set (~1.5$), the two inductors have similar net cost for core - the ferrite inductor has three core sets and costs 4.5$ (3*1.5$ per core set) while the KoolMμ core costs 6.5$.

The disadvantage of KoolMμ is that the inductor losses are nearly two to four times of that found in the ferrite core, as in Table V. The main reason is that powder iron cores are characterized by higher core losses and the switching frequency of 47kHz is more than two times of the 19kHz frequency. It is for this reason that 40μ and 26μ core are preferred over the 60μ as they have much lower losses. This is because the core with the lower permeability has a lower ΔB for the same ΔH, leading to lower core losses as shown in (21).

C. Sizing of input and output capacitor

When using an IBC, an input capacitor is sized to supply the ripple current ΔI_{in} based on:

$$C_{in} = \frac{1}{2}\left(\frac{T}{2N_i}\right)\left(\frac{V_{\mathrm{dc}}}{8f_{sw}LN_i}\right)\left(\frac{1}{\Delta V_{in}}\right) \quad @\ D = \frac{A_{int}}{2N_i} \qquad (28)$$

In this design, an input capacitor of 10μF is used which results in a voltage ripple of ΔV_{in}=0.1V for the 47kHz design. A much higher capacitor of 25μF is required for the 19kHz design. An additional LC filter (L_{fin}=47μH, C_{fin}=5μF) is used between the input capacitor and PV to further reduce this ripple voltage.

For a stand alone IBC, the output capacitor C_{out} can be sized based on [29] in order get a peak to peak output voltage ripple of ΔV_{out}, where *q, q'* are the rise and fall times of the input current:

$$C_{out} = \left(\frac{1}{\Delta V_{out}}\right)\left(\frac{I_0 q q'}{f_{sw}N_i^2(1-D)}\right) \qquad (29)$$

Since the IBC is used as an intermediate stage of a PV inverter for the Si and SiC design, the output capacitor is sized based on the speed of the closed loop control and the necessary DC link buffer capacity. Two 470μF, 450V electrolytic capacitors connected in series form the DC link buffer. A 470nF metal film capacitor is connected at the output of each of interleaved legs and located close to the diodes on the PCB to partially filter the high frequency output ripple. The ratio of output ripple shared between the film and electrolytic capacitor is difficult to

estimate before-hand as it depends on the capacitance, ESR, temperature and relative location on the PCB. The values were arrived at based on experimental measurement.

D. DCM Vs CCM operation

The operation of the converter in CCM and DCM mode is determined by the input PV voltage, power and the size of inductor. In Fig. 7, the operating mode of the converter as a function of different input PV power and voltage are shown when using the 40µ KoolMµ inductors. The plot considers the fact that the powdered core inductance reduces at high powers due to soft saturation. If larger input capacitor is used, the CCM and DCM operating regions of IBC can be varied by reducing the core permeability from 40µ to 26µ, core as in Fig. 7.

The 26µ core makes the converter to operate predominantly in DCM at high powers. The inductance reduces from 405µH to 285µH increasing the ripple in the inductor and core losses. However the benefit is that the switching losses in the DCM are lowered due to zero current switching (ZCS) during turn-on. This is especially useful when the converter is operated at high switching frequencies at 47kHz.

IV. CLOSED LOOP PV CONVERTER CONTROL

A closed loop controller for the PV converter is built which has four control loops working in parallel to control the duty cycle *D* as shown in Fig. 8 and shown by the equation:

$$D = D_{max} - d^* \qquad (30)$$

The control output d^* is the maximum value as dictated by all the four loops and the maximum duty cycle D_{max} for the converter is set at 62.5%. The diodes in the control loop show that at any time only one of the four loops will be active and will determine *d** and subsequently *D*. The first loop is a MPPT control loop that continuously

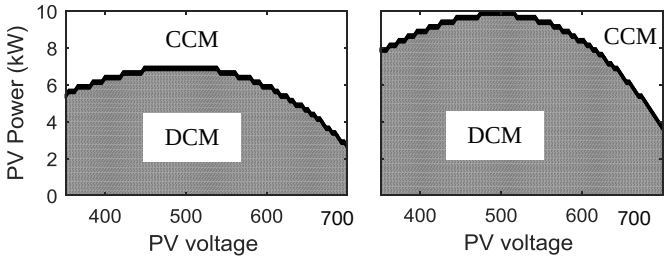

Fig. 7 – Boundary between CCM and DCM using 40µ(left) and 26µ(right) Kool Mµ core. 26µ core inductor has larger operation in DCM.

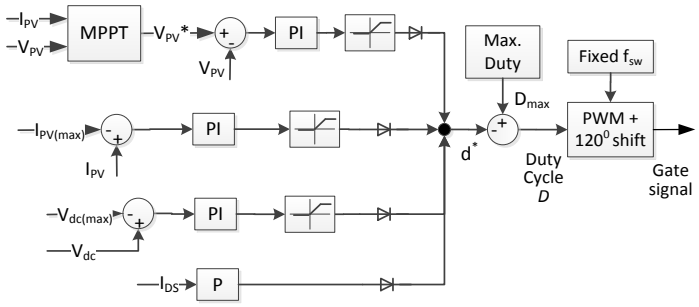

Fig. 8 – Schematic of the closed loop control of PV pre-converter

adjusts the duty cycle of the IBC by perturb and observe method based on measurements of the input voltage and current [30]. A microcontroller is used to measure V_{PV}, I_{PV} for MPPT control to determine the MPPT voltage V_{PV}*. The second and third loops are for power curtailment operation to move the PV array out of MPPT. The second loop adjusts the duty cycle to limit the input PV current I_{PV} based on a user-defined set point $I_{PV(max)}$. The absolute maximum input current is set at 32A and boost converter duty cycle is limited if the input current is higher.

The third loop reduces the duty cycle when the output voltage is beyond the rated value. The DC/AC inverter is responsible for maintaining the DC-link voltage at the rated value of V_{dc}=750V. If however, the DC link voltage goes beyond $V_{dc(max)}$=795V, the third loop has a PI controller to limit the duty and reduce the PV power fed into the DC link. The fourth loop continuously measures the drain source current of the SiC MOSFETs in each of the three legs. When the current increases beyond the switch rating, the fourth loop limits the duty or reduces the duty cycle to zero to protect the converter.

A microcontroller is used to generate three phase shifted sawtooth waveforms. This is compared with the duty cycle obtained from the control loop using a comparator, to generate the PWM signals for the three interleaved legs. A soft-start mechanism is built in to the controller to limit the duty during start-up.

The control loop in the DC/AC inverter for the IGBT version monitors the DC-link voltage and controls the PWM switching to maintain the DC-link voltage at the rated value of 750V. As mentioned in the introductory section, a common mode voltage ripple of 300Hz exists on the DC link capacitor. A secondary control loop in the DC/AC inverter controls the switching of the three phases so as to compensate and make this ripple close to zero.

By this mechanism the leakage currents from the PV panel to ground are nearly eliminated.

V. Loss Estimation in Converter

The clear distinction between the Si and SiC design can be seen in the losses in the components and the corresponding efficiencies obtained. Fig. 9 shows the on-state voltage of the Si IGBT and SiC MOSFET based on the datasheet, where the MOSFET shows lower on-state voltage at currents <20A even though it is a majority carrier device. This is primarily due to the on-state voltage of ~1V of the IGBT which exists even at <1A. For currents >20A, the IGBT has lower on-state losses. Secondly, the switching losses for the SiC are less than two times than the IGBT. This is the primary reason that enables the SiC converter to operate at nearly 2.5 times the switching frequency of the Si design. Thirdly, the conduction losses in the Si and SiC diodes are comparable at

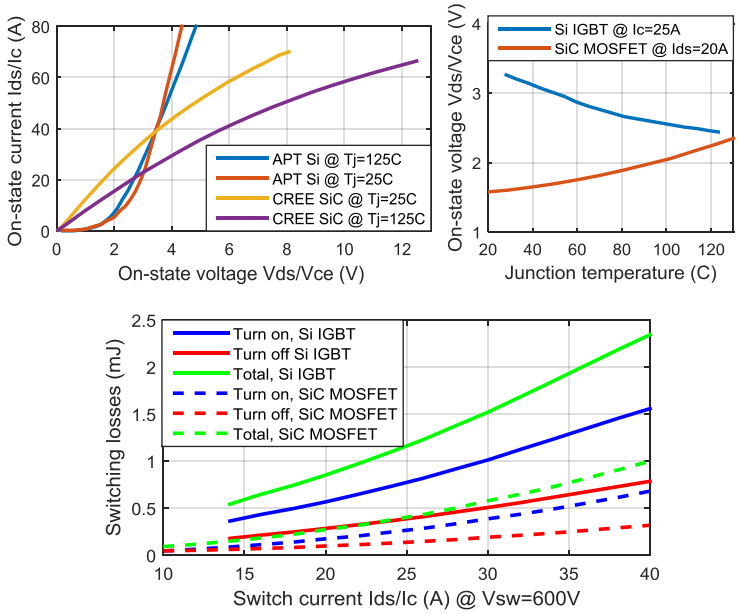

Fig. 9 – Conduction and switching loss characteristics of the APT Si and CREE SiC switch

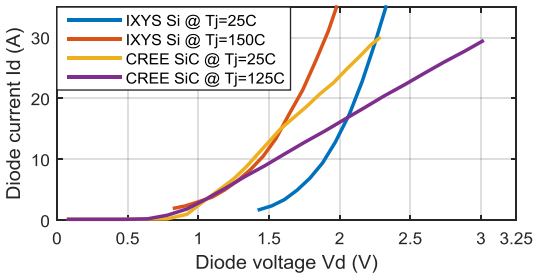

Fig. 10 – Conduction loss characteristics of the IXYS Si and CREE SiC diode

currents <20A as shown in Fig. 10. At lower temperatures, the SiC diode exhibits lower turn on voltage than the Si diode. The main advantage is however that there are practically no reverse recovery losses in the SiC diode when compared to the recovery charge of 1-2 µC for the Si diode. Without SiC, at 47kHz with 1µC recovery charge of the Si diode, the losses in the diode and switch due to reverse recovery could amount to 44W per leg. Hence the SiC devices give the double benefit of both lower conduction and switching losses.

A. Switch and diode loss estimation

The turn on and turn off currents of the switch $i_{F(on)}, i_{F(off)}$ and diode $i_{D(on)}; i_{D(off)}$ are related to inductor current by

$$i_{F(on)} = i_{D(off)} = I_{L(\min)} \tag{31}$$

$$i_{F(off)} = i_{D(on)} = I_{L(\max)} \tag{32}$$

Discrete totem-pole transistors and a comparator IC are used for the gate drive circuit. For the Si IGBT, a turn on and turn off gate resistance R_G of 56Ω and 22Ω are used respectively, with a gate voltage V_{GE} of 15V. For the SiC MOSFET, a gate voltage V_{GS} of 20V is used. A turn-on and turn-off gate resistance of 37.7Ω and 4.7Ω is added respectively to the already present internal gate resistance of 4.7Ω. There are two reasons for using a high turn-on gate resistance for the SiC even though it will reduce performance. With a motive to commercialize the SiC PV converter and to adhere to the EMI requirements as per standard EN55022, larger gate resistances were used to deliberately slowdown the switches. This results in increases switching losses but reduces the additional filters, Y caps and snubbers that will be required to keep the EMI within limits which will make the converter expensive and bigger. Hence there is a trade-off between switching performance and EMI when working with fast switching SiC MOSFETs. Secondly, the 26µ KoolMµ core makes the converter predominately work in DCM with soft-switching during turn on, so a higher gate resistor did not reduce switching performance drastically over the entire operating range.

The conduction losses P_{cond} and switching losses P_{sw} in the devices can then be estimated based on the junction temperature T_j and V_{GE}/V_{GS} using:

$$P_{cond\_MOSFET} = I_{rms}^2 R_{DSon(T_j, V_{GS})} \tag{33}$$

$$P_{cond\_IGBT} = I_{avg}V_{ce(on)(T_j,V_{GE})} + I_{rms}^2 R_{c(on)(T_j,V_{GE})} \quad (34)$$

$$P_{sw} = f_{sw}\left\{E_{on(R_G,T_j)} + E_{off(R_G,T_j)} + E_{rr} + E_{dch}\right\} \quad (35)$$

$$E_{rr} = Q_{rr}V_R \quad (36)$$

$$P_{cond\_DIODE} = I_{avg}U_{D0(T_j)} + I_{rms}^2 R_{D(T_j)} \quad (37)$$

$$E_{rr\_D} = \frac{1}{4}Q_{rr}V_R \quad (38)$$

where I_{rms}, I_{avg} are the RMS and average device current, $R_{DS(on)}/R_{c(on)}/R_d$ is on-resistance of device, E_{on}, E_{off} are turn-on and turn-off losses of switch, E_{dch} is loss due to charging of diode parasitic capacitance, E_{rr} and E_{rr_D} are the loss in switch and diode due to reverse recovery charge Q_{rr}, $V_{CE(on)}/ U_{D0}$ is on-state voltage of IGBT and diode, and V_R is turn off voltage across device. The loss in the power semiconductor devices and inductor have been estimated at the worst case operating point of 10kW and shown in Fig. 11 for different PV voltages. The ambient and junction temperature was assumed to be 25ºC and 75ºC respectively in the estimation. It can be clearly observed that the losses in the switch have been reduced by nearly half between the Si and SiC design even though the switching frequency has been increased. A marginal reduction in the diode losses can be observed mainly driven by the absence of reverse recovery in SiC schottky diodes.

Operation of the SiC devices at higher junction temperature above 75ºC was not considered due to two reasons. With the aim to create a commercial product with atleast a 10 year reliable lifetime, high junction temperature increases the average heat sink temperature of all components as the switches and diodes are mounted on the same heat sink.

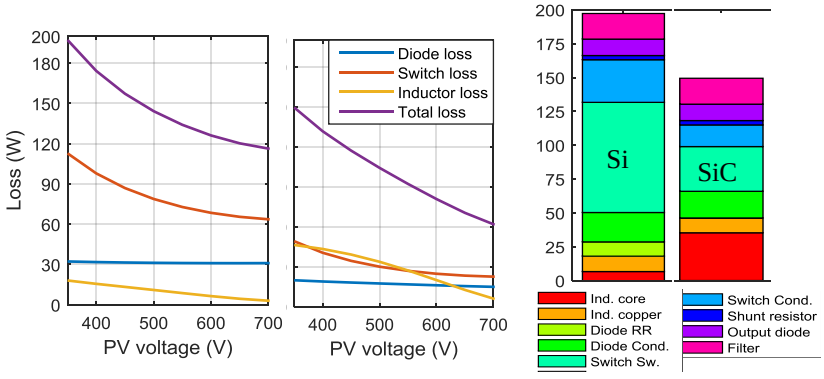

Fig. 11 – Loss characteristics of the Si (left) and SiC (middle) converter as a function of input PV voltage for 10kW power. (Right) Split up of losses for 350V PV input voltage and 10kW maximum input power for Si IBC (left side) and SiC IBC with 40µ core (right side)

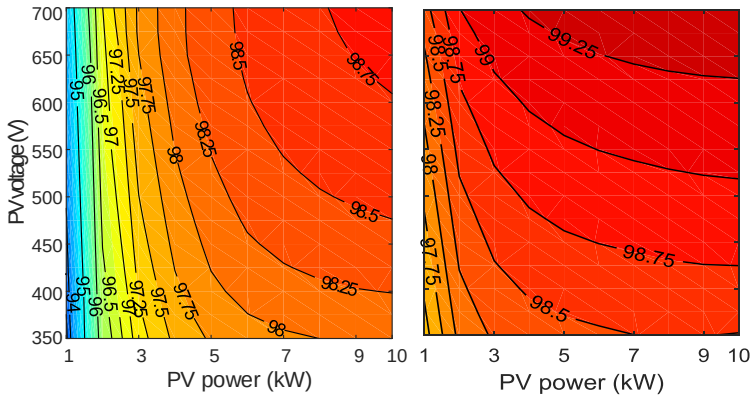

Fig. 12 – Estimated efficiency contour as a function of PV voltage and power for the Si (left) and SiC converter (right) with 40µ core

This increases the average temperature inside the enclosure and significantly reduces the lifetime of all components in the converter. Secondly, SiC MOSFET has a worse performance at higher temperature than at lower temperature with respect to conduction losses.

From the cost point of view for bulk purchase, the SiC MOSFET costs approximately three times as much as the Si IGBT which is around ~3.5$. SiC diode is four times as expensive as the Si diode of ~1.5$. This translates to around 35$ extra cost of the SiC converter considering three diodes and switches.

B. Additional losses

Additional losses are observed in the converter due to losses in the input common mode filter (4mΩ), fuse, input LC filter (11mΩ for L_{fin}, 13mΩ ESR for C_{fin}), output capacitor (C_{fdc} with tanδ=0.03) and three 20mΩ shunt resistor added to the source of the switch for current control. An extra diode (VS-40EPS) is added at the output of the IBC for protection to prevent reverse current during testing. This causes an additional loss than can be estimated using (37). Since the output current is the same for Si and SiC converters, output diode losses amounted to approximately 12W and 1.1W at full load and 10% load respectively. This diode can be removed when implementing the converter in practice when an inverter is connected at the output.

C. Total Losses & Efficiency

Fig. 12 shows the estimated efficiency of the two converters as a function of PV voltage and power. The improved efficiency of the SiC inverter over the entire operating range can be seen with efficiency of over 98% in

majority of the operating region. The improvement is not as drastic as would be expected as the improved switching performance of SiC has been traded off with increased switching frequency.

The split up of losses within the different components is shown on the right side of Fig. 11 at maximum input current when input is 350V, 10kW. The bar graph shows how the switching losses have been reduced drastically from 131W to 33W when using SiC, while losses in the inductor core have increased from 6W to 35W with the use of 40µ powdered iron core. A significant reduction in the conduction losses of the switch from 31W to 16W can be observed as well.

VI. Experimental Setup & Verification

A. Power density of the prototype

A full scale 10kW prototype was built for both Si and SiC IBC including the closed loop control as shown in Fig. 13. The DC/AC inverter was built for the Si converter and integrated on the same power PCB as the IBC.

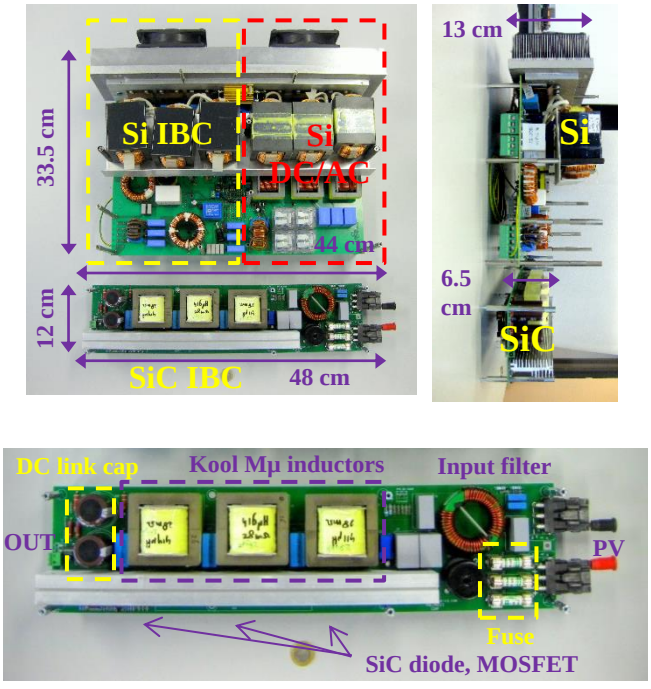

Fig. 13 – Physical realization of Si IBC + Si DC/AC converter (Dimension: 44 x 33.5 x 13 cm) and SiC IBC (Dimension: 48 x 12 x 6.5 cm). Si converter is built over two vertical levels while the SiC is compact in one level (top). Top view of SiC IBC showing the three E65 KoolMµ inductors, output DC capacitors, input filter and fuse (bottom).

The three large E65 ferrite inductors with 3 core sets each can be seen. The total converter dimensions are 44x33.5x13 cm and the Si IBC occupies approx. 50% of the total converter volume. In contrast, the SiC IBC is much smaller in size at 48x12x6.5 cm, exhibiting a nearly 2.5 reduction in volume but still maintaining a comparable efficiency over the operating range. This is mainly due to the reduced size of inductor and smaller heat sink owing to the reduced losses in the switching devices. This is the biggest benefit of using SiC devices and powdered iron core inductors for high power converters. SiC based DC/AC converter is currently being developed and hence not shown in the figure.

B. Experimental setup and waveforms

Fig. 14 shows the experimental setup used in the lab to test the prototypes of the two converters and measure its efficiency. A DC power supply (Chroma 62150H-1000S) that has the capability to mimic a PV panel was used as input and a resistive load was connected at the output. To maintain the DC link voltage at the output at 750V without the DC/AC inverter, the third control loop that operates on DC bus voltage was set with a reference of 750V. A current probe was used for measuring the inductor current I_L via an oscilloscope. A 1mΩ current shunt and voltmeters were used at both input and output terminals for the input and output current and voltage measurements respectively. The DC power supply and load were adjusted to operate the converter in different operating points with respect to input voltage and output power.

Fig. 15 shows the waveforms obtained for the SiC IBC with 26µ KoolMµ core. Waveforms for the 120º phase shifted gate-source voltage $V_{GS(1)}$, $V_{GS(2)}$, $V_{GS(3)}$ for the three legs of the SiC IBC can be seen in Fig. 15 (top). The closed loop controller determines the duty cycle D and generates the 20V PWM signals for the three legs.

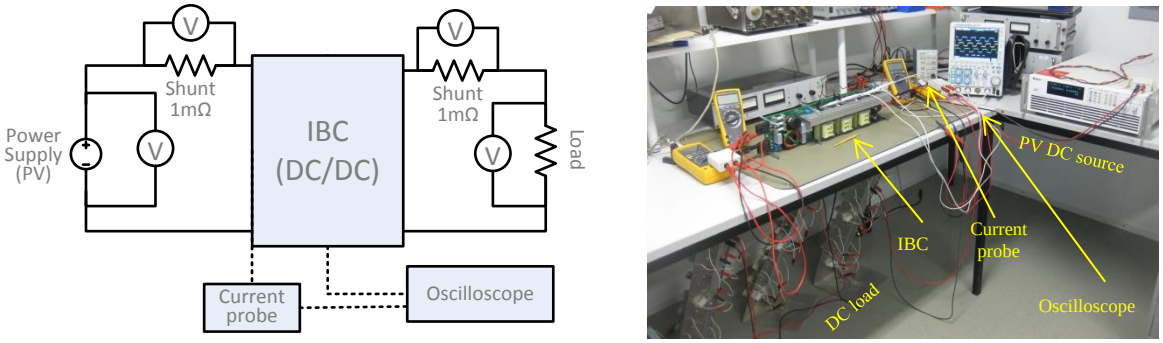

Fig. 14 – Schematic of experimental setup (left) and actual setup in lab (right)

Inductor current $I_{L(1)}$, gate voltage $V_{GS(1)}$ and drain source voltage $V_{ds(1)}$ for DCM can be observed in Fig. 15 (middle) for one of the legs when V_{PV}=400V, I_{PV}=10.75A. The inductor current $I_{L(1)}$ (pink) rises when the gate voltage $V_{GS(1)}$ (yellow) is ON and then begins to fall once the gate is OFF. In DCM, the inductor current $I_{L(1)}$ goes to zero before the end of the switching cycle causing the drain source voltage $V_{ds(1)}$ (green) to oscillate as it goes from $V_{ds(on)}$ to V_{PV}. The oscillating drain-source voltage is due to the energy exchange between the inductor and

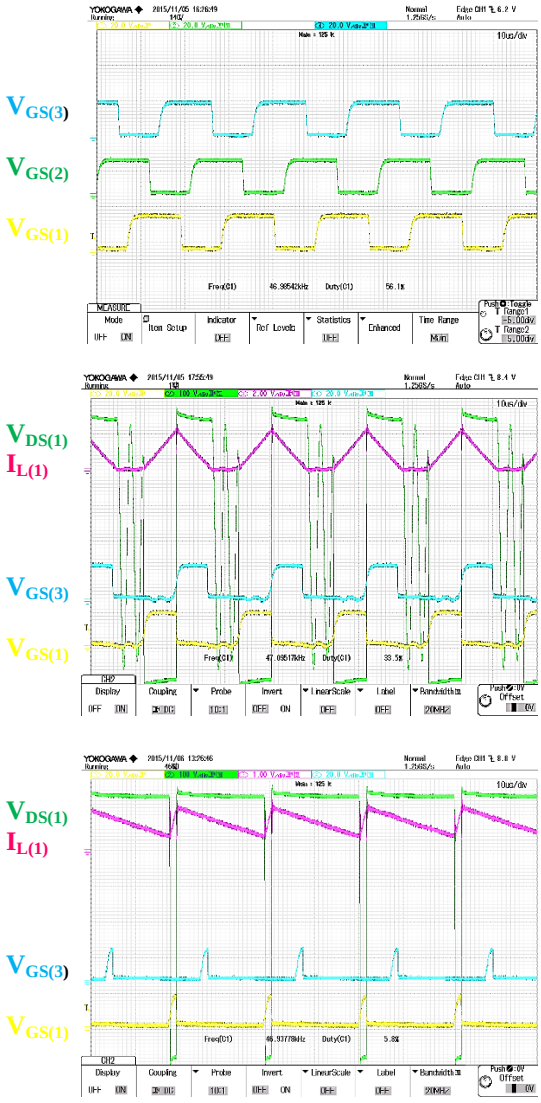

Fig. 15 – Waveforms obtained from Yokogawa DLM2024 oscilloscope for the phase shifted gate-source voltage V_{GS} for the three legs of the SiC interleaved converter (top). Inductor current I_L, gate voltage V_{GS} and MOSFET drain source voltage V_{ds} for DCM (middle) and CCM (bottom). The oscillating drain-source voltage can be observed when the inductor current reduces to zero (middle).

the drain-source capacitance of the switch. In Fig. 15 (bottom), V_{PV}=700V, I_{PV}=10A and the converter operates in CCM. The inductor current $I_{L(1)}$ (pink) flows continuously and the drain source voltage $V_{ds(1)}$ (green) does not exhibit any oscillations. The CCM, DCM mode of operation was checked for different combination of input voltage between 350V to 700V and powers between 1kW to 10kW and was found to be as estimated in Fig. 7 for Si IBC and for the SiC IBC with 26µ and 40µ core inductor.

C. Efficiency measurement

The efficiency of the Si IBC with ferrite core and SiC IBC with 26µ and 40µ core was measured for different PV voltages and loads as shown in Fig. 16. The efficiency was calculated based on the measurements of the input and output current and voltage of the IBC for different loads as shown in the schematic in Fig. 14. It can be seen that the performance of three converters shows an efficiency of >98% in majority of the operating region, even with hard switching. The efficiency of SiC IBC with 26µ core is comparable to the Si IBC, even though the switching frequency is 2.5 times and the inductor size in one-third. This has been primarily achieved due to the use of SiC devices as against Si and KoolMµ core. The performance of the Si IBC is however found to better at partial power ≤4kW. Maximum efficiency and European efficiency of the silicon PV inverter (DC/DC+DC/AC) was found to be 96.3% and 95.4% respectively.

The efficiency curves of the IBC shows small peaks and troughs especially at low powers for both converter types and at high powers with the SiC with 26µ core. This is due to operation in DCM mode. In DCM, the power

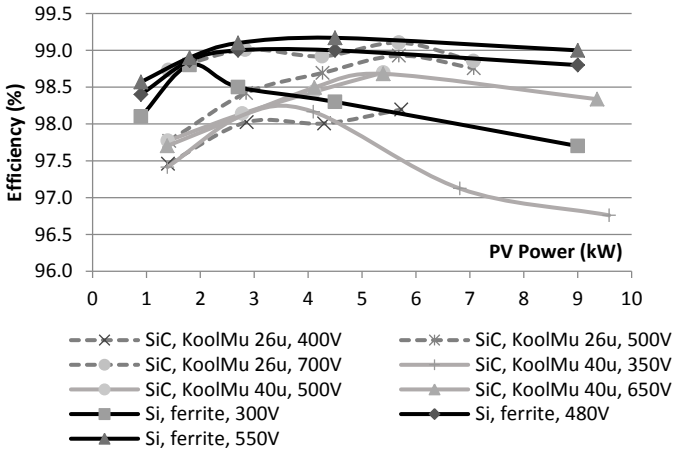

Fig. 16 – Measured efficiency of the Si IBC with ferrite inductors and SiC IBC using KoolMµ 40µ and 26µ inductors

losses in the three switches due to discharging of the drain-source capacitance is characterized by the point on the oscillating drain source voltage at which the switch turns on, as seen in Fig. 15 (middle). If the switch turns on at the bottom of the valley, the losses are the least and it results in quasi-resonant switching.

The difference between the measured and estimated efficiencies is due to the following reasons:

1. Loss estimation is made with an assumption of a fixed junction of 75ºC. In practice, the junction temperature continuously varies and affects the losses in the switch and diode.
2. The loss model for estimating the core losses does not consider the DC bias in the inductor current [31] and temperature variation.
3. The loss model linearly extrapolated several values from the datasheet to account for differences between operating conditions and datasheet measurements for device voltage, current, gate resistance, junction temperature. The turn-on gate resistance used is especially much higher than the nominal values provided by the manufacturer and loss dependency is not strictly linear. This is especially true for SiC where the losses increase drastically with gate resistance and becomes an important factor in CCM where turn-on losses are significant.
4. The current sharing between the three interleaved SiC switches was not found to be equal when operated in CCM, showing differences of upto 5 ºC on switch case temperature. This was especially true when using the 40µ core where the converter operates in CCM in practically 50% of the operating region as shown in Fig. 7. The main reasons for this is the soft saturation of the powdered iron core inductor (which causes the actual operation inductance to be slightly different in each leg), PCB layout, thermal conduction of heatsink and offsets in the duty cycle between the three legs.
5. During the testing of the Si IBC, the output diode was removed as it was connected with the DC/AC inverter. So the measured losses were hence lower than the estimated losses by approximately 12W or 0.12% at full load operating conditions shown in Fig. 11 and Fig. 12.

VII. CONCLUSIONS

In this paper, the design of a 10kW three-leg interleaved boost converter for a PV inverter has been elaborated

in detail. IBC converters are excellent choice for DC/DC converters for MPPT operation and boosting of PV voltage for interfacing with a three phase grid. The use of three interleaved legs, reduces the peak input ripple by nine times and reduces the current through each leg by three times. This allows the use of 900V/1200V, 30A switches and diodes that are widely available for commercial use. Further, interleaving reduces the physical size of inductor facilitating the ease of PCB mounting and also reduces the net volume of inductor core required in the converter.

Two designs of the IBC were compared in this study – one using Si IGBTs, diode and ferrite core inductors and the second using SiC MOSFETs, schottky diodes and powdered iron core inductors. The use of wide-band gap SiC devices and KoolMμ powdered iron core with high saturation flux density allowed the operation of the IBC at 47kHz frequency, nearly 2.5 times the switching frequency possible with the Si devices. Since MOSFETs are majority carrier devices as compared to IGBTs, the switching losses were reduced by three times even though the switching frequency was 2.5 times higher. At the same time the conduction losses remained the same, due to low $R_{DS(on)}$ on SiC devices. The use of 26μ powdered iron core inductor moved the converter operation to DCM and this further reduced the switching losses.

The higher switching frequency allowed the use of smaller size of passive elements – the inductor core size reduced from three parallel cores to one and input capacitor was reduced by nine times. The disadvantage was however that the core losses in the inductor increased by nearly five times due to the higher core losses in KoolMμ powdered core inductors as opposed to ferrite. The loss increase would have been much worse, going up to ten to twenty times if other types of powdered iron cores were used instead of KoolMμ. The use of KoolMμ cores with soft saturation resulted in variable inductance and non-linear currents during operation. This caused current sharing problems between the legs in CCM. The use of 26μ core, shifted the operation of the converter in the majority of the operating region to DCM.

Full scale 10kW prototypes were built for both converters with closed loop control. The SiC IBC had 2.5 times higher power density than the Si version with less than 1% difference in measured efficiency over the operating region. The closed loop control allowed for MPPT, input current control and output voltage control. The measured peak efficiency of both the Si and SiC IBC was above 99%.

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