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A 60mV Input Voltage, Process Tolerant Start-up System for Thermoelectric Energy Harvesting

Mohammadjavad Dezyani, Hassan Ghafoorifard, Samad Sheikhaei and Wouter A. Serdijn *Fellow, IEEE*

***Abstract*—This paper presents a 60mV input voltage start-up system for thermoelectric energy harvesting. A new process tolerant inverter cell is proposed, which is functional at supply voltages as low as 60mV. Using the proposed unit cell, a ring oscillator has been implemented. The ring oscillator is followed by 40 charge-pump stages, an ultra-low-power level detector and a boost converter. The energy harvesting system can generate an output voltage of 1V and delivers a maximum power of 4.5 µW from a 60mV supply. This system has been implemented in a standard 0.18 µm CMOS technology, uses neither zero-threshold voltage (normally-on) NMOS nor MEMS switches and occupies 3.3 mm^2.**

***Index Terms*—Energy harvesting, Thermoelectric generator, TEG, Low power design, Low voltage, CMOS.**

I. Introduction

CMOS technology advances have realized yesterday's dreams, as electronic device miniaturization has improved remarkably. Small-size electronics is widely used from bio-medical implants to wireless sensor networks (WSN). In all these tiny electronics, the power supply is one of the most challenging issues. Using batteries is, of course, a possible solution. However, batteries have some drawbacks, such as limited life time, containing toxic materials and, above all, they are very bulky. Though IC technology has advanced to nano-meter technologies, the batteries still remain bulky, as the increase in battery energy density goes at a very slow pace and even seems to a stop. In many cases, most of the volume of a portable electronic device is occupied by its battery. These drawbacks have created the need for battery-less electronics [1].

Using ambient energy sources is the key to realize battery-less electronics. Ambient sources include: light [2], RF signals [3], mechanical vibration [4], thermal gradients [5][6][7], etc. Among these sources, thermal gradients are almost available everywhere, especially in biomedical implants and body-worn devices [8]. Thermoelectric generators (TEG), which convert temperature difference into electricity, are relatively simple compared to other converters such as piezoelectric materials that convert mechanical vibration into electricity and have the highest harvested energy density [9].

The output voltage of a TEG for available thermal gradients (2-3K) is less than 100 mV [10]. This small voltage cannot drive ordinary CMOS circuits. Low-voltage start-up systems are necessary to step this low voltage up to a higher voltage (of around 1V), where ordinary circuits can be driven.

Different techniques have been proposed to enable start-up from voltages below 100 mV. These methods include transformer-based boost converters, inductive boost converters, and capacitive boost converters. The use of a transformer with a high turn ratio has been proposed in [11] and [12]. However, using a bulky transformer is not suitable for many applications that require small size, such as smart dust or implantable or wearable devices. The transformer turn ratio has been reduced to 1:1 in [13] and [14], which leads to smaller transformers. In order to further reduce the transformer size, micro-transformers have been introduced in [15] and [16]. The main drawback of these methods is the use of an off-chip transformer which is bigger than an off-chip inductor. Piezoelectric transformers have also been used to kick start a thermoelectric energy harvesting system [17][18], however the piezoelectric transformer is very bulky as well. In [19], a mechanically assisted MEMS switch has been used to activate an inductive boost converter. Another commonly used technique is to use multiple charge-pump stages. For example in [20], a differential bootstrapped ring oscillator has been used to drive a charge pump.

In all these methods an oscillator is necessary. In order to start oscillation, native, i.e., near zero-threshold voltage, also known as depletion-mode transistors have been used [21] [22]. In [21], two cross-coupled native NMOS transistors with an inductive load have been used. In [22], a very low-voltage oscillator with on-chip inductors has been proposed. In all these techniques native transistors were used. However, native

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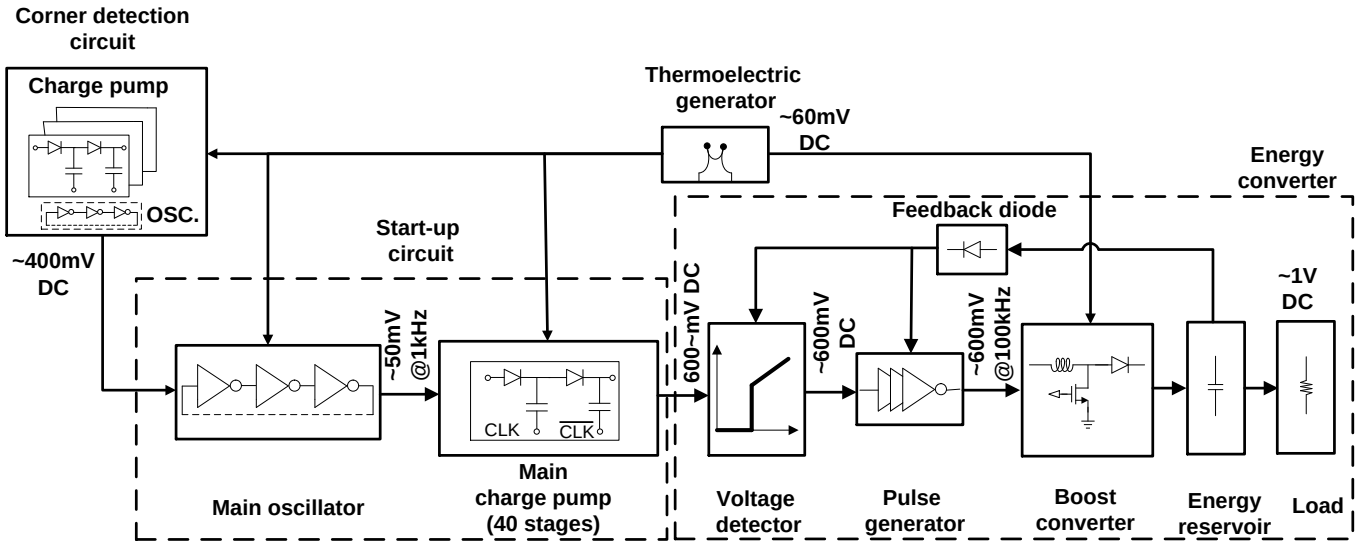


Fig. 1. Proposed energy harvesting system architecture.

transistors are not available in CMOS technologies, as extra processing steps are needed. In [23], the minimum supply voltage of an ordinary ring oscillator has been reduced using post-fabrication processing. Although this method is compatible with standard CMOS, due to the post-fabrication process, the yield is low and the cost increases. In [24], body biasing has been used to decrease the startup voltage of a ring oscillator. Unfortunately, the ring oscillator presented there is not functional in all process corners. In [25], a Schmitt-trigger based ring oscillator has been proposed. This technique also uses standard CMOS technology. However, since stacked transistors are used, it requires a higher minimum supply voltage.

In this paper, a new inverter cell is proposed that is process tolerant. Additional circuits have been added to a conventional inverter to guarantee its functionality in different process corners. The proposed inverter cell is used in a ring oscillator and in driver circuits for driving multiple charge-pump stages. Using this method, oscillation and input voltage boosting is guaranteed in all process corners. The charge pumps are followed by a sub-nW level detector and a boost converter. This method is standard CMOS compatible and does neither need post fabrication nor trimming. The only off-chip elements in the complete energy harvester are an inductor and a capacitor.

The rest of this paper is organized as follows. In Section II, the proposed startup system is introduced. In Section III, its circuit-level implementation is explained. Experimental results are presented in Section IV. Finally, Section V concludes the paper

II. Startup System Architecture

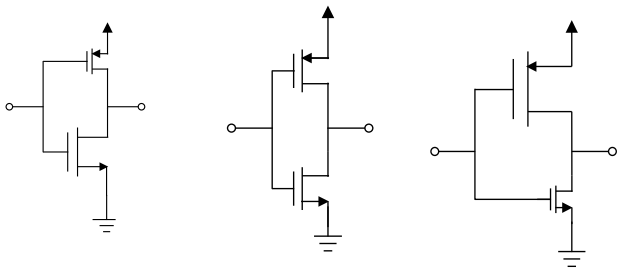
Fig. 1 illustrates the proposed energy harvesting system. The energy harvesting system delivers power from a TEG to a load. The start-up circuit consists of a ring oscillator and a 40-stage charge pump. The energy converter consists of, a level detector, a pulse generator and a boost converter. The low output voltage of the TEG (of about 60mV) is fed to a main oscillator, a corner detection circuit and a boost converter. The corner detection circuit generates a high amplitude voltage (of about 400mV) that is used to sustain system operation across all process corners. The proposed inverter cell is used in the main oscillator and the drivers of the main charge pump. With this structure, the main charge pump can generate about 600mV from the TEG output voltage. An ultra low-power voltage detector is proposed that enables the pulse generator. The pulse generator generates a switching signal for the boost converter. Once the boost converter is driven by the pulse generator, the system starts up and delivers a sufficient amount of power. After the start-up, the pulse generator is supplied from the output capacitor via a feedback diode as shown in Fig. 1. The only off-chip elements are an inductor and a capacitor.

A. Ring oscillator

In order to drive a charge pump, two periodic complementary signals (CLK and CLK_BAR) are necessary. To generate these signals, an oscillator is used. As mentioned in Section I, different techniques using native NMOS transistors with inductive loads have been used to realize an oscillator previously. However, ring oscillators at supply voltages below 100 mV are very sensitive to process variations. At these small supply voltages (2 or 3 times the thermal voltage V_T), the transistors operate in their subthreshold region and their I_{ON}/I_{OFF} ratio is very small. Simulation results show that for a 60mV supply voltage, I_{ON}/I_{OFF} is about 5, which is comparable to transistor current deviation due to process variations. If all transistor variations happen in one direction (all transistors going fast or slow at the same time) these variations are automatically compensated. An inverter cell consists of a pull-up PMOS network and a NMOS pull-down network. The FS (fast-slow) and SF (slow-fast) corners have opposite effects on these transistors, weakening one and strengthening the other. As a result, at small supply voltages, these corners can cause an inverter cell to fail. Fig. 2 illustrates a graphical view of the effect of FS and SF corners on a basic inverter cell.

As illustrated in Fig. 2 (a), in the FS corner, the pull-up network is weakened while the pull-down network is strengthened, compared to the typical TT (typical-typical) corner of Fig. 2 (b). In the SF corner or Fig. 2 (c), the pull-down network is weakened while the pull-up network is strengthened.

Fig. 3 shows the simulated minimum supply voltage for an eleven-stage ring oscillator for different corner cases in AMS 0.18 µm CMOS technology, which is the technology of choice in this paper. The minimum supply voltage increases up to 40% in the FS and SF corners, while in the FF (fast-fast) and SS (slow-slow) corners the minimum supply voltage is the same as in the TT corner. This is because in FF and SS, both NMOS and PMOS deviate from TT in one direction.



(a) (b) (c)

Fig. 2. Graphical view of an inverter in different process corners, (a) FS corner (b) TT (nominal) corner and (c) SF corner.

The deviation from the TT corner in the FS and SF corners is even worse in smaller technologies. For example, in 65nm technology, the minimum supply voltage varies from 70 mV in the TT to 220 mV in the FS corner [23].

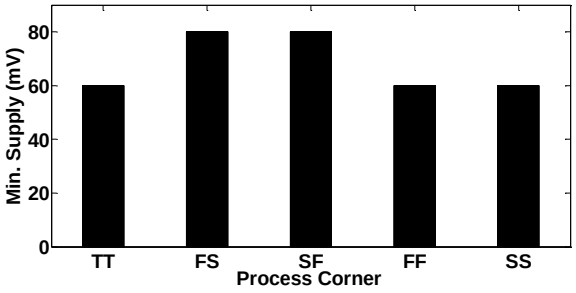


Fig. 3. Minimum supply voltage for an eleven-stage ring oscillator in different process corners.

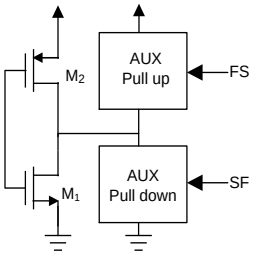


Fig. 4. Proposed process tolerant inverter cell.

A new inverter cell is proposed that is functional in all corners. Fig. 4 displays the proposed process-tolerant inverter cell. It consists of a basic inverter, M_1 and M_2, and two auxiliary pull-up and pull-down networks. Assuming operation in the SF corner, in which the NMOS transistor is slow and the PMOS transistor is fast, an auxiliary pull down transistor network is configured in a parallel scheme with the original pull-down transistor. If the auxiliary pull-down network is activated in the SF corner, the pull-down network is compensated and the inverter cell becomes functional in the SF corner. In the FS corner, an auxiliary pull-up network is added to the main pull-up network, which also makes the proposed cell functional in this corner. The transistor-level implementation of this block is explained in Section III-A.

In order to activate the auxiliary pull-up/down networks, the TEG output cannot be used due to its very small output voltage. A corner detection circuit that can generate the higher voltages necessary to activate the auxiliary pull-up/down network (SF and FS signals in Fig. 4), is proposed, which is described in the following subsection.

B. Corner detection and switch control signals generation

As explained in the previous subsection, in order to recover ring-oscillator operation in the FS and SF corners, higher voltage control signals (~10 times the TEG output voltage) are needed. Fig. 5 displays how these signals are generated. Three oscillators are used. These oscillators are designed to be functional in one corner; one for the typical (TT) corner, the two others for the FS and the SF corners. Each oscillator is followed by multiple charge-pump stages. The highest charge pump output determines the process corner. If, e.g., the chip is in the TT corner, the TT oscillator starts to oscillate and its charge-pump generates a higher voltage amplitude signal named TT. As can be seen in Fig. 5, the other two oscillators are turned off when the TT signal is high. If, e.g., the chip is in the FS corner, the FS oscillator starts to oscillate and a higher voltage signal named FS is generated, which disables the TT oscillator. In this corner, it would be very rare if the SF oscillator also starts to oscillate. The same scenario is valid for the SF corner. These FS and SF signals are used to activate the auxiliary pull up/down networks explained in the previous sub-section.

C. Charge pumps

In order to step up the TEG output voltage, multiple charge-pump stages have been used. The charge pump was over-designed to step a 50mV input voltage up to a 1V output. The optimized number of stages, as described in [26], for a minimum chip area can be obtained from (1):

$$N = 2\left(\frac{V_{OUT}}{V_{IN}} - 1\right), \qquad (1)$$

in which V_{OUT} is the output voltage, V_{IN} is the input voltage and N is the number of stages. For a 50mV input and a 1V output, $N=38$ is obtained. The capacitor value for each charge-pump stage can be obtained from (2) [26]:

$$C = N\frac{I_L T}{(N+1)V_{IN} - V_{OUT}}, \qquad (2)$$

in which C is the capacitance value, I_L is the load current and T is the switching period. Simulations show that the frequency of the proposed ring oscillator is about 1kHz. For 1nA load current, a capacitor value of $C=40pF$ is obtained.

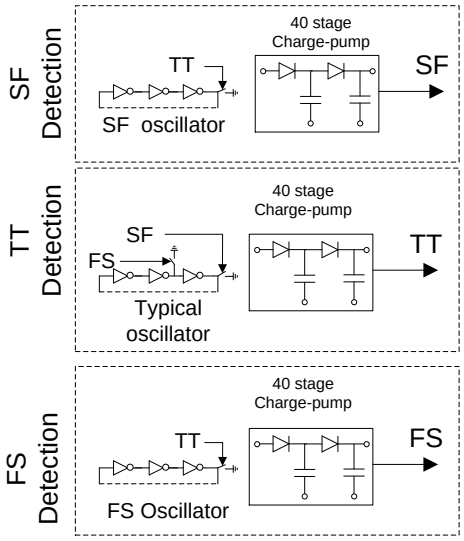


Fig. 5. Proposed architecture to generate corner detection signals.

D. Level detector

As shown in Fig. 1, the main charge pump output is directly connected to the level detector. The main charge pump is designed to deliver 1nA output current. Since the level detector is the main load of charge pump, its power consumption should be as low as possible. As the oscillation frequency in this design is very low (1kHz), more power consumption would lead to a larger capacitor value as shown by (2). A larger capacitor value directly increases the chip area and cost, since most of its area is occupied by the charge pump capacitors. Minimizing the power consumption is the most important aspect in the design process of the level detector. The level detector also enables another ring oscillator for generating pulses to drive the boost converter.

Fig. 6 depicts the input-output characteristics of an ideal level detector [27]. An ideal level detector draws zero current. The output voltage for input voltages below V_{DETECT} is zero. At $V_{IN}=V_{DETECT}$, the level detector output signal changes from zero to V_{IN}. This characteristic helps the output of the charge pump to be charged to V_{DETECT}. V_{DETECT} is designed to be 600mV, which is enough to turn on the main boost converter NMOS switch. Conventional voltage detectors consist of a bandgap reference and a comparator. Due to the use of the bandgap reference and static comparators these methods are both power hungry and need higher supply voltages. See, e.g., [28]. The voltage monitoring system proposed in [27] consumes only 1.6nW power, but its output is not rail to rail, which makes the succeeding buffer more power consuming. Therefore, a new small size cross-coupled voltage detector with sub-nW power consumption is proposed, the circuit level implementation of which is explained in Section III-D.

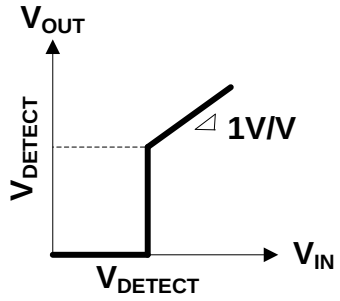


Fig. 6. Ideal input output characteristic of a level detector [27].

E. Pulse generator and boost converter

Fig. 7 illustrates the pulse generator followed by an asynchronous boost converter. The main charge pump supplies the voltage detector and inverters. The voltage detector is placed in a ring oscillator to guarantee full-swing pulses. The ring oscillator mainly consists of current starved inverters. To have a sharp input at the voltage detector input, its driving inverter is not starved. The ring oscillator is followed by multiple inverter stages with increased size for every subsequent stage, the last one of which can drive the main switch in a boost converter. The voltage generated by the boost converter is used to power the ring oscillator, once it becomes larger than the main voltage doubler output voltage. Using this technique the boost converter output can power the pulse generator.

III. Circuit Level Implementation

The transistor level implementation of the harvester is detailed in this section.

A. Proposed process tolerant inverter cell

Fig. 8 shows the proposed inverter cell. The cell consists of a conventional inverter cell (M_1, M_2) with two parallel branches. Each branch consists of two minimum-size switches and an auxiliary driving network. Each branch has one switch in the input signal path ($M_{S3,4}$) and one in the output signal path ($M_{S1,2}$). In the typical corner, the SF and FS signals are low, so all the switches (M_{S1-4}) are off and the circuit works as a conventional inverter cell. In this condition, the gates of M_3 and M_4 are tied to ground via the bulk diodes of M_{S3} and M_{S4}, respectively. This makes the gate-source voltage of M_4 equal to the power supply, but its drain source current is zero since M_{S2} is off. M_3 is off as well. In the SF corner both M_{S1} and M_{S3} are turned on by the high SF voltage, generated by the corner detection circuit. With M_{S1} and M_{S3} turned on, M_3 is added in parallel to M_1. This makes the pull-down network stronger, which leads to a functional inverter cell in the SF corner. The same scenario happens with M_{S2} and M_{S4} turned on in the FS corner leading to M_4 and M_2 being in parallel in the FS corner.

At small supply voltages, the I_{ON}/I_{OFF} ratio is below 10. In the proposed inverter cell, in order to reduce the loading effect, switches (M_{S1-4}) are minimum size. In order to reduce the on-resistance of these minimum size switches (M_{S1-4}), they are driven with high-voltage signals (i.e., the SF and SF

signals) generated by the corner detection circuit. Simulations show that the transistor drain current deviation from the typical corner in the fast and slow corners is about 2X. The auxiliary transistors (M_{S3} and M_{S4}) are sized 2X wider than the main transistors (M_1 and M_2) to overcome this deviation.

B. Corner detection circuit

The corner detection circuit is implemented by three different ring oscillators followed by three voltage doublers. Each ring oscillator is optimized to be functional in a specific corner at very low supply voltages. This has been realized by choosing an appropriate NMOS/PMOS transistor sizing ratio.

The oscillators in the corner detection circuit and the oscillator used to drive the main charge pump are 11-stage ring oscillators. There are three of these oscillators in the corner detection circuit, which are designed to oscillate with input voltages as low as 60mV and maximum output voltage swing. In order to make each oscillator functional in only one corner, the PMOS to NMOS sizing ratio has been modified. For example, for the oscillator in the SF corner, the NMOS to PMOS sizing is chosen bigger than that for the oscillators in the TT and FS corners. The simulated output amplitudes and frequencies of each ring oscillator are summarized in Table I. In this table, the TT oscillator is simulated in the TT corner, the FS oscillator in the FS corner and the SF oscillator in the SF corner.

Each oscillator also drives a charge pump that generates signals named TT, FS and SF, corresponding to each individual oscillator. Since at these small supply voltages, no ordinary digital gates can be used, a minimum-size NMOS switch has been used to ground the oscillator output, as shown in Fig. 5. This minimum-size switch is only activated when the corresponding FS, SF or TT signals are high enough, which means that at least one oscillator has started oscillating. Using this technique only one oscillator remains oscillating.

TABLE I
SIMULATED OSCILLATION AMPLITUDE AND FREQUENCY OF OSCILLATOR IN THE CORNER DETECTION CIRCUIT

	TT oscillator	**FS oscillator**	**SF oscillator**
Amplitude	40mV	39mV	36mV
Frequency	3.4kHz	2.9kHz	3.7kHz

As the corner detection circuit is only loaded by MOS gates, its charge pumps can be designed with small capacitors. In this case, to save area, the voltage doublers in the corner detection circuits are sized 10 times smaller than the main voltage doublers. Each voltage doubler consists of a 40-stage charge pump with 4pF capacitors.

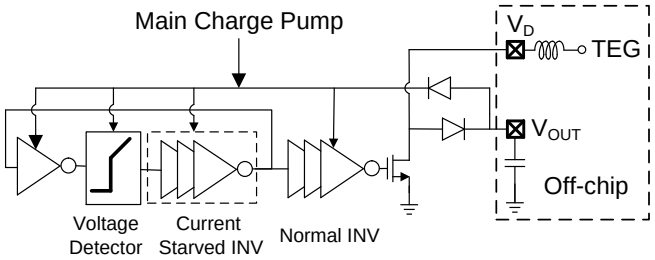


Fig. 7. Pulse generator and boost converter.

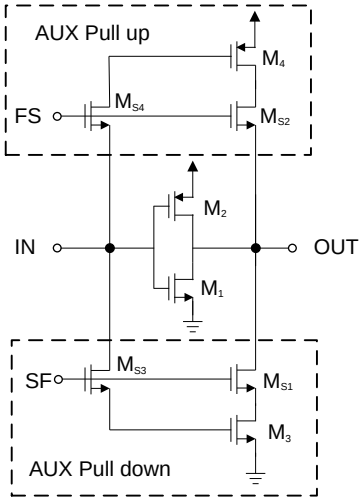


Fig. 8. Proposed process-tolerant inverter cell.

C. Charge pumps

Fig. 9 shows the circuit implementation of the charge pump used in the main charge pump and also in the corner detection circuit. Diode connected PMOS transistors are used to minimize the body effect. As explained in the previous section, the charge pump requires 40pF capacitors and at least

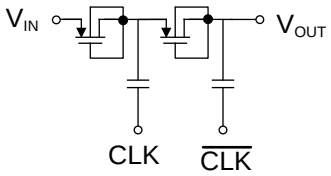
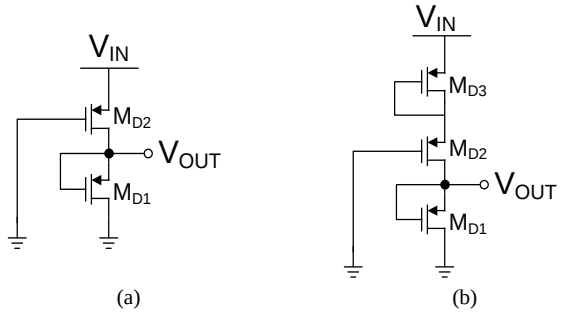


Fig. 9. Charge-pump circuit implementation.

38 stages. In order to have more headroom, a 40-stage voltage multiplier is implemented. The capacitors are implemented with MIM capacitors. In order to minimize the load on the CLK and CLK_BAR signals, each doubler stage is driven from its own driver circuit. Like in the corner detection circuit implementation, the transistors have been placed below the MIM capacitors.

D. Voltage detector

Fig. 10 depicts the voltage detector proposed in [27]. This configuration consists of two cascoded transistors M_{D1} and M_{D2}, in which the lower transistor (M_{D2}) is in its cut-off region ($V_{GS}=0$). This makes the voltage detector ultra low-power. In this design, the detection happens as soon as the pull-up current and pull-down current become equal. As explained in [27], the detection voltage can be obtained from (3), in which m is the subthreshold slope coefficient, kT/q is the thermal voltage and W and L are the transistors' width and length, respectively.



(a) (b)

Fig. 10. Voltage detector (a) main part, and (b) with a diode-connected transistor to adjust the detection voltage [27].

$$V_{DETECT} = \frac{mkT}{q}\ln\left(\frac{W_1}{W_2}\times\frac{L_2}{L_1}\right) \quad (3)$$

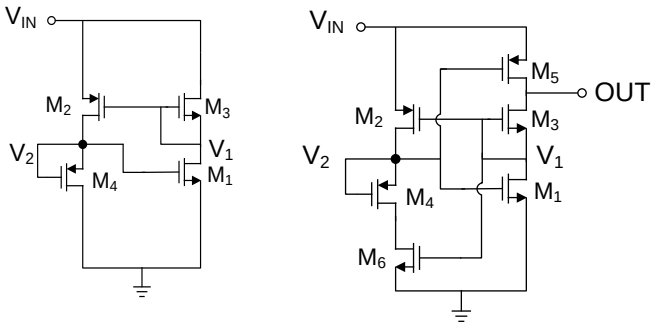
According to (3), in order to have $V_{DETECT}=600\ mV$, M_{D1} should be 2.6×10^{10} times bigger than M_{D2}, which is not practical. In order to reduce this ratio, a diode connected transistor has been added to the voltage detector as shown in Fig. 9 (b). Adding this transistor changes the detection voltage. In this configuration for having $V_{DETECT}=600\ mV$, M_{D1} should be 3100 times bigger than M_{D2}. Adding M_{D3} reduces the output swing, therefore some buffer stages have been added to make the output node full swing.

The design of [27] has some drawbacks. Although the ratio of 3100 is feasible, it is still very large. This increases the leakage current of M_{D1}, which leads to more power consumption. Since the output node swing is $V_{IN}/2$, the cascaded buffers that succeed the voltage detector consume more power compared to a buffer with a full-swing input. In order to solve this, a cross-coupled voltage detector is proposed. Fig. 11 shows the proposed cross-coupled voltage detector. The main part of the voltage detector is shown in Fig. 11 (a). It consists of two voltage-detector branches ($M_{1,3}$, $M_{2,4}$) in a cross-coupled configuration. Transistors $M_{2,4}$ form a voltage detector, similar to the one shown in Fig. 10 (a), while $M_{1,3}$ form a similar voltage detector, but in a complementary fashion. In Fig. 11 (b), M_5 and M_6 are cross-coupled transistors to help the switching mechanism. Adding the NMOS voltage detector ($M_{1,3}$) branch generates a positive feedback. Since most of power consumption happens during switching, using positive feedback makes the switching very fast, thereby reducing power consumption.

In the proposed structure, transistors M_3 and M_4 are transistors with $V_{GS}=0$, and M_2 and M_1 are detection transistors. Detection happens when the detection transistor currents equal the cut-off transistor currents, which means $I_{D2}=I_{D4}$ and $I_{D1}=I_{D3}$. The transistor drain current in the subthreshold region with $V_{DS}>100mV$ can be approximated by (4), in which K is a technology dependent constant. V_{GS} and V_{TH} are the gate-source and threshold voltages, respectively.

$$I_D = K\frac{W}{L}e^{q\frac{V_{GS}-V_{TH}}{mkT}} \quad (4)$$

When $V_{IN}<V_{DETECT}$, V_2 is almost tied to ground and $V_1\sim V_{IN}$. In this condition, transistors M_5 and M_6 can be considered to be ON. This simplifies the circuit to Fig. 10 (a). Since $V_1\sim V_{IN}$, both M_2 and M_4 have $V_{GS}\sim0$. In this case the voltage at node V_2 can be obtained from the voltage divider circuit consisting of M_2 and M_4. Using this method the voltage at node $V_2=V_{GS1}$ can be approximated by (5).



(a) (b)

Fig. 11. Proposed cross-coupled voltage detector, (a) main part and (b) implemented one.

$$V_2 = V_{GS1} = \frac{L_4/W_4}{L_4/W_4 + L_2/W_2}V_{IN} = \alpha V_{IN} \quad (5)$$

Substituting (5) in (4), The drain current of M_1, (I_{D1}), can be obtained from (6).

$$I_{D1} = K\frac{W_1}{L_1}e^{q\frac{\alpha V_{IN}-V_{TH}}{mkT}} \quad (6)$$

The drain current of M_3 (I_{D3}) can also be expressed as (7)

$$I_{D3} = K\frac{W_3}{L_3}e^{q\frac{-V_{TH}}{mkT}} \quad (7)$$

Detection happens when $I_{D1} = I_{D3}$, (8).

$$K\frac{W_3}{L_3}e^{q\frac{-V_{TH}}{mkT}} = K\frac{W_1}{L_1}e^{q\frac{\alpha V_{IN}-V_{TH}}{mkT}} \quad (8)$$

Solving (8), V_{DETECT} can be obtained from (9). Compared to (3) the sizing is reduced with a factor of $e^{1/\alpha}$.

For symmetry, the PMOS detection branch ($M_{2,4}$), should also have a detection voltage equal to (9). This leads to (10) for sizing the NMOS and PMOS branches.

$$V_{DETECT} = \frac{mkT}{\alpha q}\ln\left(\frac{W_1}{W_3}\times\frac{L_3}{L_1}\right) = \frac{mkT}{\alpha q}\ln(\beta)$$
$$\alpha = \frac{L_4/W_4}{L_4/W_4 + L_2/W_2},\ \beta = \frac{W_1}{W_3}\times\frac{L_3}{L_1} \quad (9)$$

$$\beta = \frac{\alpha}{1-\alpha} \quad (10)$$

In order to properly size the voltage detection circuit, some iterations are necessary to find the optimal transistor sizes. The simulated input-output characteristic of the proposed detection circuit is shown in Fig. 12 along with its current consumption. Compared to the voltage detector proposed in

[27], the static power consumption is further decreased. The proposed method delivers a full-swing and sharp voltage detector output, which greatly reduces the power consumption of the succeeding inverter stages.

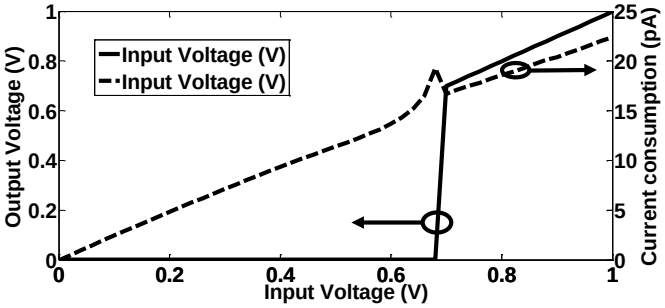


Fig. 12. Simulated input-output characteristic and current consumption of the proposed cross-coupled voltage level-crossing detector.

E. Pulse generator and boost converter

The output of the level detector enables the pulse generator circuit. The pulse generator and boost converter form a self-supplied system, which means once the boost converter has become active, the pulse generator is supplied from the boost converter. To minimize the power consumption and lower the switching frequency, a current starved ring oscillator has been used. To maximize the boost converter's efficiency in low-power designs, a discontinuous conduction mode (DCM) boost converter topology has been selected, as shown in Fig. 7. Simulation results show that the switching frequency of the pulse generator in steady state is about 100kHz, leading to a 5µS ON time for the inductor. Since the driving capability of the pulse generator is limited, some iterations were made to find the optimum NMOS switch dimensions for minimum conduction loss. After these iterations, an NMOS switch with *W/L=2mm/180nm* was selected. For a 1mA peak inductor current and V_{GS}*=0.6V*, there is less than 5mV voltage drop over the switch. For a switching frequency of 100kHz, a peak current of 1mA and a minimum input voltage of 50mV, a 250µH inductor value is obtained and a standard 220µH inductor was selected. In order to limit the output ripple to 10mV for a 10µA load, the output capacitor was set to 10nF. The rectifying diode in the boost converter was implemented using on-chip Schottky diodes available in the technology.

IV. Measurement Results

The chip has been implemented in 0.18 µm AMS technology. Fig. 13 shows the chip micrograph. The die occupies 2.2×1.5 mm^2. According to Fig. 13, the main part of the chip is occupied by the main charge pump. The drivers were placed below the capacitors to save area.

Six samples were tested. Fig. 14 (a) displays the minimum input voltage histogram of the samples. As shown in Fig. 14 (a), the minimum input voltage can be reduced down to 50mV, which is the lowest input voltage with standard CMOS technology reported to date. In order to validate the effectiveness of the proposed method, the corner detection circuit was disabled. This makes the start-up system a basic ring oscillator followed by voltage doublers. In this case, the minimum input voltage increases by 90% to 95mV, as shown in Fig. 14 (b).

In order to validate the output power delivery, the samples were tested with different input voltages and different loads. Fig. 15 shows the output ripple waveform and inductor terminal (V_D) voltages for a 80mV input and a 50kΩ load. Fig. 16 shows the measured output voltages for different input voltages and different loads. It can be noticed that the output voltage is somehow regulated for each input voltage and does not drop very much with increasing the load. The reason is that the pulse generation circuit functions as a voltage controlled oscillator (VCO); as the output voltage increases, the frequency of the pulse generator increases resulting in a smaller charging time for the inductor. This smaller charging time decreases the output voltage resulting in a semi-regulated output voltage. As this chip was implemented to prove the idea of using process-tolerant gates, precise regulation of the output voltage was beyond the scope of this work.

The measurement results also show that the chip can deliver 4.5µW output power at the minimum input voltage, which is sufficient to drive any boost converter that is designed for maximum efficiency [5].

Fig. 17 shows the efficiency versus different loads for different input voltages. The converter achieves a maximum efficiency of 47% at a 100µW load with a 300mV input voltage. The efficiency can be further improved, using a PMOS transistor instead of a diode in the boost converter [5].

In order to have a more realistic model for the TEG, the effect of the equivalent series resistance on the converter performance has also been investigated. Fig. 18 shows measured output power for a 50mV input voltage and a 470kΩ load for various source resistances (5Ω to 63Ω). The internal resistance of the TEGs reported in [29] varies from 5Ω to about 27Ω, a range that is covered in Fig. 18. As shown in Fig. 18, the delivered output power varies from 2.6µW to 1.8µW.

Table II compares this work with state of the art thermoelectric energy harvesting start-up systems. The work reported in [17] shows a very interesting minimum input voltage of -8mV/15mV. This very small input voltage is achieved using a piezoelectric transformer in the oscillation loop. However the piezoelectric transformer used is very bulky compared to this work that uses only two off-chip elements. The proposed method shows the lowest start-up voltage among standard CMOS chips [23][25]. Unlike [23], the proposed circuit does not need any post-process trimming. The lower startup voltage obtained in this work, compared to [25], is due to the absence of stacked transistors at small supply voltages. The startup voltage is also comparable to those with native NMOS transistors without transformers [21].

V. Conclusions

This paper presents an ultra low-voltage startup system for thermoelectric energy harvesting. The system has been implemented in 0.18 µm CMOS technology and occupies 3.3mm^2. A new inverter cell has been proposed, which is functional at ultra-low voltages. The overall system can start with input voltages as low as 60mV and can deliver a 4.5µW output power at this input voltage.

TABLE II
RECENT THERMOELECTRIC ENERGY HARVESTING CMOS ICS COMPARISON TABLE

Ref.	Min. Input Voltage	Max Efficiency	Max Output Power @ Min Input Voltage	Output Voltage	MPPT	Technology	Start-up technique
[19]	35 mV	58% *	10 µW	1.8 V	+	350nm	MEMS switch
[12]	20 mV	40% *	N.A	2.3 to 5V	N.A	N.A	Native NMOS + off-chip transformer
[11]	40 mV	61% *	N.A	2V	+	130nm	Native NMOS +off-chip transformer
[21]	50 mV	73% **	N.A	1.2V	N.A	65nm	Native NMOS +off-chip inductor
[22]	30 mV	N.A	N.A	N.A	N.A	130nm	Native NMOS + on-chip inductor
[23]	80 mV	72% **	N.A	1.3V^{+}	N.A	65nm	Post process trimming
[17]	-8mV/15mV	1.7%	N.A.	1 to 1.3V^{+}	N.A.	180nm	Off-chip piezoelectric transformer
[24]	60mV	59%	N.A.	1 to 3V	+	180nm^{X}	Body-biased inverter + off-chip inductor
[25]	70 mV	60% *	12 µW	1.25V	N.A	130 nm	Modified Schmitt-trigger gate + off-chip inductor
This Work	60mV	47% **	4.5 µw	1V^{+}	N.A	180nm	Standard CMOS technology Modified inverter cell + off-chip inductor

*End to End efficiency **Just converter efficiency $^{+}$Unregulated output voltage ^{X} Simulation Results

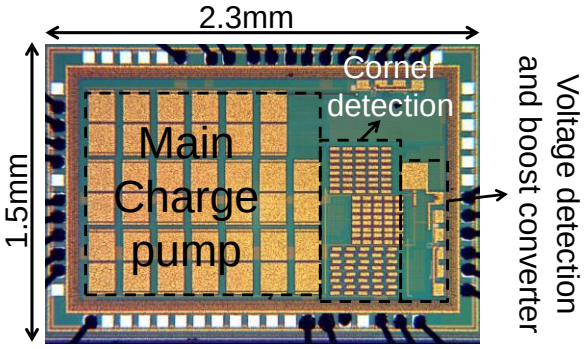


Fig. 13. Chip micrograph.

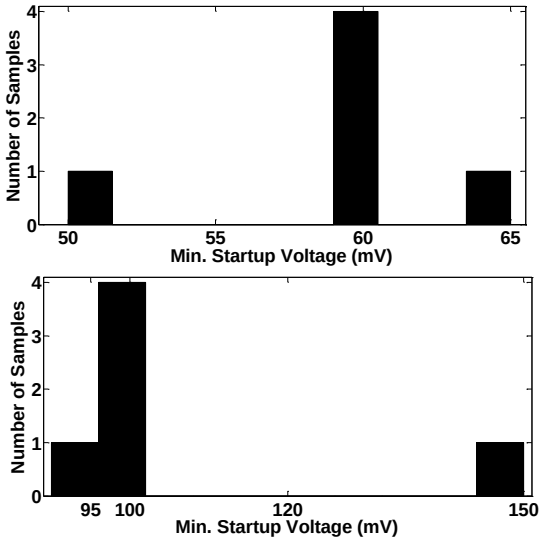


Fig. 14. Minimum input voltage histogram, (a) proposed method activated, (b) proposed method deactivated.

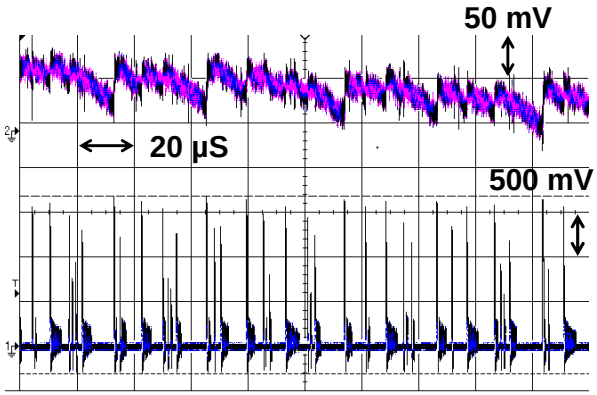


Fig. 15. Measured output voltage ripple (top) and measured voltage at inductor terminal V_D (bottom).

(a)

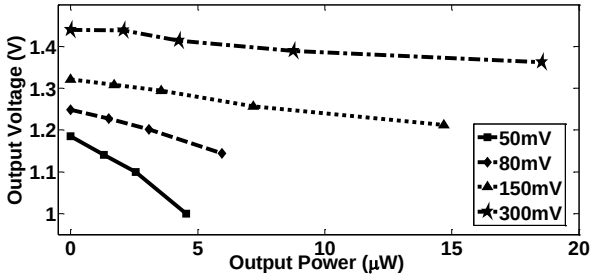


Fig. 16. Measured output voltage for different input voltages and different loads.

(b)

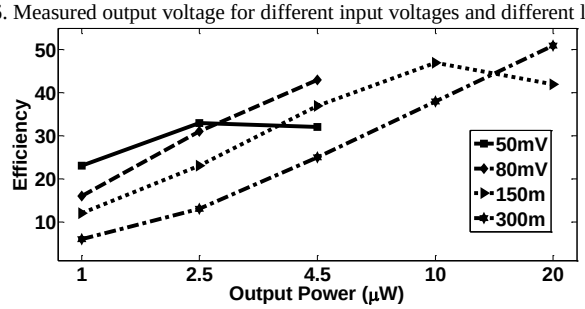


Fig. 17. Measured efficiency for different input voltages and different loads.

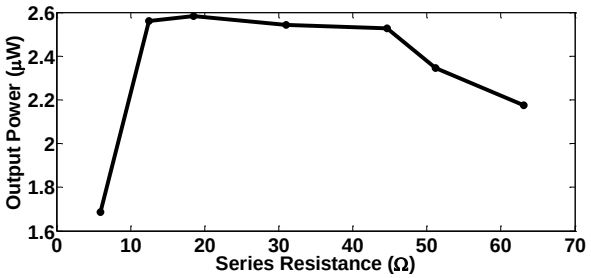


Fig. 18. Measured output power for 50mV input voltage and 470kΩ load for different source resistances.

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