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An RF Energy Harvester with MPPT Operating Across a Wide Range of Available Input Power

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***Abstract*—In this paper we present the design and simulation results of an RF energy harvesting circuit that operates across a wide range of available input power, from $-27\,\mathrm{dBm}$ to $6\,\mathrm{dBm}$. The system comprises an adaptive impedance matching network, a single-stage cross-connected differential rectifier, a start-up charge pump, an adaptive buck-boost converter and a Maximum Power Point Tracking (MPPT) circuit. The MPPT circuit controls the switching frequency of the buck-boost converter and configures the impedance matching network, optimizing the interfaces between the rectifier and antenna and between the rectifier and the storage capacitor, thereby guaranteeing that maximum power is being harvested. The system is designed in a standard $0.18\,\mu\mathrm{m}$ CMOS technology. The peak efficiency is 49.1% at an available input power of $-18\,\mathrm{dBm}$ and signal frequency of $403.5\,\mathrm{MHz}$.**

I. INTRODUCTION

Energy harvesting (EH) is an enabling technology for powering devices that are difficult or inconvenient to access physically, such as IoT, biomedical or several industrial applications. Among the EH modalities, radio-frequency energy harvesting (RFEH) is promising due to the ubiquity of RF signals in urban environments and due to its ability to reach environments in which other sources of energy (sunlight, vibration, temperature gradients, etc.) are not present. The available power presented on the antenna terminals of the RFEH can vary due to many factors, such as antenna alignment, distance to the source and network traffic. However, RFEHs are conventionally designed to present high sensitivity and do not accommodate for such power variations. Therefore, it is possible to observe a reduction in the power conversion efficiency (PCE) once the available power increases.

In order to tackle this problem, some systems in the literature present a certain degree of reconfigurability. For example, both in [1] and [2], a reconfigurable rectifier is used. However, in both cases, the extra stages are always connected to the input and the extra capacitances reduce the input voltage amplitude, reducing the PCE [3], which is a problem especially when the available power is low. In [4], three power paths are connected in parallel: a reference path, a low-power path and a high-power path. The voltage at the output of the reference path is sensed to make the decision about using the high-power path or the low-power one. Still, the switches in the signal path introduce losses and when the low-power path is activated the high-power one is also connected to the antenna terminals, which increases the parasitic capacitance.

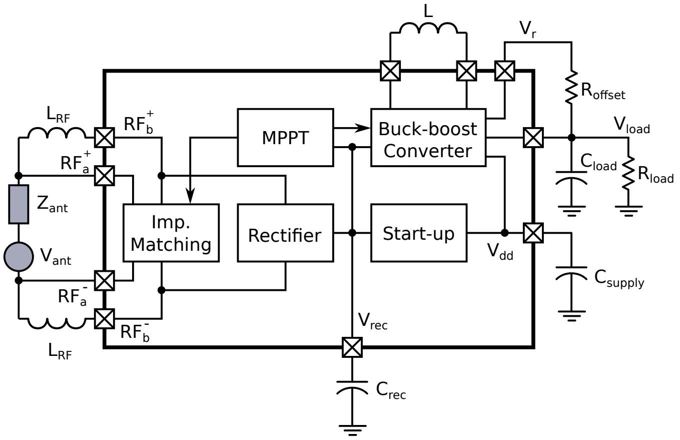
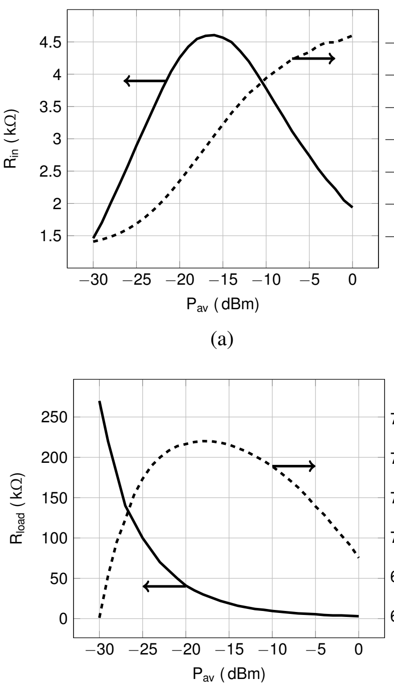


Fig. 1. System block diagram

In this work, we employ a single-stage cross-connected differential rectifier to perform the RF-DC conversion and we design the impedance matching circuit and a DC-DC converter to be configurable in order to adapt for the input power variation. The system architecture and specific circuit schematics are presented in the next section. In Section III, the post-layout simulation results are presented. In Section IV, the concluding remarks are discussed.

II. SYSTEM DESCRIPTION

The system block diagram is presented in Fig. 1. The goal of the system is to convert the RF power received by the antenna into DC power delivered to R_{load}. The impedance matching network performs a conjugated match of the antenna impedance to the rectifier input impedance, in order to maximize the power transfer from the antenna to the rectifier. To convert the RF signal into DC, a cross-connected differential rectifier is used [5]. A buck-boost DC-DC converter up-converts the rectifier output voltage to supply R_{load}. Because the rectifier input impedance and optimum output load change with the available power P_{av} presented to the antenna, we employ a Maximum Power Point Tracking (MPPT) circuit to configure the impedance matching and the buck-boost converter. A charge pump that can operate with a low supply voltage starts the system up by initially charging C_{supply}. The buck-boost converter control circuitry draws energy from C_{supply} to operate. One of the outputs of the converter is



(a)

(b)

Fig. 2. Rectifier response to input power variation: (a) Input impedance; (b) efficiency and optimum load.

connected to C_{supply} in order to charge it whenever V_{dd} is below a critical level (after the start-up phase is completed).

A. Impedance Matching Network and Rectifier

The rectifier topology used in this work is a single-stage cross-connected differential rectifier [5]. The system is designed for an input frequency of $403.5\,\text{MHz}$. The rectifier output voltage is boosted by the DC-DC converter. In Fig. 2, post-layout simulation results are presented (not considering the pads). For this simulation, P_{av} is swept and, for each point, the source impedance Z_s is matched to the rectifier impedance ($Z_s = R_{in} - jX_{in}$) while R_{load} is set to the optimum value. As expected, the rectifier input impedance and the optimum R_{load} change for different values of P_{av} [6].

A loop antenna that has an impedance $Z_{ant} = 40 + j380\ \Omega$ is used. Ideally, the impedance of the rectifier should be always matched to the antenna, but since the rectifier impedance changes with the input power, this cannot be achieved with a fixed impedance matching network. With the chosen antenna impedance, we can employ the capacitor-bank technique on a π-network topology to design the adaptive matching network presented in Fig. 3. The matching is implemented for two cases: high and low power. When V_{hp} is low, switches M_1 and M_2 are off and the network is configured for harvesting at low power levels. When V_{hp} is high, the network is in high-power mode. The signal V_{hp} is provided by the MPPT block. The inductors L_{RF} are off-chip components.

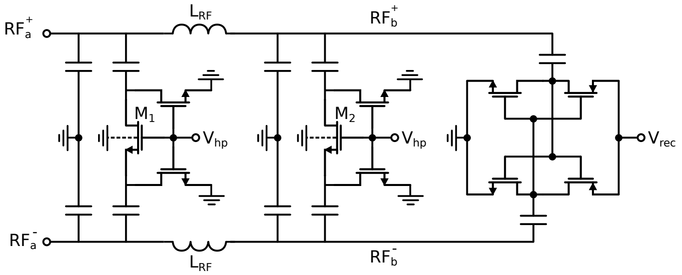


Fig. 3. Adaptive impedance matching and rectifier circuit schematics.

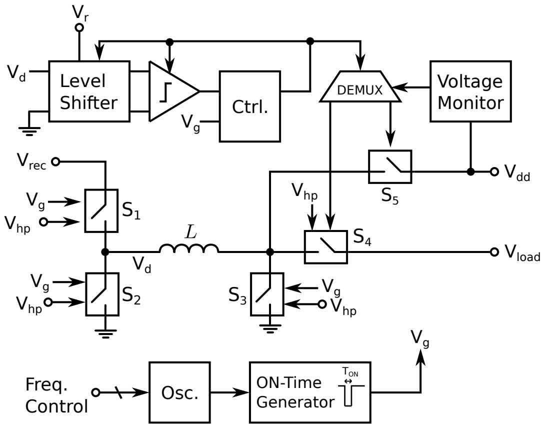


Fig. 4. Simplified diagram of the non-inverting buck-boost converter.

B. Buck-boost converter

In order to boost the rectifier output voltage and provide a suitable load to it, a non-inverting buck-boost converter is used. Such a converter guarantee that the load presented to the rectifier (the converter's equivalent input resistance) is independent of the output voltage when operating in open loop and discontinuous conduction mode (DCM) [7]. The simplified circuit diagram of the converter is presented in Fig. 4. Switches S_1-S_4 can be configured depending on the input power, in order to balance the conduction and switching losses. They are composed of two switches in parallel. When V_{hp} is low, signaling that the input power is low, one of the switches will not be turned on, decreasing the switching loss and increasing the conduction loss. When V_{hp} is high, both parallel switches are used.

Because the converter is operating in DCM, zero current detection is necessary. It is performed by detecting when V_d crosses the ground voltage. The voltage V_d and the ground voltage are shifted up to a level that is convenient for the comparator. To counteract the existing delays and to increase the conversion efficiency, an offset can be added to the level shifter through resistor R_{offset}, connected to V_r (see Fig. 1). The comparator is adaptively biased to decrease its power consumption while also decreasing its delay. See [7] for more information on these blocks.

The ON-time of switches S_1 and S_3 is fixed. Therefore, the average input resistance of the converter is controlled by the

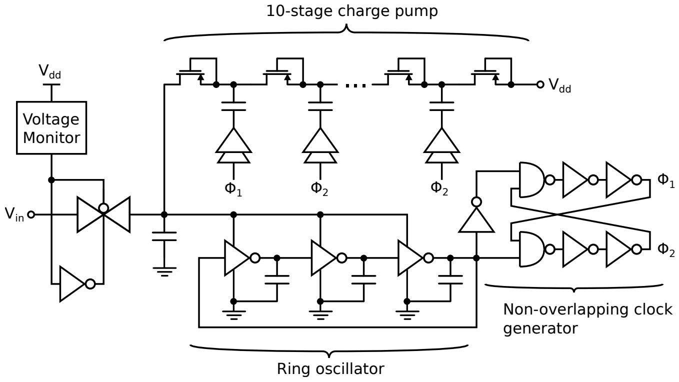


Fig. 5. Start-up circuit diagram.

switching period T_s and is given by:

$$R_{in,avg} = \frac{V_{in}}{I_{in,avg}} = \frac{2L}{D^2 T_s}, \tag{1}$$

in which D is the duty cycle of the switching control signal (DT is the ON-time of the converter) and L is the inductor value. The inductor used is a $220\,\mu\text{H}$ inductor with a maximum parasitic series DC resistance of $21.1\,\Omega$ (Coilcraft XPL2010-224ML). The switching frequency f_s is controlled by the MPPT, which outputs a 9-bit control signal along a thermometric scale. This control signal is used to control the bias current that drives the relaxation oscillator, whose frequency ranges from $10\,\text{kHz}$ to $1\,\text{MHz}$.

The current necessary for the operation of the converter is drawn from C_{supply}. This capacitor is recharged by the buck-boost converter itself, through switch S_5. A voltage monitor checks if V_{dd} is below $1.8\,\text{V}$ and, if this is the case, the next current pulse is directed to C_{supply}. The configurable switch technique is not applied to this switch, since it is operating sporadically (as most of the power is directed to the load). This avoids an unnecessary increment of parasitic capacitance, which degrades the efficiency.

C. Start-up Charge Pump

The buck-boost converter can operate from $V_{dd} > 1.1\,\text{V}$. If this condition is met, it can charge C_{supply} until its voltage reaches $1.8\,\text{V}$. To charge C_{supply} up to $1.1\,\text{V}$, the start-up circuit presented in Fig. 5 is used. It comprises a charge pump with 10 stages (which provides a 9x multiplication of the input voltage, ideally), a ring oscillator and a non-overlapping clock generator. It is supplied by the rectifier output V_{rec}, the same node it draws energy from to charge C_{supply}. After the start-up is complete, this circuit is turned off and it is activated only if V_{dd} becomes too low. Simulation results show that it can start-up the system with V_{rec} as low as $300\,\text{mV}$.

D. Maximum Power Point Tracking

The hill climbing algorithm is used since it is a low-power MPPT algorithm, due to its simplicity [8]. The block diagram of the MPPT is shown in Fig. 6. It consists of estimating the input power P_{in} of the buck-boost converter, holding this value, changing f_s and comparing the new P_{in} value to the previous one. In case the new P_{in} is higher, the frequency is further increased. Otherwise, the frequency is decreased. This is done by activating the up-down counter, which controls the oscillator frequency (by controlling its bias current I_N). When the counter value is higher than a certain threshold, V_{hp} is high, signaling the presence of a high input power to the other blocks.

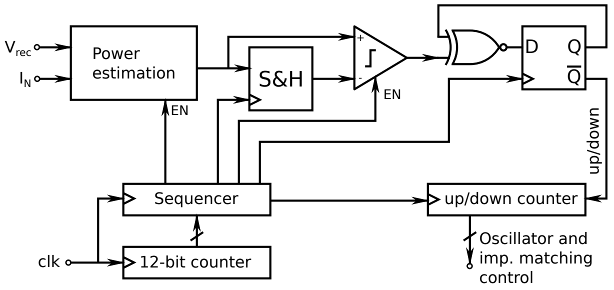


Fig. 6. MPPT block diagram.

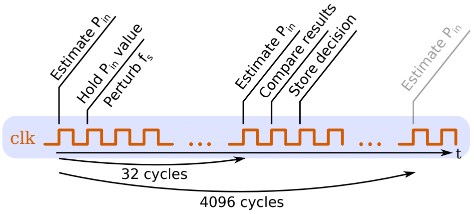


Fig. 7. Timing diagram of the MPPT circuit.

If the MPPT cycle is performed frequently, the average power consumption of the MPPT will be high. However, power is wasted to hold the input power value for a long period, since the holding circuit cannot be switched off between estimations. To overcome this problem, the sequence presented in Fig. 7 is proposed. The MPPT cycle begins with estimating P_{in}. The perturbation is performed (either increasing or decreasing the switching frequency) and the current value of P_{in} is held for just enough time for V_{rec} to settle. Subsequently, the new estimation and the comparison are done. The result of this comparison is held on a flip-flop, which does not dissipate static power, except for leakage. This cycle is continuously repeated during the operation of the energy harvester. The power consumption of the MPPT is $17.4\,\text{nW}$ for $f_s = 20\,\text{kHz}$, for which P_{in} is nominally equal to $1\,\mu\text{W}$ (at $V_{rec} = 0.38\,\text{V}$).

III. SIMULATION RESULTS

The system described in this paper was designed in AMS $0.18\,\mu\text{m}$ CMOS technology. The chip layout is shown in Fig. 8. Its active area is less than $0.2\,\text{mm}^2$. The results presented here are post-layout simulation results.

To perform the system simulations, we apply a $403.5\,\text{MHz}$ differential signal at the harvester input and place a resistive load R_{load} in parallel with C_{load} at its output. The value of R_{load} is selected so that $V_{load} = 1.8\,\text{V}$ in steady state. Therefore, a different R_{load} is selected when applying a

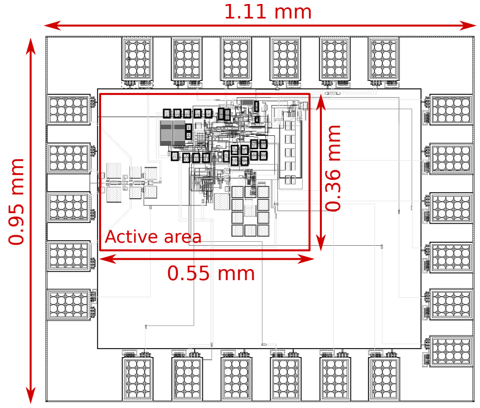


Fig. 8. Chip layout.

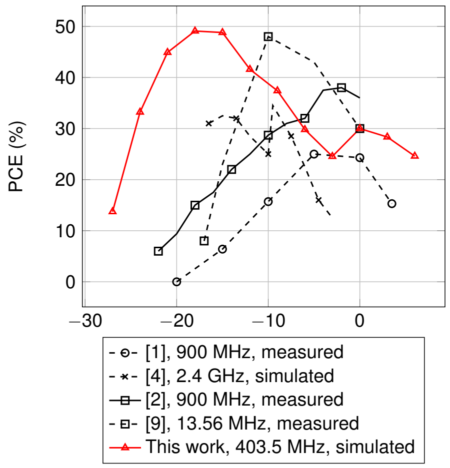
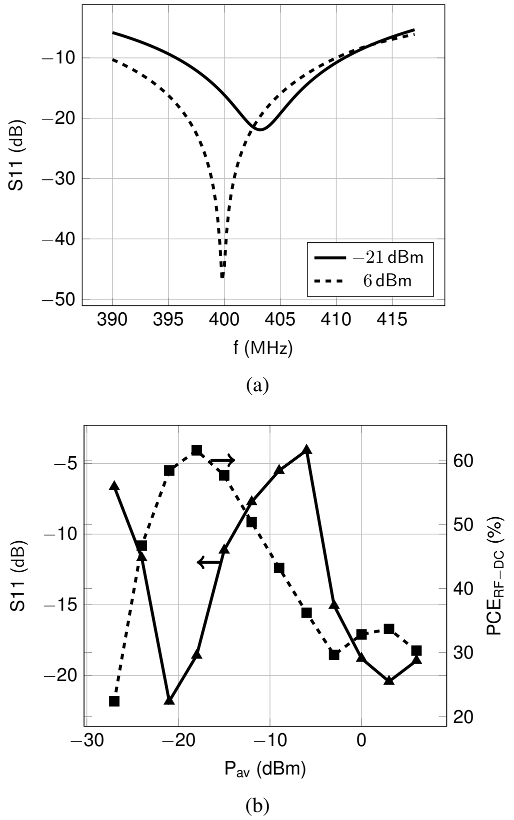


Fig. 9. Power conversion efficiency versus available input power for state-of-the-art RF energy harvesters.

different P_{av}. In Fig. 9, the PCE is presented for a varying P_{av}, also in comparison with other state-of-the-art works. The peak efficiency is 49.1% at $P_{av} = -18\,\mathrm{dBm}$.

In Fig. 10a, we present the S11 variations as a function of the RF input frequency. Since the rectifier input impedance changes with P_{av}, the bandwidth and reflection coefficient change as well. The variation of the S11 with P_{av}, as well as the RF-DC conversion efficiency, are presented in Fig. 10b. As can be seen, the S11 decreases with P_{av}, when P_{av} is between -18 and $-3\,\mathrm{dBm}$. However, when higher available power is detected (around $P_{av} = -3\,\mathrm{dBm}$), the MPPT activates the high-power mode of the adaptive impedance matching block, decreasing the S11. This results in an RF-DC conversion efficiency ($\mathrm{PCE}_{\mathrm{RF-DC}}$) increase for $P_{av} > -3\,\mathrm{dBm}$, extending the operating power range of the RFEH. The $\mathrm{PCE}_{\mathrm{RF-DC}}$ in the high-power configuration is not as high as in the low-power configuration because the rectifier is not optimized for high power levels and because there are more losses in the implemented high-power impedance matching network compared to the low-power one.



(a)

(b)

Fig. 10. Harvester S11 variation with (a) frequency and (b) available power.

IV. CONCLUSION

We have presented the circuit design and simulation results of an RFEH circuit that presents a competitive peak efficiency while operating across a wide range of available input power, of more than 3 decades. To achieve this, we employ adaptive techniques to the impedance matching and buck-boost converter blocks. Other techniques such as the adaptively-biased comparator, the configurable switches and the minimal input power estimator allow for a reduction of the power consumption when P_{av} is low and an increased power conversion efficiency for the specified P_{av} range. The antenna-rectifier and rectifier-load interfaces are controlled by the MPPT in order to accommodate for the changing input power. Simulation results show the system can operate for available input powers that range from $-27\,\mathrm{dBm}$ to $6\,\mathrm{dBm}$. Its peak efficiency is 49.1% at $P_{av} = -18\,\mathrm{dBm}$ and $f = 403.5\,\mathrm{MHz}$.

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