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A CMOS-Imager-Pixel-Based Temperature Sensor for Dark Current Compensation

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***Abstract*—This paper proposes employing each of the classical 4 transistor (4T) pinned photodiode (PPD) CMOS image sensor (CIS) pixels, for both imaging and temperature measurement, intended for compensating the CISs' dark current and dark signal non-uniformity (DSNU). The proposed temperature sensors rely on the thermal behavior of MOSFETs working in subthreshold region, when biased with ratiometric currents sequentially. Without incurring any additional hardware or penalty to the CIS, they are measured to have thermal curvature errors less than ±0.3 ^{0}C and 3 σ process inaccuracies within ±1.3 ^{0}C, from 108 sensors on 4 chips, over a temperature range from –20 ^{0}C to 80 ^{0}C. Each of them consumes 576 nJ/conversion at a conversion rate of 62 samples/s, when quantized by 1st-order 14 bit delta-sigma ADCs and fabricated using 0.18 µm CIS technology. Experimental results show that they facilitate digital compensation for average dark current and DSNU by 78 % and 20 %, respectively.**

***Index Terms*—Temperature sensors, delta-sigma (Δ-σ) modulator, CMOS image sensor (CIS), temperature compensation, dark current, DSNU**

I. Introduction

A typical CMOS Image Sensor (CIS) array usually contains several tens of megapixels, among which, as all semiconductor devices, are process variations. However, in semiconductors, almost all process dependent parameters are also thermal sensitive. For instance, in a stacked image sensor, the thermal profile of the CIS or heat dissipation due to the underlying logic can elevate and can be non-uniform. In other words, the temperature variations across the image sensor chip will affect the dark current and will increase DSNU, adding to the process variation components as the spatial dark Fixed Pattern Noise (FPN). Therefore, digital compensation of dark current and dark FPN [1] should be considered along with thermal compensation, especially for applications requiring a wide temperature range. The compensation can be performed using a reference dark frame taken with a physical shutter, which, however, is infeasible for low cost or very high speed video applications. In [2][3], an array of over 500 BJT based temperature sensors are imbedded inside a CIS array, each occupying an area of two image pixels, to sense the temperature locally. Nevertheless, the imbedding or the close location of a heterogeneous forward biased BJT device has tradeoffs.

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It has been reported in [3][4] to incur additional electro luminescence (EL) and dark current proportional to its forward-biased current and distance to the image sensor array. To overcome the aforementioned challenges, in this paper, the existing 4T PPD CIS pixels are employed as temperature sensors (during their idling time) by reconfiguring their current biasing, to sense the temperature locally, for thermal compensation of the dark current and DSNU. MOS based temperature sensors [5]–[9], including delay-line based ones, have been popular in literature, due to their smaller area and reasonable accuracy, compared to, e.g., their larger-area, better-accuracy resistor based [10] or BJT based, or hybrid counterparts [11]–[14]. Compared to previous publications, this paper's employment of CIS pixels themselves for temperature sensing when the pixels shift between the imaging and the thermal sensing has incurred no additional area penalty, within minimum additional conversion time and power consumption and has never been reported in literature. The proposed temperature sensor achieves thermal curvature accuracy less than ±0.3 ^{0}C, with 3 σ inaccuracies within ±1.3 ^{0}C, measured from 27 sensors on each of the 4 chips (108 sensors in total), over a temperature range from –20 ^{0}C to 80 ^{0}C, with a power consumption of 36 µW and conversion time of 16 ms, so an energy consumption of 576 nJ/conversion, when quantized by a 1st-order 14 bit delta-sigma ADC (DSADC) and fabricated using 0.18 µm CIS technology. Along with their thermal sensing functions, they facilitate digital compensation, for the averaged dark current and DSNU up to 78 % and 20 %, respectively, with its temperature information. This brief is organized as follows. Section II describes the operating principle of the proposed imager based temperature sensors. Section III shows the experimental results of the temperature sensor and its effects on facilitating digital compensations of the dark current and DSNU. Section IV concludes this brief.

II. Operating Principles

A. Imager based temperature sensor front-end

The operating principle of the imager based temperature sensor is as follows. Shown in Fig. 1 is a classical architecture of a 4T PPD image pixel. When the row select switch (*RS*) is on and the transfer switch (*TG*) is off and when the $V_{RST}>V_{PIX}+V_{TH}$ (V_{TH} being the threshold voltage of M_{RST}), the M_{SF} gate voltage equals that of V_{PIX_SUP} and the pixel output voltage $V_{PIX}=V_{PIX\_SUP}-V_{GS}$ (V_{GS} is the gate-source voltage of M_{SF}) if ignoring the voltage drop on M_{RS}. When biased in subthreshold region, an nMOS transistor has an I-V

characteristic of

$$I_1 = I_{DS} \cdot e^{(V_{GS}-V_{TH})/nV_T} \quad (1)$$

where I_1, I_{DS}, V_{TH}, V_T are the column biasing, saturation current (proportional to W/L), threshold voltage of the transistor M_{SF} and V_T=kT/q (k is Boltzmann's constant, q is electronic charge and T is temperature), respectively; while n is a process dependent factor. Since

$$ln\left(\frac{I_1}{I_{DS}}\right) = \frac{(V_{GS}-V_{TH})}{nV_T} \quad (2)$$

The differential pixel output voltage V_{PIX} between sequential ratiometric current biasing demonstrates

$$\Delta V_{GS} = V_{GS,2} - V_{GS,1} = n\frac{kT}{q}ln(N) \quad (3)$$

where N is the ratiometric current ratio, which is 4 in this design. Fig. 2 shows the timing diagram of the proposed temperature sensor. During $T_{ADC,1}$ and $T_{ADC,2}$, the SF is biased at current I_1 and I_2 (I_1/I_2 = 4), and its V_{GS} voltage corresponds to $V_{GS,1}$ and $V_{GS,2}$, which are read out through the pixel output V_{PIX} (Fig. 1) and quantized by the column-wise delta-sigma ADC, respectively. From $t_1(0)$ to $t_1(T_1)$ is one conversion period T_1 of the temperature sensor.

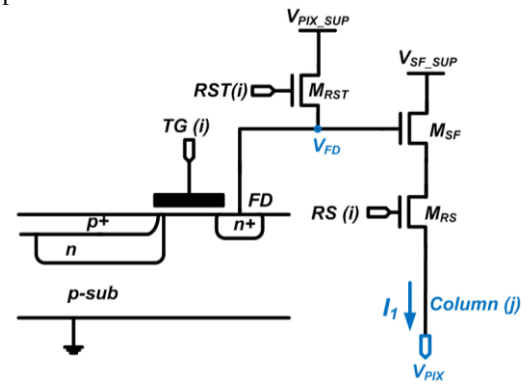

Fig. 1 Schematic of 4T PPD image pixel based temperature sensor.

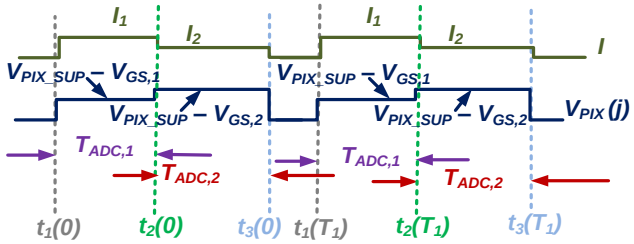

Fig. 2 Timing diagram of the proposed temperature sensor.

B. *Nonlinearity of the temperature sensor*

Due to the "n" factor in equation (3) and the small W/L size of each M_{SF} transistor, as well as the process variations of I_{DS}, each sensor suffers from some process dependency (among each other), which can be overcome by the following approach. Instead of biasing only one pixel, multiple pixels in the same column are biased. As a result, the actual device area of the temperature sensor is increased by a factor of the number of commonly-biased pixels, which can be seen as a larger parallel device with their gates and sources connected to V_{PIX_SUP} and V_{PIX} altogether. In addition, this method (of biasing multiple pixels) reduces the pixel output noise, including thermal and flicker noise, due to the increment in the biasing current and W/L ratio of M_{SF}, leading to a larger device area and hence increased transconductance g_m. This is crucial, as the noise level sets the finest resolution and hence affects the accuracy of the temperature sensor. Meantime, this approach of biasing multiple pixels releases the settling time requirements as the virtual output impedance $1/g_m$ of the pixel is decreased, by a squared factor of the number of pixels biased in the same column altogether. This improves the readout rate and optimizes the conversion energy, when the increased biasing current for M_{SF} is much lower compared to the energy saved in the delta-sigma ADC, when using this approach.

As a single device instead of a differential pair is used for thermal sensing, the effects from the geometrical mismatches of the individual sensing and the biasing devices are eliminated while those among the sensors still remain. Four main non-idealities exist in addition to the exponential I-V characteristic described in equation (1): (i) the deviation of M_{SF} from the exponential I-V relationship, (ii) the voltage drop across the row select switch RS, V_{RS}, (iii) the body effect of V_{TH}'s thermal effect and (iv) the mismatches among the biasing current circuits. For (ii), the switch RS works in linear region and its on-resistance is $1/\mu_n Cox(V_{GS,RS}-V_{TH})$ that varies with temperature and process. The effect of (iii) is minimized by the subtraction of the voltages when the sensor is biased with sequential ratiometric currents. Besides, the proposed temperature sensor outputs are usually very close to the pixel supply voltages, e.g., around 2 V, which makes V_{SB} large and hence $\partial V_{TH}/\partial V_{SB} = \gamma/2\sqrt{(2\Phi_F+V_{SB})}$ low (where V_{SB} is the source-body voltage, since its body is connected to its substrate rather than to its source, $\Phi_F = V_T \cdot \ln(N_{sub}/n_i)$, N_{sub} and n_i are the substrate doping and the intrinsic carrier concentrations, respectively, and γ is a process factor, of the M_{SF}. Transistor-level Monte Carlo simulations have been performed to verify that the thermal effects from V_{TH} and V_{RS} have introduced a CTAT and PTA offset to the sensor, both of which, however, can be corrected using a one-point calibration.

C. *Delta-sigma ADC*

Fig. 3 shows the schematic of the delta-sigma modulator employed for the ADC in this design, in reference to [15]. Through the negative feedback loop, the voltage level of the analog multiplexer (MUX) modulated by the digital output bit stream from the D-flip flop (DFF) shown in Fig. 3 equals that of the input Vi. The errors (nonlinearity) of the delta-sigma ADC for quantizing the temperature sensing front-ends discussed in Section II.A are shown in Fig. 4. They are less than 1 LSB (1 LSB = 18 µV, with 14 bit for a reference voltage of 300 mV), over the input range between 32 mV and 42 mV. The input range are relative voltages (e.g., 32 mV is 2.032 V relative to 2 V), the same as the sequential output range ΔV_{GS} in equation (3) of the temperature pixel between -20 and 80 ºC. Implemented using 0.18 µm CIS technology, the DSADC's opamp achieves a gain of 84 dB, with a unity gain bandwidth (UBW) of 23 MHz in TT simulation corner.

D. System diagram and operation

Fig. 5 shows a system block diagram of the proposed design. The temperature pixel is sequentially biased at I_1 (phase 1) and $4I_1$ (phase 2), respectively, followed by and digitized through the delta-sigma ADC shown in Fig. 3. The differential ADC outputs between two phases ($T_{ADC,1}$ and $T_{ADC,1}$ in Fig. 2) are digital representations of $\Delta V_{GS}=nkT\cdot ln(N)/q$. Matching of the ratiometric current of N is performed by DEM in the column current biasing circuit.

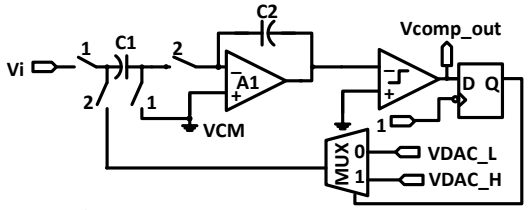

Fig. 3 Schematic of the delta-sigma ADC.

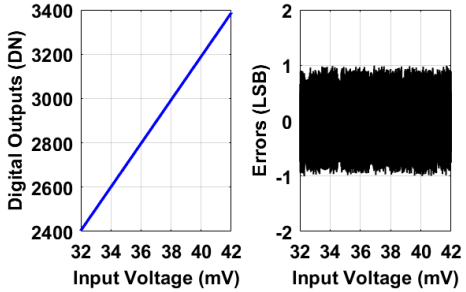

Fig. 4 Linearity and errors of the delta-sigma ADC in this design.

III. Measurement Results

A. Imager based temperature sensors

Fabricated using CIS 0.18 µm technology, the measurement results of the proposed temperature sensors from 108 temperature sensors on 4 chips are shown in Fig. 6, indicating a curvature error of ±0.3 ^{0}C with 3 σ process inaccuracies within -1.3/1.2 ^{0}C, between -20 ^{0}C and 80 ^{0}C, after a two-point calibration at 0 and 65 ^{0}C and a 2nd order master curve fitting. The design considerations for employing a single column, instead of each pixel, as a temperature sensor, is for lower process variability and noise, by having an actual larger sized SF, which equals each pixel SF's area times the number of pixels in each column. Both the two-point calibration and the 2nd order master curve fitting are post-processed using the chip digital outputs. The two-point calibration is applied to each temperature sensor, to remove the process spread among all the sensors. At the calibration temperatures 0 and 65 °C, the output codes of each sensor are trimmed (calibrated) to 3000 DN and 4000 DN, respectively. After that, a 2nd order master curve fitting is applied to all the sensors to relate their trimmed digital outputs obtained in the previous step to the temperature. This type of calibration, first removing the process spread, then trimmed by a master curve, is very similar to that performed in reference [10]. However, the first step of removing the process spread may vary from either calibrating at one temperature point or at two temperature points (this paper), or a 1st-order fit from multiple temperature points [10]. It is believed that the accuracy and the resolution of the temperature sensor after calibration depends on the accuracy of untrimmed outputs, rather than the assigned trimmed output codes at the calibration temperatures (e.g., 3000 DN and 4000 DN in this paper). The untrimmed output of each temperature sensor is around 2600 DN and 3100 DN at the calibration temperature 0 and 65 °C. This translates to 7.7 DN/°C, or, a resolution of 0.13 °C. The measured input referred noise (at the temperature pixel output) is around 10 µV, thanks to the oversampling and noise shaping in the DSADC, which also ensures minimum thermal curvature as a column readout circuit, as through feedback the output bit stream represents its analog input voltage, despite temperature and process variations. The reference range of the 14-bit ADC is around 300 mV, and its resolution is 18 µV. The thermal coefficient of the temperature sensor is 130 µV/°C. As a result, the resolution of temperature sensor can be calculated to be 0.13 °C (=18 µV /130 µV), which conforms with the measured one.

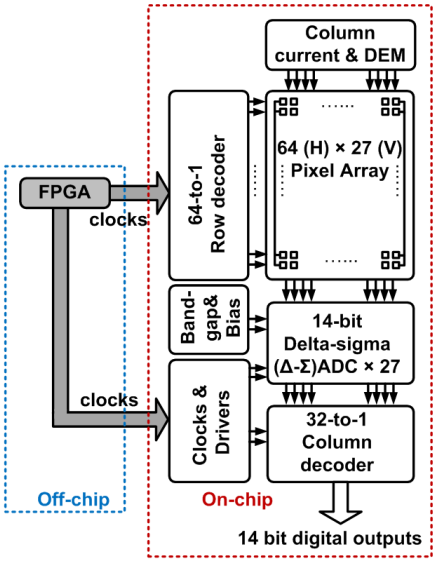

Fig. 5 System block diagram of the proposed CMOS image sensor with the capability of measuring the temperature in every image pixel.

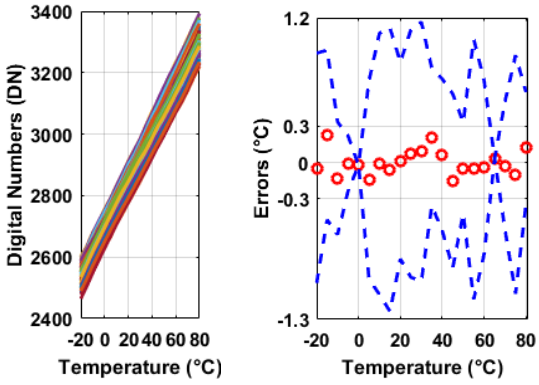

Fig. 6 Temperature sensor outputs from 27 columns in digital numbers (DN, left) from 4 chips (total 108 sensors); mean (red circles) and 3 σ errors (blue dotted lines) after a two-point calibration at 0 ^{0}C and 65 ^{0}C for each sensor, followed by a 2nd-order master curve fitting for all the sensors (right).

To save calibration costs and efforts, an automatic one-point calibration can be performed, at room temperature, as done in [5]. The calibration (correction) factor for each sensor can be a 12 bit number and stored in a FPGA, as described in [5], or in software or memory for image (post) processing.

B. Dark signal and DSNU compensation using proposed temperature sensors

Fig. 7 shows the measured dark current over the temperature range of 30 ^{0}C to 90 ^{0}C using the same image pixel sensors (shown in Fig. 1) and its exponential curve fit (y=a·exp(b·x)) while y and x refers to dark current and the temperature measured respectively. The deviations between the measured dark current and the curve fit are within ±12 %. Dark current doubles for approximately every 7 ^{0}C of temperature rise in this design.

Fig. 8 (a) shows the measured dark signal and dark non-uniformities at 60 ^{0}C. Fig. 8 (b) shows when a thermal gradient of 2 ^{0}C is present across the CIS array, the dark non-uniformities rise from 159 DN rms to 187 DN rms, despite the average temperature of the pixel array is maintained at 60 ^{0}C. The thermal gradient among the CIS is created by a hotspot at the upper right corner of the CIS, as shown in Fig. 9. To overcome the elevated dark current and DSNU in Fig. 8 (b), the thermal compensation procedures are as follows. First of all, capturing a reference image with the same exposure time (250 ms) at room temperature beforehand. Figuring out the constant a using y in the reference frame and temperature x (x is the temperature measured by the temperature sensors, e.g., 60 ºC). b is an empirical number (e.g., the constant b=0.11 for dark current that doubles for every 7 ºC). Secondly, predicting the dark current based on (y=a·exp(b·x)) and the constant a and b obtained in the first step, along with temperature information provided by the in-pixel temperature sensors. Finally, subtracting both the predicted dark signal (y in the previous step) and the reference frame (obtained in the first step) from the measured dark signal, at 60 ºC as shown in Fig. 8 (b). In particular, the rise in DSNU due to thermal gradients in Fig. 8 (b) has been overcome by using the proposed local temperature pixels' temperature information. After the aforementioned thermal compensation, Fig. 8 (d) indicates a 78 % reduction in average dark FPN and a 20 % reduction in DSNU, compared to the case without compensation as shown in Fig. 8 (b). A 15 % better effect on reducing DSNU is observed in Fig. 8 (d), compared to using an on-chip but relatively distant temperature sensor shown in Fig. 8 (c), which is incapable of detecting the local thermal gradients. In contrast to the image taken by the image sensor in [3], there is no dead pixel (hole) in the image of Fig. 9. When the imagers function as thermal sensing pixels, they cannot sense image signals at the same time. However, this trade-off is made negligible if considering that the thermal gradient of a 300 mW CIS array can be no more than 0.1 °C/mm [5]. The number (or, the spatial density) of temperature sensors needed for dark current compensation depends the aforementioned thermal gradients (e.g., 0.1 ºC/mm) and the compensation accuracy requirement. For instance, for a pixel pitch of 10 µm, to have a thermal sensing/compensation resolution of 0.1 °C, one needs to reconfigure one column of imager as a thermal sensor among every 100 columns (1 mm/10 µm) inside the CIS array. This means the temperature sensors have a spatial density of 1:100. The thermal sensing operation is performed at the end of each image caption. As a result, the trade-off of using image pixels for thermal sensing is less than 1 % additional conversion time of each frame. In this paper, each of all the 27 columns of the CIS is reconfigured and measured as a temperature sensor. In practice, not all the columns are required to be reconfigured as temperature sensors for compensating dark current.

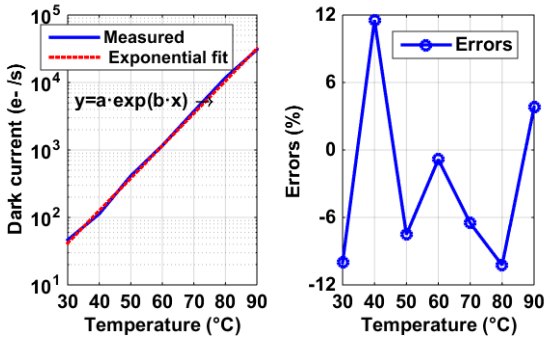

Fig. 7 Measured dark current versus temperature (left) and the errors between itself and its exponential curve fitting (right).

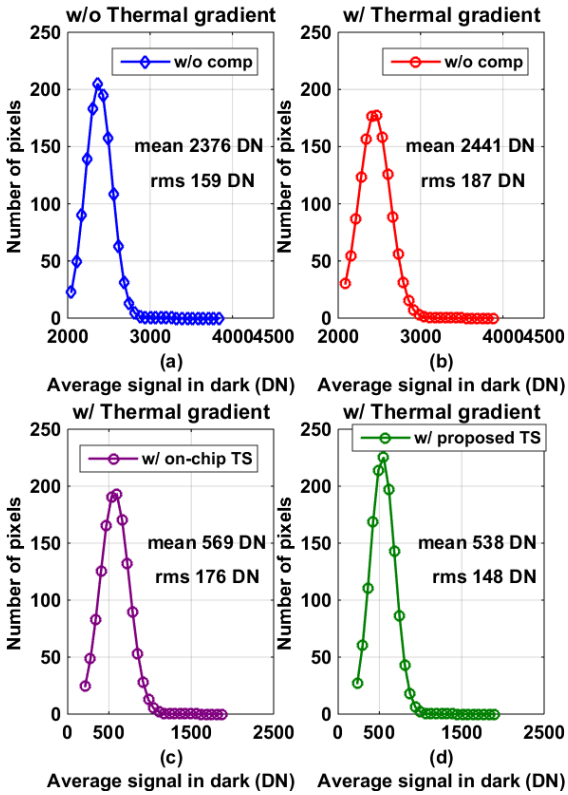

Fig. 8 Measured DSNU at 60 ^{0}C: Before compensation (w/o comp), (a) with and (b) without a thermal gradient of 2 ^{0}C (but the average temperature is maintained) across the pixel array diagonal. When a thermal gradient of 2 ^{0}C is present across the pixel array diagonal, using the proposed local temperature sensors (d) and using an on-chip but distant temperature sensor to facilitate digital compensation of DSNU (c).

Table I summarizes the performance of the proposed sensor, which can be used for both temperature and image sensing. Compared with previous publications, one of the advantages of the proposed temperature sensor is to require no additional area/hardware, while providing reasonable FOM[a] and relative accuracy (both of which are defined in [16]). Among the 36 µW of power consumption, 8 µW is used by the thermal sensing pixel (and its column biasing current) while the rest 28 µW is consumed by the delta-sigma ADC. It should be noted that

other temperature sensors shown in Table I are not imager based. Fig. 10 shows CIS chip micrograph and performance summary.

IV. Conclusion

To compensate for dark signal and DSNU in CIS, this paper proposes a CIS pixel based temperature sensor, which requires no additional hardware to the CIS. The proposed temperature sensor makes use of the temperature dependency of nMOS SF working in subthreshold region when biased with two ratiometric currents in sequence. It has been designed for the available pixel pitch and measured to have a curvature and 3 σ inaccuracies within ±0.3 ^{0}C and -1.3/1.2 ^{0}C, respectively, within a temperature range between -20 ^{0}C and 80 ^{0}C, with an energy of 576 nJ/conversion during a conversion time of 16 ms. With its thermal information, dark current and DSNU are digitally compensated by at least 78 % and 20 %, respectively.

TABLE I Comparison with the state-of-the-art works

	This work	[6]	[8]	[7]
Sensor Type	MOS	MOS	MOS	MOS
CMOS Technology	0.18 µm	65 nm	28 nm	0.18 µm
Area (µm^2)	No additional area	4000	1000	89000
Temperature Range	-20 ^{0}C to 80 ^{0}C	0 ^{0}C to 100 ^{0}C	-5 ^{0}C to 85 ^{0}C	-20 ^{0}C to 80 ^{0}C
3 σ accuracy	-1.3/1.2 ^{0}C	±2.3 ^{0}C	-3.3/1.9 ^{0}C	±1 ^{0}C
Calibration	Two-point	Two-point	One-point	Two-point
Power Consumption (µW)	36	154	56	0.8
Conversion Time (ms)	16	0.022	0.036	800
Resolution (^{0}C)	0.13	0.3	0.76	0.09
Resolution FOM (nJ·K^2)[a]	8	304.9	1.2	5.3
Rel.IA (%)	2.5	4.6	5.8	2

[a] Energy/Conversion×(Resolution)^2, in reference to [16]
[b] 3 σ accuracy /temperature range, in reference to [16]

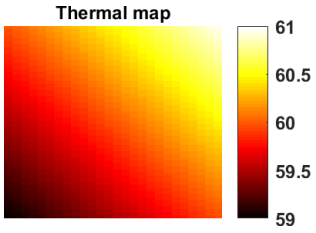

Fig. 9 Thermal map of the 64×27 CIS that has a 2 ºC thermal gradient.

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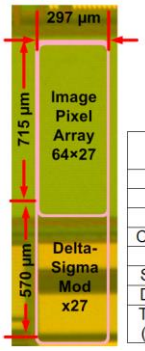

	This work (Image sensor)
Process	0.18 µm CIS 1P4M
Pixel pitch	11 µm×11 µm
Array size	64 x27
Conversion gain	78 µV/e$^-$
Fill factor	52 %
Supply Voltage	3.3 V
Dynamic range	80 dB
Temporal noise (input referred)	1.2 e$^-$

Fig. 10 Chip micrograph and summary of performances as an image sensor.

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