19.1 A Scalable Cryo-CMOS 2-to-20GHz Digitally Intensive Controller for 4×32 Frequency Multiplexed Spin Qubits/Transmons in 22nm FinFET Technology for Quantum Computers


1Delft University of Technology, Delft, The Netherlands, 2Intel, Hillsboro, OR 3Intel, Guadalajara, Mexico, 4TNO, Delft, The Netherlands 5EPLL, Neuchatel, Switzerland

*Equally-Credited Authors (ECAs), **Equally-Credited Authors (ECAs)

Quantum computers (QC), comprising qubits and a classical controller, can provide exponential speed-up in solving certain problems. Among solid-state qubits, transmons and spin-qubits are the most promising, operating at such a high clock frequency. The signals of two banks are combined in a wide frequency and output power range to support both spin qubits and transmons, and (c) can be directly integrated in an existing quantum control stack thanks to a digitally-intensive architecture with integrated instruction set.

A controller employing FDMA requires both a wide bandwidth to accommodate many qubits, each with a unique frequency [3], and pulse shaping to minimize spectral leakage to other qubits. To allow 99.99% fidelity for a n-rotation, exceeding the state-of-the-art, an SFDR >44dB is required to avoid disturbing unaddressed qubits [4]. This demands a linear transmitter architecture with good image and LO leakage rejection. For this fidelity, 44dB SNR is also required in a 25MHz noise bandwidth. To control both spin qubits and transmons, we designed a DDS and an analog RF front-end. For coherent control of 32 qubits, 32 numerically controlled oscillators (NCO) with 0.2kHz frequency resolution are used, allowing the use of a single external LO. The DDS is clocked at 1GHz, considering the number of qubits (N) and a required bandwidth of 30MHz/qubit [4]. A polar modulator is used to efficiently produce the desired pulse for each qubit at such a high clock frequency. The signals of two banks are combined in I/Q domain to achieve SSB up-conversion over a large data bandwidth. To control the required SFDR, digital I/Q and offset calibration networks are implemented for image and LO leakage rejection (κ, β, γ in Fig. 19.11). As signal replicas of the 10-bit segmented (5T-5B) current-steering DAC (see Fig. 19.12) can fall in-band after up-conversion to low carrier frequencies, a 2nd order gm-C reconstruction filter is used. High linearity is achieved by utilizing current-bleeding in the DAC and current-mode operation in the filter.

The required gain control is achieved with >200 steps, by a baseband VGA, implemented as tunable current mirror, in combination with a tunable-gain RF amplifier. The current mirror feeds the current into a quadrature double-balanced Gilbert-cell active mixer with current-bending driven by an on-chip LO driver and active balun. To cover a 2-to-20GHz output band, the RF path is split into 2 parts with the high band using the 3rd harmonic of the LO for up-conversion. Cascade switches are used at the mixer output to steer the current either into a resistor for the RF-Low band (2-to-15GHz) or a transformer tuned to 3f<sub>LO</sub> for the RF-High band (15-to-20GHz). The class-A amplifiers with wideband output baluns drive qubits over a 50Ω cable.

The chip was fabricated in 22nm FinFET CMOS with a total area of 16mm<sup>2</sup> comprising 4 controllers (M), flip-chip bonded to a BGA package (Fig. 19.1.7). A custom-made annealed and gold-plated copper enclosure was designed for efficient cooling and mounting of the PCB in a dilution refrigerator.

Figure 19.1.3 shows the measured peak output power at 3K over 2-to-20GHz with flatness limited by additional ground inductance introduced in the layout. The sampling replicas are highly attenuated by the filter, as measured at the BB-out test port. The peak output power SFDR is >45dB, equally limited by HD2 and image rejection ratio (IRR). The LO rejection ratio (LORR) of 36dB after calibration does not limit the SFDR, as this is not a favorable band for qubit control in a direct conversion topology and can be avoided by proper choice of f<sub>LO</sub>. Measured IM3 and SNR (25MHz bandwidth) are better than 50dB and 48dB, respectively.

The frequency multiplexing architecture potentially enables multi-qubit control over a single RF-cable, leading to a scalable system. The digitally-intensive architecture enables waveform shaping flexibility, minimum execution latency and straightforward integration in the existing quantum computing stack.

Acknowledgements:

References:
Figure 19.1.1: Qubit control signals, current state-of-the-art controller and presented cryogenic controller with frequency multiplexing.

Figure 19.1.3: Measured RF Bandwidth, BB-Out transfer function, RF-Low output with NCO frequency at 350MHz, two-tone RF-Low output with NCO frequencies at 241MHz and 260MHz, all at 3K.

Figure 19.1.5: Rabi oscillation and coherent qubit control experiments at 14GHz and 18GHz with the controller IC at 3K.

Figure 19.1.6: Comparison table.
Figure 19.1.7: Die micrograph (without metal layers) with cut-out of a single transmitter showing I/O bumps and RF transformers, chip package and PCB with enclosure.

Figure 19.1.S1: Top to bottom, left to right: dilution refrigerator, qubit sample SEM, PCB enclosure (open & closed), chip and qubit mounting in the fridge and measurement setup block diagram.

Figure 19.1.S2: Measurement of on-chip and refrigerator temperature (chip on X4K-plate) vs power by sweeping digital supply and clock frequency, full RF-Low two-tone spectrum at 3K and DAC INL measurement explaining HD2.

Figure 19.1.S3: RF-High output with NCO at 350MHz, Two-tone RF-High output with NCOs at 241MHz and 260MHz, Noise spectral density and power consumption of various circuit blocks, all at 3K.