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19.1 A Scalable Cryo-CMOS 2-to-20GHz Digitally Intensive Controller for 4×32 Frequency Multiplexed Spin Qubits/Transmons in 22nm FinFET Technology for Quantum Computers

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Quantum computers (QC), comprising qubits and a classical controller, can provide exponential speed-up in solving certain problems. Among solid-state qubits, transmons and spin-qubits are the most promising, operating ≪ 1K. A qubit can be implemented in a physical system with two distinct energy levels representing the $|0\rangle$ and $|1\rangle$ states, e.g. the up and down spin states of an electron. The qubit states can be manipulated with microwave pulses, whose frequency f matches the energy level spacing $E = hf$ (Fig. 19.1.1). For transmons, f ~6GHz, for spin qubits f ~20GHz, with the desire to lower it in the future. Qubit operations can be represented as rotations in the Bloch sphere. The rotation axis is set by the phase of the microwave signal relative to the qubit phase, which must be tracked for coherent operations. The pulse amplitude and duration determine the rotation angle. A π-rotation is typically obtained using a 50ns Gaussian pulse for transmons and a 500ns rectangular pulse for spin qubits with powers of -60dBm and -45dBm, respectively.

State-of-the-art QCs, with only a few qubits, are typically driven by room temperature (RT) electronics, with a single RF-cable per qubit (Fig. 19.1.1). A fault-tolerant QC requires millions of qubits, making RT control impractical due to interconnect complexity. To address this, a fully-integrated cryogenic control system close to the qubits has been proposed [1]. A cryogenic pulse modulator has been demonstrated [2], however its scalability is limited by the need of one LO and cable per qubit, and external circuitry for LO leakage cancellation, as the LO is at the qubit frequency. Moreover, the used fixed-length symmetric pulses limit theoretically achievable operation fidelity and compatible qubit technologies. In this work, we present a scalable controller that (a) exploits FDMA to reduce the number of RF-cables per qubit (Fig. 19.1.1), (b) features arbitrary I/Q pulse generation for high-fidelity operation over a wide frequency (>4× higher than [2]) and output power range to support both spin qubits and transmons, and (c) can be directly integrated in an existing quantum control stack thanks to a digitally-intensive architecture with integrated instruction set.

A controller employing FDMA requires both a wide bandwidth to accommodate many qubits, each with a unique frequency [3], and pulse shaping to minimize spectral leakage to other qubits. To allow 99.99% fidelity for a π-rotation, exceeding the state-of-the-art, an SFDR >44dB is required to avoid disturbing unaddressed qubits [4]. This demands a linear transmitter architecture with good image and LO leakage rejection. For this fidelity, 44dB SNR is also required in a 25MHz noise bandwidth. To control both spin qubits and transmons, we designed for a 2-to-20GHz output frequency range, 40dB gain control, and flexible I/Q pulse shaping with 1ns to 40μs duration.

Figure 19.1.2 shows the block diagram of the system, comprising an instruction controller, a DDS and an analog/RF front-end. For coherent control of 32 qubits, 32 numerically controlled oscillators (NCO) with 0.2kHz frequency resolution are used, allowing the use of a single external LO. The DDS is clocked at 1GHz considering the number of qubits (N) and a required bandwidth of 30MHz/qubit [4]. A polar modulator is used to efficiently produce the desired pulse for each qubit at such a high clock frequency. The signals of two banks are combined in I/Q domain to achieve SSB up-conversion over a large data bandwidth. To achieve the required SFDR, digital I/Q and offset calibration networks are implemented for image and LO leakage rejection (α, β, γ in Fig. 19.1.1). As signal replicas of the 10-bit segmented (5T-5B) current-steering DAC (see Fig. 19.1.2) can fall in-band after up-conversion to low carrier frequencies, a 2nd order gm-C reconstruction filter is used. High linearity is achieved by utilizing current-bleeding in the DAC and current-mode operation in the filter.

The required gain control is achieved with >200 steps, by a baseband VGA, implemented as tunable current mirror, in combination with a tunable-gain RF amplifier. The current mirror feeds the current into a quadrature double-balanced Gilbert-cell active mixer with current-bleeding driven by an on-chip LO driver and active balun. To cover a 2-to-20GHz output band, the RF path is split into 2 parts with the high band using the 3rd harmonic of the LO for up-conversion. Cascode switches are used at the mixer output to steer the current either into a resistor for the RF-Low band (2-to-15GHz) or a transformer tuned to $3f_{LO}$ for the RF-High band (15-to-20GHz). The class-A amplifiers with wideband output baluns drive qubits over a 50Ω cable.

The chip was fabricated in 22nm FinFET CMOS with a total area of 16mm^2 comprising 4 controllers (M), flip-chip bonded to a BGA package (Fig. 19.1.7). A custom-made annealed and gold-plated copper enclosure was designed for efficient cooling and mounting of the PCB in a dilution refrigerator.

Figure 19.1.3 shows the measured peak output power at 3K over 2-to-20GHz, with flatness limited by additional ground inductance introduced in the layout. The sampling replicas are highly attenuated by the filter, as measured at the BB-out test port. The peak output power SFDR is >45dB, equally limited by HD2 and image rejection ratio (IRR). The LO rejection ratio (LORR) of 36dB after calibration does not limit the SFDR, as this is not a favorable band for qubit control in a direct conversion topology and can be avoided by proper choice of f_{LO}. Measured IM3 and SNR (25MHz bandwidth) are better than 50dB and 48dB, respectively.

The amplitude and phase modulation information for pulse shaping (18Gb/s) is stored in on-chip SRAM allowing envelopes up to 41μs, which are referenced by a look-up table (LUT) that can define 8 instructions per qubit (Fig. 19.1.4), each with a phase offset to efficiently re-use envelopes for different rotation axes. The use of instruction tables reduces the required data rate to the controller, which is further reduced to ~1kb/s by the integrated programmable instruction set executed on external trigger with minimal delay between instructions. The versatility of this design is demonstrated in Fig. 19.1.4 showing the measurement of an instruction sequence containing 5 unique waveforms targeting 5 different qubit frequencies.

To demonstrate qubit control, a Rabi-experiment is performed at 14GHz and 18GHz on a sample with one single-electron silicon spin qubit (Fig. 19.1.5, top), in which the qubit state is rotated over an increasing angle by a pulse of incrementing duration t. For a fair comparison, the chip is left connected to the qubit with only the digital turned on when using the RT setup, to avoid any change in qubit parameters. The performance of the quantum processor when driven by our controller is similar to that of the RT setup (specifications in Fig. 19.1.6), limited by the readout fidelity due to the qubit energy level spacing being comparable to the thermal energy. To demonstrate coherent control, rotations around different axes are performed by executing two $\pi/2$-rotations around the X-axis interposed by a Z-rotation with *varying* angle θ obtaining the expected cosine shape (Fig. 19.1.5, bottom). The Z-rotation is implemented using the built-in Z-correction (designed to compensate for Stark-shift due to crosstalk in an FDMA scheme [3]) that can automatically apply an instruction-dependent phase correction (Z-corr., Fig. 19.1.1) to any NCO.

Compared to state-of-the-art qubit controller ICs (Fig. 19.1.6), this work exhibits a wide frequency and output power range compatible with multiple qubit technologies. The frequency multiplexing architecture potentially enables multi-qubit control over a single RF-cable, leading to a scalable system. The digitally-intensive architecture enables waveform shaping flexibility, minimum execution latency and straightforward integration in the existing quantum computing stack.

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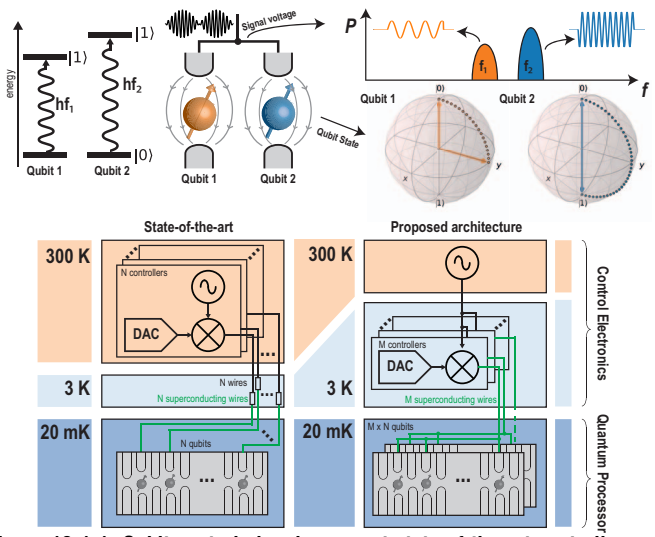

Figure 19.1.1: Qubit control signals, current state-of-the-art controller and presented cryogenic controller with frequency multiplexing.

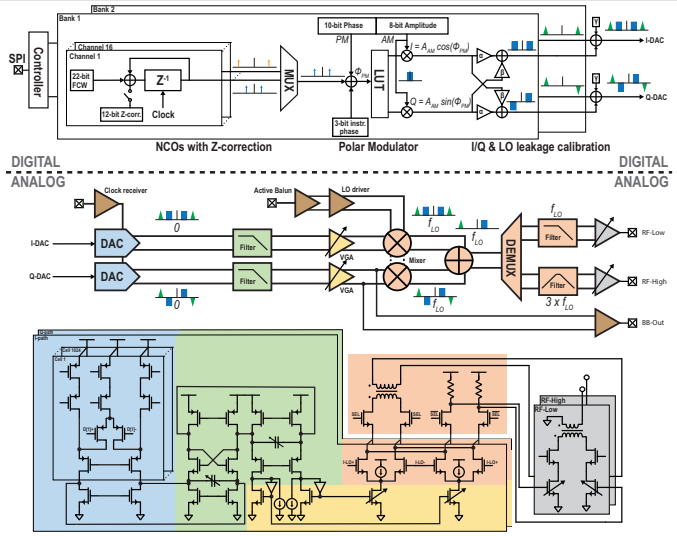

Figure 19.1.2: Block diagram and transistor level schematic (bias circuitry not shown).

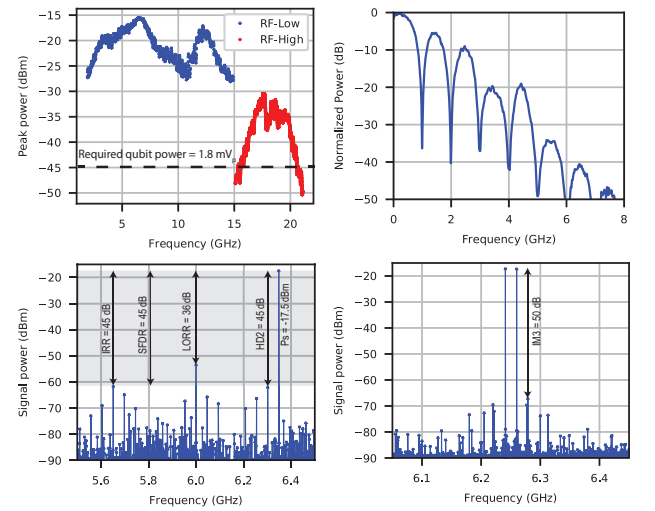

Figure 19.1.3: Measured RF Bandwidth, BB-Out transfer function, RF-Low output with NCO frequency at 350MHz, two-tone RF-Low output with NCO frequencies at 241MHz and 260MHz, all at 3K.

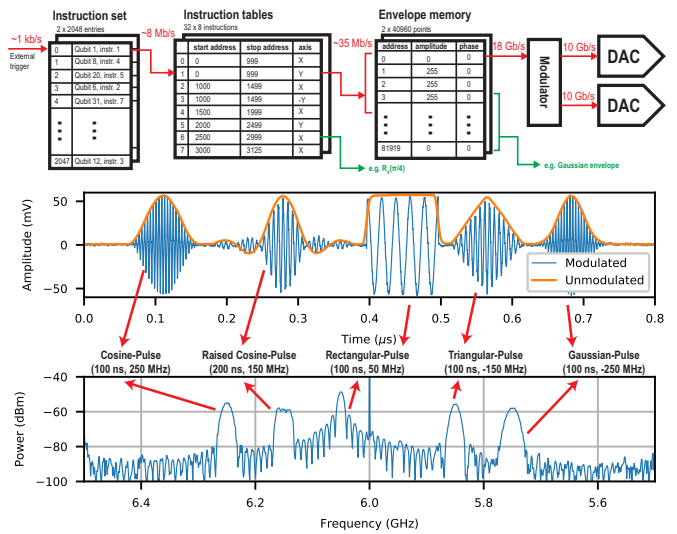

Figure 19.1.4: Qubit pulse shaping; top-to-bottom: digital backend, measured BB-Out signal and RF-Low spectrum (LO at 6GHz), both at 3K.

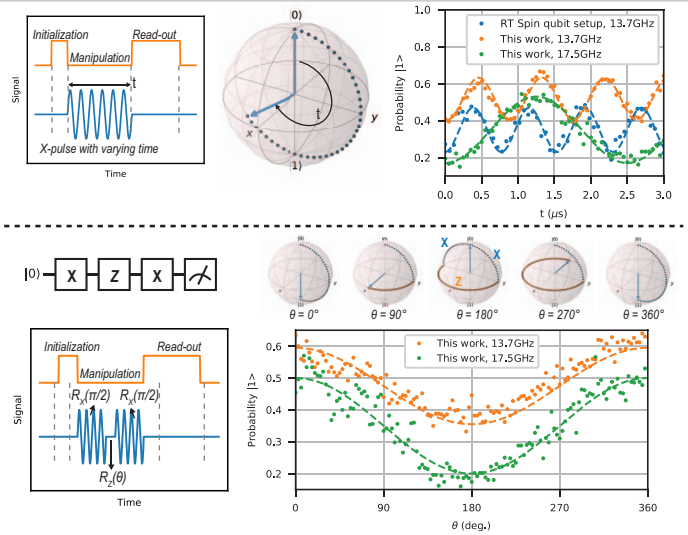

Figure 19.1.5: Rabi oscillation and coherent qubit control experiments at 14GHz and 18GHz with the controller IC at 3K.

	This work	ISSCC'19 [2]	RSI'17 [5]	Spin qubit setup
Operating Temperature	3 K	3 K	300 K	300 K
Qubit platform	Transmons + spin qubits	Transmons	Transmons	Spin qubits
Qubit frequency	2-20 GHz	4-8 GHz		< 20 GHz
Channels	128 (32 per TX)	1	4	1
FDMA	Yes, SSB	No	Yes, SSB	No
Sampling rate	1 GS/s	1 GS/s	1.2 GS/s	1.2 GS/s
Data Bandwidth	1 GHz	400 MHz	960 MHz	520 MHz
SFDR†	> 45 dB	N/A		70 dB
IM3 (Δf = 19 MHz)	> 50 dB	N/A		
SNR (BW = 25 MHz)	48 dB	N/A		
Noise Floor >10MHz	< -144 dBm/Hz (At -19 dBm)	N/A		-138 dBm/Hz (At +10 dBm)
Image & LO leakage calibration	On chip	Off chip	Yes	
Waveform/ Instructions	upto 40960 points AWG	Fixed 22 points symmetric		16M points AWG
Instruction set	Yes	No	Yes	Yes
Automatic Z-corr.	Yes	No	No	No
Power / TX	Analog: 1.7 mW/qubit* Digital: 330 mW‡	Analog: <2 mW/qubit# Digital: N/A		850 W
Chip area / TX	4 mm²	1.6 mm²	Discrete components	Rack mount
Technology	22 nm FinFET CMOS	28 nm bulk CMOS		

does not mention circuits included
* including LO/Clock driver; only RF-Low active
† single tone excluding residual LO leakage
‡ can be reduced with clock gating

Figure 19.1.6: Comparison table.

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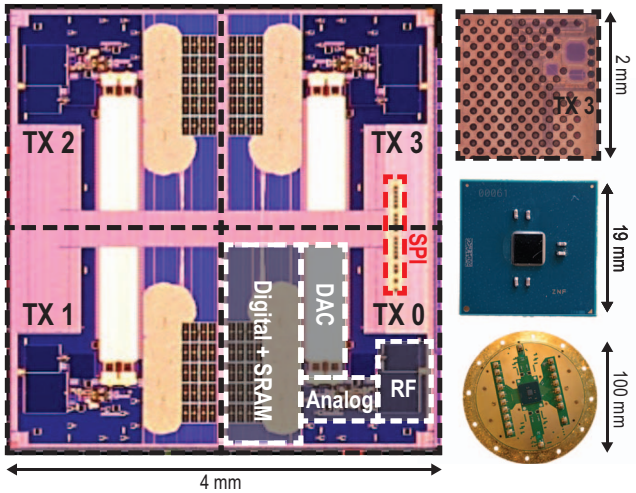

Figure 19.1.7: Die micrograph (without metal layers) with cut-out of a single transmitter showing I/O bumps and RF transformers, chip package and PCB with enclosure.

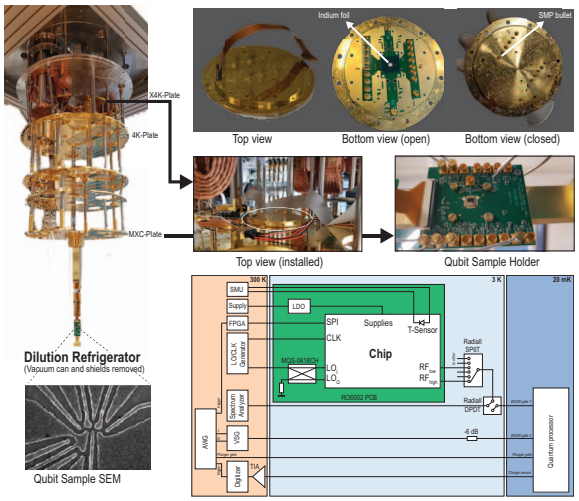

Figure 19.1.S1: Top to bottom, left to right: dilution refrigerator, qubit sample SEM, PCB enclosure (open & closed), chip and qubit mounting in the fridge and measurement setup block diagram.

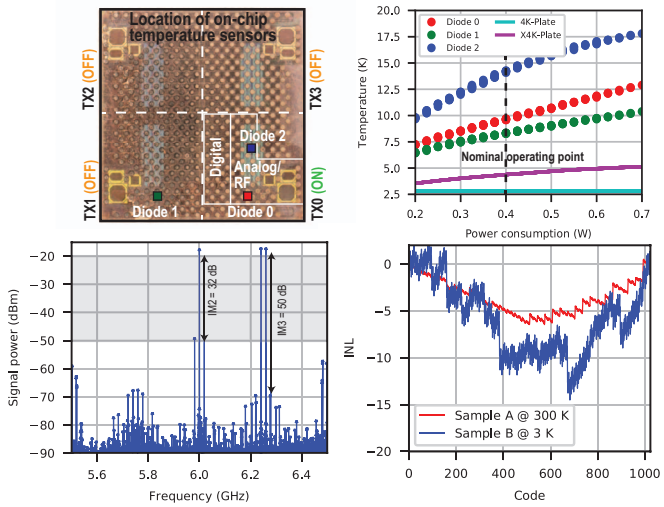

Figure 19.1.S2: Measurement of on-chip and refrigerator temperature (chip on X4K-plate) vs power by sweeping digital supply and clock frequency, full RF-Low two-tone spectrum at 3K and DAC INL measurement explaining HD2.

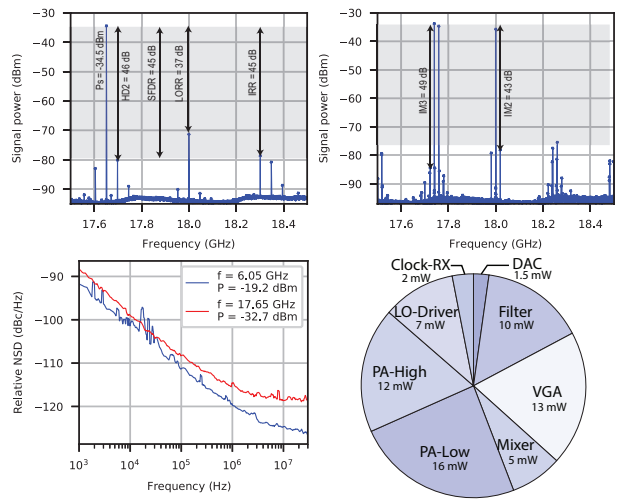

Figure 19.1.S3: RF-High output with NCO at 350MHz, Two-tone RF-High output with NCOs at 241MHz and 260MHz, Noise spectral density and power consumption of various circuit blocks, all at 3K.

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