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Modeling Static Noise Margin for FinFET based SRAM PUFs

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***Abstract*—In this paper, we develop an analytical PUF model based on a compact FinFET transistor model that calculates the PUF stability (i.e. PUF static noise margin (PSNM)) for FinFET based SRAMs. The model enables a quick design space exploration and may be used to identify critical parameters that affect the PSNM. The analytical model is validated with SPICE simulations. In our experiments, we analyze the impact of process variation, technology, and temperature on the PSNM. The results show that the analytical model matches very well with the simulation model. From the experiments we conclude the following: (1) nFET variations have a larger impact on the PSNM than pFET (1.5% higher PSNM in nFET variations than pFET variations at 25°C), (2) high performance SRAM cells are more skewed (1.3% higher PSNM) (3) the reproducibility increases with smaller technology nodes (0.8% PSNM increase from 20 to 14 nm) (4) increasing the temperature from -10°C to 120°C leads to a PSNM change of approximately 1.0% for an extreme nFET channel length.**

***Index Terms*—SRAM PUF, FinFET, Static noise margin, process variation, temperature**

I. Introduction

Physical unclonable functions (PUFs) are hardware primitives used to create identifiers and cryptographic keys [1]. SRAM PUFs are one of the most popular types of PUFs and deployed in many commercial products e.g. from Microsemi [2] and NXP [3]. The SRAM PUF type is often preferred, as SRAM is typically available in most micro controllers and systems. Using SRAM PUFs for the creation of cryptographic keys requires a high reproducibility and reliability in noisy environments. For this reason, error correction codes (ECCs) are utilized to correct the errors in PUFs. Each ECC scheme has a specific correction capability and hardware cost. In addition, the PUF responses must be unique and uniform for security purposes [4]. The reproducability, uniqueness, and uniformity are depended on environmental conditions such as voltage and temperature, but also the technology. Compared to planar devices, FinFET structures have improved short channel effects [5], making them behave differently at start-up. FinFET devices have in general different characteristics and thus are affected by variations differently [6]. Therefore, to predict the reproducability (e.g. to add a proper amount of ECC), uniqueness, and uniformity, the impact of technology and environmental conditions and technology should be known at design time. This requires proper PUF modeling to perform a quick design space exploration.

Previous studies on SRAM PUF stability have focused mainly on planar CMOS technology [7–9]. Cortez et al. [7] modeled the SRAM PUF behavior for 65nm technology while considering supply voltage, temperature, and process variation for both NMOS and PMOS transistors. Vatajelu et al. [8] identified unreliable PUF cells based on an SRAM stability test. In particular, the authors used the difference between noise margin for "1" and "0" cell values and created PUFs from cells with highest difference and showed that the reliability for the selected SRAM PUF bits can be greatly improved by it. Roelke et al. [9] studied the impact of negative bias temperature instability (NBTI) on the cell skew. In the context of FinFET SRAM PUF stability, Faragalla et al. [10] analyzed the impact of V_{TH} variation and power supply on PSNM using simulations for 16 nm technology node. To accurately characterize the PSNM, many Monte Carlo simulations are required to model the process variations properly. To the best of our knowledge, there is no analytical model proposed for FinFET SRAM PUF in the literature. Furthermore, the impact of temperature, high performance vs lower power design, and technology nodes for FinFET SRAM PUF have not been investigated yet.

In this paper, we address these limitations and model the stability of FinFET-based SRAM PUFs analytically. The model estimates the PSNM value for certain parameters and environmental conditions. It enables a quick design space exploration which can be used to perform sensitivity analysis in order to identify parameters that effect the stability the most. Our contributions can be summarized as follows:

- Proposal and simulation-based validation of an analytical PSNM model for FinFET technology.
- Comparison between the impact of nFET and pFET process variation on FinFET SRAM PUF.
- Analysis and comparison of high performance and low power SRAM PUF designs
- Analysis of the impact of temperature on $\mathrm{PSNM}_{\mathrm{noise}}$ and $\mathrm{PSNM}_{\mathrm{ratio}}$ and technology scaling on $\mathrm{PSNM}_{\mathrm{ratio}}$.

The rest of paper is organized as follows. Section II provides a background on SRAM PUF and the SNM metric. Section III explains the analytical model of PUF static noise margin in FinFET technology. Section IV provides the simulation methodology and setup. Section V presents results. Finally, Section VI discusses the results and concludes this paper.

II. Background

SRAM cell: Fig. 1(a) shows the structure of a 6T SRAM cell. It consists of six transistors, i.e., two access transistors (Q_3 and Q_4), and two cross-coupled inverters INV_1 (containing Q_1 and Q_5) and INV_2 (containing Q_2 and Q_6). During normal operation, access transistors Q_3 and Q_4 are on and used to capture the true (V_T) and complementary (V_C) node during read operations or force them to a certain value during write operations. To maximize the stability, the cells are designed fully symmetrical. In addition, during start-up access transistors Q_3 and Q_4 are disabled and hence the start-up value is affected by the two cross-coupled inverters only. During ramp up, as the supply voltage increases, the drain currents of transistors Q_1, Q_2, Q_5, and Q_6 also increase. As a sequence, the drain and connected gate voltages of these four transistors change as well. Once V_T (voltage on the true node) or V_C (voltage on the complementary node) reaches the threshold voltage of Q_1 or Q_2, the corresponding transistor will turn on.

Process variation: Although SRAM cells are designed symmetrically, a cell initializes to a certain state at power up due to process variation and noise. Process variation leads to a mismatch between the two inverters in the SRAM cell and is the main source of randomness [11]. Process variation can be categorized into two sub-categories: global and local variation. Global (inter-die) variation at the chip- or wafer-level impacts a large group of transistors simultaneously in a similar manner [6], while local (intra-die) variation impacts individual transistors [12]. Local variation creates a mismatch between the inverters which subsequenlty leads to a skewed cell. The larger the skew the stronger the preferred start-up value becomes [7]. The impact of process variation depends on the technology. FinFET devices have a different structure than planar CMOS devices. The main sources of variation in transistors come from non-deterministic placement of dopants and the geometric dimensions of the transistor; they impact the mobility, insulator thickness, channel length, and width, etc. Due to reduced short channel effects in FinFET devices, high dopant concentration is not necessarily needed [13]; therefore variations in the geometric shape of the channel are more important for FinFET devices. Examples of variations in the geometry are the fin height, width and length. Variations in the fin height is considered to be global variation as they affect all transistors, while variations in the fin width and channel length are a consequence of the lithography process and hence considered local variation [14, 15].

SRAM PUF: When SRAM cells are used for PUF, only the start-up process is relevant. This process is affected by random process variations and hence they can be exploited to create PUFs [16]. To evaluate their robustness, several metrics can be used. Among them are the *reproducibility*, *reliability*, *uniqueness*, and *uniformity*. The reproducability and reliability show how often a PUF reproduces the same value when it

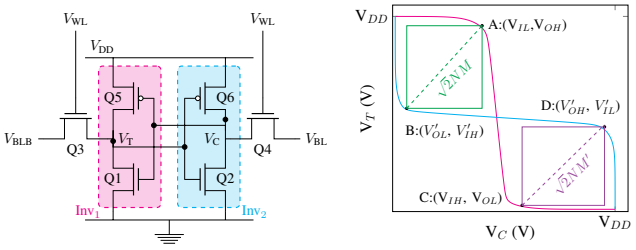

Figure 1: (a) SRAM cell (b) VTC of SRAM cell

turns on. *Reproducibility* focuses on a single condition (i.e. a certain temperature and supply voltage), while *reliability* looks at the complete life cycle. The higher the PUF tolerance is compared to the noise level, the higher the stability of the SRAM PUF. The reproducibility and reliability of a PUF can be expressed in terms of PUF static noise margin (PSNM) [7]. SNM is defined as the maximum noise that a cell tolerates before its value flips. It can be derived from the voltage transfer curve (VTC). Fig. 1(b) shows the voltage transfer curve of an SRAM cell. It consists of two graphs, one for each inverter of the SRAM cell. VTC shows the voltage output of the inverters as a function of their corresponding inputs. This curve has two "eyes" each representing a static noise margin value for the true and complementary nodes. When an SRAM cell is not fully symmetric, the relative sizes of these eyes change and as a result the SNM is affected as it creates asymmetric SNMs for the true and complementary nodes [7]. The ratio between the SNM for the true and complementary nodes is defined as PSNM ratio ($PSNM_{ratio}$). When a cell becomes more asymmetric (e.g. due to process variation), the cell becomes more skewed. As a result, the reproduciblity increases as noise and random effects have a smaller impact. The minimum value between the SNM of the true and complementary nodes is defined as the PSNM noise ($PSNM_{noise}$). Note that this is equivalent to the hold SNM of the cell. The higher the $PSNM_{noise}$, the higher the PUF stability [7]. For security purposes, *uniqueness* and *uniformity* of SRAM PUF devices are important in order to prevent the predictability by attackers.

III. Analytical Model

In this section, we model the $PSNM_{ratio}$ and $PSNM_{noise}$ for FinFET based SRAM PUFs using a compact FinFET device model.

Alternatively to using simulations to derive VTC, one can find the four critical points of the VTC analytically (i.e, points A, B, C, and D in Fig. 1(b)) and derive the noise margins from them. These critical points correspond to the points in the VTC where the operational regions of the transistors change.

$PSNM_{ratio}$ is defined as the ratio of the noise margins of the cell for the true and complementary values and $PSNM_{noise}$ as the minimum margin between the two [7]. They can be expressed as follows:

$$\text{PSNM}_{\text{ratio}} = NM/NM' \quad (1)$$

$$\text{PSNM}_{\text{noise}} = \min(NM, NM') \quad (2)$$

where NM and NM' are the noise margins for the true and complementary nodes, respectively. The noise margins represent the minimum noise that is needed to flip the cell to its other state. They can be calculated based on the four critical points (see Fig. 1(b)) as follows [7]:

$$NM = \min(NM_H = V_{OH} - V'_{IH}, NM_L = V_{IL} - V'_{OL}) \quad (3)$$

$$NM' = \min(NM'_H = V'_{OH} - V_{IH}, NM'_L = V'_{IL} - V_{OL}) \quad (4)$$

In Fig. 1, points A = (V_{IL},V_{OH}) and C = (V_{IH},V_{OL}) belong to INV_1, while points B = (V'_{OL},V'_{IH}) and D = (V'_{OH},V'_{IL}) to INV_2. The operational regions of the four critical points are as follows.

- Point A: transistor Q_1 and Q_5 are in saturation and linear region, respectively.
- Point C: transistor Q_1 and Q_5 are in linear and saturation region, respectively.
- Point B: transistor Q_2 and Q_6 are in linear and saturation region, respectively.
- Point D: transistor Q_2 and Q_6 are in saturation and linear region, respectively.

The current through the transistors is not only region dependent, but also depends on the gate voltages and physical parameters. We adopt the compact transistor model presented in [17] to model such relations. The current in saturation and linear regions are provided in Equations (5) and (6), respectively [17].

$$I_{\text{ds,sat}} \approx \frac{\mu}{2L} C_{\text{ins}} (V_{\text{g}} - V_{\text{th}})^2 \quad (5)$$

$$I_{\text{ds,lin}} \approx \frac{\mu}{L} C_{\text{ins}} \left(V_{\text{g}} - V_{\text{th}} - V_{\text{ds}}/2\right) V_{\text{ds}} \quad (6)$$

$$C_{\text{ins}} = \frac{\epsilon_{\text{ins}}}{T_{\text{ins}}} W_{\text{channel}} \quad (7)$$

$$W_{\text{channel}} = N_{fin} \times (T_{fin} + 2 \times H_{fin}) \quad (8)$$

In these equations, C_{ins} represents the insulator capacitance, L the channel length, μ the charge mobility, V_g the gate voltage, V_{ds} the drain source voltage, and V_{th} the threshold voltage. C_{ins} depends on the material of the insulator and its dimensions and hence is a function of the equivalent gate dielectric thickness T_{ins}, permittivity of the insulator ϵ_{ins} and channel width $W_{channel}$, as expressed in Equations (7) [18]. The channel width $W_{channel}$ depends on the dimensions of the transistor, such as the number of fins N_{fin}, the fin height T_{fin}, and fin thickness T_{fin}, as shown in Equation (8). T_{fin} and H_{fin} are technology dependent, while N_{fin} can be used to design a reliable cell in terms of reading and writing. The charge mobility μ in Equations (5) and (6) mainly depends on the temperature and can be modeled as follows [18]:

$$\mu(T) = \mu_0(L, N_{fin}) + \left(\frac{T}{T_{nom}}^{UTE_i}\right) + UTL_i(T - T_{nom}) \quad (9)$$

where $\mu_0(L, N_{fin})$ represents the initial mobility based on the channel length and number of fins, T the actual temperature, T_{nom} the nominal temperature, and UTE_i and UTL_i mobility temperature coefficients which equal to 0 and -0.0015 respectively [19].

During start-up, access transistors Q_3 and Q_4 in Fig. 1(a) are disabled. Hence, the currents through the transistors of INV_1 (i.e. Q_1 and Q_5) as well as INV_2 (i.e. Q_2 and Q_6) are equal. This is shown in Equation (10) for INV_1.

$$I_{d,Q1} = I_{d,Q5} \quad (10)$$

Substituting these currents with the currents for saturation and linear region expressed in Equations (5) and (6) respectively gives an expression in terms of voltage for each of the four critical points. For example, for point A the following equation can be derived:

$$\begin{aligned} &\frac{\mu_{Q1}}{2L_{Q1}} C_{\text{ins,Q1}} (V_{\text{g,Q1}} - V_{\text{th,Q1}})^2 = \\ &\frac{\mu_{Q5}}{L_{Q5}} C_{\text{ins,Q5}} \left(V_{\text{g,Q5}} - V_{\text{th,Q5}} - \frac{V_{\text{ds,Q5}}}{2}\right) V_{\text{ds,Q5}} \end{aligned} \quad (11)$$

Here $V_{ds,Q5}$ represents the drain source voltage of Q_5, and $V_{g,Q1}$ and $V_{g,Q5}$ the gate voltages of Q_1 and Q_5, respectively. Note that similar equations for points B, C and D are omitted for brevity.

To calculate the coordinates for point A on the VTC curve, expressions for V_{IL} and V_{OH} should be defined. Hence, we replace the gate and drain source voltages of Equation 11 with these voltages. This is similarly done for the equations of the other three points. Using Fig 1.(a) and (b), the following relations for transistors Q1 and Q5 can be observed:

$$\text{V}_{\text{ds,Q5}} = V_{OH} - V_{DD} \quad (12)$$

$$\text{V}_{\text{g,Q1}} = \text{V}_{\text{g,Q5}} = V_{IL} \quad (13)$$

Substituting Equations (12) and (13) into Equation (11) results in an equation with variables V_{OH} and V_{IL} for point A. Note that at this point we have four equations (i.e., one for each critical point) and eight unknowns (i.e., the coordinates of the four points). Hence, four additional equations are needed. These 4 additional equations can be obtained by considering the slope at the four points.

Using Equation (11), the derivative of V_{OH} with respect to V_{IL} can be calculated which describes the slope at point A of VTC in Fig. 1(b), i.e.,

$$\frac{dV_{\text{OH}}}{dV_{IL}}|_A = k_1 \quad (14)$$

In order to find analytical expression for V'_{OL} and V'_{IH} for point B, V_{OL} and V_{IH} for point C, and V'_{OH} and V'_{IL} for point D, similar steps are applied with two main differences: (i) the current model differs for the points B and D due to different operational regions, and (ii) the slope in points A and B are equal (i.e., equal to k_1 in Equation (14)); similarly, the slopes in points C and D are equal as well, suppose equal to k_2. In this paper we consider k_1 and k_2 to be temperature

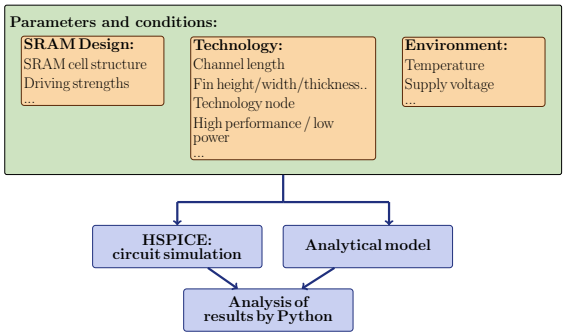

Figure 2: Validation Process

and channel length dependent, which was previously assumed to be -1 in the literature for planar devices. In particular, we found that k_1 and k_2 were generally different and hence we estimated these parameters based on simulations to have a more accurate model.

Solving the above equations give values for V'_{OH}, V'_{IL}, V'_{OL}, V'_{IH}, V_{OL}, V_{IH}, V'_{OH}, and V'_{IL}; by substituting them in Equations (1) and (2) through Equations (3) and (4) an analytical model can be derived for $PSNM_{ratio}$ and $PSNM_{noise}$. The closed form of the model is omitted for brevity.

IV. Experimental Setup and Performed Experiments

A. Setup

In order to validate the proposed analytical model for PSNM in Section III, HSPICE simulations are performed using the same inputs for both cases as shown in the validation process depicted in Fig. 2. The inputs are categorized into three main categories: design, technology and environmental parameters. With respect to the design, the typical 6 transistor (6T) cell is used. In 6T structure, the ratio between the strength of pull up (PU), pull down (PD) and access transistors (AX) must satisfy certain conditions to perform reliable read and write operations [20]. Here, we use the minimum sizes that satisfy these conditions, i.e., the relative drive strengths are PU:AX:PD=1:1:2. The design is implemented using 16 nm PTM low power FinFET library [19]. To model the impact of local process variation, a Guassian distribution with σ = 4% [21] for channel length is used. Hence, we consider a channel length between $L_{nominal} \pm 3\sigma$ i.e, 17.6 nm to 22.4 for the 16 nm technology node with $L_{nominal}$= 20 nm which correspond to 99% of the values in the Guassian distribution. Note that the channel length is one of the major sources of variations in FinFET devices as explained in Section II. We consider the nominal supply voltage, while varying the temperature from -40°C to 120°C.

In simulations, the BSIM model for FinFET in HSPICE is used for the transistors. However, as the transistor model differs from the compact FinFET model of [17], fitting parameters are used to bridge the differences between both models such as the value for $k1$ in Equation (14).

B. Performed experiments

In this paper, two main sets of experiments are performed. First, the analytical model is validated using SPICE simulations. In this experiment, the following two sub-experiments are performed and the results between the analytical and simulation model are compared:

1) Analysis of the impact of nFET and pFET channel length variation on the $PSNM_{ratio}$
2) Analysis of the impact of temperature on $PSNM_{ratio}$. Note that using nominal lengths results in a $PSNM_{ratio}$ of "1" as the cell is fully symmetric in this case. Hence, the extreme channel lengths of $L_{nominal} \pm 3\sigma$ are used here.

Second, due to lack of compact transistor models for other technologies (such as high performance libraries) and limited accuracy of the analytical model, we analyze the impact of high performance and low power designs and also different technology nodes on $PSNM_{ratio}$ using simulations only. The following experiments are performed:

3) Analysis of the impact of nFET channel length variation for high performance (HP) and low power (LP) designs on $PSNM_{ratio}$.
4) Analysis of the impact of technology scaling on $PSNM_{ratio}$; we analyze 20 nm, 16 nm, and 14 nm FinFET technology nodes.
5) Analysis of the impact of temperature on the $PSNM_{noise}$.

V. Results

In this section, we present the results of the two main sets of experiments described in the previous section.

A. Validation of Analytical Model

1. Impact of nFET and pFET channel length variation: Fig. 3 shows the impact of nFET and pFET channel length variation on the $PSNM_{ratio}$ for the analytical and simulation model at a junction temperature of 65°C. The channel length of either transistor Q_1 or Q_5 (see Fig. 1(a)) is varied linearly between their 3σ ranges while all other transistors are kept at their nominal values. From the figure we conclude the following:

- The correlation between the channel length and $PSNM_{ratio}$ is almost linear for both nFET and pFET, which can be observed both from the analytical and simulation model. The difference between the analytical and simulation results is marginal. The largest error (i.e., 0.5%) occurs for the shortest nFET channel length, where $PSNM_{ratios}$ of 0.9635 and 0.9584 are observed for the analytical and simulation model, respectively.
- Variations in the nFET have a larger impact than pFET, e.g., 1.68% for the extreme channel length, as the nFETs have more fins and the mobility of nFET transistors is higher [18]. The higher mobility of the nFET has a larger impact on the cell current and hence, leads to a larger mismatch between the cross-coupled inverters, which explains the larger impact on $PSNM_{ratio}$.

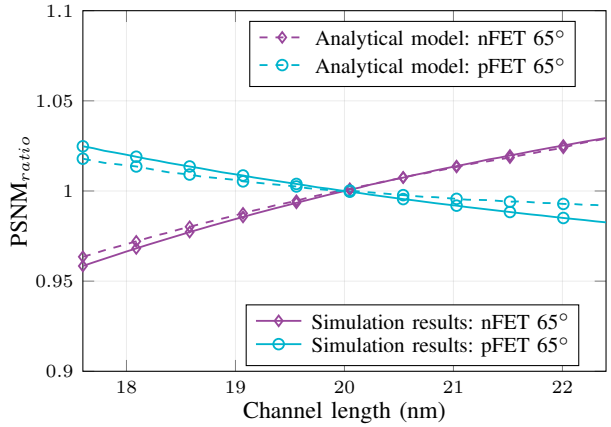

Figure 3: Impact of channel length on PSNM$_{\text{ratio}}$

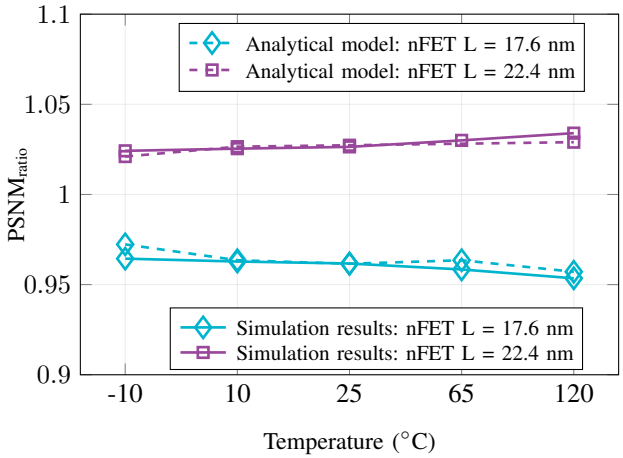

Figure 4: Impact of temperature on PSNM$_{\text{ratio}}$

2. Impact of temperature on PSNM$_{\text{ratio}}$: Fig. 4 shows the impact of temperature and the extreme nFET channel lengths (both min and max, i.e., 20 nm$\pm 3\sigma$) on the PSNM$_{\text{ratio}}$ using the analytical and simulation model. From the figure we conclude the following:

- The difference between the analytical and simulation model is again marginal. The largest differences occur at extreme temperatures due to simplification in the compact model.
- The higher the temperature, the more important process variations become. At high temperatures, the cell becomes more skewed and the PSNM$_{\text{ratio}}$ gets further away from the value one. This can be explained as follows: a higher temperature leads to a lower threshold voltage [22] and hence it affects the start-up value of the cell more. The relative PSNM$_{\text{ratio}}$ increment between -10°C to 120°C equals -1.1% and 0.98% for L=17.6 nm and L=22.4 nm, respectively.

B. Simulation results

3. Impact of nFET channel length on PSNM$_{\text{ratio}}$ for HP and LP designs: Figs. 5 shows the impact of HP and LP SRAM cells on PSNM$_{\text{ratio}}$. The same channel lengths are used as the ones in the previous experiment. Note that the libraries used for the HP and LP designs have different physical parameters,

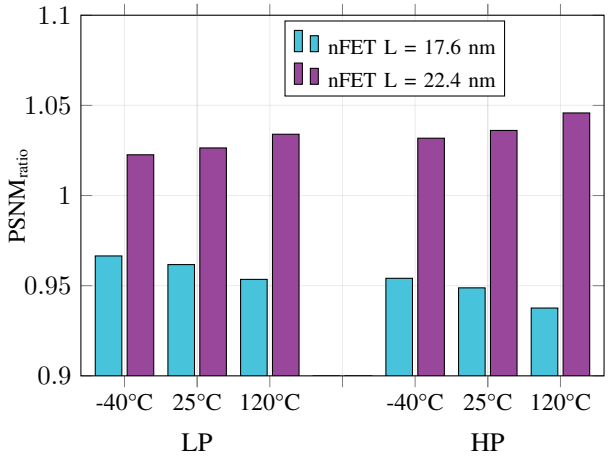

Figure 5: Impact of Design (HP vs LP) on PSNM$_{\text{ratio}}$

e.g. work function, mobility, and equivalent gate dielectric thickness and hence different 16 nm libraries are used for the low power and high performance models. From the figure we conclude the following:

- The cells are more skewed for the HP design than the LP design, as the PSNM$_{\text{ratio}}$ is further away from one. For example, the HP design has a 1.29% lower PSNM$_{\text{ratio}}$ than the LP design at 25°C for the minimum extreme nFET channel length, i.e. L=17.6 nm. As the HP library has a lower threshold voltage and a higher leakage current, it causes a similar affect as increasing the temperature as described in the previous subsection.
- Both the LP and HP design have a similar dependency on the temperature.

4. Impact of technology scaling on PSNM$_{\text{ratio}}$: Fig. 6 shows the impact of technology scaling on PSNM$_{\text{ratio}}$. 20, 16 and 14 nm PTM LP libraries are used as technology nodes and the channel lengths for each of the technology nodes are set to $L_{nominal} - 3\sigma$. From the figure we conclude the following:

- The PSNM$_{\text{ratio}}$ gets further away from one when smaller technologies is used and hence more skewed cells. The reduction equals 0.8% when moving from 20 nm technology to 14 nm node at 25°C. As the channel is getting shorter, the gate control over the channel decreases and the sensitivity of process variation increases.
- The PSNM$_{\text{ratio}}$ of the LP designs in 20nm, 16nm and 14 nm have a similar dependency on the temperature.

5. Impact of temperature on the PSNM$_{\text{noise}}$: Fig. 7 shows the impact temperature on the PSNM$_{\text{noise}}$ using L=17.6 nm. From the figure we conclude the following:

- The absolute PSNM$_{\text{noise}}$ reduces with increased temperature. This can be justified by the fact that increasing temperature leads to a decrease in threshold voltage.
- Considering 25°C as a reference condition (e.g. for enrollment), the absolute PSNM$_{\text{noise}}$ difference is higher for higher temperatures as indicated by the dashed line in the Fig 7. This shows that the stability of SRAM will decrease with higher temperatures.

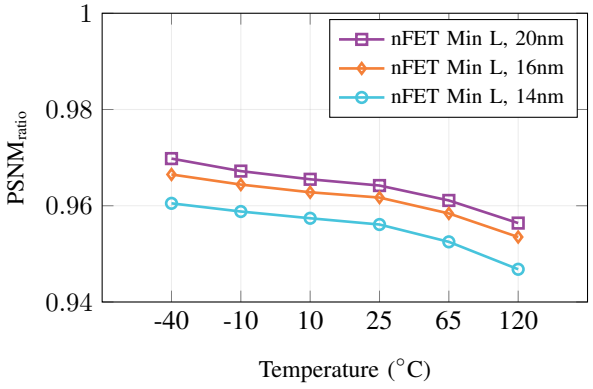

Figure 6: Impact of technology node on $PSNM_{ratio}$

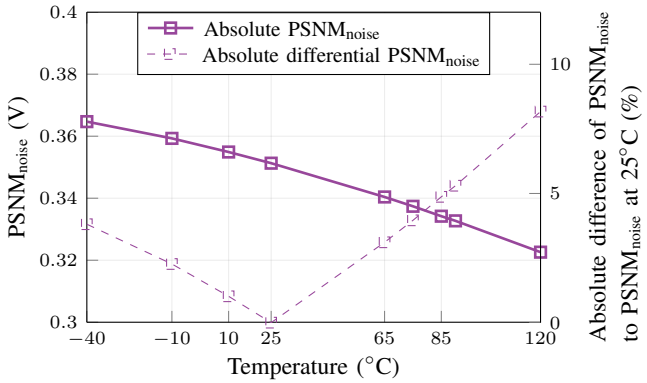

Figure 7: Impact of temperature on $PSNM_{noise}$

VI. Discussion and Conclusion

In this work we analyzed the stability of FinFET SRAM PUFs in terms of $PSNM_{ratio}$ and $PSNM_{noise}$. From the results, we conclude the following:

Analytical versus simulation model: The difference between the analytical and simulation results were marginal. However, due to lack of accurate FinFET compact models for extreme temperatures, the model did not work properly at -40°C. Hence, the validation has been limited to -10°C to 120°C in Figure 4. Nevertheless, the simulation results confirmed the methodology and other FinFET models can be used to obtain a higher accuracy and a larger range of temperatures.

Sensitivity analysis: The impact of process variation, temperature, technology node, and cell type (i.e. high performance vs low power) on PSNM has been investigated. The results showed that (1) variations in nFET have a higher impact than pFET, (2) the impact of process variation on $PSNM_{ratio}$ increases with higher temperature, (3) $PSNM_{ratio}$ increases with technology scaling due to higher impacts of lower channel lengths (4) high performance FinFETs are more sensitive to process variation than low power FinFETs.

FinFET vs planar technology: Cortez et al. showed in [7] that the maximum $PSNM_{ratio}$ change due to channel length variation equals 1.4% at 25° for 65 nm planar devices, which is much lower than the 3.84% observed for FinFET devices. Similarly, Cortez et al. showed that the $PSNM_{noise}$ changes at most 0.7% by technology parameters variation, which is 3% for FinFET devices. These higher differences in $PSNM_{ratio}$ create more skewed cells and hence positively impacts the reproducibility. Although the 65 nm planar technology is much older than the 16 nm FinFET, Narasimham et al. [23] showed that the randomness in 16 nm FinFET based SRAM PUF is better than 28 nm planar CMOS based. However, the percentage of unstable bits due to aging is marginally higher in FinFET.

PUF metrics and optimal $PSNM_{ratio}$: An increase in $PSNM_{ratio}$ leads to a more skewed SRAM cell and hence, improved reproducibility. However, at the same time it results in a lower $PSNM_{noise}$ which means that the hold SNM reduces of the cell. In addition, it also affects the read and write stability. More research is required to find ideal $PSNM_{ratio}$ and $PSNM_{noise}$ values that are on the one hand created skewed cells, but on the other hand do not impact the cell margins too much.

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