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Suitable Submodule Switch Rating for Medium Voltage Modular Multilevel Converter Design

Aditya Shekhar, Thiago Batista Soeiro, Zian Qin, Laura Ramírez-Elizondo and Pavol Bauer

***Abstract*—An important step in Voltage-Source Modular Multilevel Converter (MMC) design is the selection of adequate semiconductor blocking voltage class. This paper highlights that particularly for grid connected medium voltage applications, the choice of suitable switch blocking voltage class is not so straightforward. The market available switch voltage ratings results in a discrete integer relationship for the number of sub-modules (N) with a fixed dc link voltage. This is shown to introduce interesting design trade-offs in consideration to investment costs, required capacitance for reasonable ripple voltage, sub-module redundancy requirements, conduction & switching losses. Using the example of a 10 MVA half bridge MMC connected to a 10 kV grid, it is shown that 1.7 kV and 3.3 kV insulated gate bipolar transitors (IGBTs) can be possible choices as compared to 1.2 kV, 4.5 kV and 6.5 kV blocking voltage.**

***Index Terms*—cascaded cells, half bridge, high power, medium voltage distribution, multilevel converter design, MVDC, number of submodules, IGBT, optimum semiconductor voltage level**

I. Introduction

The concept of modular multilevel converters (MMC) was first introduced by Alesina in [1]. The potential of this concept was extended for a wide power range in [2]. Based on the extensive research on various aspects pertaining to MMC operation, it has particularly become the preferred topology for high voltage direct current (HVDC) applications [3].

In HVDC applications, the number of levels are adequately high corresponding to the commercial range of insulated gate bipolar transitors (IGBT) blocking voltage ratings. In such cases, minimizing the number of levels while selecting the switch with highest voltage rating and ensuring efficient performance at the expected operating power range could be more important. For example, in [4], it is shown that for HVDC applications, higher switch ratings are preferred with increasing operating power level based on cost-efficiency trade-offs. With decreasing grid voltage, lower blocking voltages may become preferable for cascaded full bridge cells [5].

Section II discusses the degrees of freedom available during the design of a half bridge MMC. Their inter-dependencies are highlighted and the important trade-offs are identified. The focus of this paper is to offer a non-comprehensive analysis on some less explored associations and emphasize that a careful selection of blocking voltage class is particularly important for medium-voltage high power applications. Further research on this is relevant due to increasing focus on medium voltage dc distribution [6]–[9] as well as high power drive and wind turbine applications [10]–[14].

In Section III, the influence of three degrees of freedom associated with the required number of submodules (N) for a fixed dc link voltage is explored. It is shown that since N can only take discrete integer values, the appropriate capacitor voltage ripple and reliability factors should be carefully chosen to maximize the installed semiconductor utilization. Using installed semiconductor power as an indicator of cost, it is shown that it disproportionately increases with a unit increase in N for higher blocking voltage class.

In Section IV, the steady state losses of the half bridge MMC are analytically determined for different IGBT blocking voltage classes. The computations discussed are specific to the case with 10 MVA power delivered at unity power factor to a 10 kV ac grid and support the intuitive understanding that as N increases, the conduction losses increase but the switching losses decrease for a fixed dc link voltage.

Section V reiterates that the final choice of suitable switch rating must consider inter-dependencies between various degrees of freedom that influence the cost, efficiency, size, reliability and power quality of the converter.

II. Design Considerations

Fig. 1. shows the schematic of a phase leg (M) of the three phase ac-dc medium voltage MMC.

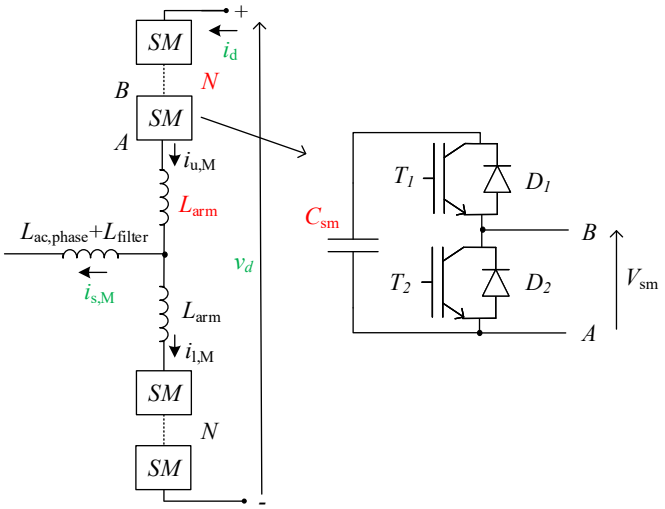

Fig. 1: Schematic of a single leg of a three phase ac-dc modular multilevel converter with half bridge submodules.

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It consists of 'N' submodules (SM) and inductance L_{arm} per arm. Each SM consists of two IGBT switches (T_1,T_2) with anti-parallel diodes (D_1,D_2) and a capacitor (C_{sm}). The specifications of the converters are fixed with dc link voltage v_{d} and the operating active (P) and reactive (Q) powers. The upper and lower arm currents $i_{\text{u,M}}$ and $i_{\text{l,M}}$, dc link current i_{d} and the output current $i_{\text{s,M}}$ are shown. The available degrees of freedom and associated trade-offs during the design stage are depicted in Fig. 2.

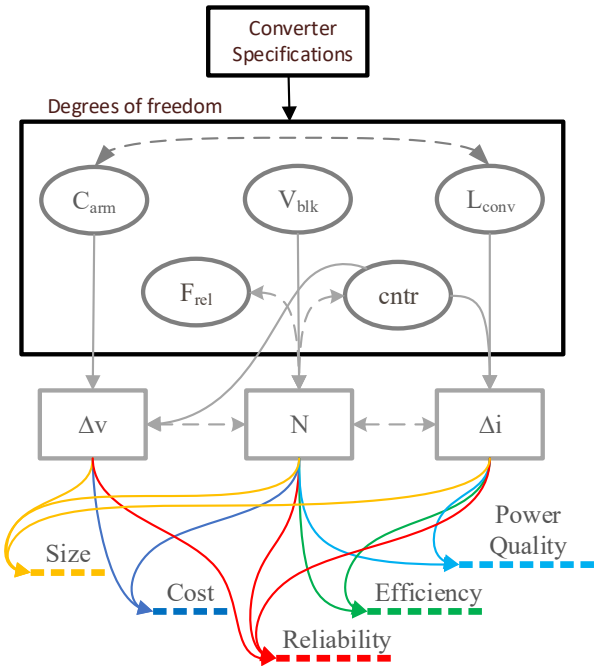

Fig. 2: Degrees of freedom and performance criteria for MMC design of given specification.

A. Arm Capacitance (C_{arm})

An interesting discussion is carried out in [15] on the capacitive energy storage requirements. It shows the influence of rated power on the requirement for C_{arm} for a given v_{d} and thus influences the ripple voltage ΔV. In [16], two parts of ΔV are identified: (i) The average part which is a function of C_{arm} and the converter power independent of control (ii) The local part due to the imbalance in C_{sm} which can be influenced by the blocking voltage class (V_{blk}) (refer Section II-B) and control methodology (refer Section II-E). As the selected voltge ripple factor (k_{max}) based on the acceptable ΔV increases, the required C_{arm} decreases but may increase the required N. The importance of including the capacitor ripple voltage during the selection of N is also highlighted in [17]. This relationship is explored in Section III and it is shown that since N can only take integral values, the value of k_{max} should be carefully chosen to maximize the semiconductor utilization, particularly for IGBTs with higher V_{blk}.

B. Rated Blocking Voltage (V_{blk})

V_{blk} strongly governs N. It is discussed in [5] that for a cascaded H-bridge topology, lower switch ratings are preferred as the operating ac grid voltage decreases. This is because the efficiency of the converter is limited by switching losses for lower grid voltages, and by conduction losses for higher voltages. For HVDC application of half bridge MMC, an interesting discussion is presented in [4] about the choice between 3.3, 4.5 and 6.5 kV IGBTs based on investment cost, efficiency and transmitted power. Specifically, it was shown that as transmitted power increased, SMs based on higher blocking voltage may be preferred. Increasing preference for 3-level neutral point clamped voltage source converter (VSC) over a 2-level VSC with higher operating powers is also shown in [18]. Applying the combined influence of such principles for a medium voltage half bridge MMC, this paper supports the relevance of such a design study using a single power level (10 MVA) and grid voltage (10 kV) as an example. An exhaustive investigation on the efficiency boundaries for V_{blk} with varying grid voltage and operating powers is beyond the scope of the present work.

V_{blk} can independently effect the ΔV. For example, in [16], it is shown that as N increases, the local part of ΔV decreases, but this trend is valid only upto a certain number of SMs. Nevertheless, it should be kept in mind that the capacitor voltage ripple maybe inherently lower for an MMC with higher number of SMs. Trade-offs for optimal selection of N related to other degrees of freedom are discussed in subsequent subsections.

C. Reliability Factors (F_{rel})

The degree of freedom in reliability (F_{rel}) involves two factors. The first is the safety factor (S_{f}) that governs voltage limit for safe switching of IGBT (0.65-0.75) as well as the average voltage (0.5-0.65) with respect to reliability due to cosmic ray [4], [19]. In Section III, it is shown that a careful selection of S_{f} and C_{arm} can minimize the minimum required number of SMs for the specific blocking voltage class. This is necessary to maximize the utilization of installed semiconductor power. Secondly, the use of redundant SMs to improve the overall converter reliability is important [20]. In this paper, it is discussed that while higher number of redundant SMs are necessary as number of components increase, integral increase in N ensures that the penalty in terms of cost and mass density is greater if IGBTs of higher V_{blk} are used, particularly for medium voltage level.

D. Inductance (L_{conv})

The required converter inductance L_{conv} has three important components as described in (1),

$$L_{\text{conv}} = L_{\text{ac,phase}} + L_{\text{filter}} + \frac{L_{\text{arm}}}{2} \tag{1}$$

The phase inductance $L_{\text{ac,phase}}$ appears at the point of common coupling (PCC) where the MMC is connected with the ac grid. In case an isolating transformer is used, $L_{\text{ac,phase}}$ can incorporate the transformer's leakage inductance as discussed in [17]. More importantly, the magnitude of $L_{\text{ac,phase}}$ limits the rate of rise of surge currents when the ac grid feeds the dc link faults in a half bridge topology [21]. L_{arm} is

designed to suppress the frequency components of circulating currents between the MMC phase arms and limit the capacitor discharge currents during dc link faults [22]. An interesting insight on resonance circuit in the half bridge MMC associates L_{arm} with C_{arm} [23]. The filter requirements influence the sizing of L_{filter} as a trade-off with effective frequency for the necessary harmonic mitigation. The association between L_{filter} and N is, therefore, necessary to account for the efficiency and size trade-off [5]. However, since the component of L_{conv} that is independent of N in half bridge MMC ([17], [22], [23]) also contributes towards the performance characteristics, an increase in N may not necessarily imply a strong variation in the final inductance required as suggested in [5]. The subject of these trade-offs within the power and harmonic constraints on ripple current Δi are not dealt with in this paper.

E. Control Aspects (cntr)

Switching frequency f_{sw} influences the synthesized power quality as a trade-off between the required filter inductance and the converter efficiency. For cascaded cells, the effective frequency for the same switching frequency and Δi improves as the square of N for the same filter inductance requirements [5], [24]. Furthermore, it was shown in [16] that as the switching frequency increases, the local part of ΔV decreases for the same N. Thus, the ideal choice of f_{sw} must consider the combined influence on ΔV, N and Δi while considering the efficiency-size trade-off.

Different modulation techniques can be used for the MMC operation [25]. In [26], it was shown that different switching strategies can have different efficiency under similar operating conditions. Furthermore, in [16] it was shown that these can have different impact on ΔV for the same N and f_{sw}. Therefore, the choice of the switching strategy is intimately tied to the efficiency and sizing trade-offs relevant to the optimal choice of f_{sw}, N and ΔV.

III. Required Number of Submodules

The design trade-offs in this paper are shown specifically for a 10 kV r.m.s line-to-line medium voltage ac grid ($v_{\text{ll,rms}}$). Correspondingly, v_{d} is fixed at 16.33 kV based on the empirical study presented in [27] comparing the cable insulation performance under ac and dc voltages. The relationship between the MMC dc link voltage with $v_{\text{ll,rms}}$ is shown in (2).

$$v_{\text{d}} = 2.\frac{\sqrt{2}.v_{\text{ll,rms}}}{m.\sqrt{3}} \tag{2}$$

Here, the modulation index m is considered as 1. For the MMC to function properly within its PQ limits, third harmonic injection can be used [15], giving 15 % margin in operation. The minimum number of submodules (N_{min}) is given by (3),

$$N_{\text{min}} = ceil\left(\frac{k_{\text{max}} v_{\text{d}}}{S_{\text{f}} V_{\text{blk}}}\right) \tag{3}$$

The factor k_{max} ensures that the instantaneous value of capacitor voltage is never greater than $\frac{k_{\text{max}} v_{\text{d}}}{N}$ [15]. S_{f} is in accordance to the voltage limit for safe switching of IGBT [4]. The minimum required SM capacitance decreases with increasing k_{max} for the specified rated power but the consequent semiconductor requirement increases. Based on this trade-off, N_{min} increases with k_{max} for the specified V_{blk}. Considering the market available values of T_1 and T_2 from [28], the possible choices of blocking voltage class explored are 1.2 kV (FF450R12ME4), 1.7 kV (FF450R12ME4), 3.3 kV (FF450R33TE3), 4.5 kV (FZ800R45KL3) and 6.5 kV (FZ500R65KE3). In Fig. 3, N_{min} for different V_{blk} are shown for varying k_{max} and S_{f}.

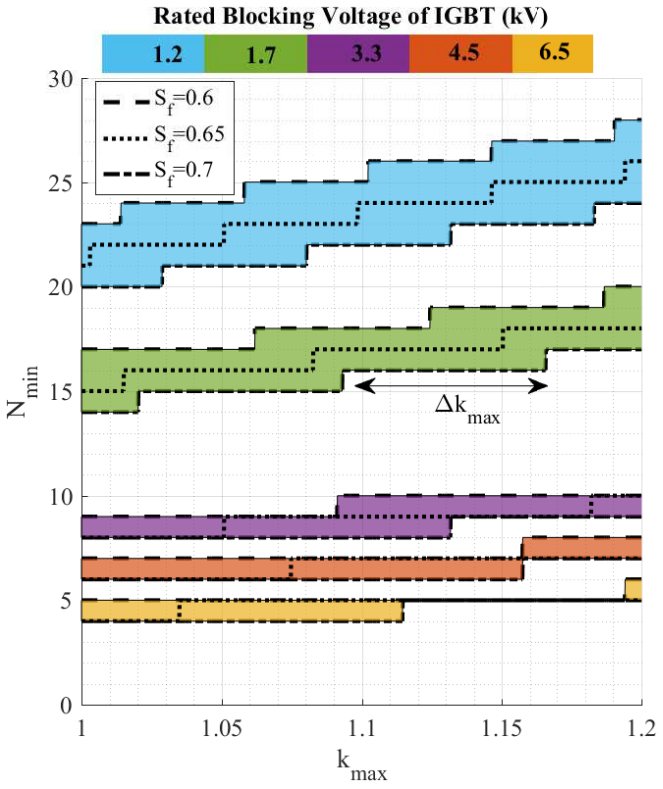

Fig. 3: Minimum required submodules (N_{min}) for different blocking voltage classes (V_{blk}) with varying capacitor voltage ripple factor (k_{max}) and safety factor (S_{f}).

It can be observed that with an integral increase in N_{min}, there is a range of possible k_{max} for the specified S_{f} at a given V_{blk}. The width (Δk_{max}) of this range governs the utilization of the installed semiconductor. Ideally, the S_{f} and k_{max} should be chosen such that Δk_{max} is fully utilized. While the former influences the reliability, the latter influences the size and cost of the converter; and because the Δk_{max} increases proportionally with V_{blk}, the impact of this trade-off is correspondingly more significant. For example, in [5], S_{f} was varied to improve utilization. As a result the lower rated switches had 5-10 % higher S_{f} as compared to 3.3 kV. This difference can be minimized using k_{max} to give power density improvement, particularly when converters have high operating power (required capacitance being directly proportional to the converter power [15]).

The total installed semiconductor power $S_{\text{installed}}$ of the converter, given by (4), is used as an indicator for the costs.

$$S_{\text{installed}} = 6 * 2 * N * V_{\text{blk}} * I_{\text{r,IGBT}} \tag{4}$$

The factor of '6' comes from the six arms of a three phase implementation and the factor 2 is due to the number of IGBT switches per half bridge submodule. Fig. 4 shows the $S_{\text{installed}}$ corresponding to N_{min} for different V_{blk} and rated switch current $I_{\text{r,IGBT}}$ of 450 A with varying k_{max} and normalized with the base power of 10 MVA. The observation supports the intuitive understanding that a unit increment in N_{min} has a higher impact on $S_{\text{installed}}$ (thus cost & size) with higher V_{blk}.

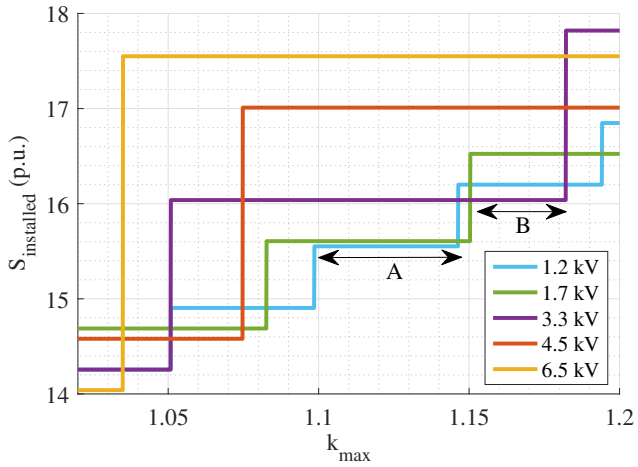

Fig. 4: Total installed semiconductor power for different IGBT blocking voltage class with varying voltage ripple factor.

For example in region A, $S_{\text{installed}}$ for the 1.7 kV IGBT is almost 12 % lower than that with 6.5 kV IGBT and the lowest for 1.2 kV IGBT. The difference is halved in region B while 3.3 kV switch has the lowest $S_{\text{installed}}$.

For medium voltage applications, this disproportionate increase in installed power to an unit increment in N should be considered while evaluating the various trade-offs involved in the design choices for the MMC. This is even more significant when considering the redundancy requirements. It is valid that with lower V_{blk}, the number of components increase and therefore, greater redundancy is require to improve the system reliability. On the other hand, from the stand point of costs and size, a unit increment in N with higher V_{blk} has greater penalty. This can be observed in Fig. 5, where the total number of SMs (N_{tot}) including 10 % redundancy requirements and the corresponding $S_{\text{installed}}$ are shown for varying k_{max}.

The $S_{\text{installed}}$ for 1.2-3.3 kV switches is 15-20 % lower than that for 6.5 kV for k_{max} in the range of 1.1-1.15. In summary, the interplay of reliability, redundancy and energy storage should be carefully compared to cost and size indicators before choosing the blocking voltage class.

IV. Converter Losses

This section describes the MMC conduction and switching losses for different switch ratings considered in this paper. A good basis for the steady state loss modelling of MMC is provided in [29]–[32].

A. Conduction Losses

The IGBT output characteristics and the diode forward characteristics governing the conduction losses for different

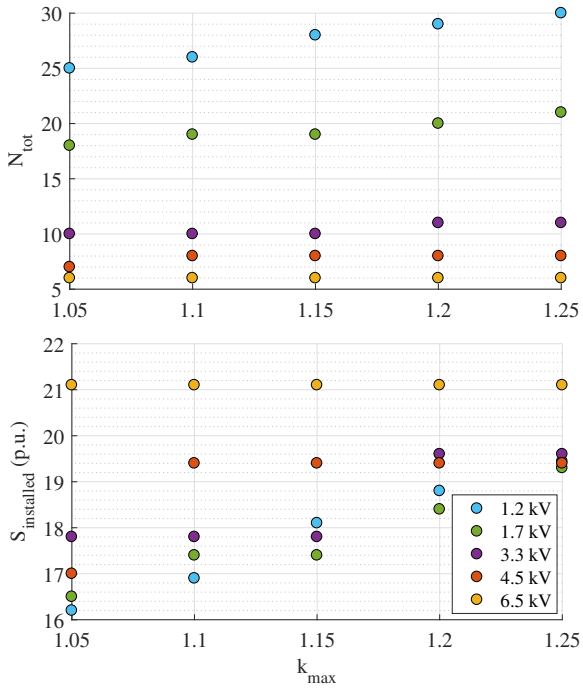

Fig. 5: Variation in (a) Total number of submodules (b) Installed semiconductor power with energy storage requirements for different submodule switch ratings including redundancy requirements with k_{max}.

V_{blk} at junction temperature of 125 °C is shown in Fig. 6 and Fig. 7 respectively.

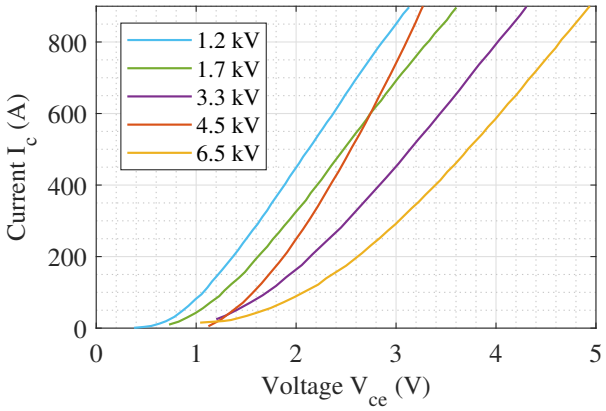

Fig. 6: IGBT output characteristics for different blocking voltages at 125 °C from the datasheets [28].

In general, it can be seen that the voltage drop across these devices increases with V_{blk} for the same conduction current. The outlier is 4.5 kV because a higher switch current rating was selected as compared to the other devices. This was because the manufacturer [28] did not offer the specific current rating for this voltage level. On the other hand, since N increases with decreasing V_{blk}, the cumulative conduction losses can be higher for lower blocking voltages. In order to compute the conduction losses, it is necessary to establish

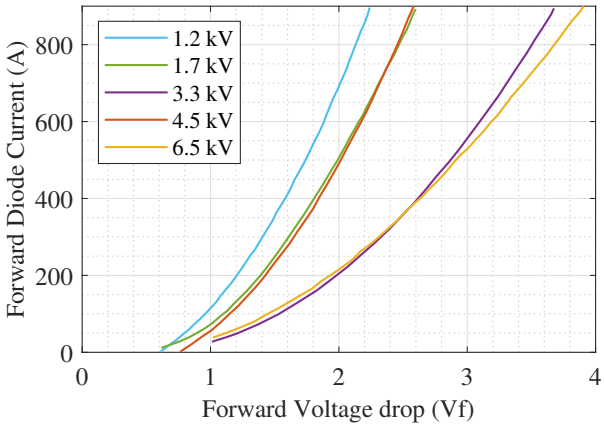

Fig. 7: Diode forward characteristics for different blocking voltages at 125 °C from the datasheets [28].

which power electronic component of the SM is conducting at any given instant of operation [29]. Fig. 8 (a) and (b) show that with positive arm current, the diode D_1 conducts when the SM is inserted, while IGBT T_2 conducts when the SM is bypassed. Similarly, Fig. 8 (c) and (d) depict that when arm current is negative, IGBT T_1 conducts in inserted while diode D_2 conducts in bypass state.

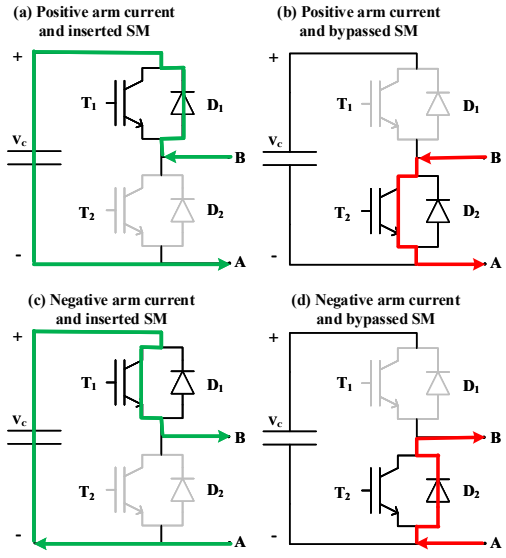

Fig. 8: Current Flow in inserted/bypassed SMs for different arm current directions.

Based on the current flow in SM devices, the instantaneous total upper arm conduction losses corresponding to the active IGBTs ($P^{\Sigma}_{\text{cond,u,T}}$) and active diodes ($P^{\Sigma}_{\text{cond,u,D}}$) in one fundamental time period T_{f} are given by (5) and (6) respectively. Similar equations can be written for the lower arm conduction losses.

$$P^{\Sigma}_{\text{cond,u,T}} = \begin{cases} \frac{1}{T_{\text{f}}} \int_0^{T_{\text{f}}} (N - n_{\text{u}}) \cdot V_{\text{ce}} \cdot i_{\text{u}} \cdot dt & ; \text{if } i_{\text{u}} \geq 0 \\ \frac{1}{T_{\text{f}}} \int_0^{T_{\text{f}}} n_{\text{u}} \cdot V_{\text{ce}} \cdot i_{\text{u}} \cdot dt & ; \text{if } i_{\text{u}} < 0 \end{cases} \tag{5}$$

$$P^{\Sigma}_{\text{cond,u,D}} = \begin{cases} \frac{1}{T_{\text{f}}} \int_0^{T_{\text{f}}} n_{\text{u}} \cdot V_{\text{f}} \cdot i_{\text{u}} \cdot dt & ; \text{if } i_{\text{u}} \geq 0 \\ \frac{1}{T_{\text{f}}} \int_0^{T_{\text{f}}} (N - n_{\text{u}}) \cdot V_{\text{f}} \cdot i_{\text{u}} \cdot dt & ; \text{if } i_{\text{u}} < 0 \end{cases} \tag{6}$$

V_{ce} is the voltage drop of the IGBT and V_{f} is the forward voltage drop across the diode while conducting current i_{u} given by (7) under considered operating conditions.

$$i_{\text{u}} = \frac{i_{\text{d}}}{3} + \frac{i_{\text{s,M}}}{2} \tag{7}$$

The instantaneous conduction current dependent voltage drops at 125 $^{\circ}C$ are found using interpolation of data-points in a look-up table obtained from the datasheets provided by the manufacturer [28]. The upper and lower devices in the SM will have unequal power losses, but this aspect is neglected in this analysis. n_{u} is the number of inserted SMs in the upper arm, computed based on the nearest level control (NLC) [33], [34]. Instantaneous insertion indices corresponding to other modulation techniques such as carrier based pulse width modulation can also be used for computation, but this is not the focus of this present paper.

$$n_{\text{u}} = round\left(N * \left(\frac{v_{\text{u}}}{V^{\Sigma}_{\text{cu}}}\right)\right) \tag{8}$$

Here, v_{u} is the inserted upper arm voltage and V^{Σ}_{cu} is the total sum of voltages across all the capacitors of the upper arm. $P^{\Sigma}_{\text{cond,u,T}}$, $P^{\Sigma}_{\text{cond,u,D}}$ and the total instantaneous conduction losses in the upper arm of one phase leg of the MMC for the rated operation of 10 MVA at unity power factor with modulation index of 1 is shown in Fig. 9.

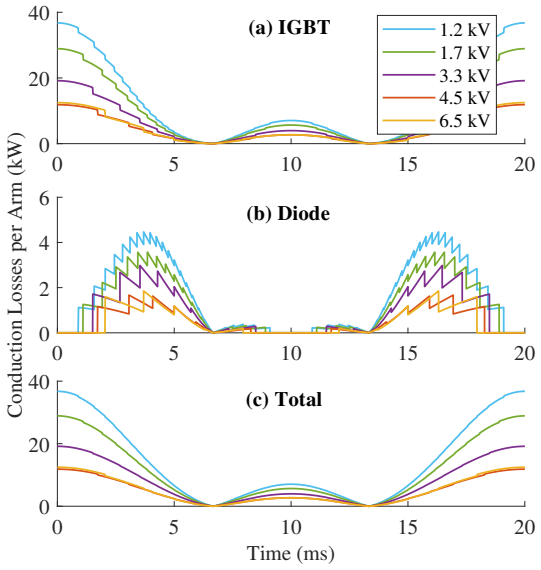

Fig. 9: Instantaneous conduction loss in a single MMC arm for one fundamental period under rated operation for different switch ratings (a) IGBT (b) Diode (c) Total.

The average conduction losses (assuming uniform losses in the top and bottom IGBT devices of the submodules) increase as the V_{blk} decreases.

B. Switching Losses

In order to compute the switching losses, the data for switching energy loss (E) in mJ with respect to the switching currents was extracted from [28]. The diode turn-off losses, IGBT turn-on and turn-off energy for different V_{blk} is shown in Fig. 10, Fig. 11 and Fig. 12 respectively.

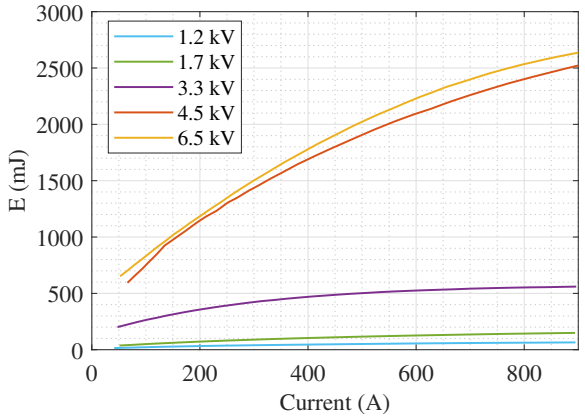

Fig. 10: Diode switching losses for different blocking voltages at 125 °C from the datasheets [28].

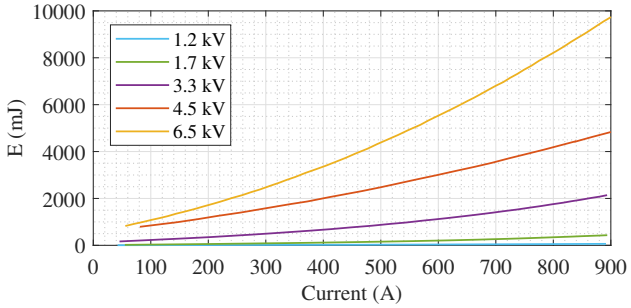

Fig. 11: IGBT turn-on energy loss for different blocking voltages at 125 °C from the datasheets [28].

As expected, it is observed that with higher voltages, the switching energy increases. Furthermore, as N increases, the switching frequency needed to maintain the same harmonic performance reduces. Therefore, the switching losses can be expected to be lower when smaller V_{blk} is selected. To calculate the switching loss, the commutation of specific device (IGBT or Diode) based on the level transition and the direction of the arm current must be known. This is shown in Fig. 13 for a 6-level 6.5 kV IGBT operating with NLC at fundamental switching frequency.

The level transition is +1 if a SM in upper arm inserted and -1 if a upper arm SM is bypassed. Since there are 5 SMs per arm, total number of transitions $N_{\text{transitions}} = 10$ are observed. For the associated arm current direction, the highlighted turn-on and turn-off of devices can be inferred from Fig. 8.

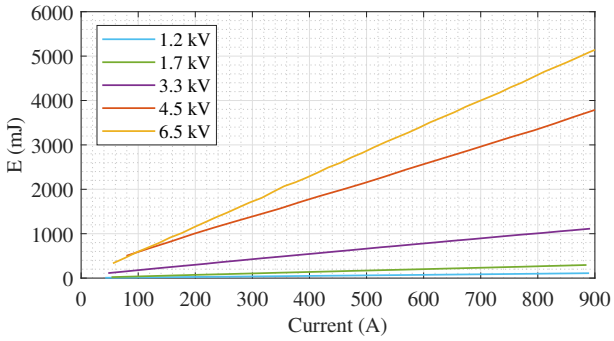

Fig. 12: IGBT turn-off energy loss for different blocking voltages at 125 °C from the datasheets [28].

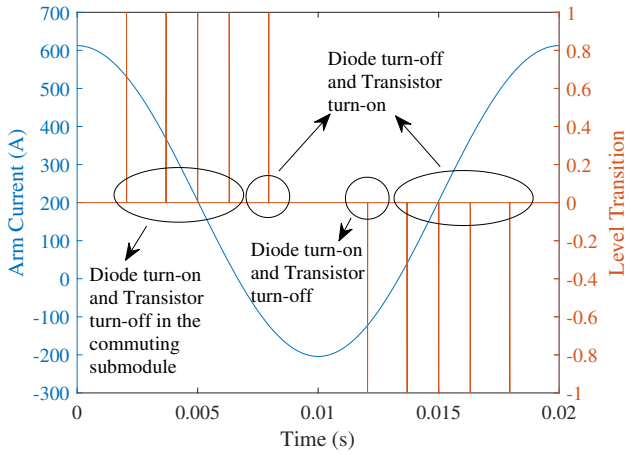

Fig. 13: Commutation of devices based on directions of level transitions and arm current for one fundamental period with 6.5 kV switch based 6-level MMC in steady state operation for NLC at fundamental switching frequency.

The average converter efficiency including both conduction and switching losses, cumulative for all 6 arms of the MMC is shown in Fig. 14 with respect to the effective frequency F_{eff}.

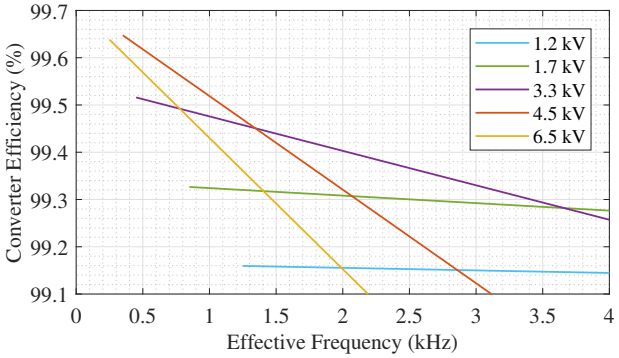

Fig. 14: Total converter efficiency considering both conduction and switching power loss for different IGBT switch voltage rating with respect to effective frequency of operation.

F_{eff} is given by the product of actual switching frequency F_{sw} and N. It can be seen that the crossover from 3.3 kV to 1.7 kV occurs at the F_{eff} of about 3.5 kHz, corresponding to a F_{sw} of 389 Hz for the former and 206 Hz for the latter. As discussed in Section II-E, the optimal value of the F_{eff} for the given V_{blk} is a trade-off between power quality requirements in combination with L_{filter}, the local capacitor voltage ripple and the switching strategy employed. If the fault current limitation requires a certain minimum $L_{\text{ac,phase}}$, this condition could favour a higher V_{blk} in its F_{sw} trade-off with L_{filter}. On the other hand, a reduced N can require a higher F_{sw} to balance the individual SM capacitors, even though this relationship is shown to be less significant above $N = 12$ [16]. Furthermore, minimum switching requirements for capacitor balancing efforts for voltage ripple minimization could set a lower limit on the achievable reduction in F_{sw} with lower V_{blk}. Therefore, the efficiency crossover points depicted in Fig. 14 should be considered in relation to the performance, size and cost before choosing the optimum IGBT voltage rating. These crossover points vary with the operating voltage and power level of the MMC. Such considerations are important, but beyond the scope of this discussion.

V. Conclusions and Future Work

This work emphasizes that the selection of the suitable IGBT switch blocking voltage class is important for medium voltage high power applications of modular multilevel converters. Highlighting that this choice is not straightforward, the various inter-dependencies with respect to capacitor sizing, reliability, inductance requirement, switching frequency and control strategy are identified.

It was shown that as the required switching frequency increases, the IGBTs with lower V_{blk} become more favourable from converter efficiency standpoint. In general, an increase in V_{blk} is almost always accompanied by an increase in required switching frequency in a trade-off with L_{filter} for achieving acceptable power quality. However, this dependence can be limited if N is already high enough to necessitate improvement in the harmonic performance and/or a constant inductance is required for protection needs. Therefore, as a future work, the optimal switching frequency requirement as a function of V_{blk} should be incorporated in the design stage.

Some evidence in the available literature indicates that with lower ac and dc side operating voltages, lower V_{blk} offer greater MMC efficiency. At the same time, an increase in power level favours higher V_{blk}. Mapping the effect of these two factors towards the complete design of a half bridge MMC for medium voltage, high power applications can be an interesting research effort.

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