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A Low-Jitter and Low-Spur Charge-Sampling PLL

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***Abstract*— This article presents a low-jitter and low-spur charge-sampling phase-locked loop (CSPLL). A charge-domain sub-sampling phase detector is introduced to achieve a high phase-detection gain and to reduce the PLL in-band phase noise. Even without employing any power-hungry isolation buffers, the proposed phase detector dramatically suppresses the reference spurs by both minimizing the modulated capacitance seen by the voltage-controlled oscillator (VCO) tank and by reducing the duty cycle of the sampling clock. A 50-μW RF-dividerless frequency-tracking loop is also introduced to lock the CSPLL robustly when the VCO faces a sudden frequency disturbance. Fabricated in a 40-nm CMOS process, the prototype CSPLL occupies a core area of 0.13 mm^2 and synthesizes 9.6-to-12-GHz tones using a 100-MHz reference. At 11.2 GHz, it achieves a reference spur of −77.3 dBc and an RMS jitter of 48.6 fs while consuming 5 mW.**

***Index Terms*— Charge-sampling phase detector (CSPD), charge-sampling phase-locked loop (CSPLL), divider-less frequency-tracking loop (FTL), in-band phase noise (PN), low jitter, reference spur, sub-sampling.**

I. Introduction

PHASE-LOCKED loops (PLLs) with high spectral purity are in great demand for high-performance data converters, optical communication links, wireline, and wireless transceivers. For example, directly digitizing signals via an RF sampling analog-to-digital converter can significantly reduce the system's complexity, power consumption, and cost in macro-cellular base stations and satellite communication systems [1]. However, it imposes stringent requirements on the PLL's power consumption (P_{DC}), phase noise (PN), RMS jitter, and reference spur (S_{REF}). Consequently, significant effort has been made in the last decade to improve PLLs' spectral purity and power efficiency [2]–[31].

A divider-less sub-sampling PLL (SSPLL) based on voltage sampling can achieve low jitter while dissipating low power, as it eliminates the noise of the feedback divider and suppresses the noise of the charge pump and phase detector (PD) due to its high phase-detection gain (K_{PD}) [9]–[18]. Unfortunately, the direct sampling of the voltage-controlled oscillator (VCO) voltage by a low-frequency reference clock (REF) can introduce a high S_{REF} due to the periodic tank-capacitance perturbation, reference clock feedthrough, and charge injection from the sampling switch to the VCO. The periodic switching of the sampling capacitor modulates the VCO's frequency, F_{VCO}, in a similar fashion to the case of binary frequency-shift keying (BFSK), which creates a spur at the reference frequency (F_{REF}) given by

$$S_{REF-BFSK} = 20 \cdot \log_{10}\left[\sin(\pi \cdot D_{REF}) \cdot \frac{N}{2\pi} \cdot \frac{C_{MOD}}{C_{TANK}}\right] \quad (1)$$

where D_{REF} is the reference clock duty cycle, C_{MOD} is the modulated capacitance seen by the VCO tank, and C_{TANK} is the total tank capacitance [10]. S_{REF} can be improved by directly decreasing the sampling capacitor (C_S) [10] to reduce C_{MOD}. However, a small C_S degrades the in-band PN due to the sampling noise, diminishing the benefit of a sub-sampling PD. Hence, a dummy sampler was added in [14] such that the VCO could see a small C_{MOD}. Yet, this approach suffers from the mismatch between these two sampling capacitors, thus limiting S_{REF} to −56 dBc for a 2.2-GHz carrier.

Consequently, to target a low S_{REF} (e.g., <−70 dBc) through lowering C_{MOD}, an isolation buffer with either inductive or resistive load is typically employed between VCO and sampler [10], [20]. However, the buffer operates at F_{VCO}, resulting in a substantial penalty in the PLL's area, P_{DC}, and jitter. Moreover, the rise and fall times of the signal at the sampler input may be reduced, shrinking the linear phase-detection range of the PD. Hence, a power-hungry slope generator is added in [10] and [20] to realize a triangular-like waveform for the sampler.

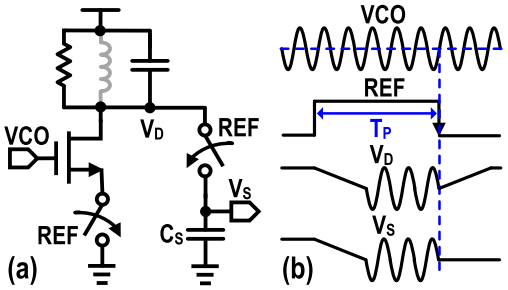

Fig. 1. (a) Schematic and (b) conceptual waveforms of a voltage-sampling PD using a power-gated isolation buffer.

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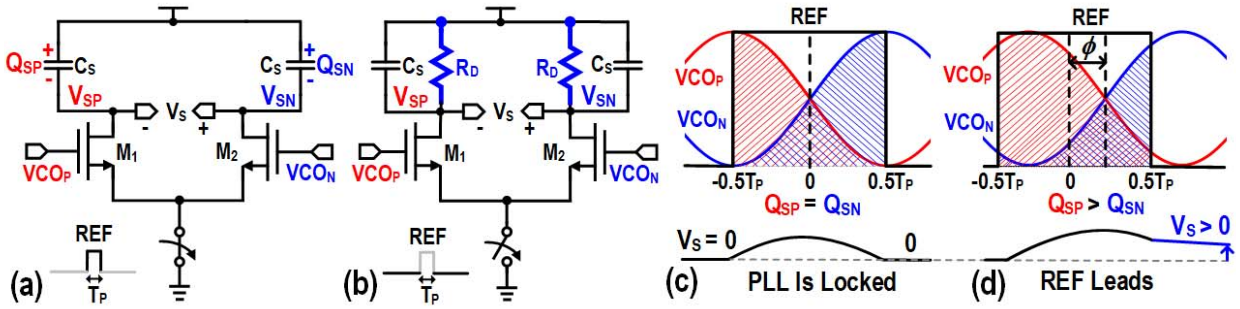

Fig. 2. Simplified schematic of the proposed CSPD when REF is (a) high and (b) low; its conceptual waveforms (c) without and (d) with a phase error.

Power-gated operation of the isolation buffer, as shown in Fig. 1(a), reduces D_{REF}, thus alleviating S_{REF} and $\mathrm{P_{DC}}$ overhead [12], [13]. However, the REF pulsewidth (T_P) cannot be shorter than a few cycles (e.g., 5–10) of the VCO period (T_{VCO}) to ensure that the resonant buffer reaches its steady-state amplitude before the sampling instants. In the case of the resistive buffer, the common-mode (CM) settling time sets the shortest possible T_P, thus limiting S_{REF} and $\mathrm{P_{DC}}$ improvement. Moreover, to provide a low-noise signal amplification at F_{VCO}, the buffer's transistors must be wide enough to draw a relatively large current during the ON-state. Due to the use of wide transistors, the buffer's input capacitance significantly changes when the devices enter saturation from the cutoff region and vice versa. Therefore, the VCO experiences a large C_{MOD}, thus limiting the PLL spur performance. Besides, the clock feedthrough and charge injection issues still exist through the large gate parasitic capacitance of the isolation buffer. Consequently, due to the constraints on the minimum achievable C_{MOD} and D_{REF}, even by using a gated isolation buffer in [13], S_{REF} and figure of merit (FOM) are still limited to -67 dBc and -256 dB at 2.4-GHz carrier frequency, respectively.

To improve on those limitations, we propose a charge-sampling PLL (CSPLL), first introduced in [19], whose phase-detection mechanism is based on a windowed current integration. Without exploiting any isolation buffers, the proposed CSPLL achieves -77-dBc S_{REF} by simultaneously minimizing C_{MOD} and D_{REF}. It also offers a high K_{PD} even without requiring an RF bandwidth (BW) at the sampler output, resulting in -259-dB jitter-power FOM. Furthermore, a highly digital frequency-tracking loop (FTL) without the use of any RF dividers is proposed to guarantee the PLL's robust operation.

This article is organized as follows. Section II focuses on the detailed theoretical analysis and design considerations of the charge-sampling PD (CSPD). Section III describes the complete CSPLL architecture and FTL operation. The circuit implementation of critical building blocks of the CSPLL is shown in Section IV. Section V presents the measurement results, while Section VI wraps up this article with conclusions.

II. Charge-Sampling PD

A. Voltage Sampling Versus Charge Sampling

Voltage-sampling phase detectors (VSPDs) capture the instantaneous input voltage when the sampling switch is turned off [see Fig. 1(b)]. Their ideal locking point is when the VCO zero crossings occur at the REF falling edge [9]. The VSPD phase-detection gain is directly proportional to the voltage swing at the sampler's output, thus demanding a high power consumption for both the isolation buffer and the sampling circuit for realizing an RF BW close to F_{VCO}. On the other hand, charge sampling is based on integrating an input current on a capacitor over a fixed time window and taking the resulting voltage as the sampler output. It is a well-known technique to reduce the sampling error caused by the clock jitter in high-speed sample-and-hold amplifiers [32], [33]. It is also widely used in software-defined radio receivers due to its built-in anti-aliasing and reconfigurability [34]–[37]. However, the interesting properties of the charge-sampling concept have not yet been exploited in the PLL design. This article shows that the fundamental differences in the voltage sampling and charge-sampling operation profoundly impact the PLL performance in terms of locking point, K_{PD}, S_{REF}, PN, and $\mathrm{P_{DC}}$.

B. Locking Point

Fig. 2 shows the schematic and conceptual waveforms of a CSPD. The transconductors ($M_{1,2}$) convert the VCO's output voltage $\mathrm{VCO}_P - \mathrm{VCO}_N = 2A_{\mathrm{VCO}} \cdot \sin(\omega_{\mathrm{VCO}} t + \phi)$ into a differential RF current, realizing a charge difference on C_S when REF is high. If the VCO zero crossings occur at the center of the REF pulse, $M_{1,2}$ charge C_S during the first half of the REF pulse (i.e., from $-0.5\ T_P$ to 0) and discharge C_S during the second half of the REF pulse (i.e., from 0 to $0.5\ T_P$). Consequently, the sampled net charge difference $Q_S = (Q_{\mathrm{SP}} - Q_{\mathrm{SN}})$ is zero, which is represented by the equaled shaded blue and red areas in Fig. 2(c). Hence, the sampled differential voltage V_S ($=V_{\mathrm{SN}} - V_{\mathrm{SP}}$) remains zero after the phase comparison, corresponding to the ideal locking condition of the PLL. If there is any phase error (ϕ), the CSPD converts it into a non-zero Q_S and V_S, as shown in Fig. 2(d), thus indicating that the PLL is not locked. Consequently, similarly as in sub-sampling PDs, the CSPD works without using RF dividers if $N = F_{\mathrm{VCO}}/F_{\mathrm{REF}}$ is an integer number.

When REF is low, V_S is partially discharged via load resistors (R_D) and C_S since $M_{1,2}$ are turned off. This peculiar discharging process is crucial for the CSPD's operation, which will be discussed in Section II-C.

C. Phase-Detection Gain

Fig. 3 shows the time-domain differential-mode model of the CSPD, where a periodic sampling function [$p(t)$] samples

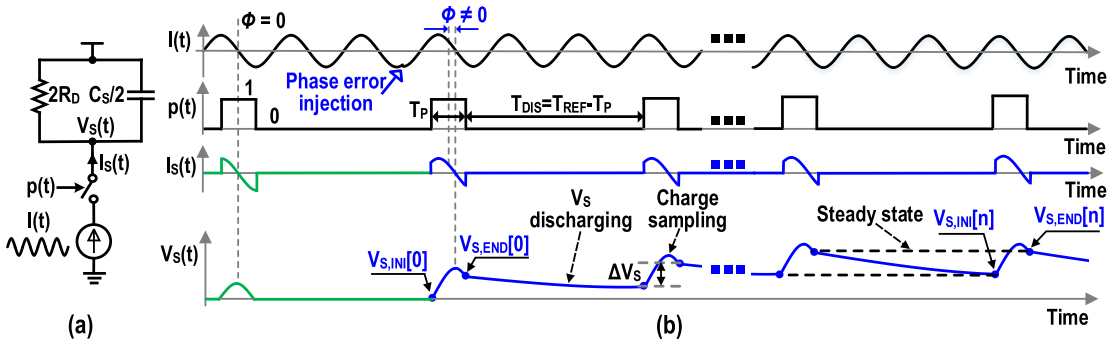

Fig. 3. (a) Time-domain differential-mode model of the CSPD. (b) Waveforms of the CSPD before and after applying a phase error to the VCO.

a continuous-time RF current $I(t) = G_M A_{\rm VCO} \sin(\omega_{\rm VCO} t + \phi)$. This results in a train of discrete-time narrow current pulses

$$I_S(t) = G_M A_{\rm VCO} \sin(\omega_{\rm VCO} t + \phi) \cdot p(t) \tag{2}$$

where G_M is the large-signal transconductance of $M_{1,2}$ and

$$p(t) = \begin{cases} 1, & \dfrac{-T_P}{2} + n \cdot T_{\rm REF} \le t \le \dfrac{T_P}{2} + n \cdot T_{\rm REF} \\ 0, & \text{otherwise.} \end{cases} \tag{3}$$

Due to the phase error (ϕ) between the VCO zero crossings and middle of the REF pulse [see Fig. 3(b)], V_S increases by[1]

$$\begin{aligned} \Delta V_S &= V_{S,\rm END}[n] - V_{S,\rm INI}[n] = \frac{2}{C_S} \int_{-0.5T_P}^{0.5T_P} I_S(t) dt \\ &= \frac{4 G_M A_{\rm VCO}}{\omega_{\rm VCO} C_S} \cdot \sin(0.5\omega_{\rm VCO} T_P) \cdot \sin(\phi) \end{aligned} \tag{4}$$

during each phase comparison, where $V_{S,\rm INI}[n]$ and $V_{S,\rm END}[n]$ represent the voltages of V_S at the beginning and end of the charge sampling, respectively, at the nth reference clock cycle. Following the phase comparison, $p(t)$ becomes 0 for a duration of $T_{\rm DIS} = T_{\rm REF} - T_P$. $V_{S,\rm END}[n]$ is exponentially discharged through R_D and C_S and brings $V_{S,\rm INI}$ to

$$V_{S,\rm INI}[n+1] = V_{S,\rm END}[n] \cdot \exp^{-k} \tag{5}$$

at the next cycle, where k is defined as $T_{\rm DIS}/(R_D C_S)$. By combining (4) and (5), $V_{S,\rm END}[n]$ can be calculated as

$$V_{S,\rm END}[n] = \Delta V_S \sum_{k=0}^{n-1} \exp^{-n \cdot k} \tag{6}$$

and it reaches a steady-state value given by $V_{S,\rm END}[n]|_{\rm st} = \Delta V_S / (1 - \exp^{-k})$.

The unique discharging process of V_S is critical for the proper operation of a CSPD. Let us consider two extreme cases here. In the first one, k approaches 0 by removing R_D. Therefore, the sampled charge is accumulated, and CSPD resembles an ideal integrator, exhibiting a pole at dc and causing instability issues in the PLL. In the second case, if k is chosen to be $\sim N$ by picking a small R_D and C_S, which is a typical case in a VSPD using a power-gated isolation buffer [12], [13], the detected V_S will rapidly return to zero, thus destroying the PD's memory and requiring a hold switch at the sampler output. In this design, k is designed to be $\sim$0.4, so as to satisfy the PLL's required phase margin and simultaneously guarantee the PD's charge-sampling operation. As a result, CSPD resembles a leaky phase integrator with a pole location determined by k. We will discuss this further in Section III.

In the steady state, V_S becomes a periodic function of $T_{\rm REF}$, and its average value can be estimated by[2]

$$\begin{aligned} \overline{V_S} &\approx \frac{1}{T_{\rm REF}} \int_{0.5T_P}^{T_{\rm REF} - 0.5T_P} V_{S,\rm END}[n]|_{\rm st} \cdot \exp^{\frac{-t}{R_D C_S}} dt \\ &\approx \frac{2 G_M A_{\rm VCO} R_D}{N\pi} \cdot \sin(0.5\omega_{\rm VCO} T_P) \cdot \sin(\phi). \end{aligned} \tag{7}$$

$K_{\rm PD}$ is then defined as $\overline{V_S}/\phi$ and can be calculated by

$$K_{\rm PD} = \frac{2 G_M A_{\rm VCO} R_D}{N\pi} \cdot \sin(0.5\omega_{\rm VCO} T_P) \cdot \frac{\sin(\phi)}{\phi}. \tag{8}$$

We can inspect the validity of the above equation by using an alternative method. The phase error modifies the shape of the sampled current pulses [see Fig. 3(b)] and creates a non-zero dc current ($\overline{I_S}$). Notice that $\overline{I_S}$ must flow into the resistive load R_D, thus creating a dc voltage given by

$$\begin{aligned} \overline{V_S} &= \frac{2R_D}{T_{\rm REF}} \cdot \int_{-0.5T_P}^{T_{\rm REF} - 0.5T_P} G_M A_{\rm VCO} \sin(\omega t + \phi) dt \\ &= \frac{2 G_M A_{\rm VCO} R_D}{N\pi} \cdot \sin(0.5\omega_{\rm VCO} T_P) \cdot \sin(\phi). \end{aligned} \tag{9}$$

Interestingly, $K_{\rm PD}$ is not a function of C_S. This indicates that an arbitrarily large C_S can be used without sacrificing $K_{\rm PD}$. The complete phase-detection gain by considering the PD delay can be estimated by $K_{\rm PD}(s) \approx K_{\rm PD}/(1 + s \cdot R_D C_S)$.

Notice that, unlike a VSPD, $K_{\rm PD}$ of a CSPD is a function of both T_P and N. At first glance, it seems that $K_{\rm PD}$ of a CSPD with $N\pi$ factor in the denominator is much smaller than that of a VSPD (i.e., $K_{\rm PDVS} \approx 2 G_M A_{\rm VCO} R_D$). However, the reduction of $K_{\rm PD}$ by $N\pi$ can be easily compensated by choosing a large R_D. Note that the finite output impedance of $M_{1,2}$ ($r_{\rm ds}$) has a marginal impact on $K_{\rm PD}$, as long as $1/(\omega_{\rm VCO} C_S) \ll r_{\rm ds}$. This condition can be easily satisfied in a CSPD by choosing a large C_S. Hence, without compromising $K_{\rm PD}$, a minimum channel length device can be used for $M_{1,2}$ to minimize $C_{\rm MOD}$ and to improve $S_{\rm REF}$. In contrast to the CSPD, $r_{\rm ds}$ significantly reduces $K_{\rm PDVS}$ in deep-submicrometer technologies due to short-channel effects, enforcing the use of long channel length devices and thus degrading $S_{\rm REF}$.

[1]Here, we assume that $1/(C_S \omega_{\rm VCO}) \ll R_D$. Also, it will be shown later that this assumption is valid for a CSPD.

[2]This approximation is valid since $T_P \ll T_{\rm DIS}$ in a CSPD.

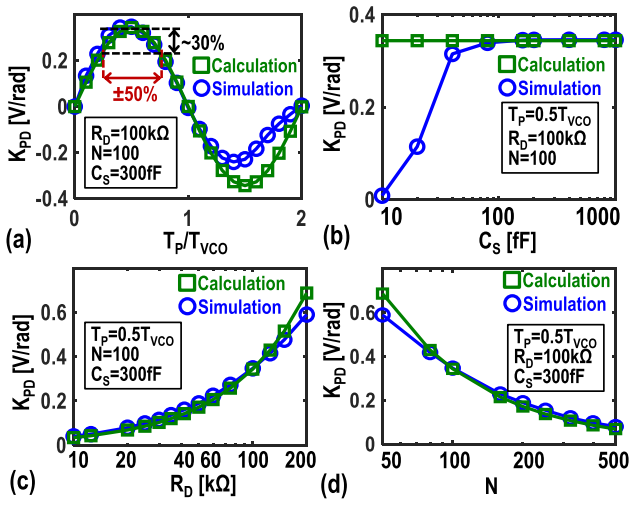

Fig. 4. Simulated and calculated K_{PD} as a function of (a) T_P, (b) C_S, (c) R_D, and (d) N.

Due to the integration operation, K_{PD} is a periodic function of T_P and reaches its maximum at $T_P = 0.5\ T_{VCO}$. Using $T_P \gg 0.5\ T_{VCO}$ does not improve K_{PD} but degrades the reference spur. Notice that, due to the sinusoidal dependence of K_{PD} to T_P, a ±50% variation of T_P around its optimum point only reduces K_{PD} by 30%, suggesting that CSPD is robust against process, voltage, and temperature (PVT) variations. In this design, K_{PD} of ~0.35 V/rad is achieved by choosing $R_D = 100$ kΩ, $(W/L)_{1,2} = 2\ \mu$m/40 nm, $G_M = 1.2$ mS, and $N = 100$. Note that the achieved gain is sufficiently high to suppress the noise of PLL loop components. Further increasing K_{PD} would require a pulser circuit to reduce the loop gain (LG) [9], complicating the design. Fig. 4 shows the simulated and calculated K_{PD} versus various parameters of the CSPD. Although there are some deviations especially if a large T_P and a small C_S are used, simulations match the presented theory very well. The discrepancies will be justified in Section II-D by investigating the CM behavior of the CSPD.

D. CM Settling

Fig. 5 shows the time-domain CM model and waveforms of the CSPD, where the sampling function $p(t)$ is used to sample a constant current. Consequently, a train of current pulses with a fixed amplitude of $G_M V_{DC}$ and a duration of T_P is pumped into R_D and C_S irrespective of the phase error, where V_{DC} is $M_{1,2}$ gate-source bias voltage. This results in a CM voltage drop of $\Delta V_{CM} = G_M V_{DC} T_P / C_S$ when $p(t)$ is 1 (i.e., during the phase comparison). When $p(t)$ is 0, the output CM voltage (V_{CM}) is exponentially precharged to a high level such that $M_{1,2}$ can be turned on very fast (i.e., <15 ps), only limited by the ON-resistance and parasitic capacitance of the tail switch. Note that CSPD CM settles to its steady-state right after the power-up and follows the same pattern regardless of the phase error variations.

K_{PD} could be potentially compromised if $M_{1,2}$ enter the triode region, as shown in Fig. 4(a) and (b), where the simulated K_{PD} deviates from its theoretical value if a larger T_P or a smaller C_S is used. Therefore, a large C_S and very narrow pulsewidth for the REF must be utilized to maintain a high output CM voltage and keep $M_{1,2}$ in saturation during each phase comparison.[3]

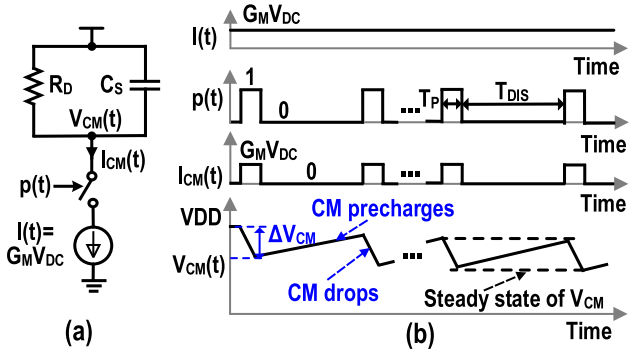

Fig. 5. (a) Time-domain CM model of the CSPD. (b) CM waveforms of the CSPD.

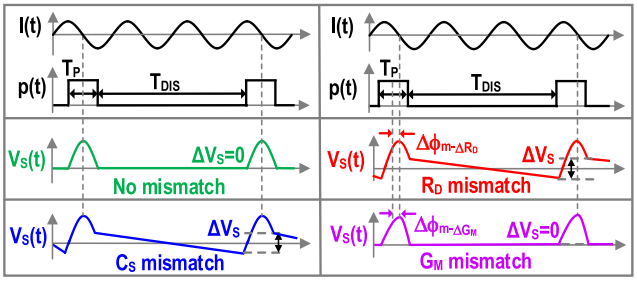

Fig. 6. Conceptual waveforms of the CSPD due to C_S, R_D, and transistor mismatch.

The current consumption of the CSPD is obtained by averaging the CM current over one reference period

$$\overline{I_{CM}} = \frac{2}{T_{REF}} \int_{-\frac{T_P}{2}}^{T_{REF}-\frac{T_P}{2}} G_M V_{DC} dt = \frac{2 G_M V_{DC} T_P}{T_{REF}}. \quad (10)$$

By considering $V_{DC} = 0.6$ V, $(W/L)_{1,2} = 2\ \mu$m/40 nm, and $T_P = 0.3 T_{VCO}$, the CSPD consumes less than 5 μA. Consequently, a low power consumption and a high K_{PD} can be simultaneously achieved by having a small T_P (e.g., 0.3 T_{VCO}) in the proposed CSPD. On the contrary, to deliver a maximum voltage gain, a VSPD needs a large T_P for proper CM settling of its gated isolation buffer, thus degrading both power consumption and S_{REF}.

E. Mismatch Analysis

1) C_S Mismatch: As discussed earlier, since the averaged differential output of CSPD ($\overline{V_S}$) is not a function of C_S, the locking point and K_{PD} are also not sensitive to the mismatch between the sampling capacitors (ΔC_S). However, due to ΔC_S, even when the phase error is zero, the CSPD's differential output in steady state experiences a voltage jump (ΔV_S) during each phase comparison followed by an exponential voltage change over the discharging phase [see the blue curve in Fig. 6]. This results in a sawtooth ripple in V_S, whose fundamental amplitude is given by

$$A_{rip-\Delta C_S} \approx \frac{\Delta C_S}{C_S} \cdot \frac{\Delta V_{CM}}{\pi}. \quad (11)$$

[3]Interestingly, in contrast to a VSPD, a proper CSPD design always favors a small T_P and a large C_S.

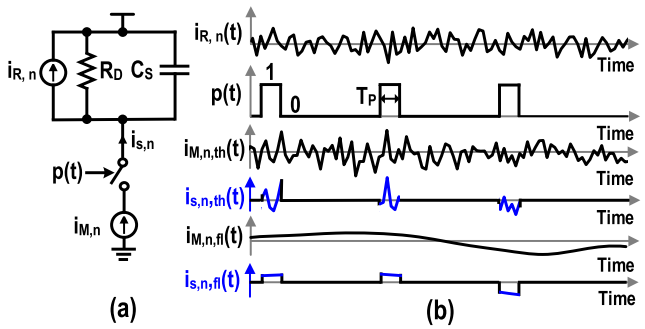

Fig. 7. (a) Half-circuit noise model and (b) time-domain noise waveforms of the CSPD.

The effect of this sawtooth-like ripple on the reference spur will be discussed further in Section III.

2) R_D Mismatch: If the VCO zero crossings occur at the center of the REF pulse, then a non-zero $\overline{V_S}$ ($=G_M V_{\rm DC}\Delta R_D T_P/T_{\rm REF}$) will be created due to the mismatch between the CSPD load resistors (ΔR_D), indicating that the PLL is not locked. The loop must therefore develop a phase offset of

$$\Delta\phi_{m-\Delta R_D} \approx \frac{\Delta R_D}{R_D}\cdot\frac{N\pi T_P}{2\sin(0.5\omega_{\rm VCO}T_P)T_{\rm REF}} \tag{12}$$

to compensate for ΔR_D and realize $\overline{V_S}=0$ in the locked state. Even considering a pessimistic $\Delta R_D/R_D = 10\%$, $\Delta\phi_{m-\Delta R_D}$ would be $<4^\circ$ with almost no penalty on $K_{\rm PD}$. Nevertheless, due to this offset, a sawtooth ripple will show up in V_S again [see the red curve in Fig. 6], whose fundamental amplitude can be found by

$$A_{{\rm rip}-\Delta R_D} \approx 4G_M A_{\rm VCO}\cdot\sin\left(\Delta\phi_{m-\Delta R_D}\right)\cdot\frac{\sin(0.5\omega_{\rm VCO}T_P)}{\pi\omega_{\rm VCO}C_S}. \tag{13}$$

The impact of this ripple on $S_{\rm REF}$ will be quantified in Section III.

3) $M_{1,2}$ Mismatch: Similar to the R_D mismatch, the loop must create a phase offset to compensate for the mismatch between the transconductance of the transistors (ΔG_M), as shown in Fig. 6. The phase offset can be estimated by

$$\Delta\phi_{m-\Delta G_M} \approx \frac{\Delta G_M}{G_M}\cdot\frac{N\pi T_P}{2\sin(0.5\omega_{\rm VCO}T_P)T_{\rm REF}}. \tag{14}$$

By considering $\Delta G_M/G_M = 50\%$, $\Delta\phi_{m-\Delta G_M}$ is $\sim 16.9^\circ$, degrading $K_{\rm PD}$ by only $\sim$0.4 dB. Fortunately, since C_S and R_D are matched, there is no sawtooth ripple in V_S at the steady state [see the pink curve in Fig. 6]; hence, $S_{\rm REF}$ is not affected by ΔG_M.

F. Phase-Noise Analysis

1) Noise of R_D: Since R_D is always connected to the CSPD output, the effective power spectral density (PSD) of its noise current can be simply expressed as $\overline{i^2_{s,R,n}}/\Delta f = 4KT/R_D$. Note that this expression slightly overestimates R_D noise when transferred to the CSPD output, as its noise current partially flows to the ground due to the finite $r_{\rm ds}$ of $M_{1,2}$.

2) Thermal Noise of $M_{1,2}$: As shown in Fig. 7, $M_{1,2}$ contribute noise only when the REF is high by injecting a train of narrow noise current pulses [$i_{s,n}(t) = i_{M,n}(t)\cdot p(t)$] into R_D and C_S. Suppose that $i_{M,n}(t)$ contains only thermal noise [$i_{M,n,{\rm th}}(t)$] with a variance of $i^2_{M,n,{\rm th}}$. The resulting $i_{s,n}(t)$ is a white and cyclostationary process, and its auto-correlation function can be expressed as

$$R_{i_{s,n}}(t, t+\tau) = i^2_{M,n,{\rm th}}\cdot\delta(\tau)\cdot p(t+\tau)\cdot p(t) \tag{15}$$

which is a function of both t and the lag τ. The $i_{s,n}(t)$ PSD is obtained by averaging $R_{i_{s,n}}(t, t+\tau)$ over one reference period and taking the Fourier transformation, and it is given by

$$\begin{aligned}\frac{\overline{i^2_{s,n,{\rm th}}}}{\Delta f} &= \int_{-\infty}^{+\infty}\exp^{-j2\pi f\tau}\int_{-\frac{T_P}{2}}^{T_{\rm REF}-\frac{T_P}{2}}\frac{R_{i_{s,n}}(t, t+\tau)}{T_{\rm REF}}dtd\tau \\ &= i^2_{M,n,{\rm th}}\cdot\frac{T_P}{T_{\rm REF}}.\end{aligned} \tag{16}$$

As expected, a smaller T_P also reduces the $M_{1,2}$ contribution to the PLL total PN.

3) Flicker Noise of $M_{1,2}$: Since the flicker noise of $M_{1,2}$ [$i_{M,n,{\rm fl}}(t)$] is a slow process and varies little during the charge-sampling window, it can be assumed that its time average determines the root mean square of the flicker fluctuations [38]. Consequently, the output flicker noise current can be modeled as an impulse train with a height of $T_P/T_{\rm REF}\cdot i_{M,n,{\rm fl}}(t)$ sampled at the reference frequency

$$i_{s,n,{\rm fl}}(t) = \frac{T_P}{T_{\rm REF}}\cdot\sum_{k=0}^{n}\left(i_{M,n,{\rm fl}}(t)\cdot\delta(t-k\cdot T_{\rm REF})\right). \tag{17}$$

Its PSD at low frequencies can be estimated by

$$\frac{\overline{i^2_{s,n,{\rm fl}}}}{\Delta f} = \frac{T_P^2}{T_{\rm REF}^2}\cdot\frac{\overline{i^2_{M,n,{\rm fl}}}}{\Delta f} \tag{18}$$

where $\overline{i^2_{M,n,{\rm fl}}}/\Delta f$ is the PSD of $M_{1,2}$ flicker noise. Note that the spectrum of the flicker noise current at the CSPD output consists of sampled replicas appearing at integer multiples of $F_{\rm REF}$, which are sufficiently suppressed by the large time constant of $R_D C_S$.

4) In-Band PN Due to CSPD: The in-band PN is obtained by considering the noise contributions of R_D and $M_{1,2}$ at the CSPD output and referring the resulting voltage noise to the input of CSPD

$$\mathcal{L}_{\rm CSPD} = 2\cdot\left(\frac{\overline{i^2_{s,R,n}}}{\Delta f}+\frac{\overline{i^2_{s,n,{\rm th}}}}{\Delta f}+\frac{\overline{i^2_{s,n,{\rm fl}}}}{\Delta f}\right)\cdot\frac{R_D^2}{K_{\rm PD}^2}. \tag{19}$$

Notice that, in contrast to a VSPD, the theoretical PN of a CSPD is not a function of C_S. Fig. 8 shows the simulated and calculated in-band PN at 200-kHz offset from a 10-GHz carrier due to both the flicker and thermal noise of CSPD (but excluding any other noise sources) when $R_D = 100$ kΩ and $(W/L)_{1,2} = 2$ μm/40 nm. The simulation results are in good agreement with the presented calculations if C_S is not chosen too small, which is anyway outside the optimum range. If a very small C_S is used, the simulated PN is much higher than the theoretical value due to the reduced $K_{\rm PD}$ caused by $V_{\rm CM}$ drop. However, if a larger C_S is used, the simulated in-band PN is very weakly related to C_S, as expected. This is very

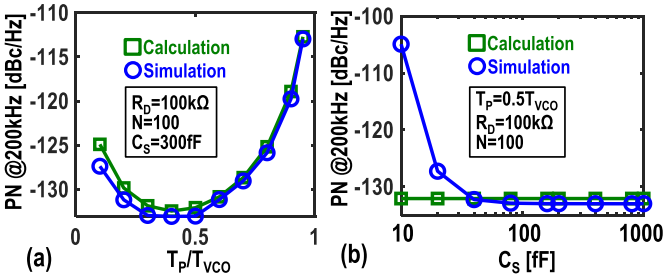

Fig. 8. Simulated and calculated PN at 200-kHz offset from a 10-GHz carrier as a function of (a) T_p and (b) C_S due to CSPD only.

different from a VSPD, where a large C_S is essential to reduce the KT/C noise.

As shown in Fig. 8(a), the CSPD displays a minimum in-band PN (<-133 dBc/Hz) when T_P reaches $\sim 0.5\ T_{\rm VCO}$. While $M_{1,2}$ flicker noise corner is very high (i.e., $\sim$60 MHz) due to their small dimensions, the charge sampling suppresses the flicker noise much more than the thermal counterpart [compare (16) with (18)]. As a result, the R_D thermal noise, the $M_{1,2}$ thermal noise, and the $M_{1,2}$ flicker noise contribute almost equally to the total PN at 200-kHz offset. A larger T_P degrades both $K_{\rm PD}$ and voltage noise contributed by $M_{1,2}$, worsening the in-band PN. Although a smaller T_P reduces the PN originated from the flicker noise of $M_{1,2}$, it degrades in-band PN due to the reduced $K_{\rm PD}$. Nevertheless, choosing T_P between 0.2 $T_{\rm VCO}$ and 0.6 $T_{\rm VCO}$ maintains the PN within 3 dB of the optimum performance.

5) PN Due to Clock Jitter: The jitter of the reference clock alters the moment when $M_{1,2}$ are both turned on and off, thus randomly changing the sampling function $[p_j(t)]$, as shown in Fig. 9. The resultant sampling error $[i_{s,n,j}(t)]$ contains two noise current pulses with a fixed amplitude of $I_P = G_M A_{\rm VCO} \sin(\omega_{\rm VCO}(T_P/2))$ and variable widths of $|\Delta t_r|$ and $|\Delta t_f|$ over one reference period, where Δt_r and Δt_f are the clock jitter of the REF rising edge and falling edge, respectively. Since Δt_r and Δt_f are very small, $i_{s,n,j}(t)$ can be represented as the sum of two impulse trains sampling at the reference frequency

$$i_{s,n,j}(t) = \sum_{k=0}^{n} \frac{I_P \cdot \Delta t_r[k]}{T_{\rm REF}} \cdot \delta\left(t - \left(\frac{-T_P}{2} + k \cdot T_{\rm REF}\right)\right) + \sum_{k=0}^{n} \frac{I_P \cdot \Delta t_f[k]}{T_{\rm REF}} \cdot \delta\left(t - \left(\frac{T_P}{2} + k \cdot T_{\rm REF}\right)\right). \quad (20)$$

If Δt_r and Δt_f are uncorrelated but with the same variance, $i_{s,n,j}(t)$ PSD can be estimated by

$$\frac{\overline{i_{s,n,j}^2}}{\Delta f} = \frac{I_P^2}{T_{\rm REF}^2}\left(\mathrm{psd}(\Delta t_r) + \mathrm{psd}(\Delta t_f)\right) = \frac{I_P^2}{2\pi^2} \cdot \mathcal{L}_j(f) \quad (21)$$

where $\mathcal{L}_j(f)$ is the PN at the rising edge and falling edge of the reference clock. The in-band PN of the PLL due to the uncorrelated jitter can be derived as

$$\mathcal{L}_{{\rm pll},j}(f) = \frac{\overline{i_{s,n,j}^2}}{\Delta f} \cdot \frac{(2R_D)^2}{K_{\rm PD}^2} = \frac{N^2}{2}\mathcal{L}_j(f). \quad (22)$$

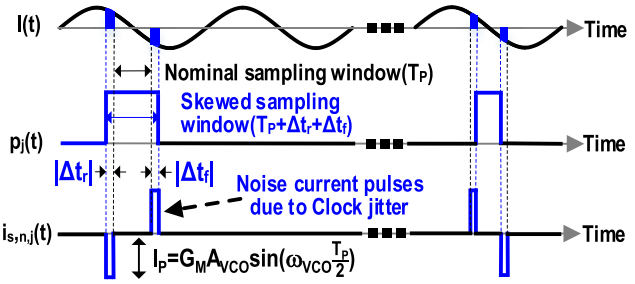

Fig. 9. Sampling error due to the REF jitter.

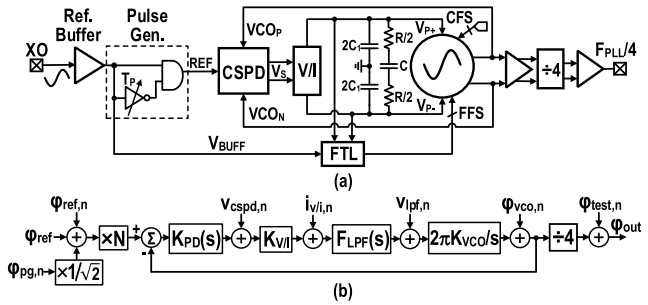

Fig. 10. (a) Block diagram of the proposed CSPLL with an RF-dividerless FTL. (b) Linear phase-domain model of the CSPLL.

Consequently, in a CSPD, the uncorrelated noise of the rising and falling edges of REF is only multiplied by $N^2/2$ when transferred to the PLL output, alleviating the noise requirement of the pulse generator (PG). On the contrary, this noise is still multiplied by N^2 for a VSPD in [12] and [13]. However, similar to a VSPD, the correlated noise generated by the off-chip crystal and on-chip reference buffer is still multiplied by N^2 when transferred to the PLL output.

III. Charge-Sampling Phase-Locked Loop

Fig. 10(a) shows the block diagram of the proposed type-II CSPLL with an FTL operating in the background. A reference buffer and a PG are used to generate a narrow pulse signal (REF) from an off-chip sine reference. The CSPD converts the phase error between the VCO and REF into a differential voltage, V_S. A fully differential V/I stage then rejects the CM ripples on the CSPD output and converts its desired differential-mode signal into a current, which is further filtered by the loop filter (composed of R, C, and C_1) to generate a fine-tuning voltage V_P ($=V_{P+} - V_{P-}$) for the VCO. Note that there is no isolation buffer between the VCO and CSPD so as to verify the inherent low-spur performance of the CSPD. There is still a need for a VCO buffer in a practical system to drive the corresponding load (e.g., an IF mixer or a divider). If the CSPD is driven by the VCO buffer, even a lower reference spur could be obtained. However, this results in poor isolation between the CSPD and IF mixer or divider, leading to unpredictable noise coupling.

A. Phase-Domain Model

Fig. 10(b) shows the linear phase-domain model for the proposed CSPLL, where $K_{V/I}$ is the transconductance of the V/I stage and $F_{\rm LPF}(s)$ represents the transfer function of the loop filter. This model is accurate as long as the PLL

BW is much smaller than F_{REF}. Like an SSPLL, there is no divide-by-N in the feedback path, and a virtual frequency multiplier "$\times N$" is added to the reference path due to the sub-sampling process. However, a factor of $1/\sqrt{2}$ is used for the PG noise to capture the charge-sampling process, as discussed in Section II. The closed-loop transfer function of the CSPLL can be found as

$$H_{\mathrm{cl}}(s) = \frac{H_{\mathrm{ol}}(s)}{1 + H_{\mathrm{ol}}(s)} \tag{23}$$

where $H_{\mathrm{ol}}(s)$ is the open-loop transfer function and can be expressed as

$$\begin{aligned} H_{\mathrm{ol}}(s) &= K_{\mathrm{PD}}(s) \cdot K_{V/I} \cdot F_{\mathrm{LPF}}(s) \cdot \frac{2\pi K_{\mathrm{VCO}}}{s} \\ &= \frac{2\pi \cdot K_{\mathrm{PD}}}{1 + s \cdot R_D C_S} \cdot K_{V/I} \cdot \left(R + \frac{1}{s \cdot C}\right) \Big\| \frac{1}{s \cdot C_1} \cdot \frac{K_{\mathrm{VCO}}}{s}. \end{aligned} \tag{24}$$

Here, we ignored the sinc-type low-pass filtering response of $K_{\mathrm{PD}}(s)$ introduced by the windowed current integration since T_P is very small compared to T_{REF}.

1) Phase Margin Analysis: By considering the presented phase-domain model, the phase margin of CSPLL can be estimated as

$$\mathrm{PM} \approx \tan^{-1}(\omega_u RC) - \tan^{-1}(\omega_u RC_1) - \tan^{-1}(\omega_u R_D C_S) \tag{25}$$

where ω_u is the frequency in which $|H_{\mathrm{ol}}(s)| = 1$. Since $k \approx T_{\mathrm{REF}}/(R_D C_S)$, we can rearrange this equation as

$$\mathrm{PM} \approx \tan^{-1}(\omega_u RC) - \tan^{-1}(\omega_u RC_1) - \tan^{-1}\left(\frac{\omega_u T_{\mathrm{REF}}}{k}\right). \tag{26}$$

Note that there is also a delay between the CSPD differential output and VCO waveforms due to the current integration. Nevertheless, the resulting phase delay is ignored in the phase margin calculations as it is $<\tan^{-1}(2\pi F_{\mathrm{REF}} T_P/2) \approx 0.1°$ in a realistic design. Due to the extra pole introduced by CSPD, C_1 should be much smaller than that in a conventional loop filter ($\sim 0.015 \times C$ in this design) to minimize PM degradation. By ignoring the pole introduced by CSPD ($-1/R_D C_S$), we can approximate ω_u as

$$\omega_u \approx \omega_n \cdot \sqrt{2\zeta^2 + \sqrt{4\zeta^4 + 1}} \tag{27}$$

where ω_n ($=(K_{\mathrm{PD}} K_{V/I} K_{\mathrm{VCO}}/C)^{1/2}$) and ζ ($=0.5RC\omega_n$) are the natural frequency and the damping factor, respectively. Given a certain damping factor and PLL BW,[4] one can calculate C and R to find the phase margin. Fig. 11(a) shows the simulated and calculated phase margins versus k factor for various BW settings with $\zeta = 1.5$, where the discrepancy at high BW is due to the neglected pole of CSPD in estimating ω_u. A large k factor improves the system phase margin, especially for large PLL BWs. However, to ensure a proper charge-sampling operation without sacrificing K_{PD}, the k factor must be smaller than 2. By choosing k factor between 0.4 and 2, PM varies between 51.9° and 70.9° for a BW of 5 MHz.

[4]BW can be estimated by $(2\zeta^2 + 1 + ((2\zeta^2+1)^2 + 1)^{1/2})^{1/2} \cdot \omega_n/(2\pi)$.

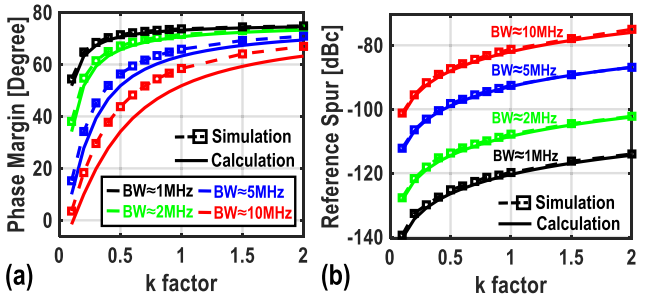

Fig. 11. Simulated and calculated (a) phase margin and (b) reference spur due to differential-mode ripple versus the k factor.

B. Spur Due to Charge Sampling

In this section, the reference spur due to CSPD's non-idealities will be discussed and quantified.

1) Spur Due to BFSK Effect: Due to the windowed current integration, the CSPD can operate with a small T_P. In addition, the transconductors ($M_{1,2}$) of CSPD can be sized very small without sacrificing in-band PN due to the CSPD's high K_{PD} and short T_P. Those lead to a substantial spur reduction due to the BFSK effect as predicted by (1). Based on design parameters (i.e., $C_{\mathrm{MODE}} \approx 0.3$ fF, $D_{\mathrm{REF}} = 0.003$, and $C_{\mathrm{TANK}} = 650$ fF), $S_{\mathrm{REF-BFSK}}$ is -83 dBc, where C_{MODE} is mainly originated from the gate-source capacitance (C_{gs}) variation of $M_{1,2}$ due to the REF switching.

Apart from the spur due to the BFSK effect, unlike a conventional SSPLL in [10], a CSPLL contains other spur mechanisms that disturb the VCO through its tuning voltage. In other words, there is a tradeoff between the maximum BW and minimal reference spur level. Nevertheless, it will be shown in Section III-B2 that the spur level due to those mechanisms is much lower than $S_{\mathrm{REF-BFSK}}$.

2) Spur Due to Differential-Mode Ripple: Unfortunately, as can be gathered from Fig. 3(b), the differential output of CSPD (V_S) experiences a ripple with a worst case peak value of $2G_M A_{\mathrm{VCO}}/(\omega_{\mathrm{VCO}} C_S)$ during each phase comparison even if the PLL is locked. This ripple is first attenuated by the loop filter and then upconverted to spurious tones around the carrier. However, since C_S does not affect K_{PD}, the V_S ripple can be easily suppressed by increasing C_S as long as the PLL phase margin is satisfied. Therefore, the output voltage swing of the CSPD can be very small (i.e., <100 mV) in the lock state, which is also beneficial to reduce the spur due to the charge kickback.

The fundamental component of this differential ripple at F_{REF} can be estimated as $A_{\mathrm{drip}} \approx 4G_M A_{\mathrm{VCO}}/(N\pi\omega_{\mathrm{VCO}} C_S)$. The resulting spur level can be estimated by

$$S_{\mathrm{REF-drip}} \approx 20 \cdot \log_{10}\left(\frac{A_{\mathrm{drip}} \cdot K_{V/I} R K_{\mathrm{VCO}}}{2F_{\mathrm{REF}}\sqrt{1 + (2\pi F_{\mathrm{REF}} RC_1)^2}}\right). \tag{28}$$

Based on the expression of A_{drip}, K_{PD}, and k, $S_{\mathrm{REF-drip}}$ can be rearranged as

$$S_{\mathrm{REF-drip}} \approx 20 \cdot \log_{10}\left(\frac{k \cdot K_{\mathrm{PD}} K_{V/I} R K_{\mathrm{VCO}}}{\omega_{\mathrm{VCO}}\sqrt{1 + (2\pi F_{\mathrm{REF}} RC_1)^2}}\right). \tag{29}$$

Fig. 11(b) shows the simulated and calculated spur level due to the differential-mode ripple versus the k factor for various

BW settings. By choosing $k = 0.4$, the resulting spur level is below -100.4 dBc for a 5-MHz BW, which is marginal compared with the spur due to the BFSK effect.

3) Spur Due to CM Ripple: In addition, the output of CSPD also contains a CM ripple [see Fig. 5], with a very large amplitude of $\sim\Delta V_{\rm CM}/\pi$ at $F_{\rm REF}$. First, this ripple can be converted to a differential one by the V/I and results in a spur level estimated by

$$S_{\rm REF-crip1} \approx 20\cdot\log_{10}\left(\frac{G_M {\rm V_{DC}} T_P}{C_S\pi}\cdot A_{\rm CM-DM}\cdot\frac{K_{\rm VCO}}{2F_{\rm REF}}\right) \tag{30}$$

where $A_{\rm CM-DM}$ is the CM-to-differential-mode gain of the V/I at $F_{\rm REF}$. Second, the CM ripple is attenuated by the V/I and then appears at the input of the VCO. It will also introduce a spur due to the finite CM rejection of VCO. The resulting spur level can be estimated as

$$S_{\rm REF-crip2} \approx 20\cdot\log_{10}\left(\frac{G_M {\rm V_{DC}} T_P}{C_S\pi}\cdot\frac{A_{\rm CM}}{\rm CMR}\cdot\frac{K_{\rm VCO}}{2F_{\rm REF}}\right) \tag{31}$$

where $A_{\rm CM}$ is the CM gain of the V/I and CMR is the CM rejection ratio of the VCO. By considering $K_{\rm VCO} = 50$ MHz/V and $C_S = 250$ fF (or $k = 0.4$), $A_{\rm CM-DM}$ and $A_{\rm CM}/{\rm CMR}$ must be below -47 dB so as to suppress $S_{\rm REF-crip1,2}$ below -90 dBc, which can be satisfied by a proper design.

4) Spur Due to C_S and R_D Mismatch: As discussed in Section II, the mismatch of C_S and R_D also creates a differential ripple at the CSPD output [see Fig. 6]. The resulting spur level can be estimated by

$$S_{\rm REF-ms} \approx 20\cdot\log_{10}\left(\frac{A_{\rm rip-ms}\cdot K_{V/I} R K_{\rm VCO}}{2F_{\rm REF}\sqrt{1+(2\pi F_{\rm REF} R C_1)^2}}\right) \tag{32}$$

where $A_{\rm rip-ms}$ is the ripple amplitude due to mismatch (i.e., equal to $A_{{\rm rip}-\Delta C_S}$ or $A_{{\rm rip}-\Delta R_D}$). By considering a moderate C_S or R_D matching (e.g., $\Delta C_S/C_S = \Delta R_D/R_D = 1\%$), the resulting spur level is below -105 dBc for a 5-MHz BW.

C. Frequency Locking

Like a VSPD, the CSPD also has a limited lock-in range and one cannot distinguish between the desired Nth harmonic and other harmonics of $F_{\rm REF}$. To avoid locking to a wrong harmonic, the works [9]–[15] employed an RF divider-based FTL to bring the VCO frequency within the SSPLL's lock-in range. In the locked condition, the same FTL is also used to correct the frequency error ($F_{\rm ERR}$) introduced by the sudden frequency disturbance on the VCO. However, when the PLL is locked, the maximum $F_{\rm ERR}$ due to voltage and temperature variations or power leakage from other chip components is in the order of tens of MHz.[5] Consequently, it is not wise to use a full range FTL as its high-frequency divider consumes substantial power consumption. We address this issue by introducing a power-efficient FTL that does not rely on any power-hungry RF dividers and can be implemented chiefly by digital blocks, as can be gathered from Fig. 12.

Due to the removal of the RF divider, the lock-in range of the proposed FTL is limited to $\pm 0.5F_{\rm REF}$ (e.g., ± 50 MHz).

[5]The measured VCO frequency of this work is within ± 27 MHz over a VCO supply variation of 100 mV and a temperature variation of 160 °C.

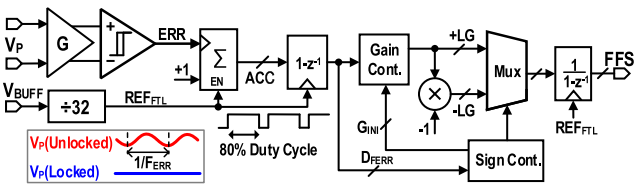

Fig. 12. Block diagram of the FTL.

Hence, the VCO's frequency must be initially calibrated within $\pm 0.5F_{\rm REF}$ of the desired frequency. This is done offline by adjusting the coarse switchable capacitor at power ON. In a future design, a conventional FTL as in [9]–[15] can be used to automatically tune the VCO frequency. Once $F_{\rm ERR}$ is within $\pm 0.5F_{\rm REF}$, our proposed FTL takes over and the RF divider-based FTL is shut down to save power consumption.

Now, suppose that the VCO experiences a frequency disturbance during the CSPLL's nominal operation. If $F_{\rm ERR}$ is within the lock-in range (e.g., $\sim$5 MHz), it can be corrected by the CSPLL. However, if $F_{\rm ERR}$ exceeds the lock-in range, it causes a lock failure of the CSPLL. An aliasing signal with an amplitude of $\sim$20-to-40 mV and $F_{\rm ERR}$ of $|N\times F_{\rm REF} - F_{\rm VCO}|$ will appear at the CSPD output [39], [40]. Instead of using the divided RF clock, the proposed FTL relies on this aliasing signal to initiate the feedback and calculate the frequency error. An amplifier and a Schmitt trigger are employed to convert this aliasing signal to a digital bitstream (ERR). A $\div 32$ frequency divider generates the FTL master clock ($\rm REF_{FTL}$) from the reference. To ensure that the following digital logics are synchronized with $\rm REF_{FTL}$, the number of ERR rising edges is first accumulated only when $\rm REF_{FTL}$ is high. Then, a differentiator clocked by $\rm REF_{FTL}$ is used to obtain the digital representation of the frequency error ($D_{\rm FERR}$). As a result, the ratio of $\rm REF_{FTL}$ frequency to its duty cycle determines the minimum detectable $F_{\rm ERR}$, which must be smaller than CSPLL lock-in range to ensure a seamless frequency locking operation.

FTL should first determine the $F_{\rm ERR}$ sign since the aliasing signal does not provide that information. Consequently, FTL is initially set to decrease $F_{\rm VCO}$ once the detected $D_{\rm FERR}$ is larger than a programmable threshold. Depending on whether $D_{\rm FERR}$ is decreasing or increasing, the initial loop sign is kept or flipped. To speed up the frequency locking process, FTL LG can be adaptively controlled based on the $D_{\rm FERR}$ value. Once FTL brings $F_{\rm VCO}$ into the PLL's lock-in range, the CSPLL rapidly locks the VCO phase to REF, forcing a nearly constant V_P. Hence, ERR stops toggling due to the insufficient input swing and low gain of the amplifier at frequencies below the PLL's lock-in range, eliminating the power of the digital logic. To avoid a false unlock detection, the noise of the amplifier is optimized such that it does not trigger the FTL when the CSPLL is locked.

IV. Circuits Implementation

A. Reference Buffer and PG

Fig. 13(a) shows the reference buffer schematic adapted from [14]. The main transistor (M_1) is a thick-oxide device to allow a higher input swing and is sized large and wide (3.2 mm/550 nm) to achieve a low PN floor (<-168 dBc/Hz).

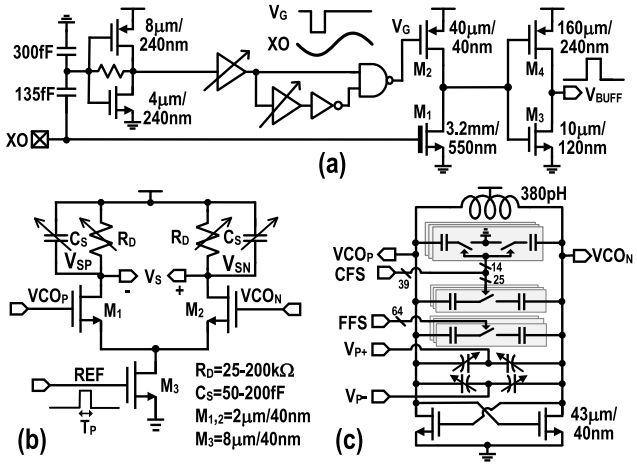

Fig. 13. Schematics of (a) reference buffer, (b) CSPD, and (c) VCO.

The gate terminal of the PMOS transistor (M_2) is driven by a pulse signal, V_G, derived from the delayed reference clock edge. In this way, the short-circuit current of M_1 and M_2 is minimized since M_2 is OFF when M_1 conducts current. The rising edge of the reference buffer then drives the PG to realize the required CSPLL reference, whose pulsewidth (∼35–55 ps) can be adjusted by a 4-bit switched-capacitor bank. While the simulated pulsewidth of PG varies ∼±50% over PVT variations, the maximum PD gain degradation is limited to 30%.

B. PD, V/I, and Loop Filter

Fig. 13(b) shows the CSPD schematic, whose phase-detection gain can be changed (∼0.1–0.6 V/rad) by a 7-bit poly resistor. Moreover, a 4-bit switched metal–oxide–metal (MOM) capacitor is added to adjust the CSPD output CM voltage (e.g., >500 mV) over PVT variations. The VCO output directly drives the CSPD without any isolation buffers to eliminate their power consumption and noise. V/I is based on a fully differential folded-cascode operational transconductance amplifier whose transconductance can be tuned by a 4-bit source-degenerated poly resistor. Due to the achieved high K_{PD}, even by consuming a negligible power (i.e., <20 μW), the simulated in-band PN due to the V/I thermal noise is extremely low (i.e., <−148 dBc/Hz). The simulated $A_{\mathrm{CM-DM}}$ and A_{CM} are below −63 and −32 dB, respectively. The total capacitance of the loop filter is only 20.7 pF due to the fully differential structure, optimized K_{PD}, and wide PLL BW. The compensation resistance of the loop filter can be adjusted by a 4-bit poly resistor to regulate the BW and damping factor of the PLL.

C. VCO

As shown in Fig. 13(c), the VCO employs an NMOS-only cross-coupled pair with a single-turn inductor to achieve a low PN. The implicit CM resonance technique is used to reduce PN further [41]–[43]. To cover a wide tuning range with a small K_{VCO}, a combination of discrete tuning by switched-capacitor banks and continuous tuning by accumulation-mode MOS varactors is adopted. The control of the varactors is fully differential [15] to reject any CM ripples originated from the heavily switched reference path with CMR > 15 dB according to post-layout simulations. In order to further minimize reference spurs due to the reference switching noise, the ground of the VCO, VCO test buffer, and loop filter is shared but is isolated from the ground of the reference buffer, PG, CSPD, V/I, and FTL.

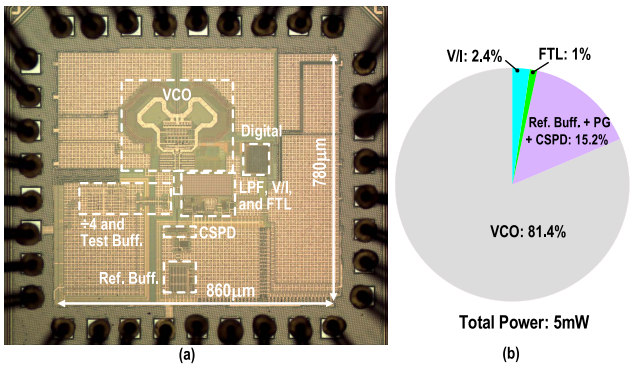

Fig. 14. (a) Chip micrograph. (b) Measured power breakdown.

V. Measurement Results

The CSPLL was fabricated in a standard 40-nm bulk CMOS and the core circuit occupies 0.13 mm^2, as shown in Fig. 14(a). The PLL is powered by 0.6- and 1.1-V supplies. The 0.6-V supply is used for the VCO to satisfy time-dependent dielectric breakdown (TDDB) requirements for thin-oxide transistors, thus securing PLL's long-term reliability [44]. In a future design, thick-oxide devices can be used in the VCO such that the entire PLL can operate under a single power supply. This would not compromise the PLL PN and jitter performance but would slightly degrade VCO's tuning range. Alternatively, a complementary VCO can be used without sacrificing the tuning range and jitter performance. The entire PLL (excluding the test divider and buffer but including the reference buffer) dissipates 5 mW, and its power breakdown is shown in Fig. 14(b). The test buffer between the VCO and divider consumes 2.1 mW. The FTL consumes 50 μW in total, of which the amplifier, the digital logic, and the reference clock divider consume 39, 8, and 3 μW, respectively. The power and area overhead of the CSPD and FTL are negligible compared to the VCO.

The reference clock is derived from an off-chip high-quality VLCU-Type series crystal oscillator offered by Taitien. Fig. 15(a) shows the measured PN plot at a PLL frequency (F_{PLL}) of 11.2 GHz after an on-chip divide-by-four. The RMS jitter is 48.6 fs (integrated from 1 kHz to 100 MHz but excluding reference spurs). To optimize the jitter performance at this frequency, T_P tuning code was adjusted to achieve the highest K_{PD}, and the PLL BW was digitally regulated at ∼6 MHz by adjusting the resistance of the loop filter, the transconductance of the V/I converter, and R_D of the CSPD. The measured PN, RMS jitter, and FOM plots covering the PLL's tuning range (i.e., 9.6–12 GHz) are shown in Fig. 15(b) and (c). The in-band PN, RMS jitter, and FOM are better than −121 dBc/Hz, 55 fs, and −258 dB, respectively. As shown in Fig. 15(d), the CSPLL appropriately works over a wide temperature range (i.e., from −80 °C to +80 °C), but its integrated jitter increases to 65 fs at 80 °C. Notice that all of the above measurements were carried

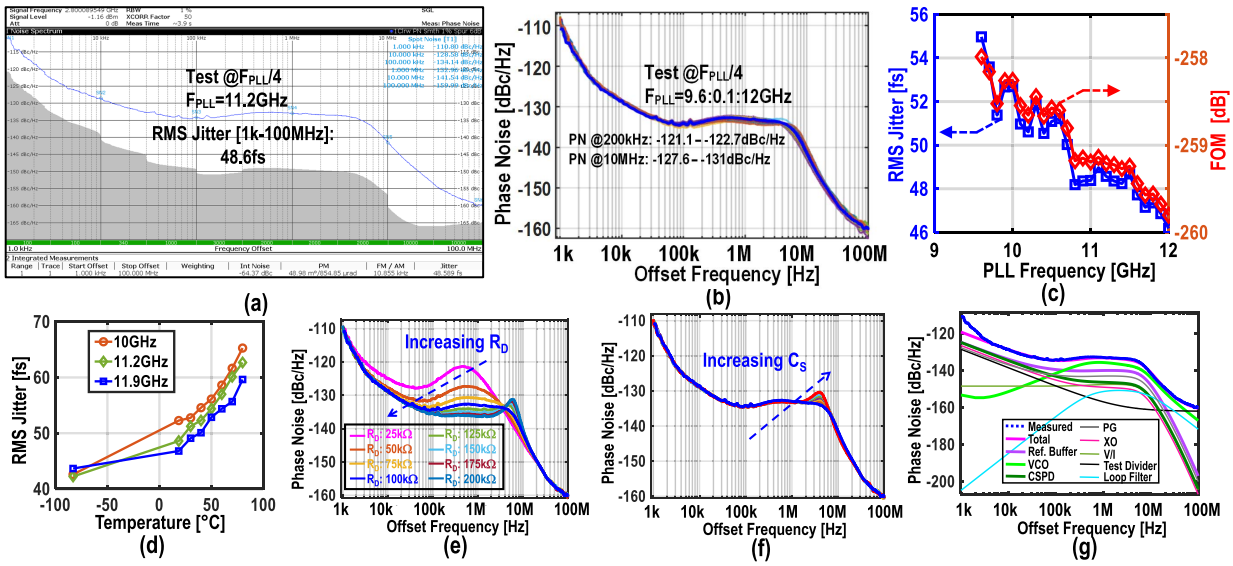

Fig. 15. (a) Measured PN at 11.2 GHz after an on-chip divide-by-four. (b) Measured PN for all integer channels. (c) RMS jitter and FOM versus PLL tuning range. (d) Measured RMS jitter versus temperature; measured PN for different values of (e) R_D and (f) C_S. (g) Simulated PN contribution of different PLL blocks with the measured PN performance.

out under the same loop parameters setting,[6] indicating the robustness of the design.

Fig. 15(e) shows the measured PN plots for different R_D values. As predicted by (8), by enlarging R_D, K_{PD} increases, and the in-band PN at 200 kHz is monotonically reduced. Furthermore, for small R_D values, the CSPLL BW is not wide enough to sufficiently attenuate the VCO PN. As the PLL loop BW is widened by increasing R_D, the VCO PN is suppressed and the reference buffer eventually dominates the in-band PN. However, increasing R_D or C_S beyond their practical useful range introduces peaking on the measured PN plots [see Fig. 15(e) and (f)] due to the reduced phase margin. Changing T_P control code only marginally affects the measured PN performance due to the sine characteristics of K_{PD} [see Fig. 4(a)] and the limited T_P tuning range of the PG. To verify the phase-domain model presented in Section III, the measured reference and free-running VCO PN, in addition to simulated loop parameters of the CSPLL, were used to calculate the closed-loop PN and compare it to the measured result, as shown in Fig. 15(g). The measured PN in blue matches very well with the predicted PN in pink. The discrepancy between two curves at 1-kHz–to–4-kHz frequency offsets mainly originates from the neglected supply noise in the phase-domain analysis.

Fig. 16(a) shows the measured spectrum at the divide-by-four output. The measured reference spur is -89.3 dBc at the divider output, translating to -77.3 dBc when referred to F_{PLL}. Since the measured spur level is $\sim$25 dB lower than the integrated PN (~ -52 dBc), the impact of reference spur on RMS jitter is marginal. The measured reference spur for two wire-bonded samples is <-74 dBc over the tuning range and varies <3 dB over temperatures, as shown in Fig. 16(b) and (c). The measured spur level varies <0.7 dB by sweeping C_S control code, indicating that the voltage ripple on V_S and the

[6]Unless otherwise specified, we fixed the loop parameters setting for all of the remaining measurements in this article.

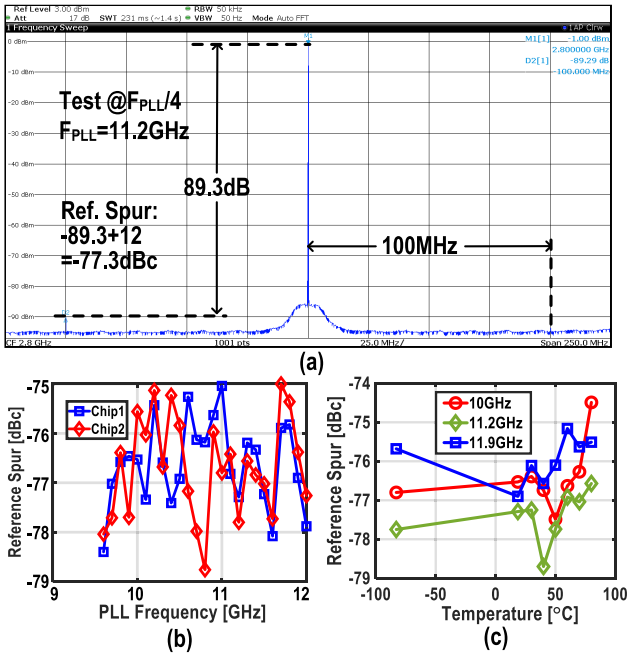

Fig. 16. (a) Measured CSPLL spectrum after an on-chip divide-by-four. Measured reference spur versus (b) PLL tuning range and (c) temperature.

mismatch between CSPD components have a minor impact on reference spur. In addition, the measured spur level is also weakly related to T_P control word and is $\sim$5 dB higher than the theoretical prediction given by (1). The dominated spur mechanism of the CSPLL is charge injection and clock feedthrough according to simulations. Compared with the CSPLL originally presented in [19], the spur performance is improved by modifying the PCB layout and reducing the PCB ground bounces originated from the high current spike of the reference pin. In the modified PCB, the reference ground and VCO ground are merely connected near their corresponding power supplies to minimize unwanted couplings.

TABLE I

COMPARISON TABLE WITH STATE-OF-THE-ART INDUCTANCE–CAPACITANCE (*LC*)-BASED INTEGER-*N* PLLS

	This Work	[11] JSSC'20	[12] ISSCC'19	[23] ISSCC'20	[13] JSSC'20	[15] JSSC'18	[3] JSSC'19	[16] ISSCC'19	[2] ISSCC'18	[4] VLSI'19
PLL Architecture	Type-II CSPLL	Type-II SSPLL	Type-II iSSPLL	Type-II SSPLL	Type-II SSPLL	Type-I SSPLL	Type-II RSPLL	Type-II SSPLL	Type-II CPPLL	Type-II ILCM
Power Supply [V]	1.1/0.6	0.65	1/0.55	NA	1	0.8	1.2/0.5	NA	NA	NA/0.14
F_{REF} [MHz]	100	200	103	50	100	100	50	100	500	100
F_{PLL} [GHz] FTR [GHz]	11.2 9.6-12 (22.2%)	14 12-16 (28.6%)	26.4 25.4-29.5 (14.9%)	13.05 12-14.5 (18.9%)	2.4 NA (NA)	5 4.6-5.6 (19.6%)	2.55 2.05-2.55 (21.7%)	3.8 3.3-4.3 (26.3%)	12.5 7.4-14 (61.7%)	2.4 2.2-2.6 (16.7%)
PLL Bandwidth [MHz]	~6	~7	~4	~3	~0.6	~6	~1	~3	~3	~10
S_{REF} [dBc]	-77.3	-64.6	-63	-75	-67	-64.1	-63	-75	-75	-66.5 $
*S_{REF_Nor} [dBc]	-77.3	-66.5	-70.4	-76.3	-53.6	-57.1	-50.1	-65.6	-76	-53.1
RMS Jitter, σ_{rms} [fs] [Int. Bandwidth]	48.6 [1k-100MHz]	56.4 [1k-100MHz]	71 [1k-100M]	83 [1k-100M]	161 [10k-100M]	162.2 [10k-100MHz]	110 [10k-100M]	72 [1k-30MHz]	53.6 [10k-10M]	298 [0.1k-100M]
P_{DC} [mW]	5	7.2	15.3 ^	6.7	0.9 #	1.1	3.7	19.1	45	0.17 #
P_{DC} of Iso. Buffer [mW]	0	1.4	0.56	~1.5	0	0.15	~0.4	~7	NA	0
Inductor Used in Iso. Buffer ?	NO	YES	YES	YES	NO	NO	NO	NO	NO	NO
**FOM [dB]	-259.2	-256.4	-251.1	-253	-256.3	-255.4	-253.5	-250.1	-248.9	-258.2
***FOM_N [dB]	-279.7	-274.9	-275.4	-277.2	-269.8	-272.4	-270.6	-265.8	-262.8	-272
Core Area [mm²]	0.13	0.234	0.24	0.23	0.42	0.01	0.36	0.21	0.35	0.25
Process [nm]	40	40	65	65	65	65	65	65	16	65

*$S_{REF\_Nor} = S_{REF}+20*\log_{10}(11.2GHz/F_{PLL})$ **$FOM = 20*\log_{10}(\sigma_{rms}/1s)+10*\log_{10}(P_{DC}/1mW)$ ***$FOM_N = FOM+10*\log_{10}(1/N)$ defined in [8]

^Reference buffer power of 5.08mW excluded #FTL power excluded or not reported $Reported value using an 800MHz reference

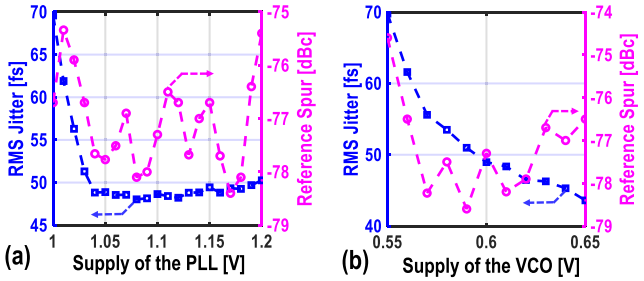

Fig. 17. Measured RMS jitter and reference spur versus the power supply of (a) PLL and (b) VCO at 11.2 GHz.

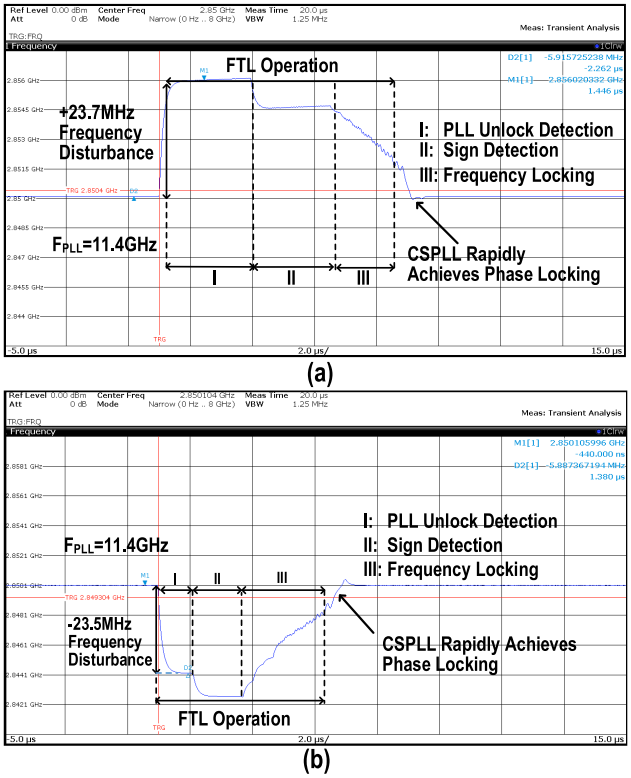

Fig. 18. Measured FTL transient response to (a) positive frequency disturbance and (b) negative frequency disturbance.

Fig. 17 shows the measured RMS jitter and reference spur versus the power supply of the PLL and VCO at 11.2 GHz. The RMS jitter varies <4 fs when the PLL supply was swept from 1.04 to 1.2 V. However, it degrades to 70 fs under a 1-V supply mainly due to the higher PN contribution of the reference buffer. As the oscillation swing increases by raising VCO's supply voltage, both VCO PN and K_{PD} are improved, leading to a lower RMS jitter. The measured reference spur is still <-74 dBc over a wide supply variation.

Fig. 18 shows the measured transient response of the FTL to a positive or negative frequency disturbance injected to the VCO by intentionally changing the VCO control code. In both cases, the FTL successfully detects the frequency error and relocks the VCO within 10 μs due to the implemented adaptive gain adjustment technique.

Table I summarizes the CSPLL performance and compares it with the state of the art. Due to the proposed CSPD and low-power FTL, the proposed CSPLL shows the lowest reference spur, lowest jitter, best FOM, and a 2.5-dB improvement in FOM_N. While the SSPLL in [23] achieved a comparable reference spur level, an area-hungry VCO isolation buffer with an inductive load was used. The CSPLL also occupies the smallest area compared to other type-II PLLs.

VI. Conclusion

We presented a CSPLL and analyzed in-depth its transient response, phase-detection gain, reference spur, and PN performance. Due to its high phase-detection gain and excellent isolation between the VCO and the sampling capacitor, the PLL can simultaneously achieve an ultra-low-RMS jitter and an outstanding reference spur with a large frequency multiplication factor. Moreover, a power-efficient highly digital FTL is introduced to lock the CSPLL robustly when the VCO faces a sudden frequency disturbance. Measurement results show that the CSPLL achieves 48.6-fs RMS jitter and −77.3-dBc reference spur at an 11.2-GHz carrier frequency while consuming 5 mW. This corresponds to the best-reported jitter-power FOM and reference spur performance.

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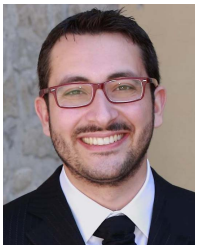

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