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Lifetime Comparison of Power Semiconductors in Three-Level Converters for 10-MW Wind Turbine Systems

Udai Shipurkar^{ID}, Emmanouil Lyrakis, Ke Ma^{ID}, Henk Polinder^{ID}, and Jan A. Ferreira, *Fellow, IEEE*

Abstract—The power electronic converter, especially the power semiconductor, is a major contributor to the failure rates of the wind turbine drivetrain. As the temperature is a major driving factor behind the failure mechanisms of these power semiconductors, the choice of topology and switching strategy can have a significant effect on the reliability of the converter. This paper presents a detailed comparison of several three-level converter topologies and switching strategies on the basis of loss distribution, thermal, and lifetime performance. This investigation is done through simulations on a 10-MW direct drive permanent magnet drivetrain. The study shows that overrating in the form of using overrated topologies, or the use of overrated components can result in large gains in lifetime expectancy and quantifies these gains. It concludes that the improvements offered by overrated topologies and overrated components are comparable and this use of the overrated topologies do not offer a significant advantage over the use of topologies with overrated components.

Index Terms—Direct drive PM generator, lifetime estimation, multilevel converter, semiconductor device reliability, wind energy.

I. INTRODUCTION

WIND power, though unpredictable, has been an important factor in the energy transition with the installed capacity of wind power increasing continuously. Therefore, the reliability performance of the wind turbine systems has been of great concern. The reduction of produced energy is not the only concern as the maintenance expenses are not negligible. Especially for offshore wind farms, maintenance times are longer and costly, and not possible during the whole year. It is estimated that the operation and maintenance costs account for about 20%–30% of the levelized cost of energy [1] and in this scenario, the reliability of the wind turbine becomes even more important.

The wind turbine drivetrain has a large share of the overall failures in a wind turbine system and amongst the components

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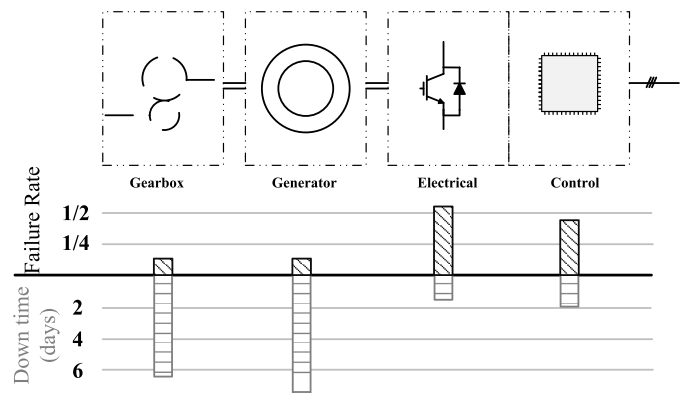


Fig. 1. Failure rate distribution in the wind turbine drivetrain. From [2], [5].

of the drivetrain, the power electronic converters have the highest failure rates [2] as highlighted in Fig. 1. Of the power electronic converter components, the power semiconductors have the highest share of failures [3]. Furthermore, the major driving force behind the failure mechanisms of these power semiconductors is temperature [4], i.e., the mean junction temperature and the amplitude of junction temperature cycles. For this reason, the focus now is to develop power converter topologies with an extended reliability which would result in increased energy yields and reduced costs. The current practice is to do this by using overrated components; however, another solution could be the use of overrating in terms of topology, i.e., the designing of more complex topologies or control strategies that offer a more evenly distributed loading of the power converter or even topologies that can sustain faults and preserve their functioning ability.

The two-level back-to-back voltage source converter (VSC) has been the most popular converter topology in wind turbines [5], [6]. However, with the increasing power rating of turbines leading to higher voltage ratings, the increased switching losses in a two-level converter make this prohibitive. For this reason multilevel converter topologies, especially the neutral point clamped (NPC) topology, are becoming popular. Their operation is based on the composition of sinusoidal output using multiple levels of dc voltage [7]. By going up a level in a multilevel converter, the maximum voltage that each switch has to sustain is decreased. In addition, the output power quality is improved as the levels of voltage increase and the need for filtering the output decreases. Consequently, the total harmonic distortion tends to decrease [8]. However,

the cost of the converter is increased because of the additional power electronic components. Moreover, the pulse width modulation (PWM) methods used by converters with higher levels become complicated.

This paper investigates the multilevel converter topologies to compare their reliability. Although the range of multilevel converters can in theory be extended to any $(2n + 1)$ -level topology, this paper limits itself to a comparison of topologies from the three-level family. The three-level topologies are chosen as they are the next step-up from the two-level converters and address their issues while not complicating design and control to a large extent. Furthermore, a number of different topologies for multilevel converters can be found in the literature [9]–[12]; however, this analysis is limited to the NPC, active NPC (ANPC), H-bridge, and T-type topologies as these are the most prominent ones. The approach followed in this paper uses stress and strength modeling to map the loads that drive the failure mechanisms in the considered components [13]. The assessment is based on the power losses of each converter, the distribution of these losses through their components, and the impact that they have on the thermal behavior of the power electronic components. The study of the power loss and the thermal behavior of the components offers useful conclusions about their lifetimes and their improvement.

Prior comparisons of converters focused on aspects of efficiency and harmonic distortion as in [9], as well as a host of other parameters as in [14]. However, with the growth of interest in reliability, this has become an important comparison criterion for modern converter topologies and some studies have focused on this aspect. Ma *et al.* [15], [16] compared three-level and five-level H-bridge (HB) topologies with the three-level NPC (3L-NPC) topology and extended this paper to a comparison of reliability for these topologies. Also, Gierschner and Eckel [17] have compared the lifetime estimation of the Bimode insulated gate transistor-based A-NPC and T-type converters. This paper extends the available comparisons to include the most prominent three-level topologies and modulation techniques, thus leading to a comprehensive comparison with the aim to draw conclusions on the suitability of these topologies from the view of reliability. The contribution of this paper, therefore, lies in the variety of three-level converter topologies and modulation strategies that have been included in this comparative study. Furthermore, these configurations are built into complete drivetrain models and judged on wind distribution over an annual cycle that gives a realistic comparison.

This paper describes the multilevel converter topologies in Section II and details the converter topologies and switching strategies compared in this paper. Furthermore, in Section III, it details the system analyzed and its modeling. Section IV compares the performance of topologies and switching strategies. Finally, Section V gives the conclusions drawn from this paper.

II. MULTILEVEL POWER ELECTRONIC CONVERTERS

For this paper, the power electronic converters that are investigated include topologies and switching regimes of

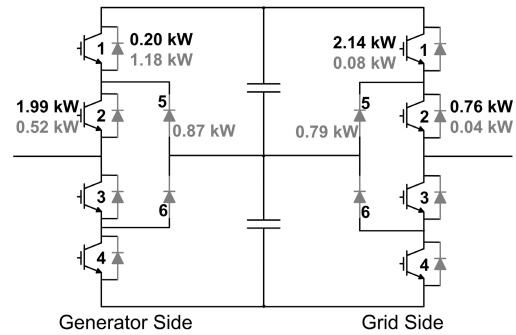


Fig. 2. NPC (3L-NPC) with losses at rated operation. Black values: losses in the IGBT. Gray values: losses in the diode. These are calculated based on the equations in Section III.

three-level converters as well as those of the classical two-level converter. The basic two-level VSC topology is used as a reference model; primarily because it represents the most simple and basic building block of power electronic converters. The topologies analyzed in this paper are listed in the following:

- 1) two-level VSC (2L-VSC);
- 2) 3L-NPC;
- 3) three-level ANPC (3L-ANPC)
 - a) double frequency (3L-ANPC-DF);
 - b) adjustable loss distribution (3L-ANPC-ALD);
- 4) three-level HB (3L-HB);
- 5) three-level T-type (3L-T2C).

The 3L-NPC requires double the number of IGBTs as a two-level converter and also has two additional diodes that clamp the neutral point as can be seen in Fig. 2. These two diodes provide the neutral or zero state. Even though the overall number of the power electronic components is higher, their voltage rating is half compared to that of the two-level converter topology with the same dc-link voltage. The main drawback of this topology is the uneven loss distribution among its power components as can be seen in Fig. 2.

The 3L-ANPC topology is derived from the 3L-NPC with the aim of reducing or better distributing losses amongst the components. The fundamental difference between them is that the 3L-ANPC topology has two additional IGBT switches that clamp the neutral point. The two active switches that replace the diodes give the topology of the capability of more than one way of neutral point clamping. With the use of the right switching strategies, the switching losses can be controlled by using the variety of different commutations that are now available. This paper analyzes the system with two different switching strategies for the ANPC–DF and ALD.

In the PWM-DF (Fig. 3) switching strategy for the 3L-ANPC converter [18], [19], the output phase voltage has an apparent switching frequency that is double the switching frequency, even though all switches do not switch more than once per switching period; this feature enables this switching strategy to produce the same output as any other ANPC PWM strategy with only half of the switching frequency, resulting in lower switching losses. The PWM-ALD (Fig. 4) strategy introduces a new way of distributing the switching losses and

TABLE I
SUMMARY OF TOPOLOGIES

	2L-VSC	3L-NPC	3L-ANPC	3L-HB	3L-T2C
No. of Converters	8	4	4	4	8
Types of Switches	1	1	1	1	2
No. of IGBTs	12	24	36	24	24
No. of Diodes	12	36	36	24	24
DC-Link Voltage	$2kV$	$4kV$	$4kV$	$2kV$	$2kV$
Converter IGBT Rating*	$96 \cdot V_s I_s$	$96 \cdot V_s I_s$	$144 \cdot V_s I_s$	$96 \cdot V_s I_s$	$144 \cdot V_s I_s$
Converter Diode Rating*	$96 \cdot V_s I_s$	$144 \cdot V_s I_s$	$144 \cdot V_s I_s$	$96 \cdot V_s I_s$	$144 \cdot V_s I_s$

* V_s and I_s are the rated voltage and current of each switch which is common to all topologies.

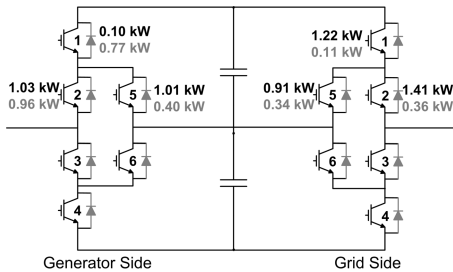


Fig. 3. ANPC - DF (3L-ANPC-DF) with losses.

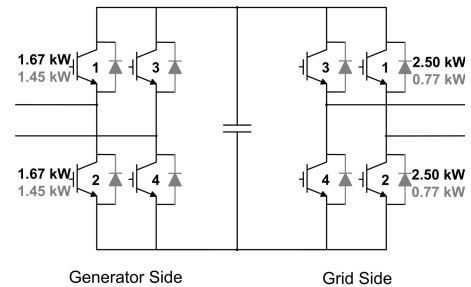


Fig. 5. H-bridge (3L-HB) with losses.

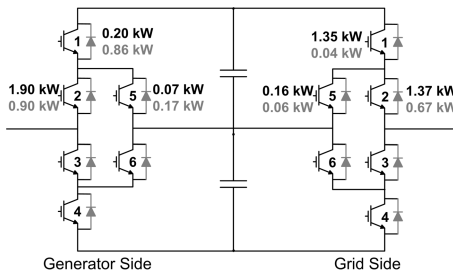


Fig. 4. ANPC - ALD (3L-ANPC-ALD) with losses.

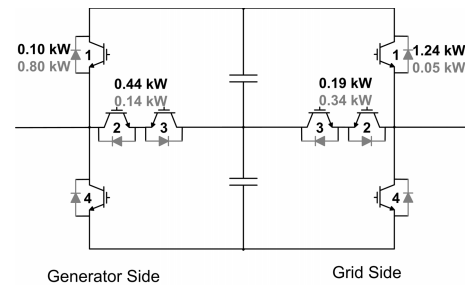


Fig. 6. T-type (3L-T2C) with losses.

is explained in detail in [20]. During certain commutations where IGBT modules have to switch ON and OFF simultaneously, one switch can switch ON earlier and switch OFF later than the other. As a result, the switching losses load only one of the switches as the other turns ON and switches off with zero current. Each voltage period is featured by a stress-in/stress-out percentage that defines the proportionality of loading the inner or the outer IGBT modules with the switching losses during the extent of a voltage period. This way, the ALD-PWM strategy can achieve a more even distribution of overall losses among the power electronic components as can be seen in Fig. 4.

Another topology is the 3L-HB that consists of two single-leg converters or it can be said that it is the combination of two half-bridge converters as seen in Fig. 5. It only needs half of the dc-link voltage to produce the same voltage output as any other three-level converter. If each one of the two legs of the H-bridge are seen individually, the voltage output of each is the output of a 2L-VSC. Due to this, the dc-link voltage that is needed for the 3L-HB is half of that needed for the rest of topologies that have been mentioned. Instead

of a reference or neutral point, the 3L-HB ends in an open winding.

The 3L-T2C converter is a topology that combines the structural and operational characteristics of the 2L-VSC and the 3L-NPC converters. Structurally, the 3L-T2C converter can be considered as a development of the 2L-VSC with an extension of one bidirectional switch to clamp the neutral point of the dc-link as can be seen in Fig. 6. A unique feature of the T-type converter is that it uses switches of two different voltage ratings. Its outer switches block the full dc-link voltage. On the other hand, the middle switches are designed to have half the voltage rating of the two outer switches. Even though the outer switches block the dc-link voltage, they only switch at half the dc-link voltage, and therefore, experience reduced switching losses. Table I summarizes the prominent features of the topologies under consideration.

III. SYSTEM MODELING

A detailed model of the wind turbine drivetrain is constructed to compare the lifetimes of power semiconductors

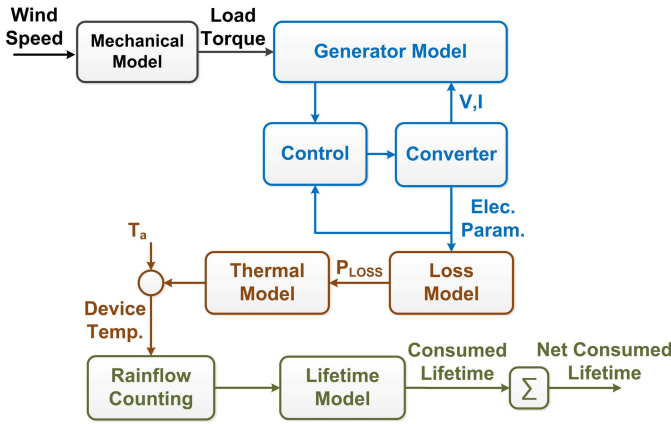


Fig. 7. Schematic of system model.

in wind turbine converters. The schematic is shown in Fig. 7. The input is wind speed; this is fed to the mechanical model that generates the load torque signal. Based on the generator, control block, and converter models, the required electrical signals are generated. These are used by the loss models to calculate the losses in the switches and diodes. This is converted to a temperature signal by the thermal model of the power semiconductors. Furthermore, a rainflow counter and lifetime models are used to calculate the consumed lifetimes.

The drivetrain under consideration is a 10-MW direct drive permanent magnet generator with fully rated converters. The turbine is based on the design proposed by Polinder *et al.* [21]. For a fair comparison between topologies, the switch rating in each topology is identical. This, results in the 2L-VSC and 3L-T2C topologies employing half the dc-link voltage and twice the number of converters compared to the rest. This also has consequences for the design of the generator, and therefore, two different generator designs have been used in this paper. Section III-A describes the used wind scenario and Section III-B describes the mechanical and generator model of the turbine. Similarly, Section III-C develops the converter's design and modeling. Sections III-D and III-E describe the loss and thermal models used in this paper, respectively. Finally, Section III-F1 describes the lifetime model.

A. Wind Model

Wind turbines are designed based on wind classes according to IEC61400-1. For the purpose of this comparison, the wind class Ia has been selected as it poses the highest wind speeds and turbulence intensities. Furthermore, the wind model is based on the measured data of a KNMI (The Royal Netherlands Meteorological Institute) offshore weather station (L9-FF-1). The wind speed distribution used is shown in Fig. 8 and the main characteristics of the wind profile are described in Table II.

B. Turbine and Generator Model

The mechanical model describes the wind turbine rotor and is modeled to convert a wind speed input to the appropriate

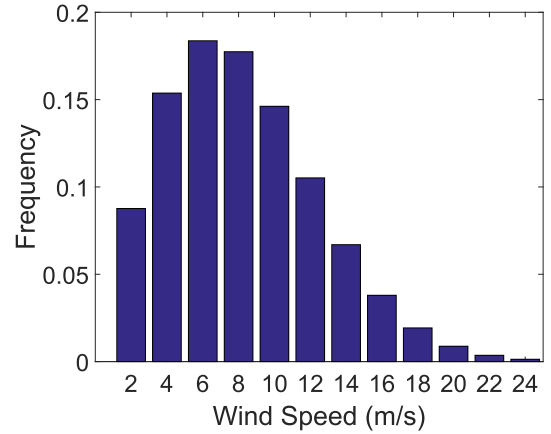


Fig. 8. Distribution of mean wind speed.

TABLE II
TURBINE CHARACTERISTICS

Wind Characteristics	
Mean Wind Speed (m/s)	8.2
Turbulence Intensity (%)	18
Weibull Parameters	
Shape Parameter	2.01
Scale Parameter	9.30

TABLE III
TURBINE CHARACTERISTICS

10 MW Turbine Characteristics	
Rotor Diameter (m)	170
Rated Wind Speed (m/s)	12
Rated Rotor Speed (rpm)	10
Optimum Tip Speed Ratio	9.5
Maximum Power Coefficient	0.515

shaft power and torque. The shaft power, neglecting mechanical losses, is described by

$$P_{\text{shaft}} = \frac{1}{2} \cdot \rho_{\text{air}} \cdot C_p(\lambda, \theta) \cdot A \cdot v_{\text{wind}}^3 \quad (1)$$

where ρ_{air} is the density of air, C_p is the power coefficient that is a function of tip speed ratio (λ) and pitch angle (θ), and A is the area of the turbine rotor. The characteristics of the wind turbine rotor are detailed in Table III. The variation of the power coefficient, C_p with the tip speed ratio is plotted in Fig. 9.

The design of the generator is based on the design by Polinder *et al.* [21]. As there are two levels of topologies that are compared, the design of the generator is adapted for use with both two- and three-level converters. The details of the generator are given in Tables IV and V. Design I is the generator used with three-level converters, while design II is used with the two-level converter. The dynamic model of a permanent magnet synchronous generator has been covered extensively in the literature [22], [23] and is not presented here.

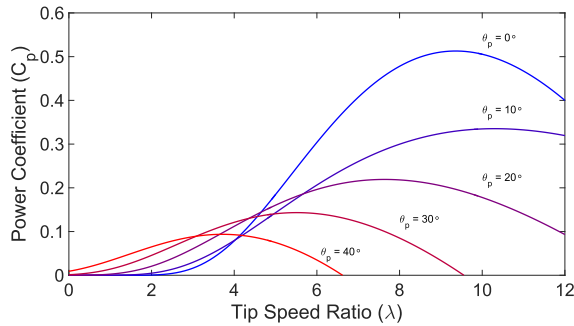


Fig. 9. Power coefficient curve.

TABLE IV
GENERATOR CHARACTERISTICS—GEOMETRY

10 MW Generator Geometry Characteristics	
Stator Diameter (m)	10
Stack Length (m/s)	1.6
Pole Pairs	160
Air-gap (mm)	10
Stator Slot Width (mm)	16.4
Stator Tooth Width (mm)	16.4
Stator Slot Height (mm)	80
Stator and Rotor Yoke Height (mm)	40
Magnet Height (mm)	20

TABLE V
GENERATOR CHARACTERISTICS—ELECTRICAL

10 MW Generator Electrical Characteristics		
	I	II
Generator Rating (MVA)	12	12
Rated Line Voltage (kV)	2.5	1.5
Rated Current (kA)	2.75	4.50
Stator Resistance (pu)	0.02	0.03
Stator Leakage Inductance (pu)	0.35	0.51
Stator Main Inductance (pu)	0.21	0.30
Rated Electrical Frequency (Hz)	26.67	

C. Converter Model

The main design parameters for this converter are summarized in Table VI, these are for a 10 MW application. Design I is for the 3-level converters, while design II is for the 2-level converter.

1) *DC-Link*: The dc-link voltage is related to the ac voltage in the lines through

$$V_{dc} = x \cdot \frac{2\sqrt{2}}{\sqrt{3}} \cdot \frac{1}{m} \cdot V_{l-l} \quad (2)$$

where m is the modulation ratio, and V_{l-l} is the rms line voltage of the ac side. For the space vector modulation strategy, the value of m is limited to 1.15. Furthermore, to account for grid fluctuations, the dc-link voltage is scaled with an overvoltage factor, x , which is 1.15 for medium voltage systems [24], [25]. This results in a 4-kV dc-link

TABLE VI
CONVERTER CHARACTERISTICS

Converter Characteristics		
	I	II
Parallel Converters	4	8
Switching Frequency (kHz)	2	
DC Link		
DC Link Voltage (kV)	4	2
DC Link Capacitance (mF)	97	160
Grid Side		
Line Voltage (kV)	2.5	1.5
Grid Frequency (Hz)	50	
Line Reactance (pu)	0.15	
Line Resistance (pu)	0.003	
Power Factor	0.9	
Generator Side		
Line Voltage (kV)	2.5	1.5
Rated Frequency (Hz)	26.67	

voltage for a 2.5-kV ac system (3L converter) and a 2-kV dc-link voltage for a 1.5-kV system (2L converter).

2) *DC-Link Capacitance*: The sizing of the dc-link capacitor is done based on the allowed voltage ripple [25] through

$$C = \frac{S}{4\pi f V_{dc} \Delta V_{dc}} \quad (3)$$

where S is the apparent power of each converter, f is the nominal generator-side frequency, V_{dc} is dc-link voltage, and ΔV_{dc} is the allowed voltage ripple that is taken as 2% of the dc-link voltage [25].

3) *Grid-Side Line Reactor*: The line reactor is used for protection and filtering. As proposed in [25], the line reactor resistance and inductance are taken as 0.003 and 0.15 pu, respectively. Converters also usually include filters as they can improve quality of the energy exchanged. This has not been considered in this paper; however, the details about sizing a filter can be found in [26].

4) *Switch Ratings*: The selection of switches is based on their blocking voltage and their rated currents. The switches are required to block the dc-link voltage. Furthermore, a safety margin of 50% or 60% on this dc-link voltage is used for the selection of the voltage rating of the switches [24]. For the purpose of this paper, Infineon switch-FZ1000R33HE3 is selected.

The rated current that needs to be processed by the three-level converter is 2.75 kA. To handle this current, a set of parallel converters is used. Each topology uses four parallel converters. Similarly, the 2L-VSC and 3L-T2C topologies use eight parallel converters.

5) *Heat Sink*: As the switches used are high power modules, liquid cooled heat sinks are considered in this paper. The heat sink based on that used by the Semikron SKiiP modules (SKiiP 3614 GB17E4-6DUW) and the details are given in Table VII. In the converters, one heat sink module is used for each 3.3-MVA rated switch.

6) *Control*: The generator-side converter controller regulates the current through the stator of the generator controlling

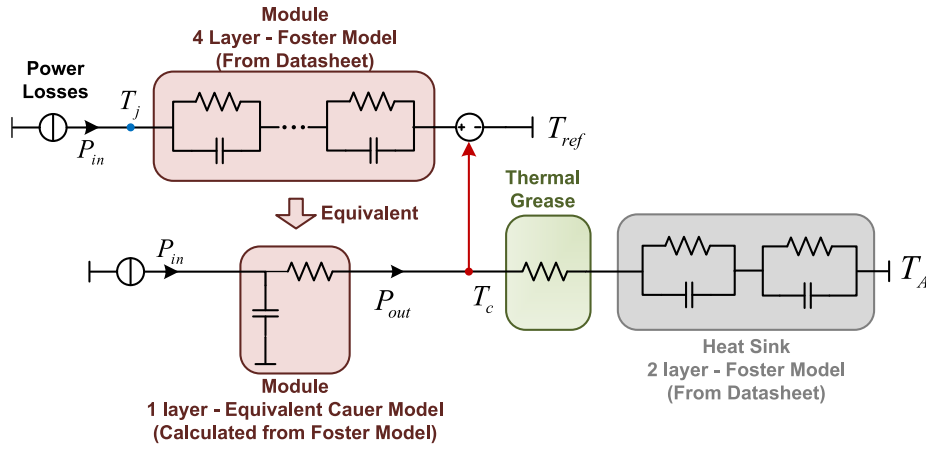


Fig. 10. Thermal model of the power semiconductor. From [31].

TABLE VII
SWITCH AND HEAT SINK CHARACTERISTICS

Switch and Heat Sink Characteristics	
Switch Selection	
Converter Switch Rating (kV)	3.3
Heat Sink Details	
Fluid Flow Rate (l/min)	15
Water:Glycol Ratio	50%:50%
Fluid Inlet Temperature (°C)	40
Foster Model Impedence (K/kW)	1.7 & 3.4
Thermal Time Constants (s)	32.30 & 5.94

the rotational speed of the rotor speed so as to extract the maximum power from the wind. The grid-side converter controls the power flow to the grid. Current in the d -axis maintains the dc-link voltage level controlling the amount of real power that is being fed to the grid, and reactive power is regulated by the q -axis current. In this paper, the power factor of the grid-side controller is maintained at 0.9.

The converters use the sinusoidally modulated PWM for controlling the modules. Although a number of other modulation strategies are available, studies in [27] and [28] show that the effect of these is not significant compared to the results in this paper. Therefore, these different modulation strategies have not been considered.

D. Loss Model

The models that are described for the calculation of the losses are based on work by Ma *et al.* [29], [30]. The conduction loss, averaged over a switching period, can be calculated by

$$P_{\text{Cond,IGBT}} = u_{\text{CE}}(i) \cdot i \cdot d_{\text{IGBT}} \quad (4)$$

$$P_{\text{Cond,Diode}} = u_{\text{F}}(i) \cdot i \cdot d_{\text{Diode}} \quad (5)$$

where u is the ON-state voltage that is a function of the current and is estimated on the basis of datasheet curves, i is the current through the component, and d is the duty cycle. The conduction loss, therefore, requires the knowledge of the duty cycle of the component and the current through it. This

loss is further dependent on the junction temperature and a linear interpolation of losses is used to calculate the loss for the component. The switching loss can be calculated by

$$P_{\text{sw,IGBT}} = (E_{\text{ON,IGBT}} + E_{\text{OFF,IGBT}}) \cdot f_{\text{sw}} \quad (6)$$

$$P_{\text{sw,Diode}} = (E_{\text{ON,Diode}} + E_{\text{OFF,Diode}}) \cdot f_{\text{sw}} \quad (7)$$

where E_{ON} and E_{OFF} are the switching energies for the components that are a function of the current through the component and the switched voltage and are estimated using datasheet curves, and f_s is the switching frequency of the component. The switching loss, therefore, requires the knowledge of the current, switched voltage, and the switching frequency of the component. Again, the loss is further dependent on the junction temperature and a linear interpolation is used to calculate the loss for the component.

E. Thermal Model

The thermal model used in this paper is based on [29] and [31]. This model combines Cauer and Foster thermal networks to address shortcomings of both models and is shown in Fig. 10.

F. Calculation of Lifetime

1) *Lifetime Model*: The lifetime model used in this paper is based on the work by Bayerer *et al.* [32]. The number of cycles to failure is given as

$$N_f = A \cdot \Delta T_j^{\beta_1} \cdot e^{\frac{\beta_2}{T_j + 273}} \cdot t_{\text{ON}}^{\beta_3} \cdot I^{\beta_4} \cdot V^{\beta_5} \cdot D^{\beta_6} \quad (8)$$

where A is a technology factor, ΔT_j is the amplitude of the thermal cycling, T_j is the mean junction temperature, t_{ON} is the pulse duration, I is the current per wire, V is the blocking voltage of the chip, and D is the diameter of the bonding wire. The impact of these factors is represented by power laws with exponents β_1 – β_6 . Here, the exponential factors used are, $\beta_1 = -4.416$, $\beta_2 = 1.285 \times 10^3$, $\beta_3 = -0.463$, $\beta_4 = -0.716$, $\beta_5 = -0.761$, and $\beta_6 = -0.5$. The value of A depends on the type of switch, $A = 2.03 \times 10^{14}$ for standard packages and $A = 9.34 \times 10^{14}$ for IGBT4 modules [33].

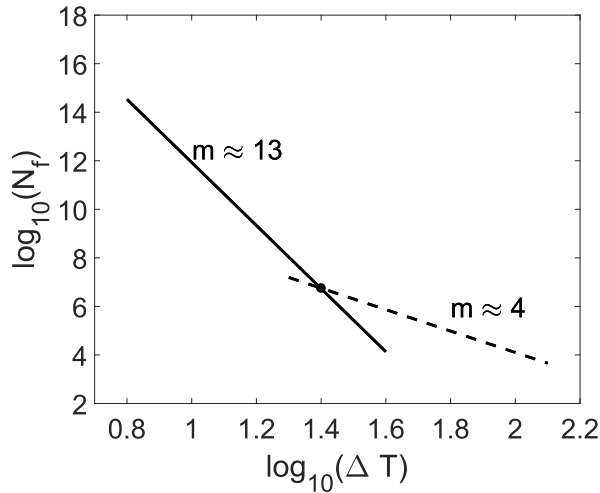


Fig. 11. Lifetime model. From [32], [34].

The experiments on which this lifetime model is based, use a minimum junction temperature cycling of approximately 40 K. The extension of this model, to cycling amplitudes much below this value, could introduce a large error in the results. Therefore, this model has been extended based on the work by Kovacevic-Badstuebner *et al.* [34]. The updated model has two asymptotic linear dependencies in a log–log plot. One is for low-amplitude cycling ($m \approx 13$) and the other derived from the Bayerer model discussed earlier for large-amplitude cycling ($m \approx 4$). This is shown in Fig. 11. The use of this updated lifetime model increases the accuracy of the lifetime prediction and, therefore, results in a more realistic comparison.

2) *Calculation Procedure:* The lifetime calculation in this paper involves analyzing the system for wind profiles with two different time scales (shown schematically in Fig. 12).

- 1) *Long-Duration Profile:* This uses the annual wind profile with wind speed averaged over 10 min periods. As the 10-min period is large enough for the wind turbine drivetrain to have reached an equilibrium, the steady-state model is used to generate a temperature profile. This profile is used to calculate the damage (or lifetime) due to the long-duration profile.
- 2) *Short-Duration Profile:* This uses stochastic 10-min profiles. The profiles are generated such that each has a particular mean wind speed (the number of profiles depends on the number of bins in the selected Weibull distribution). These profiles represent the wind speed variation within 10 min over which the measured wind speed is averaged and recorded.

The short-duration profiles are used in conjunction with the dynamic model of the drivetrain to generate the temperature profile of the semiconductors. This temperature profile is used to calculate the damage due to each 10-min profile. This damage along with the frequency of occurrence of the respective 10-min profile is used to calculate the net consumed lifetime for the short-duration profiles.

G. Limitations of the Study

There are a number of assumptions taken in this paper that may give rise to inaccuracy in the results. However, we believe that the results presented in this paper remain a good indication of the lifetime performance of the topologies considered, especially with regard to a comparative study.

- 1) *Thermal Effect of IGBT on Diode and Vice Versa:* In the modules considered, the IGBT and the antiparallel diode are part of the same package and share the baseplate. This would mean that the losses of the IGBT would influence the temperature of the diode junction and vice versa. However, the thermal model used has not considered this effect. This would lead to the introduction of error but as the model considers the effect of these two components on each other through the heat sink, this inaccuracy is minimized.
- 2) *Disturbances:* The model used in this paper neglects grid disturbances as well as the effect of wind gusts. Therefore, the results obtained do not consider these aspects as well.
- 3) *Reactive Power:* In this paper, a constant power factor of 0.9 for the grid-side converter is considered. Apart from increasing losses with the increase in reactive power required by the grid, varying reactive power is another source of power cycling and can, therefore, affect lifetimes. However, these effects have not been considered in this paper.

IV. COMPARISON OF TOPOLOGIES

The comparison of topologies presented in this paper is based on three aspects—the distribution of losses, the thermal performance, and the lifetimes of the power semiconductors. As the paper focusses on the power semiconductors, it does not consider the effects (or lifetimes) of the other components of the converter. Furthermore, as reliability can be linked to the reliability of the most stressed or weakest component, the focus of this paper is the reliability of its most stressed power semiconductor component.

A. Loss Distribution

A topology that distributes the stresses more evenly amongst its power semiconductors would result in a higher lifetime of the weakest (or the most stressed) power semiconductor, therefore, the loss distribution amongst the components is an important consideration. Figs. 13 and 14 show the distribution of losses amongst the power semiconductor components, in both the generator- and grid-side converters, for an operating point with an average wind speed equal to 12 m/s. In these figures, the 3L-T2C losses are for a set of two parallel converters to keep the rating of the compared topologies equal. However, the 2L-VSC losses are for a single converter (therefore, half the rating of the rest) so that its results do not skew the scale of the figures.

1) Grid-Side Converter:

a) *3L-NPC:* For the 3L-NPC converter, the outer switches (T1 and T4) experience the most losses. The inner IGBTs suffer the most conduction losses as they conduct during both positive and neutral states. However, the switching

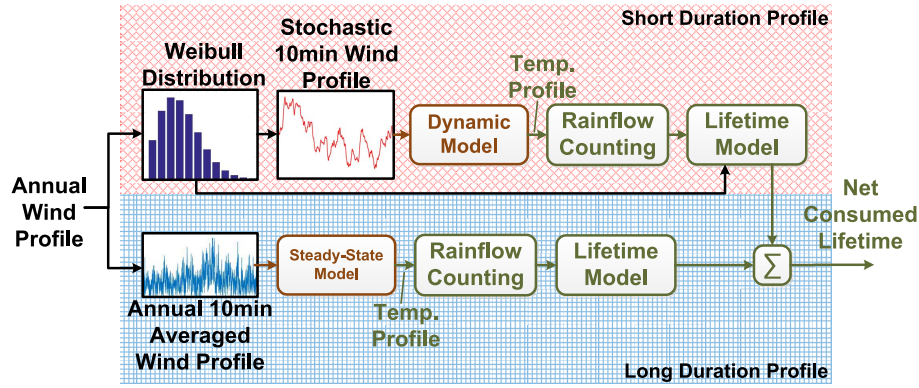
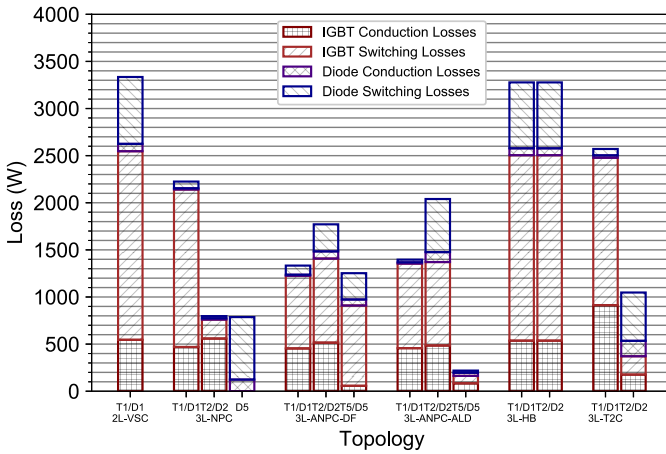
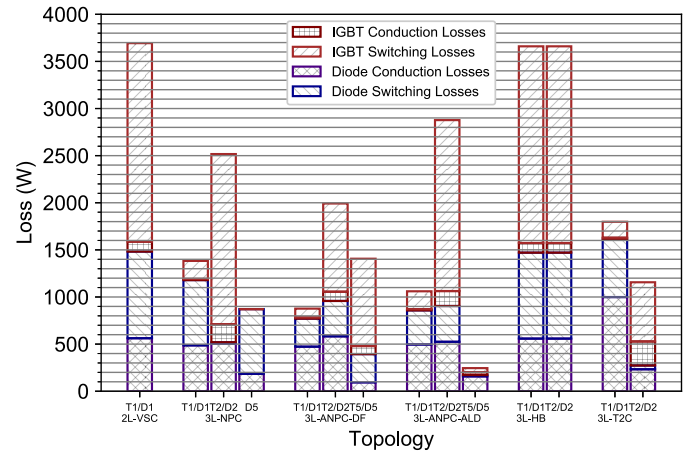


Fig. 12. Lifetime calculation procedure.


 Fig. 13. Loss distribution for the grid-side converter with $v_{wind} = 12$ m/s.

 Fig. 14. Loss distribution for the generator-side converter with $v_{wind} = 12$ m/s.

losses of the outer switches are significantly higher than those of the inner modules. This highlights the problem of inequality of loss distribution.

b) 3L-ANPC-DF: In the DF strategy of the ANPC converter, the halving of switching frequency creates a better distribution of losses among the components. As a result of this switching technique, the switching losses of the active switches increase but their losses remain lower than those of the other two types of switches. The resulting losses are more evenly distributed.

c) 3L-ANPC-ALD: In the ALD strategy, a 25%–75% of stress-in/stress-out has been chosen for the grid-side converter. The choice of this factor depends on a number of factors, such as power factor, current, and voltage. This selection has been made so that the total losses of the most heavily loaded components (in this case, the inner and outer IGBTs) are as balanced as possible. As a result, the switches are observed to have the best distribution of losses among the tested topologies. The neutral point clamping modules switch with voltage frequency, and thus are lightly stressed compared to the other types of switches.

d) 3L-HB: For this converter, even though the losses are optimally distributed among the switches, the magnitude of losses is higher compared to other topologies. This is due to

the larger conduction times as well as the continuous switching during both voltage cycles.

e) 3L-T2C: Here, the components with the heaviest loading are the outer switches which also have a higher voltage rating. However, because these switches switch at only half the dc-link voltage, the losses are reduced when compared to the 2L-VSC.

2) Generator-Side Converter:

a) 3L-NPC: For the 3L-NPC converter, the largest part of losses is at the inner modules (T2/D2 module). However, the conduction losses are now better distributed between the inner diodes and IGBTs.

b) 3L-ANPC-DF: In the DF strategy of the ANPC generator-side converter, the smaller switching frequency has the same impact as in the grid-side converter. Switching losses are also shared between the inner and outer modules. However, when it comes to the inner power module, the diode is taking most of the conduction losses. This makes the inner diode the most heavily loaded component of the converter.

c) 3L-ANPC-ALD: In the ALD strategy of the generator-side converter, a 33%–67% stress-in/stress-out strategy has been chosen. This selection has again been made in an attempt to balance the losses between the most heavily loaded components. Therefore, the total amount of the distributable

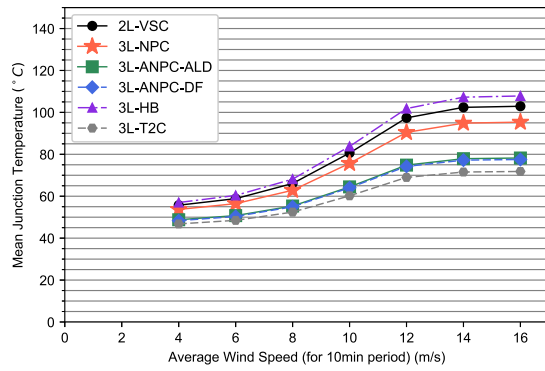


Fig. 15. Mean temperatures—grid-side converter.

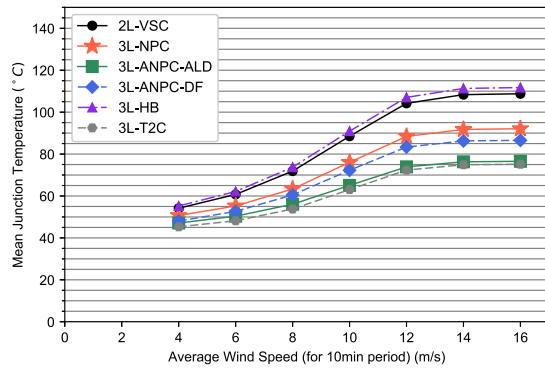


Fig. 16. Mean temperatures—generator-side converter.

switching losses loads the outer switches in order to relieve the inner module that displays the largest part of dissipated losses. Even though the inner module still experiences the largest losses, the distribution among the individual parts of each module is improved.

d) 3L-HB: Again, for the 3L-HB converter, even though the losses are almost optimally distributed among the switches, the amount of losses is higher than that in the other converters.

e) 3L-T2C: In the 3L-T2C converter, although the inner switch has large losses, the poorer thermal properties of the outer diode couple with the large losses making them also heavily loaded.

B. Thermal Performance

The thermal response of the power semiconductors to the losses that they are subjected to is closely linked to their reliability. In particular, the junction temperature and the amplitude of temperature cycling affect the lifetime of the power semiconductor as seen in (8). For the comparison here, two quantities are being compared: the mean temperature for each converter over a 10-min period and the range of temperature cycle amplitudes. Furthermore, this comparison is presented for the most stressed power semiconductor of each topology. These quantities for the grid-side converter are shown in Figs. 15 and 17, while those for the generator-side converter are presented in Figs. 16 and 18.

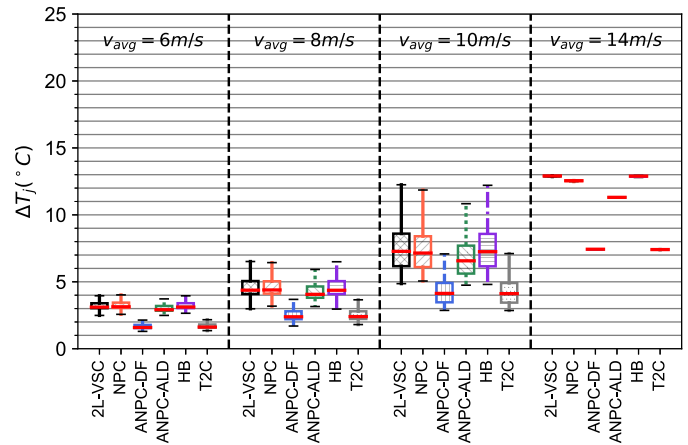


Fig. 17. Distribution of temperature cycling amplitudes for the grid-side converter.

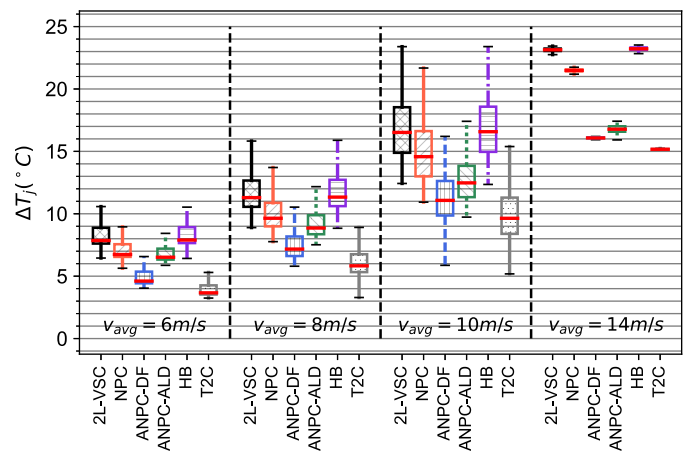


Fig. 18. Distribution of temperature cycling amplitudes for the generator-side converter.

The 2L-VSC develops high mean temperatures as well as high temperature cycle amplitudes both in the grid and the generator sides. In the 3L-ANPC topologies, the improvement in the distribution of losses is reflected in the temperature profiles, resulting in a lower mean temperature as well as lower temperature cycling amplitudes. Even though the 3L-HB displays an excellent distribution of losses amongst its components, compared to other topologies, the amount of losses increases the mean temperature and cycling amplitude. Finally, the 3L-T2C also shows low mean temperatures and lower temperature cycling amplitudes.

In all cases, the loading of the generator-side converter is higher, which is attributed to the lower frequency of the generator side that accounts for higher temperature cycling amplitude being attained as well as the poorer thermal characteristics of the diode that takes a bulk of the load in the generator-side converters.

C. Lifetime

Following the analysis of the thermal performance of the examined converters, the temperature profiles generated for the different wind profiles are used as an input to the lifetime

TABLE VIII
COMPARISON OF LIFETIMES OF THE MOST STRESSED POWER SEMICONDUCTORS. X AND Y REPRESENT THE LIFETIMES FOR THE 3L-NPC CONVERTER

Topology Lifetimes (in years)					
	Grid Side Converter		Generator Side Converter		Annual Losses (GWh)
2L-VSC	5.15	$(\frac{X}{1.71})$	0.51	$(\frac{Y}{3.13})$	1.54
3L-NPC	8.80	(X)	1.61	(Y)	0.95
3L-ANPC-DF	57.49	$(6.53X)$	11.85	$(7.37Y)$	0.96
3L-ANPC-ALD	48.16	$(5.47X)$	8.31	$(5.17Y)$	0.86
3L-HB	3.93	$(\frac{X}{2.24})$	0.46	$(\frac{Y}{3.52})$	1.50
3L-T2C	110.08	$(12.50X)$	32.16	$(20.02Y)$	1.13

TABLE IX
COMPARISON OF LIFETIMES OF THE MOST STRESSED POWER SEMICONDUCTORS. X AND Y REPRESENT THE LIFETIMES FOR THE RATED 3L-NPC CONVERTER

Topology Lifetimes (in years)					
	Grid Side Converter		Generator Side Converter		Annual Losses (GWh)
3L-ANPC-DF	57.49	$(6.53X)$	11.85	$(7.37Y)$	0.96
3L-T2C	110.08	$(12.50X)$	32.16	$(20.02Y)$	1.13
1.25 x 3L-NPC	28.33	$(3.22X)$	14.83	$(9.23Y)$	1.00
1.50 x 3L-NPC	63.69	$(7.24X)$	46.51	$(28.95Y)$	1.05

model. The individual consumed lifetimes for each mean wind speed profile are multiplied by the frequency of occurrence (based on the Weibull distribution in Fig. 8) and added to give the total life consumption for a period of one year. In the lifetime model, the damage is assumed to be linear and the sequence at which the power and temperature cycles occur do not have any effect according to Palmgren–Miner’s rule

$$LC = \sum_{i=1}^k \frac{n_i}{N_i} \quad (9)$$

where N_i is the lifetime for the i th load, n_i is the number of cycles the component has been exposed to the i th load profile, and k is the total number of load profiles. To this, the consumed lifetime based on the long-duration profile (using the annual 10-min averaged wind speed profile) is added. Failure occurs when the lifetime consumption LC equals one. Table VIII gives the lifetimes of the most stressed power semiconductors of each topology, both in terms of years as well as a factor in relation to the 3L-NPC topology. It also shows the annual semiconductor power loss.

It is important to state that although all the modeling-related choices and assumptions have been made so that the drivetrain model is a suitable design for a 10-MW wind turbine; there are a number of limitations when calculating the absolute lifetime of the topologies in terms of years (see Section III-G). As a result, the consumed lifetime values of each converter topology should not be considered in absolute terms; however, the fact that all the simulations and calculations are executed based on

the same references offers a solid basis upon which a fruitful reliability comparison can be conducted.

It is noted that there is a consistency between the thermal response of the power semiconductors and their reliability. The switches or diodes that display high temperatures and large temperature cycles have been proved to have a smaller expected lifetime. The results show that the 3L-ANPC topology with the DF and ALD switching strategies, and the T2C topology show a large improvement over the 2L-VSC, 3L-HB, and the 3L-NPC. In both these cases, the improvement in the grid side is larger than that of the generator-side converter.

D. Effect of Overrating

The lifetime performance with the use of overrated topologies (3L-ANPC and 3L-T2C) has been explored in Section IV-C. This comparison was based on designs with the same total power rating. Another possibility is the use of overrated components, which is explored in this section. As the 3L-NPC is a popular converter topology for high-power wind turbine generator systems, it is important to consider the effect of overrating this converter.

This comparison is done for a 1.25 and a 1.5 times overrated NPC topology (resulting in a five and six parallel converter systems) with the 3L-ANPC-DF and 3L-T2C converter topologies (with four parallel converters). The 1.5 times rated NPC topology results in a net IGBT rating (VA) equal to that of the 3L-ANPC and 3L-T2C topologies but a 50% overrating

of the diodes. The IGBT VA rating is another benchmark for comparison and the $1.5 \times 3L$ -NPC topology is equal to the 3L-ANPC and 3L-T2C topologies in this aspect. Also, as the VA rating is an indicator of cost, this benchmark can be used as an indicator for power semiconductor cost. The resultant lifetimes for this comparison are given in Table IX.

These results also show that overrating the components of the 3L-NPC leads to a large improvement in lifetime performance. The use of the $1.25 \times 3L$ -NPC results in a grid and generator-side lifetime that is about 3 and 9 times than that of the rated 3L-NPC, and this increases to 7 and 29 times when a $1.5 \times 3L$ -NPC is considered. The calculated lifetimes for the 1.5 times overrated 3L-NPC topology has the highest lifetimes, except for the grid side of the T2C topology. However, the loss performance of the 3L-ANPC remains better than that of the overrated NPC topologies. The reduced losses in the power semiconductors would result in an approximately 0.1% increase in the annual energy production.

V. CONCLUSION

This paper has compared the lifetime performance of the power semiconductors in a number of three-level topologies for the use in the wind turbine drivetrain. This comparison has been done on the basis of loss distribution, thermal performance, and a final lifetime number.

It has been found that in a comparison of different three-level topologies, the 3L-ANPC and the 3L-T2C show the highest lifetimes. When a component overrating is considered, the 3L-NPC topology shows a large improvement and the lifetime performance is comparable to that of the overrated topologies. However, the loss performance of the 3L-ANPC remains marginally better than the other cases considered in this paper.

In conclusion, the use of overrating—be it in the form of overrated topologies (like the ANPC and the T2C), or the use of overrated components—is successful in improving the lifetime performance of power semiconductors in converters. However, the improvement offered by overrated topologies over the use of overrated components is not significant and it is unlikely to replace the current practice of using overrated components.

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