On-chip integration of Si/SiGe-based quantum dots and electronic circuits for scaling

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Publication date
2021

Document Version
Final published version

Citation (APA)
Xu, Y. (2021). *On-chip integration of Si/SiGe-based quantum dots and electronic circuits for scaling*. [Dissertation (TU Delft), Delft University of Technology].

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ON-CHIP INTEGRATION OF SI/SIGE-BASED QUANTUM DOTS AND ELECTRONIC CIRCUITS FOR SCALING

Dissertation

for the purpose of obtaining the degree of doctor
at Delft University of Technology
by the authority of the Rector Magnificus, Prof.dr.ir.T.H.J.J. van der Hagen,
chair of the Board for Doctorates
to be defended publicly on
Monday 22 November 2021 at 10:00 o'clock

by

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Keywords: floating gate, quantum dots, integration, scalability

Printed by: Gildeprint

Cover designed by: Fan Zheng

ISBN 978-94-6419-370-1

An electronic version of this dissertation is available at
http://repository.tudelft.nl/.

CONTENTS

SUMMARY

With continuous breakthroughs in quantum science and technology in recent years, the development of quantum computers is moving from pure scientific research to engineering realization. Meanwhile, the underlying physical structures also develop from the initial single qubit to multiple qubits or medium-scale qubit registers. Since qubits are operated by many sophisticated instruments under strict environmental conditions, people need a scalable solution to support many qubits working at the same time, so as to achieve high computing speed for a practical quantum computer.

The physical qubits we discuss in this study are realized by spin states of electrons confined in Si/SiGe based quantum dots, which has good compatibility with the semiconductor fabrication technology. We focus on the wiring bottleneck for scaling the qubits. Specifically, in a normal operation mode, every qubit requires at least one wire connected to the control electronics at higher temperature stages. When scaling towards a fault-tolerant quantum computer, which needs hundreds of thousands of quantum dots, simply adding more wires and electronics would face space constraints in the connection from the sample to the sample carrier and dilution refrigerator. To reduce the number of wires needed, we explore a DRAM-like circuit to bias the quantum dot gates. A single voltage supply line connected at the input of a demultiplexer can provide different voltages to several DRAM-like cells sequentially, while the switched-capacitor circuits are used to float the gate of the dots, isolate them from the voltage supply, and store the voltage locally on the capacitors. We aim for all the elements to be integrated on Si/SiGe based substrate and functional at the same cryogenic temperature as the dots.

As a proof of concept, we make devices with a floating plunger gate of a single quantum dot. We develop processes to monolithically fabricate parallel plate capacitors, transistors and quantum dot devices on a Si/SiGe heterostructure. The processes combine electron-beam and photolithography to define tens of nanometer and micrometer scale structures, respectively. We discuss temperature limitations to prevent strain relaxation in the substrate while having a functional doping area. Furthermore, we compare several dielectric materials to make gate oxide with fewer defects and lower leakage current.

Then we characterize discrete transistors and quantum dots before the measurement of combined devices. We first simulate the temperature dependency of transistor threshold voltage and field-effect mobility. Then we measure the transfer and output curves from several batches of devices along with the process development. We observe a higher turn-on voltage and higher field-effect mobility for transistors working at cryogenic temperatures as expected. We also notice a hysteresis when scanning to higher voltages. Thus, defining a stable operation range is necessary. Besides, We measure single quantum dots without floating gates to obtain their bias voltage range and charging energy.

After that, we measure the devices that combine a switched-capacitor circuit and a single quantum dot. We observe Coulomb peak shifts in voltage between the static

and floating test mode. We analyze the parameters that affect the offsets by comparing devices with different transistor and capacitor sizes. The device with the largest capacitance and smallest transistor channel provides the least systematic offsets. The random components in the offsets are mainly introduced by the 1/f noise. In addition, we apply a pulsed voltage to one of the quantum dot gates while floating another gate. We extract Coulomb peaks corresponding to the high and low voltage levels of the pulses and find that the electrochemical potential of the quantum dot can follow the voltage pulses, which is essential for applying the floating gate strategy in qubit experiments.

We move on to discuss designs for demultiplexers connected to a quantum dot array. The structure of an on-chip integrated demultiplexer depends on the demultiplexing signal and the available technology given the constraints of integration with quantum dots. Furthermore, a sparse dot array is proposed to provide more space for the electronic circuits on-chip. Taking a specific unit cell design for concreteness, we calculated the required number of signal lines and power dissipation under general assumptions.

This work shows that integrating a DRAM-like floating gate structure with quantum dots on-chip has the potential to overcome the wiring bottleneck in scaling. In the end, we discuss some alternative approaches for biasing a large number of quantum dot gates with a reduced number of wires.

SAMENVATTING

Met voortdurende doorbraken in kwantumwetenschap en -technologie in de afgelopen jaren, gaat de ontwikkeling van kwantumcomputers van puur wetenschappelijk onderzoek naar technische realisatie. Ondertussen ontwikkelen de onderliggende fysieke structuren zich ook van de eerste enkele qubit tot meerdere qubits of middelgrote qubitregisters. Omdat qubits worden bediend door veel geavanceerde instrumenten onder strikte omgevingsomstandigheden, hebben mensen een schaalbare oplossing nodig om veel qubits tegelijkertijd te ondersteunen, om een hoge rekensnelheid te bereiken voor een praktische kwantumcomputer.

De fysieke qubits die we in deze studie bespreken, worden gerealiseerd door spintoestanden van elektronen die zijn opgesloten in op Si/SiGe gebaseerde kwantumdots, die goed compatibel zijn met de halfgeleiderfabricagetechnologie. We richten ons op de bedradingsbottleneck voor het schalen van de qubits. In een normale bedrijfsmodus vereist elke qubit met name ten minste één draad die is aangesloten op de besturingselektronica bij hogere temperatuurtrappen. Bij het opschalen naar een fouttolerante kwantumcomputer, die honderdduizenden kwantumdots nodig heeft, zou het eenvoudigweg toevoegen van meer draden en elektronica te maken krijgen met ruimtebeperkingen in de verbinding van het monster naar de monsterdrager en verdunningskoelkast. Om het aantal benodigde draden te verminderen, onderzoeken we een DRAM-achtig circuit om de quantum dot-poorten te beïnvloeden. Een enkele voedingslijn aangesloten op de ingang van een demultiplexer kan achtereenvolgens verschillende spanningen leveren aan verschillende DRAM-achtige cellen, terwijl de circuits met geschakelde condensatoren worden gebruikt om de poort van de stippen te laten zweven, ze te isoleren van de voedingsspanning en op te slaan de spanning plaatselijk op de condensatoren. We streven ernaar dat alle elementen worden geïntegreerd op Si/SiGe-gebaseerd substraat en functioneel zijn bij dezelfde cryogene temperatuur als de stippen.

Als proof of concept maken we apparaten met een zwevende plunjerpoort van een enkele kwantumdot. We ontwikkelen processen om monolithisch parallelle plaatcondensatoren, transistors en quantum dot-apparaten te fabriceren op een Si/SiGe-heterostructuur. De processen combineren elektronenstraal en fotolithografie om respectievelijk tientallen nanometer- en micrometerschaalstructuren te definiëren. We bespreken temperatuurbeperkingen om spanningsrelaxatie in het substraat te voorkomen terwijl we een functioneel dopinggebied hebben. Verder vergelijken we verschillende diëlektrische materialen om poortoxide te maken met een lagere lekstroom en minder defecten.

Vervolgens karakteriseren we discrete transistoren en kwantumdots vóór de meting van gecombineerde apparaten. We simuleren eerst de temperatuurafhankelijkheid van transistordrempelspanning en veldeffectmobiliteit. Vervolgens meten we de overdrachts- en uitvoercurves van verschillende batches apparaten samen met de procesontwikkeling. We zien een hogere inschakelspanning en een hogere veldeffectmobiliteit voor transistors die werken bij cryogene temperaturen zoals verwacht. Ook merken we een

hysterese bij het scannen naar hogere spanningen. Het definiëren van een stabiel werkbereik is dus noodzakelijk. Bovendien meten we enkele kwantumdots zonder zwevende poorten om hun voorspanningsbereik en laadenergie te verkrijgen.

Daarna meten we de apparaten die een geschakeld condensatorcircuit en een enkele kwantumdot combineren. We observeren Coulomb-piekverschuivingen in spanning tussen de statische en zwevende testmodus. We analyseren de parameters die de offsets beïnvloeden door apparaten met verschillende transistor- en condensatorformaten te vergelijken. Het apparaat met de grootste capaciteit en het kleinste transistorkanaal zorgt voor de minste systematische offsets. De willekeurige componenten in de offsets worden voornamelijk geïntroduceerd door de 1/f-ruis. Bovendien passen we een gepulseerde spanning toe op een van de quantum dot-poorten terwijl we een andere poort laten zweven. We extraheren Coulomb-pieken die overeenkomen met de hoge en lage spanningsniveaus van de pulsen en ontdekken dat de elektrochemische potentiaal van de kwantumdot de spanningspulsen kan volgen, wat essentieel is voor het toepassen van de zwevende poortstrategie in qubit-experimenten.

We gaan verder met het bespreken van ontwerpen voor demultiplexers die zijn aangesloten op een kwantumdot-array. De structuur van een on-chip geïntegreerde demultiplexer hangt af van het demultiplexsignaal en de beschikbare technologie gezien de beperkingen van integratie met kwantumdots. Verder wordt een spaarzame dot-array voorgesteld om meer ruimte te bieden voor de elektronische schakelingen op de chip. Met een specifiek eenheidscelontwerp voor concreetheid, hebben we het vereiste aantal signaallijnen en vermogensdissipatie berekend onder algemene aannames.

Dit werk laat zien dat het integreren van een DRAM-achtige zwevende poortstructuur met kwantumdots op de chip het potentieel heeft om het bedradingsprobleem bij het schalen te overwinnen. Uiteindelijk bespreken we enkele alternatieve benaderingen voor het voorinstellen van een groot aantal quantum dot-poorten met een verminderd aantal draden.

1

INTRODUCTION

A quantum computer is a machine that performs computation using the principles of quantum mechanics. The concept was first proposed by Richard Feynman in the 1980s. Prior to that, quantum physics had been developed for more than half a century. Feynman mentioned that nature is not classical, so it is better to use quantum mechanical systems to simulate quantum phenomena[1]. Although this idea became the quantum simulation branch later, quantum computers started to develop as an important application of quantum technology since then.
Quantum computers have received widespread attention in recent years because of their powerful computing capabilities in specific fields. Unlike classical computers that encode data with bits (either 0 or 1), quantum computers use quantum bits (qubits) based on the principle of superposition, allowing 0 and 1 to exist simultaneously. As a result, it requires 2^n complex amplitudes to describe the state of n qubits. This offers quantum computers a significant advantage in data processing. They are able to solve problems that classical computers cannot solve efficiently, such as factoring very large numbers[2, 3]. In addition, since the 1970s, the density of transistors and computing power roughly doubled every two years following Moore's Law. However, with the device sizes further reduced to 5-7 nanometer scale, the influence of quantum effects, such as transistor gate leakage due to quantum tunnelling, became serious. The updating speed of new devices in the semiconductor industry is therefore slowing down[4–7]. People expect the development of quantum computers to be one of the solutions to the continuation of ever increasing computing power.

1.1. INTERFACING SPIN QUBITS IN QUANTUM DOTS

A qubit is the basic unit of information in a quantum computer. At present, its physical implementation is inconclusive. There are several promising options including superconducting qubits[8, 9], spin qubits in quantum dots[10, 11], trapped ions[12, 13], position-based charge qubits [14, 15] and so on. People in general use the DiVincenzo

criteria to evaluate a physical qubit system, which describes that qubits need to have long coherence times, a universal gate set, be able to be initialized and read out. In addition, they are also required to have a good scalability [16]. That is, firstly, the properties of single qubits remain the same as the number of qubits grows. Secondly, a scalable interface between qubits and classical electronics to properly address and control each particular qubit [17].

The qubits we focus on in this study is implemented by the spin of single electrons in quantum dots (QDs). To form the quantum dots, voltages are applied to metal gates to define the potential landscape in the semiconductor substrate[18]. Such spin qubits hold the advantage of good compatibility with current semiconductor fabrication techniques and potential for easy integration with classical electronics[19–21]. Spin qubits based on Si/SiGe substrates have already been demonstrated to satisfy most of the DiVincenzo criteria [22–26]. Their promising results prompt people to investigate strategies to control a large number of qubits.

Since qubits are very sensitive to thermal noise, they generally work at temperatures around 10 mK in a dilution refrigerator. To further avoid errors during computation, quantum error correction algorithms are introduced, which needs thousands of physical qubits to encode one logical qubit. Therefore, it is estimated that millions of physical qubits are required to build a fault-tolerant quantum computer [27, 28]. Connecting signal lines of each qubit from the coldest plate in the refrigerator directly to electronic instruments at room temperature would lead to fan-out and routing issues. Besides, excessive heat would be introduced through signal lines to quantum devices. Many solutions are proposed to solve these problems in scaling, including making hot qubits that working at temperatures in the 1-4 K range[29, 30] or bringing down the front-end of control electronics to deep-cryogenic temperature stages [31, 32]. One possible strategy is depicted in Fig.1.1 [33]. Groups of spin qubits are arranged in dense two-dimensional arrays and controlled using a cross-bar addressing scheme (we will discuss it in detail in the next section). Then these arrays are sparsely placed and communicate via long-range qubit couplers[34–37]. Such a layout provides more space for electronics on-chip and routing. The functions of the integrated electronics depend on the actual space and thermal budget. Demultiplexers would be a priority since they can effectively reduce the number of wires going off the chip. Besides, analog to digital converters (ADC), digital to analog converters (DAC), and vector modulation are also expected in close proximity for a more compact quantum computing system [38, 39].

1.2. CROSS-BAR ADDRESSING AND CHARGE-LOCKING

For every dot in a typical quantum dot array, one gate controls the electrochemical potential and a second controls the tunnel barrier to the next dot in the array. Even if quantum dots are designed to be identical, the required gate bias voltage still differs among the dots due to non-uniformities in the substrate and variations during the fabrication process. With a small number of quantum dots, each gate is connected to a separate room temperature DAC through the bond wires from the chip to the sample carrier and the dilution refrigerator wiring. However, this linear approach poses a bottleneck in scaling. By comparison, today's classical processor has billions of transistors integrated and operated on a single chip, while only about 2000 contact pins are used for the in-

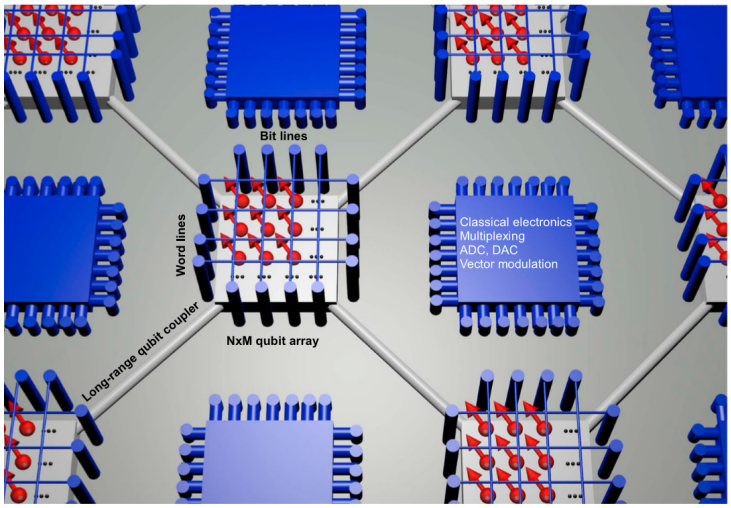

Figure 1.1: Dense qubit arrays are placed sparsely to leave spaces for on-chip electronics. The arrays are addressed locally by bit and word lines. Communication among the qubit blocks is via long-range qubit couplers. The operating temperature is considered to be four Kelvin given the heat generated by the electronic circuits and the current cooling power of a dilution refrigerator [33].

put/output signals. This large ratio between active components and pins is described by Rent's rule and is made possible by implementing shared control methods[40]. In order to operate the millions of qubits for practical quantum computation, similar methods will therefore have to be implemented in quantum integrated circuits.

Inspired by the matrix of dynamic random access memory (DRAM) that uses word lines and bit lines to address a large number of storage cells [42], proposals for controlling spin qubits using the cross-bar structure exist [41, 43, 44]. Another concept that can be borrowed from classical electronics is charge-locking. In DRAM, the stored voltage encodes a "0" or "1", according to a threshold. In contrast, the voltage maintained on a quantum dot gate needs to be a precise analog value. The required precision of such a stored voltage ranges from 1 μV to 1 mV, depending on the gate function and coupling of the gate to the dot potential. Charge-locking is thus used in the form of a sample-and-hold circuit. When the input line is electrically detached, the gate of the quantum dot is floating and the voltage maintains there for a certain period. Figure 1.2 is an example that uses the cross-bar scheme and charge-locking circuit to address a spin qubit matrix from the third dimension[41].

Although the primary role for DC gates of quantum dots is to achieve electron confinement, additional voltage pulses must be applied to these gates for qubit experiments. For example, in a commonly used single-shot read-out method to determine the state of an electron spin, a few kHz signal is applied to the gate to load, read and empty a quantum dot [45, 46]. When an electronic circuit is integrated with these gates as an interface, the extra transistor or capacitor should not affect the voltage pulses arriving at the quantum dot gates. Prototypes have been made with on-chip or off-chip integrated floating gate circuits and GaAs quantum dots [47, 48]. For silicon-based quantum dots,

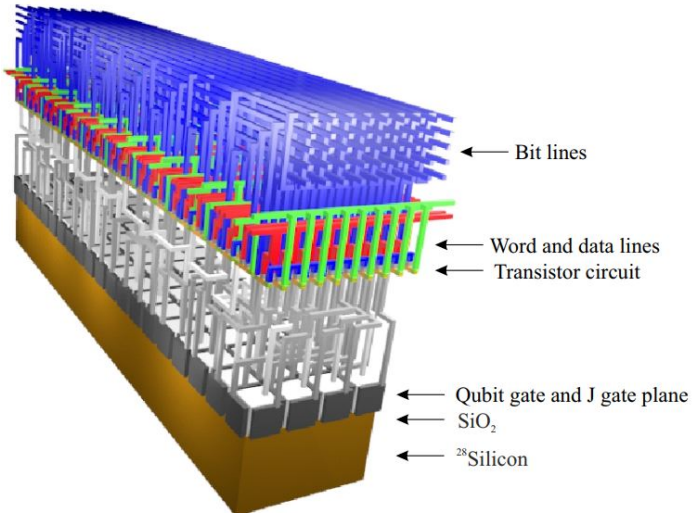

Figure 1.2: Architecture of a quantum-classical interface. The bottom purified silicon layer (^{28}Silicon) hosts qubits, which are controlled by metal gates isolated by the SiO_2 layer. Signals to the qubit gates are transferred through the cross-bar structure and switched-capacitor circuits in the higher layers [41].

switching circuits have been integrated with quantum devices on-chip [49, 50]. In addition, charge-storage devices and quantum devices have been fabricated using the same CMOS process and connected through wire bonds [51, 52]. However, a fully on-chip integrated solution, without the need for wire bonds, is still waiting to be achieved.

1.3. MAIN DEVICE IN THIS STUDY

In this study, we implement a switched-capacitor (SC) circuit for charge-locking and use it to float the plunger gate of a single quantum dot. Here we integrate the circuit and the dot on a Si/SiGe-based substrate. The device schematic is shown in Fig.1.3. The SC circuit contains an n-type transistor FET_1 and a parallel-plate holding capacitor C_H. The accumulation ($A1$ and $A2$), barrier ($B1$ and $B2$) and T gates of the QD are connected to voltage sources at room temperature in the later experiments. (We introduce the quantum dot structure in detail in Section 2.1.1. The layout and cross-section of the combined device are provided in Section 3.1.) Gate P is connected to the output of the SC circuit. It is regarded as a floating gate in the following contents. We analyze the parameters that affect the variability of the floating gate voltage and experimentally study the impact of the size of the capacitor and the transistor. In addition, we apply a pulsed voltage to one of the quantum dot gates while floating another gate, as a relevant test for qubit measurements.

1.4. THESIS OUTLINE

After the introduction in Chapter 1, background information is provided in Chapter 2. Here we review the working principle of spin qubits and switched-capacitor circuits, fol-

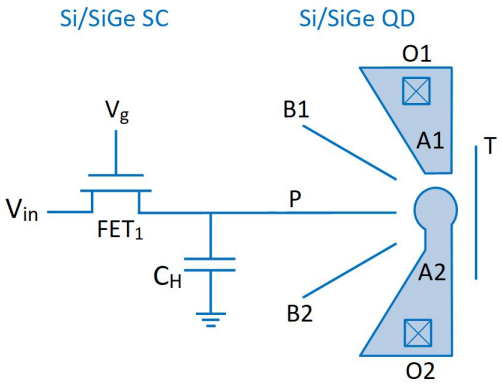

Figure 1.3: Schematic of a device fabricated in this study, a switched-capacitor circuit is connected to gate *P* of a single quantum dot.

lowed by considerations of voltage accuracy on the floating node and power consumption of the device.
In Chapter 3, we firstly give an overview of the device fabrication process. Then a few parameters are discussed in detail including the temperature limitation during the process, conditions to activate the implantation areas and options for the dielectric layers. Setups for the device measurements are also introduced here.
Chapter 4 starts with a discussion about transistor temperature dependence. Then we present results of the characterization on separated quantum dots, transistors and capacitors from several batches.
Results of the combined devices are reported in Chapter 5. We analyze the parameters that affect the variability of the floating gate voltage. After that, we check the dot potential modulation in response to a voltage pulse while the dot is partially floating.
In Chapter 6, we discuss structures for the demultiplexer, followed by a proposal for a sparse quantum dot array, intended to allow for scaling up to one million qubits. Taking a unit cell from the array, we particularly discuss its line scaling and heat dissipation.
Finally, we conclude in Chapter 7 and propose future works.

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2

BACKGROUND

To make an interface between quantum devices and classical electronics, we provide background information on both aspects. We start with a brief introduction to electron spin qubits. The quantum dot structure and readout scheme that are relevant to the following chapters are described in detail. Then we move on to the switched-capacitor circuits. We discuss the relationship between the floating voltage accuracy and device sizes. In the end, we mention a method to estimate the power dissipation of a switched-capacitor circuit.

2.1. ELECTRON SPIN QUBITS IN QUANTUM DOTS

A qubit is a two-level quantum system. In this study, it is implemented with the spin of an electron in a static magnetic field, which takes spin up and spin down as the two basis states, represented by $|0\rangle$ and $|1\rangle$ below. The superposition state of a qubit can be described as

$$|\psi\rangle = \alpha|0\rangle + \beta|1\rangle. \tag{2.1}$$

Since the coefficients α and β are complex numbers that satisfy $|\alpha|^2 + |\beta|^2 = 1$, the state can be rewritten as[1]

$$|\psi\rangle = \cos\frac{\theta}{2}|0\rangle + e^{i\varphi}\sin\frac{\theta}{2}|1\rangle \tag{2.2}$$

with $\theta \in [0,\pi]$ and $\varphi \in [0,2\pi)$. Hence, a single qubit can be visualized as a point on the surface of a sphere often called the Bloch sphere, as shown in Fig.2.1[1, 2].

The electrons are physically confined in 3 spatial dimensions in a quantum dot (see subsection 2.1.1). The energy levels for the spin-up and spin-down states are split due to the Zeeman effect. The energy difference is expressed as

$$E_z = g\mu_B B, \tag{2.3}$$

[1] A global phase $e^{i\gamma}$ is ignored as it has no physical significance.

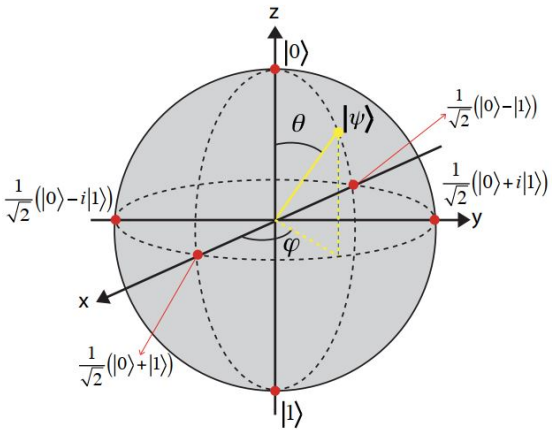

Figure 2.1: Bloch sphere representation of a single qubit state [3]. The north pole and the south pole are defined as the basis states $|0\rangle$ and $|1\rangle$. A superposition state can be plotted in the angular coordinates of a point. A single qubit operation is equivalent to one or more rotations on the Bloch sphere.

where g is the electron g-factor, B the applied static magnetic field and μ_B the Bohr magneton. For electrons in silicon, when B is 1 T, the energy splitting is about 100 μeV.
Similar to AND, OR and NOT gates for a classical computer, quantum circuits also require logical gates as building blocks. For spin qubits, applying logical gates means physically changing the direction of the electron spins using a rotating magnetic field or fast voltage pulses. A single-qubit gate operation can be viewed as a rotation of the state vector around the Bloch sphere. Full control of a qubit requires the ability to rotate about two axes of the Bloch sphere. Two-qubit gates are able to create entanglement between qubits. An example of a two-qubit gate is a rotation of one spin dependent on the state of the other[4, 5].
Measurement of a quantum state collapses the state to either $|0\rangle$ or $|1\rangle$ with probability $|\alpha|^2$ or $|\beta|^2$ (from equation 2.1), respectively. We describe readout schemes in subsection 2.1.3.

2.1.1. GATE-DEFINED QUANTUM DOTS FORMED IN SI/SIGE SUBSTRATE

Quantum dots confine electrons in all three dimensions. First, a heterostructure is used to restrict the movement of electrons to a two-dimensional plane. As shown in the left panel of Fig.2.2, a strained silicon layer is sandwiched between two relaxed $Si_{0.7}Ge_{0.3}$ layers. The structure is grown epitaxially so silicon atoms in the quantum well will align with the relaxed $Si_{0.7}Ge_{0.3}$ lattice and a tensile strain is formed. Such strain alters the bandgap of silicon. Thus, the band diagram of the heterostructure is aligned to make the conduction band minimum (CB) of the strained-silicon layer lower than that of $Si_{0.7}Ge_{0.3}$ on both sides. When the dielectric layer (Al_2O_3) and metal gates are deposited on top and voltages are applied to the gates, the Fermi level (E_F) could cross CB, as shown in the right panel of Fig.2.2. Electrons trapped in this triangular potential well form the 2-dimensional electron gas (2DEG) at the interface between the strained-Si layer and

the top relaxed $Si_{0.7}Ge_{0.3}$ layer. In terms of energy levels in this quantum well, there are in general six-fold degenerate states (with equivalent energy level) at conduction band minimum for relaxed crystalline silicon. Due to the strain in the lattice, these six states split into four states that go up in energy and two states that go down in energy. The lower two states are also split in energy and we call this splitting the valley splitting.[6, 7].

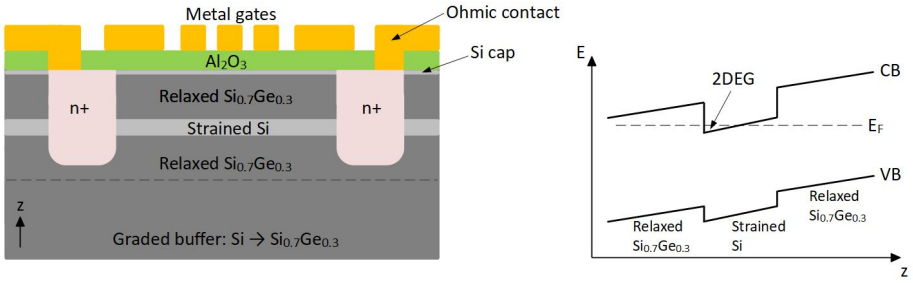

Figure 2.2: Left: cross-section of a Si/SiGe based quantum dot. A step-graded $SiGe_x$ buffer layer is grown until reaching a stably 30% germanium composition. A thin silicon layer (around 10 nm) is strained between two relaxed $Si_{0.7}Ge_{0.3}$ layers. The upper layers are composed of Si/SiO_2 cap, dielectric and metal in sequence. The reservoirs are defined by phosphorus implantation. Right: band diagram of the substrate heterostructure. A corner of the conduction band minimum falls below the Fermi level, allowing electrons to fill the energy states inside. 2DEG is then formed at the interface between the top $Si_{0.7}Ge_{0.3}$ layer and the strained-silicon layer[6].

A 1-2nm thick silicon cap layer deposited on top of the heterostructure is used to prevent oxidation of SiGe. Metal gates isolated by dielectric layers (Al_2O_3) define the potential landscape in the quantum well. Thus, few electrons are confined in a nanoscale island, and the remaining two-dimensional freedom in the 2DEG is removed. Fig.2.3 shows the top view of a single quantum dot, the accumulation gates *A1* and *A2* induce electrons from reservoirs (phosphorus implantation areas) to the Si quantum well. The plunger gate *P* controls the electrochemical potential of a quantum dot and the barrier gates *B1* and *B2* control the tunnel barrier to the next dot. When a bias voltage is applied between the reservoirs on both sides of the quantum dot, a current flows through the quantum dot depending on the alignment of the quantum dot electrochemical potentials, as discussed in the next section[8].

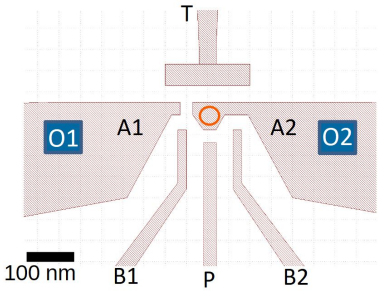

Figure 2.3: Layout design of a single quantum dot. Electrons are confined in the region indicated by a red circle.

2.1.2. COULOMB PEAKS AND COULOMB DIAMONDS

The number of electrons on a quantum dot is limited by the Coulomb blockade effect, which can be observed through Coulomb peaks or Coulomb diamonds in the measurement. We provide some explanation in this section.

The electrochemical potential of a quantum dot is defined as the difference in total energy of an N-electron dot and an $(N-1)$-electron dot, expressed as

$$\mu(N) = U(N) - U(N-1). \tag{2.4}$$

Due to the small size of the quantum dots, adding an electron to the dot results in a change in its electrochemical potential, the amount can be calculated as

$$E_{add} = \mu(N+1) - \mu(N) = E_c + \Delta E, \tag{2.5}$$

where E_c is the charging energy that equals to e^2/C (e the elementary charge and C the total capacitance of the dot), ΔE is the energy spacing between two discrete orbital levels[2]. Since the conditions for electron tunnelling are critically related to the electrochemical potential on both sides of the barrier, the electron tunnelling from a reservoir to the dot can be blocked if the electrochemical potential of the dot after adding the next electron is higher than that of the reservoir. To remove this blockade, voltages are applied to the plunger gate to change the dot's electrochemical potential[3].

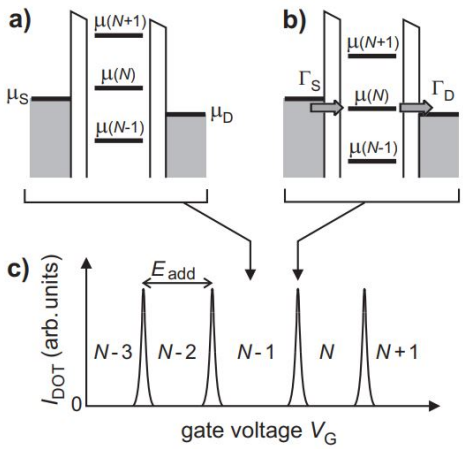

Figure 2.4: The electrochemical potential of the dot is altered by the plunger gate voltage V_G. a) No energy level falls within the window set by the bias voltage at source and drain reservoirs $\mu_S - \mu_D = -|e|(V_S - V_D)$. b) One level falls within the bias window and one electron after another can pass through the dot. The current depends on the tunneling rate between the dot and the reservoir on the left Γ_S and on the right Γ_D as indicated with arrows. c) Schematic plot of the current flowing through the dot as a function of the plunger gate voltage, giving rise to Coulomb peaks. The distance between peaks reveals the addition energy[4].

[2] A quantum dot can be viewed as an artificial atom with quantized orbital levels. ΔE can be zero when two electrons are added to the same orbital[9].

[3] The electrochemical potential depends linearly on the gate voltage.

As illustrated in Fig. 2.4, the electrochemical potentials corresponding to different numbers of electrons on the dot ($\mu(N-1), \mu(N), \mu(N+1)$...) form a ladder. Applying voltages on the plunger gate (V_G) moves the ladder up or down while keeping the space between the levels constant. A bias voltage is applied to the source and drain reservoirs, opening an energy window of $\mu_S - \mu_D$. When no electrochemical potential level in the dots falls within the bias window (Fig. 2.4(a)), no current flows through the dot. When the energy level satisfies $\mu_S \geq \mu(N) \geq \mu_D$ (Fig. 2.4(b)), an electron can tunnel from the source to the dot and then to the drain. Then another electron can tunnel from the source to the dot and so on. This cycle forms a current. The current value depends on the tunnelling rate Γ_S and Γ_D. Therefore, sweeping the gate voltage while measuring the current flowing through the dot results in a plot showing single-electron tunnelling current (Fig. 2.4(c)), known as Coulomb peaks. The distance between the peaks is constant as long as the dot size remains the same and the orbital level spacing can be neglected (constant-interaction model). The peaks broaden with increased temperature[4, 10].

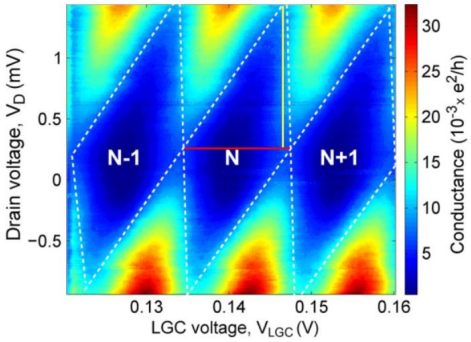

Figure 2.5: Coulomb diamond plot of an SET at 30mK. A 2D scan of the drain voltage V_D (source voltage V_S=0) and the gate voltage V_{LGC}, with colours representing the conductance. Diamond-shaped areas corresponding to the zero-conductivity can be observed [11].

So far we are assuming that the source-drain bias voltage is low such that at most one level falls in the bias window (low-bias regime). When increasing the bias voltage, multiple electrochemical potential levels could fall within the energy window. In this case, multiple electrons can pass through the dot simultaneously, resulting in a higher current (high-bias regime). The Coulomb diamond plot is obtained by a 2-dimensional scan of the source-drain voltage and the plunger gate voltage, with current flowing through the dot (or the conductance) represented by colours. Fig. 2.5 shows an example of the Coulomb diamond plot of a single electron transistor (SET)[4]. In the diamond-shaped areas (in dark blue), the current is blocked and the number of electrons on the dot is constant. Outside the diamond area, currents are flowing through the dot, the amplitude of which is higher with higher bias voltages. With this plot we could further check the stability of the dot. From the Coulomd diamond size, we can extract the lever arm from the gate to the dot potential. The lever arm α_G converts the change of the plunger gate voltage ΔV_p to the change of the electrochemical potential of the dot ΔE, expressed

[4] A single quantum dot can be viewed as a SET.

as $\Delta E = -\alpha_G \Delta V_p$. From the Coulomb diamond plot, α_G can be extracted as the ratio between the bias voltage and the gate voltage (represented by line segments in yellow and red, respectively, in Fig. 2.5). This type of diamond plot provides more information when a static magnetic field is applied, there are additional lines to reveal the spin up and down states[4].

2.1.3. MEASUREMENT TECHNIQUES

Charge sensing

As just mentioned, the number of electrons on a quantum dot can be counted according to the measurement of Coulomb peaks or diamonds. However, when electrons are depleted to the last few, the tunnelling rate could be very low, so it would be difficult to measure the tunnelling current directly. (With the tunnelling rate of 100 kHz, the tunnelling current is about 10 fA.) A widely used way to monitor the electron numbers on a dot is placing a sensing dot or quantum point contact (QPC) close to the quantum dot. The sensing dot is capacitively coupled to the quantum dot area. Adding electrons to the quantum dot leads to a change of the current flowing through the sensing dot or QPC. One advantage of this so-called charge sensing technique is that the quantum dots states are not affected by the measurement[4].

Spin readout

When applying a static magnetic field, the energy state of a single electron in the dot is split into spin-up and spin-down states. The spin-down state is regarded as ground state for silicon based qubits. Since it is hard to measure the tiny magnetic moment of a spin directly, the spin state is measured indirectly by making the charge state change depending on the spin state. The method that converts the spin states to charge states, which can be detected with a sensing dot nearby is called spin-to-charge conversion[12, 13].

The spin readout experiment consists of 3 stages as shown in Fig.2.6(a). The plunger gate voltage V_p is tuned to empty the dot, inject an electron and read out its spin state. Firstly, the dot is emptied by making the dot's energy levels corresponding to both spin up and spin down states higher than the Fermi energy E_F of the reservoir, as depicted in the first column of Fig.2.6(c). (Since the figure describes electron spin states based on GaAs dots, here spin-up is regarded as a ground state and spin-down is regarded as an excited state.) Then the plunger gate voltage is increased to pull both levels below E_F. This allows an electron to tunnel from the reservoir to the dot with a random spin state (second column of Fig.2.6(c)). After t_{wait}[5], the plunger gate voltage is reduced to make E_F lies between the spin up and spin down levels (third column of Fig.2.6(c)). If the electron is spin up, it remains in the dot. No change in the current flowing through the sensing dot (ΔI_{QPC}) occurs. If the electron is spin down, it tunnels out from the dot and another electron with up state tunnels into the dot afterwards. This results in current changes on the sensing dot, as shown in the red circle of Fig.2.6(b). Thus, the electron spin states can be determined according to the features in the sensing dot current[12].

[5] t_{wait} needs to be longer than the electron tunnelling time. Meanwhile, when increasing t_{wait}, the possibility of spin down in readout results decreases due to the spin relaxation.

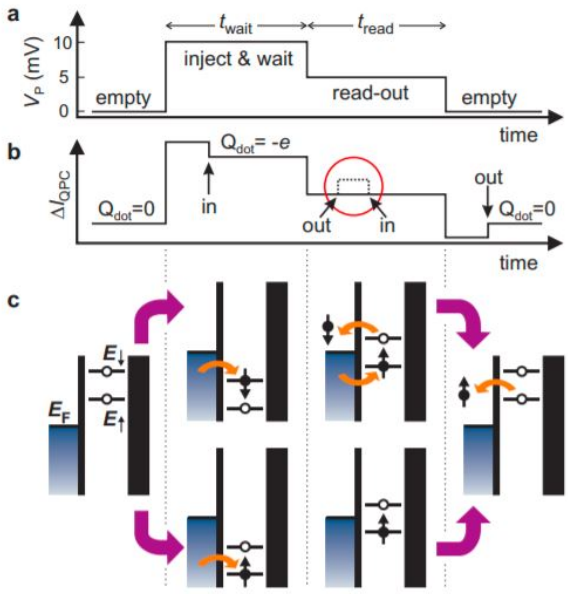

Figure 2.6: Elzerman spin-to-charge readout technique. a) Voltage pulses are applied to the plunger gate (V_p) to inject a single electron onto the quantum dot and measure its spin state. b)Changes of the current flowing through the sensing dot, which is affected by 2 factors: the amplitude of V_p and electron tunnelling on and off the dot. c) Energy diagrams for different stages of the experiment, details are described in the main text[12].)

2.2. SWITCHED-CAPACITOR CIRCUIT AND APPLICATION

Next, we move on to the electronics aspect to discuss the switched-capacitor circuit. It consists of a transistor as a switch and a capacitor as a local battery. The circuit schematic is shown in the left half of Fig.1.3. It is also known as a simple sample-and-hold circuit in analog electronics. To switch on an n-type transistor, the voltage on the transistor gate V_g needs to satisfy $V_g^{ON} - V_{th} > V_{in}^{MAX}$, where V_{th} and V_{in}^{MAX} are the transistor threshold voltage and the maximum input voltage, respectively. Then the output voltage (the voltage on the plunger gate V_p in Fig.1.3) follows V_{in}, namely it samples the signal. When switching off the transistor by setting $V_g^{OFF} - V_{th} < V_{in}^{MIN}$ (V_{in}^{MIN} being the minimum input voltage)[6], V_p remains constant. Thus, the input voltage is held locally on the capacitor. A sample-and-hold circuit is often used to maintain the input of an ADC during conversion. For the ADC to produce accurate results, the holding voltages need to be precise and stable. Therefore, extra structures (e.g. complementary switches, differential inputs, etc) are sometimes implemented to improve its performance[14].

This structure of a transistor and a capacitor in series is also commonly applied as a memory cell. The structure is repeated and arranged in a rectangular array to form a DRAM matrix. The transistor gates share the word-lines and the drain of the transistors share the bit-lines. Each cell encodes one data bit of information by the charged/discharged

[6]The voltage region between V_g^{ON} and V_g^{OFF} is much larger than $V_{in}^{MAX} - V_{in}^{MIN}$ to avoid false switches in the subthreshold region.

state of the storage capacitor. The most significant advantage of a DRAM is that the memory cell structure is simple, which also results in high cell densities. However, charges on the capacitor always slowly leak off, so memory refreshing is required to periodically rewrite the data in the capacitors[15].

For the application in this study, we take advantage of the structure simplicity of switched-capacitor circuits. However, since the maintained voltages are used for electron confinement, requirements on the voltage accuracy here are higher than that for DRAMs, ranges from 1μV to 1 mV[16].

2.2.1. PRECISION CONSIDERATIONS

Here we review considerations on the accuracy of the floating gate voltage in the literature, which is the basis for our choices of device dimensions. We will first discuss two mechanisms that lead to a random error in the floating node voltage, and next review mechanisms that in principle produce a systematic error.

Fundamentally, the voltage resolution ΔV of a floating node is limited by the electron charge, e, as

$$\Delta V = e/C_H\,, \tag{2.6}$$

where C_H is the total capacitance of the floating node to ground. It is dominated by the holding capacitor in our case. In order to keep ΔV below 1 μV, C_H should be larger than 160 fF.

Next, thermal noise is present due to the transistor channel resistance when the transistor is switched on. The random thermal noise voltage is maintained on the holding capacitor after switching off the transistor. The root-mean-square (RMS) noise voltage on the capacitor is calculated as [17]

$$V_n^{rms} = \sqrt{k_B T/C_H}\,. \tag{2.7}$$

For instance, to obtain a noise level below 1 μV at a temperature of 10 mK, the holding capacitance must exceed 138 fF.

Note that the final noise level is independent of the transistor channel resistance. We summarize the derivation of Eq. 2.7 below for a better understanding.

When an SC circuit works in sampling mode, the transistor can be modelled as a noise source V_{ni} in series with an ideal resistor R (the resistance equal to the on-resistance of the transistor). The noise spectral density of the resistor is

$$V_{ni}^2 = 4kTR, \tag{2.8}$$

expressed in units of V^2/Hz. Here k is the Boltzman constant and T the temperature in kelvin. Since the transfer function of an RC circuit from input to output is

$$H(j\omega) = \frac{1}{1+j\omega RC}\,, \tag{2.9}$$

with $\omega = 2\pi f$, the noise spectral density at the output is

$$V_{no}^2(f) = \left|H(j2\pi f)\right|^2 V_{ni}^2(f) = 4kTR\left|\frac{1}{1+j2\pi fRC}\right|^2. \tag{2.10}$$

The total mean-squared voltage at the output is obtained by integrating the spectral density over the entire frequency spectrum,

$$V_{no(rms)}^2 = \int_0^\infty V_{no}^2(f)df = 4kTR\int_0^\infty \frac{1}{1+(j2\pi fRC)^2}df. \tag{2.11}$$

Since

$$\int_{y=0}^\infty \frac{1}{1+y^2}dy = (tan^{-1}y)\Big|_{y=0}^\infty = \frac{\pi}{2}, \tag{2.12}$$

we have

$$V_{no(rms)}^2 = \frac{4kTR}{2\pi RC}\int_0^\infty \frac{1}{1+y^2}dy = \frac{kT}{C}. \tag{2.13}$$

In short, we see that the thermal noise spectral density at the input is proportional to R, while it is filtered by an RC low-pass circuit with the bandwidth inversely proportional to R. This results in kT/C in the end [18].

A first systematic offset in the floating node voltage is caused by channel charge injection. This effect refers to the charges that get redistributed to the drain and source upon switching a transistor off[14, 18]. As indicated in the left panel of Fig.2.7 , when FET_1 is switched off, charges in the channel of FET_1 are injected into the floating node and cause an error ΔV_c in the stored voltage. Under the assumption that charges split equally to the source and drain, this error can be expressed as

$$\Delta V_c = \frac{C_{channel}(V_g^{ON} - V_{in} - V_{th})}{2C_H}, \tag{2.14}$$

with $C_{channel}$ the capacitance between the transistor gate and the channel, V_g^{ON} the "on" voltage on the gate of FET_1. Assuming V_g^{ON} is set 0.1 V higher than $V_{in} + V_{th}$, the holding capacitance needs to be 50 times larger than the transistor channel capacitance to make ΔV_c less than 1 mV. In practice, the splitting fraction is also related to the switching speed, impedance at both sides and so on[19, 20].

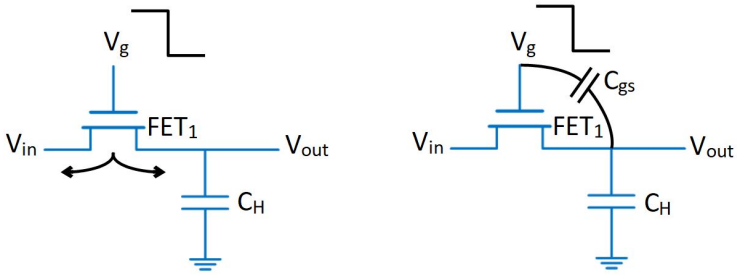

Figure 2.7: Systematic voltage offsets due to channel charge injection (left panel) and gate-source parasitic capacitance (right panel).

Another factor that introduces systematic offsets in the maintained voltage is the parasitic capacitance from the transistor gate to the floating node (see the right panel of Fig.

2.7). In series with the holding capacitance, it shifts the voltage on the floating node by an amount that depends on the voltage on the gate of FET_1, given by [14, 18]

$$\Delta V_p = \Delta V_g \frac{C_{gs}}{C_{gs} + C_H}, \tag{2.15}$$

where ΔV_g is the switching range used to turn the transistor on and off and equals $V_g^{ON} - V_g^{OFF}$. Assuming ΔV_g is 1 V, to make ΔV_p less than 1 mV, the ratio of C_H to C_{gs} should be larger than 1000.

Importantly, different from the random variations in the floating gate voltage, the systematic shifts can be accounted for in the calibration phase, hence they do not impose strict requirements on C_H.

Table 2.1 summarizes the specifications for providing bias voltages to the floating node. As we shall see, in general a larger holding capacitance reduces these errors, however, it also increases the footprint and power dissipation, both of which eventually can limit scalability as well [21].

	$\Delta V < 1\mu V$	$\Delta V < 1mV$
Single charge limit (Eq. 2.6)	$C_H > 160fF$	$C_H > 160aF$
Thermal noise (Eq. 2.7)	$C_H > 138fF$	$C_H > 138zF$
Channel charge injection (Eq. 2.14)	$C_H > 5\times10^4\, C_{channel}$	$C_H > 50C_{channel}$
Parasitic capacitor (Eq. 2.15)	$C_H > 10^6 C_{gs}$	$C_H > 10^3 C_{gs}$

Table 2.1: Specifications of the transistor and the capacitor in an SC circuit for reaching 1μ V or 1 mV resolution of maintained voltages.

In the end, we briefly introduce the imperfection of holding capacitors. There are always defects in the dielectric materials used for capacitors, which form low-resistance conduction paths and slowly discharge the capacitor. Fig. 2.8 describes some sources of defects in a MOS capacitor. The conduction process in insulators includes tunnelling, thermionic emission, ionic conduction and so on. Each of them may dominate the leakage current depending on the insulator qualities, temperature and voltage conditions. In many cases, these mechanisms are not independent of each other [22, 23].

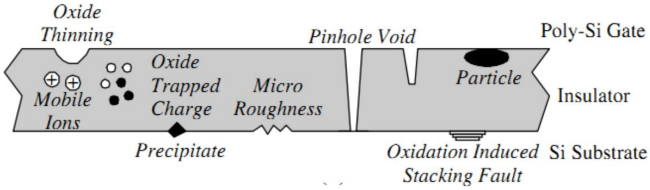

Figure 2.8: Schematic of defects in an insulator[23].

2.2.2. POWER CONSUMPTION

To charge a capacitor C through a resistor R, we denote a general calculation of power consumption before adapting the results in our specific circuit.

When charging the capacitor, the current can be expressed as

$$i(t) = Ie^{(-t/\tau)}, \tag{2.16}$$

where the initial current $I = V/R$, V is the final capacitor voltage. The time constant $\tau = RC$.
The power dissipated in the resistor as a function of time is

$$P(t) = i(t)^2 R = I^2 Re^{(-2t/\tau)} \tag{2.17}$$

Integrate the power over time to calculate the total energy as

$$E = \int_0^\infty I^2 Re^{(-2t/\tau)} dt = \frac{I^2 R\tau}{2} = \frac{1}{2}CV^2. \tag{2.18}$$

Note that during the charging phase, the energy dissipated in the resistor of an RC circuit is equal to the energy stored in the capacitor and independent of the resistance. The stored energy is converted to heat during the discharging phase.

In our case, consider charging the floating node with an RC module shown in the left panel of Fig. 2.9, and discharging the node through parasitic resistance on the leakage path, then the total generated heat can be expressed as

$$P_1 = C_H f_g (V_1 - V_2)^2, \tag{2.19}$$

where V_1 and V_2 are the high and low voltages on the holding capacitor during operation, and f_g is the switching frequency of the transistor. If we refresh the floating node to compensate for a 1 mV drop with a 1 Hz frequency, the power dissipation associated with repeatedly refreshing the stored voltage is 10^{-18} W when the holding capacitor is 1 pF. This is orders of magnitude smaller than the heat dissipated during switching in

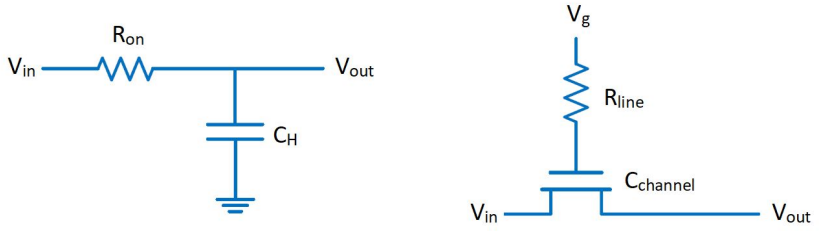

Figure 2.9: Left: when refreshing the holding capacitor, currents flow through the on-resistance of the transistor to charge/discharge the holding capacitor. Right: when switching the transistor, currents flow through the signal line resistance to charge/discharge the transistor channel capacitor.

the resistance in the line between a pulse generator and the gate of the transistor (right panel of Fig.2.9), which can be expressed as

$$P_2 = C_{channel} f_g (V_g^{ON} - V_g^{OFF})^2. \tag{2.20}$$

For a transistor with a 0.01 pF channel capacitance and 1 V switching range, the power dissipated on the signal line to its gate is 10^{-12} W. Even if we assume that this power is entirely dissipated on-chip, it would still in principle allow 10^8 floating gate voltages to be maintained assuming 100 μW available cooling power at the chosen operating temperature.

Making the transistors smaller reduces $C_{channel}$ and C_{gs}, which reduces switching power dissipation as well as the systematic shifts in the floating gate voltage. However, secondary effects appear when the device is scaled down. For instance, when the channel width is lower than 1 μm, the threshold voltage V_{th} increases due to the narrow-channel effect [24, 25]. Then a higher gate voltage is required to turn on the transistor which is more likely to cause hysteresis and breakdown.

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3

PROCESS DEVELOPMENT AND EXPERIMENTAL SETUP

On-chip integration of electronic circuits and quantum dots is currently not an industry-standard process. Therefore, prototypes are made in research labs for the proof of concept. Since quantum dots are more fragile and demanding compared to micrometer scale electronic circuits, the general rule of integration is to integrate the electronic circuits where possible without affecting the fabrication flow of quantum dots.

3.1. FABRICATION PROCESS

Before describing fabrication steps in detail, we will first give an overview of the device layout. Fig.3.1(a) shows the whole design of a 1 cm by 1 cm chip consisting of 16 cells, among which, relevant to this study are Cell 2: individual transistors; Cell 5: individual single quantum dots; Cell 12 and 15: quantum dots with floating gates; and Cell 16: test structures. Fig.3.1(b) zooms in part of Cell 12 and shows the pattern of a floating gate device composed of a single quantum dot and a switched-capacitor circuit. Here the fine gates of the quantum dot are in tens of nanometer scale and the transistor and capacitor are a few micrometers. There are generally two ways to process them: define all patterns on a chip using ebeam-lithography, or first define large patterns (micrometer scale) on a wafer using photo-lithography, then dice the wafer and continue making fine patterns (nanometer scale) using ebeam lithography. The former approach saves substrate in the early process development period and avoids transferring samples between labs in practice[1]. The latter method accelerates the process and improves the reproducibility once the large scale fabrication (pre-fab) is a success. Information on the full ebeam-lithography option is provided in appendix A. We will describe the combined-lithography option step by step in section 3.1.1 and appendix B. We process optical lithography at Else Kooi Lab (EKL), and ebeam-lithography at Van Leeuwenhoek Laboratory (VLL).

[1] Early samples with gold gates are forbidden to process in the Else Kooi Lab.

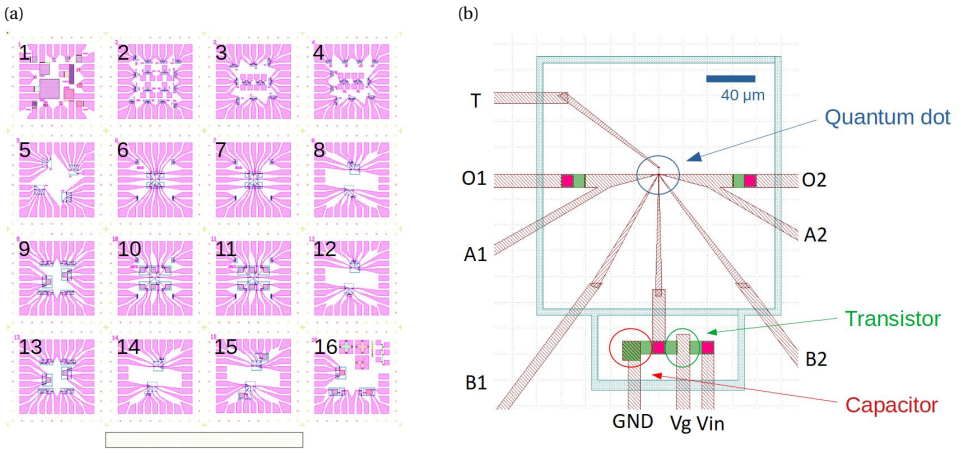

Figure 3.1: (a) Device layout with 16 cells on a 1 cm by 1 cm chip. Capacitors, transistors, quantum dots, floating gate devices and test structures are fabricated through the same process. (b) The pattern of a quantum dot with floating plunger gate. The quantum dot is in tens of nanometer scale and the switched-capacitor circuit in the micrometer scale.

The cross section of a quantum dot with a floating gate is shown in Fig. 3.2. We use a single patterned metal layer to define the potential landscape that confines electrons in the quantum dot. For the capacitor, the top plate is formed by a metal gate and the bottom plate by a heavily implanted region in the semiconductor, with a dielectric separating the plates. The transistor is a field-effect transistor with the buried quantum well acting as the channel at cryogenic temperature.

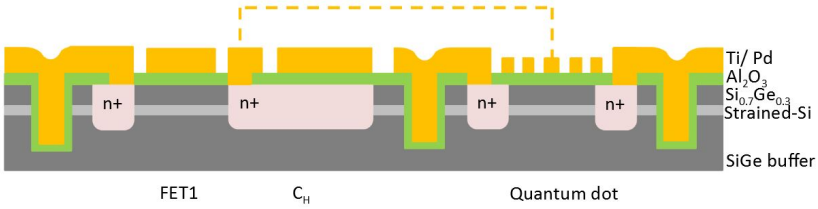

Figure 3.2: Schematic of the cross section of a single floating gate device (not to scale)

3.1.1. DEVICE FABRICATION OVERVIEW

Substrate

The Si/SiGe heterostructure is grown by reduced-pressure chemical vapor deposition on a 4-inch diameter crystalline Si wafer in EKL. From bottom to top, it contains a $Si_{1-x}Ge_x$ buffer layer with 0% to 30% germanium concentration, a 10 nm strained-Si layer, a 30 nm $Si_{0.7}Ge_{0.3}$ layer and a 1-2 nm Si/SiO_2 cap. The substrate used in this study is provided by Amir Sammak under supervision of Giordano Scappucci, both at QuTech [1].

Optical markers and trench etching
The first pattern in the fabrication process is to define optical markers for mask alignment. In addition, to prevent electron accumulation in the quantum well from contact pads or drain of the transistor to the quantum dot gates, trenches (light blue pattern in Fig. 3.1(b)) used to isolate the quantum dot are also defined in this step, both require 100 nm deep etching into the Si/SiGe substrate.
The patterning process is executed on EVG 120 Coater-Developer and ASML PAS 5500/80 wafer stepper (with exposure wavelength of 365 nm) as follows. Same processes are applied to define implantation areas in the next step.

- Spin coating:
  - Pre-bake at 130 °C for 95 seconds with hexamethyldisilazane (HDMS) treatment to improve photoresist adhesion
  - Spin coat 1.4 µm positive photoresist (SPR3012)
  - Post-bake at 95 °C for 90 seconds
- Exposure:
  - Optical lithography with energy density of 150 mJ/cm^2 to pattern markers
  - Optical lithography with energy density of 140 mJ/cm^2 to pattern trenches
- Development:
  - Post-exposure bake at 115 °C for 90 seconds
  - Develop with MF322 for 57 seconds
  - Hard bake at 100 °C for 90 seconds

The Si/SiGe substrate is dry-etched in Trikon Omega 201 plasma etcher. The sequence and conditions are listed in Table 3.1.

Step	Gasses and flows	Pressure	Platen RF	ICP RF	Platen temperature	Etch time
1. breakthrough native oxide	CF_4/O_2 40/20 sccm	5 mTorr	60 W	500 W	20 ° C	10 s
2. Si/SiGe etch	Cl_2/HBr 80/40 sccm	60 mTorr	10 W	500 W	20 ° C	10 s

Table 3.1: Si/SiGe etching condition

After etching the desired patterns through the openings of the photoresist mask, the resists are removed by oxygen plasma (in TePla300) with 400 ml/min flow and 1000 W power for approximately 5 minutes with endpoint detection.

Implantation
Phosphorus ions are implanted using a Varian Implanter E500HP to form electron reservoirs for the quantum dots, the source and drain of the transistors, and the electrodes for the capacitors. It is implanted with 20 keV ion energy and 5×10^{15} atoms/cm^2 dose. Simulation results based on silicon substrate[2] reveal that under this condition, the maximum impurity concentration appears at a depth of about 30 nm below the surface,

[2] https://cleanroom.byu.edu/implantcal

where it can exceed 5×10^{20} atoms/cm^3. In practice, considering the Si/SiGe substrate and cryogenic operation temperature, the doping profile deviates from the simulation results, so we will confirm sufficient electrons in the quantum well later by measurement.
Subsequently, the dopants are activated (in SSI Solaris 100) by rapid thermal annealing at 700 °C for 15 s in forming gas (mixture of hydrogen and nitrogen).

Dielectric layer
After a standard cleaning process (see appendix B), the wafer is dipped in 0.55% hydrofluoric acid (HF) for 4 minutes, followed by deionized (DI) water cleaning and N_2 dry to remove native oxide. A 20 nm Al_2O_3 layer is then grown as the gate oxide for both quantum dots and transistors, and the dielectric layer for capacitors. Here we use thermal atomic layer deposition (ALD) that synthesizes Al_2O_3 from trimethylaluminum (TMA) and water at 300 °C in Picosun R-200 Advanced. The dielectric strength is reported to exceed 6 MV/cm [2]. Post-annealing in forming gas at 450 °C for 20 minutes further improves the oxide quality by passivating the interface states using hydrogen atoms.

Ohmic contacts and e-beam markers
The Al_2O_3 on top of part of the implantation area is removed by wet etching in buffered hydrofluoric acid (BHF) 1:7 for 40 seconds. Then the wafer is quickly transferred to the evaporator (CHA solution) to avoid native oxide growth. We make metal contacts to the implanted regions by lifting off a 5 nm titanium (Ti) sticking layer and a 45 nm platinum (Pt) layer. Meanwhile, e-beam markers for the alignment of the subsequent patterns are also created. Metal layers deposited in the following steps are all processed by the "lift-off" technique to prevent damage of the substrate from dry etching.

Metal gates
The wafer is then diced into dies of 1 cm^2 each. We use electron-beam lithography to pattern the metal gates. Fine quantum dot gates and distances in between are all about 20 nm wide, we lift off an electron-beam evaporated 5/15 nm Ti/Pd stack for the fine structures to avoid pillar standing. Transistor gates, top electrodes of capacitors, leads of quantum dots and bonding pads are fabricated by lifting off a 5/195 nm Ti/Pd film. Since the leads should go over ~100 nm trenches to make connections between bond pads and the devices, the metal layer here needs to be sufficiently thick to prevent step-coverage problems[3].

3.1.2. SI/SIGE SUBSTRATE AND TEMPERATURE LIMIT

Unlike standard CMOS based on silicon, the substrate for our process is a Si/SiGe heterostructure provided by Intel Corporation (for the process in appendix A) or Qutech (for the process in appendix B). It contains a strained-Si layer that is sandwiched between two relaxed $Si_{0.7}Ge_{0.3}$ layers. The strained-Si layer is designed to host a 2DEG in which the quantum dot is formed. As the channel of the transistors, it has the advantage of a larger lattice constant than unstrained silicon, which leads to higher field-effect mobil-

[3] Detailed recipes are presented in appendix B.

ity for transistors. However, high-temperature treatment may relax the strain or lead to inter-diffusion. In our process, the highest temperature of 700 °C occurs in the annealing step after implantation to active dopants. Here we use the Raman spectrum to test whether this temperature affects the substrate structure.

Raman spectroscopy is based on the Raman scattering principle. When projecting a laser beam on a sample, the laser light is scattered on the sample surface. Most of the scattered light has the same frequency as the incident light, but a small fraction is shifted in frequency due to interactions with the lattice. These offsets can be used to characterize material components or molecular bonds. By detecting the incident and scattered signal, filtering out the same frequency component, a plot can be made from the detected signal intensity versus the shift in wavenumber (cm^{-1}), which is proportional to the frequency [3].

In this study, the Si/SiGe sample is irradiated under a green laser with 515 nm wavelength. Taking germanium content x and lateral strain in the lattice ϵ into consideration, peak positions in the Raman spectrum corresponding to the Si/SiGe substrate can be calculated as [4]:

$$\omega(Si-Si) = 520.2 - 62x - 815\epsilon \tag{3.1}$$

$$\omega(Si-Ge) = 400.5 + 14.2x - 575\epsilon \tag{3.2}$$

$$\omega(Ge-Ge) = 282.5 + 16x - 385\epsilon \tag{3.3}$$

where x is 0 for the silicon substrate and 0.3 for $Si_{0.7}Ge_{0.3}$. ϵ is 0 for relaxed layers. For the strained-Si layer, since the lattice constants of Si and $Si_{0.7}Ge_{0.3}$ are 0.543nm and 0.549nm respectively [5], when the Si lattice is aligned with $Si_{0.7}Ge_{0.3}$, the lateral strain can be calculated as:

$$\epsilon = \frac{\Delta L}{L} = (0.549 - 0.543)/0.543 = 0.011 \tag{3.4}$$

Fig. 3.3 is a TEM image of the substrate (before annealing) for our Raman test[4]. Expected peak positions that indicate molecular bonds from each layer are listed in Table 3.2.

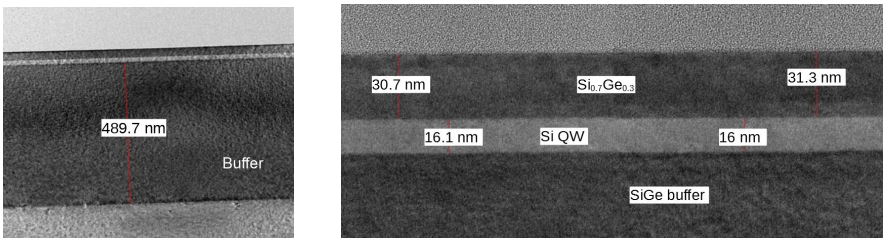

Figure 3.3: TEM image of a Si/SiGe substrate

The sample is cut in pieces and annealed in a pottery furnace at 700 °C, 800 °C, 900 °C and 1000 °C, respectively, for 30 minutes. It is processed in the open air so the chips

[4] Substrate is provided by Intel Corporation.

Wavenumber (cm^{-1})	Corresponding material bonds
286	Ge-Ge from relaxed $Si_{0.7}Ge_{0.3}$
405	Si-Ge from relaxed $Si_{0.7}Ge_{0.3}$
501	Si-Si from relaxed $Si_{0.7}Ge_{0.3}$
511	Si-Si from strained Si layer
283 - 286	Ge-Ge from SiGe buffer
401 - 405	Si-Ge from SiGe buffer
501 - 520	Si-Si from SiGe buffer
520	Si-Si from relaxed Si substrate

Table 3.2: Expected peak positions in the Raman spectrum of the Si/SiGe substrate

get oxidized in the meantime. The consumed SiGe thickness is estimated to be less than 5 nm for the chip annealed at 700 °C and over 30 nm for the chip annealed at 1000 °C [6].

Since the green laser has hundreds nanometer penetration depth, we can detect signal from part of the Si substrate to the top $Si_{0.7}Ge_{0.3}$ layer. Raman spectra of the original sample and after annealing at vary temperatures are shown in Fig.3.4. The left figure has a large spectral range to show the left two peaks around 286 cm^{-1} and 405 cm^{-1}, corresponding to Ge-Ge bonds and Si-Ge bonds from both the $Si_{0.7}Ge_{0.3}$ top layer and $SiGe_x$ buffer layer. These peaks are broad since the composition of Si and Ge is gradual in the buffer layer. The right three peaks are zoomed in in the right figure, the highest one at Raman shift of around 501 cm^{-1} indicating the quantity of Si-Si bonds from $Si_{0.7}Ge_{0.3}$ top layer and $SiGe_x$ buffer layer. The rightmost peak is corresponding to Si-Si bonds in the Si substrate. Although it has the highest quantity in the sample, they are far from the surface thus most of them are out of the detection range. These four peaks mentioned so far do not change obviously along with the annealing temperature. Although the top $Si_{0.7}Ge_{0.3}$ layer may get oxidized, this change is not visible in the Raman spectrum.

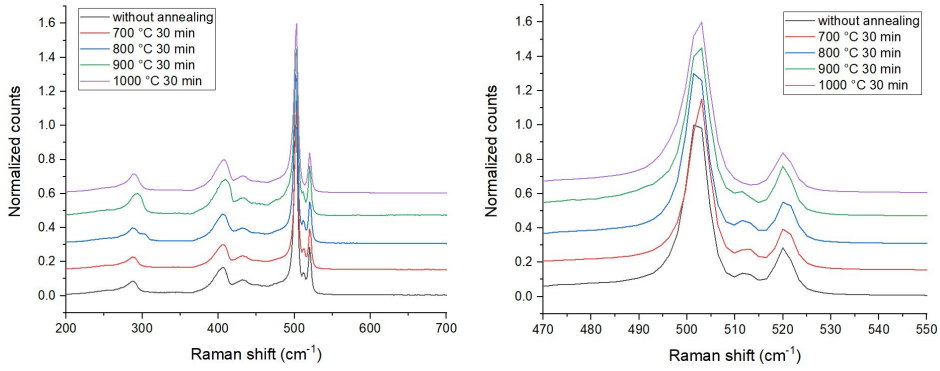

Figure 3.4: Raman spectrum of the Si/SiGe substrate without annealing and annealed at 700 to 1000 °C for 30 minutes. Left: full spectrum with peaks of all vibration modes. Right: zoom in the peaks around raman shift of 511 cm^{-1}, the feature peak for Si-Si bonds in the strained silicon layer.

We pay most attention to the tiny peak at 511 cm^{-1} that indicates the strained Si-Si

bonds from the quantum well. Since the layer is quite thin, it is reasonable that the signal is much weaker compared to other peaks. A laser of shorter wavelength can penetrate less, and thus generates a relatively stronger signal closer to the surface, but is currently not within our options. In principle, the strain relaxation leads to a rightward shift of the peak position, while inter-diffusion at the SiGe and Si interface thin down the strained-Si layer and leads to a decrease in the strained-Si peak intensity [7]. With a limited resolution of the equipment, the normalized curves of samples under none, 700 °C and 800 °C annealing follow the same trend, showing that the strained-Si layer remains in good condition. The peak intensity of strained-Si decreases for the sample annealed at 900 °C, indicating the occurrence of inter-diffusion. One of the reasons for the peak disappearance of the 1000°C annealed sample may be inter-diffusion, in addition, it may also be due to the oxidation of the $Si_{0.7}Ge_{0.3}$ and the strained-Si layers at such a high temperature in the open air.

In short, even taking temperature overshoot in the furnace into account, we conclude from this test that 700 °C maximum temperature in our process is a safe option to prevent damage to the substrate due to stain relaxation and inter-diffusion. We will discuss in the next section whether this temperature is sufficient for dopant activation.

3.1.3. IMPLANTATION AND DOPANT ACTIVATION

There are some considerations regarding the implantation step. Firstly, dopants usually require thermal energy to ionize and produce carriers in the semiconductor. "Freeze-out" occurs at cryogenic temperature when the dopants are not sufficiently ionized and there are insufficient carriers. The way to prevent freeze-out is to heavily dope the material to a degeneracy level (e.g. higher than 10^{19} cm^{-3} for Si), where the dopants require no energy for ionization [8]. However, overdoping results in clusters in the substrate that create defects. In practice, implantation with a high dose also leads to a resist removal problem that leaves organic residues on the sample surface. Secondly, after implantation, the Si/SiGe substrate undergoes an annealing step to let the dopants replace the silicon or germanium atoms inside the lattice. However, the annealing temperature of 700 °C in this process is actually at the lower end of the general annealing temperature range. Thirdly, lateral diffusion occurs during annealing, which may lead to a short of source and drain of the transistors. In other words, the lateral diffusion range limits the size of the devices. Therefore, in this section,we characterize the implantation region using some test structures.

The phosphorous ion implantation is processed with 20 keV energy and 5×10^{15} cm^{-2} dose, 700 °C annealing for 15 s afterwards. We use a Van der Pauw (VDP) structure to measure the resistivity of the doped area. This four-point probe method avoids the influence of contact resistances. Fig. 3.5a shows the VDP structure fabricated together with other devices. The width of the cross defined by implantation is 30 μm[5]. The pads labelled A, B, C and D are made of metal and connected to the implanted region through ohmic contacts. A current I is feed through Pads A and C, and we measure the voltage difference across Pads B and D (denoted $(V_1 - V_2)$ below). The resistivity of the implantation area is calculated as

[5]The cross dimension is set for easy fabrication, it is irrelevant to the sheet resistance.

$$\rho = \frac{\pi}{\ln 2} d \frac{V_1 - V_2}{I}, \tag{3.5}$$

where $\frac{\pi}{\ln 2} \times \frac{V_1 - V_2}{I}$ is the measurement result, also called sheet resistance $R_\square$. d is the depth of the implantation region[9]. According to simulation results based on the Si substrate[6], we estimate d to be around 100 nm. Results of the sample tested at both 300 K and 4 K are listed in Table 3.3. The resistance of the doped region at 4 K is lower than that at 300 K, indicating that freeze-out does not occur. Low temperature reduces the lattice vibration and improves the electron mobility, thus leads to a lower resistivity. Although we cannot calculate the dopant density accurately due to a lack of reference data that can relate the resistivity of a Si/SiGe heterodtucture to its doping concentration, according to a Si-based online calculator[7], we estimate it to be in the order of 10^{20} atoms/cm^{-3}, which roughly expresses a proper activation.

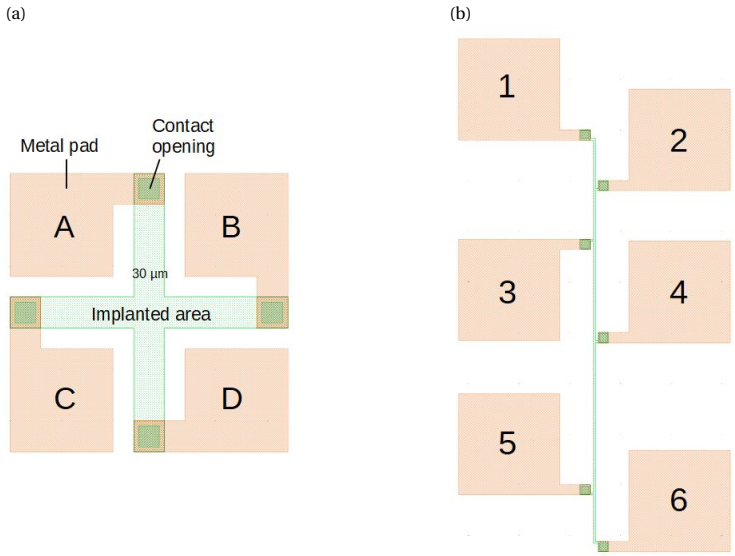

Figure 3.5: (a) Van der pauw test structure to measure the resistance of the doping area (b) Test structure to measure the lateral diffusion of the doping area

T (K)	$R_\square$ (Ω/□)	d (nm)	ρ (Ωcm)	Dopant density (cm^{-3})
300	95.6	100	9.5e-4	1e20
4	74.7	100	7.5e-4	-

Table 3.3: Resistivity of the implantation region measured using van der Pauw method

Next, we move on to measure the lateral diffusion of the implanted region. The test

[6] https://cleanroom.byu.edu/implantcal
[7] https://www.pvlighthouse.com.au/resistivity

structure is shown in Fig. 3.5b. A very narrow bar is defined by ion implantation, which resistance is very sensitive to its width. A current is injected from pad 1 through the implanted bar to pad 6, and we measure the differential voltage between pad 2 and pad 5. The implanted area between pad 2 and pad 5 is designed to be 2 µm by 300 µm on the pattern that contains 150 squares of 2 by 2 µm^2 in series. Measuring from a VDP structure closeby, the sheet resistance of the implanted region is 97.8 Ω/□ (at room temperature) and the resistance between pad 2 and 5 is 10515.3 Ω excluding contact resistance, which means 107.5 squares in series. Assuming the length of the implanted bar is still 300 µm (the length change due to lateral diffusion is negligible compare to the total length), the actual width of the bar is calculated to be 2.8 µm, thus, 0.4 µm wider than the mask design on each side. The result is summarized in Table 3.4.

pattern size (µm^2)	$R_{1,2}$(Ω)	$R_{1,5}$(Ω)	$R_{2,5}$(Ω)	$R_{□}$ (Ω/□)	actual width (µm)
2 × 300	2738.5	13253.8	10515.3	97.8	2.8

Table 3.4: Parameters for the lateral diffusion calculation

Although we estimate the later diffusion range to be 0.4 μm in this process, we did not build statistic data for further improvement. To minimize the effect of lateral diffusion on the actual length of the channel when we make transistors, all transistor channel lengths are chosen to be 10 μm. To scale down the device dimensions in the future, laser annealing is an option for a diffusion-less dopant activation[10, 11].

3.1.4. GATE OXIDE OPTIONS

The choice of gate oxide is critical for devices to work properly. In order for the gate voltages to tightly control the potential landscape in the quantum well, a thin oxide layer is preferred. Meanwhile, when considering the film uniformity, leakage and breakdown voltages, a thicker oxide layer is more reliable. Materials employed in industrial processes for gate oxide including SiO_2, Al_2O_3, HfO_2 etc. SiO_2 holds the advantage of a good interface with the semiconductor substrate. Both Al_2O_3 and HfO_2 are high-k (high-permittivity) materials that can prevent leakage due to tunneling when the layers are very thin. Al_2O_3 has a lower permittivity but higher bandgap compared to HfO_2. We choose Al_2O_3 as the dielectric for our devices also because its deposition process is relatively reliable in practice in our lab. The Al_2O_3 can be prepared by ALD, which also offers an advantage that the operating temperature is far below the temperature limited by substrate strain relaxation. More specifically, Al_2O_3 can be deposited by thermal ALD or plasma-assisted ALD, the former uses H_2O as the oxidizing agent and the latter uses O_2 plasma. It has been reported that plasma-assisted ALD produces Al_2O_3 layers with better dielectric properties, which get further improved by forming gas annealing afterwards [12]. However, we implement thermal ALD in this study limited by the instrument capacity.

Nevertheless, in the early stage of the process development, we evaluated Al_2O_3 and other dielectric films deposited with plasma-assisted ALD, including dielectric stacks aiming to take advantage of various materials. We present their dielectric constant and defect density here for comparison with the specification of our current gate oxide.

Four p-type crystalline silicon wafers with 1-5 Ωcm resistivity were sent to Eindhoven

University of Technology and processed in the following steps:

1. Expose in 1% HF for 2 minutes and transfer quickly to the ALD chamber
2. Plasma-assisted ALD deposition at 300 °C
   - wafer 1: 10 nm Al_2O_3
   - wafer 2: 10 nm SiO_2
   - wafer 3: 3 nm SiO_2 + 7 nm Al_2O_3
   - wafer 4: 2 nm SiO_2 + 8 nm HfO_2
3. Anneal in forming gas at 450 °C for 30 minutes

After receiving the wafers, we form 80 µm by 80 µm electrodes on top by sputtered aluminium (with 1% silicon) to make MOS capacitors. Fig.3.6a shows the schematic of a capacitor cross-section. The devices are placed on a probe station and measured by an LCR meter. The backside of the wafer is in contact with a grounded gold plate in the probe station. The voltage applied on the top electrode consists of two parts, a DC sweep voltage to bias the capacitor in the accumulation, depletion or inversion operation mode, and a small AC voltage for the capacitance measurement corresponding to every bias condition. High frequency (1 MHz) C-V curves of both forward and backward scans are shown in Fig.3.6b.

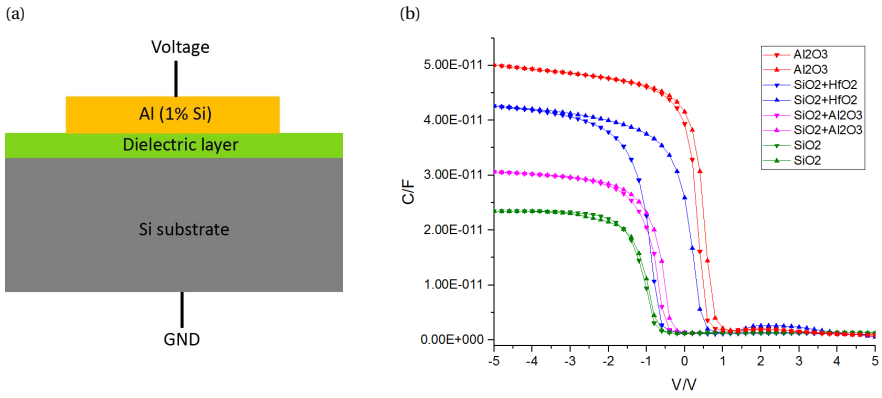

Figure 3.6: (a) cross section of a MOS capacitor. (b) high frequency C-V curve of MOS capacitors with different dielectrics

Since the Si substrate is p-type with holes as majority carriers, applying a very negative voltage on the top electrode accumulates positive charges close to the semiconductor-oxide interface. The MOS capacitance in the accumulation mode is the same as parallel plate capacitance, with gate oxide as the dielectric layer. Therefore, the effective relative permittivity can be extracted from the measured capacitance at -5 V bias voltage.

When increasing the applied voltage, holes are repelled from the oxide interface. Then a depletion layer builds up, in series contact with the oxide layer to reduce the total capacitance. When the depletion region width reaches its maximum, we obtain the minimum capacitance.
It can be seen from Fig. 3.6b that there are voltage shifts between forward and backward scans, especially for the layer of combined SiO_2 and HfO_2, which has a maximum offset of around 1 V. We presume that this hysteresis is caused by mobile ionic charges in the oxide film. Since the initial voltage polarities of the forward and backward scans are different, the mobile charges are staying either close to the semiconductor-oxide interface or the oxide-metal interface. The voltages required to add on the top electrode to build depletion layers are different for these two cases[13].
With the knowledge of the material properties of the metal, oxide and semiconductor, ideal C-V curves can be calculated under the assumption that no defects are presented in the oxide or at the interface. In practice, fixed charges in the oxide lead to a parallel shift along the voltage axis, usually to the negative direction with positive oxide charges. Besides, the presence of interface states leads to a "smearing out" in the experimental curve[14, 15].

By comparing the experimental C-V curves with theoretical curves, densities of fixed oxide charges and interface states can be extracted. To exclude effects from mobile charges, we take an average curve of the forward and backward scans of each dielectric layer. The results are listed in Table 3.5.[8]

	wafer 1 Al_2O_3	wafer 2 SiO_2	wafer 3 SiO_2 + Al_2O_3	wafer 4 SiO_2 + HfO_2
Effective relative permittivity	8.6	4.1	5.3	7.4
Fixed oxide charges (cm^{-2})	6.1×10^{12}	8.35×10^{12}	1.2×10^{12}	2.7×10^{12}
Interface state density ($eV^{-1}cm^{-2}$)	7.1×10^{11}	14.8×10^{11}	9.1×10^{11}	12.8×10^{11}

Table 3.5: Oxide properties extracted from C-V measurements

Among the four types of dielectrics, Al_2O_3 gives the highest relative permittivity. However, the table does not show the expected trends in the defect densities of the films. Si-SiO_2 interface is expected to have fewer interface states than Al_2O_3, but according to the results, Al_2O_3 film gives the lowest value. There is a wide variety of sources to introduce defects, including discontinuity of the crystal structure, contamination of the facilities or organic chemical reagents, etc. Besides, the doping concentration of the substrate also slightly varies (resistivity ranges 1-5 Ωcm). It is reasonable that a few single tests cannot represent the whole trend.
The thermal ALD Al_2O_3 used for our devices is characterized at Aachen University[9]. The relative dielectric constant of the film is 7.2, fixed oxide charges around 5×10^{12} cm^{-2} and

[8] Calculation details are presented in the master thesis of Gautham Rangasamy
[9] Presented by Jan Klos in July, 2019

interface state density around 6×10^{11} $eV^{-1}cm^{-2}$. Thus the overall quality is comparable to the films prepared by plasma-assisted ALD, which is a great advantage since thermal ALD require less on the hardware setups.

3.1.5. COMPLETED DEVICES

Devices are fabricated with all the considerations mentioned above. Fig. 3.7 shows the SEM image of a completed device (to prevent damage from high-speed electrons, the device is actually checked under SEM when all tests at cryogenic temperature are completed). The switched-capacitor circuit and quantum dot are connected on-chip as described in Fig. 1.3. The device layout follows the design in Fig. 2.3 and Fig. 3.1. The micrometer and tens of nanometer scale patterns are well defined as shown in the left and right panel of Fig. 3.7, respectively.

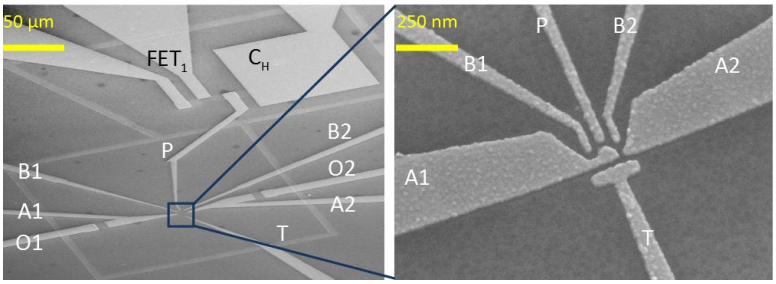

Figure 3.7: SEM image of a completed device

We wire-bond the device on a print circuit board (PCB) for the electronic characterization (see Fig. 3.8b). We will introduce the experimental setups in the next section.

3.2. EXPERIMENTAL SETUP

Devices after being inspected by optical microscope and wire bonding, are first cooled down to 4 K with a dipstick. Then we check if all signals are able to reach the device without open or short lines. Working devices are moved to a dilution refrigerator and cooled down to temperatures below 20 mK for further testing related to quantum phenomena.

Printed Circuit Board

The chip to be tested in the refrigerator is glued by PMMA to a PCB shown in Fig.3.8a[10]. Then aluminum bond wires connect bond pads on-chip to the gold pads on the PCB as shown in Fig.3.8b. There are 48 DC lines connected from the gold pads on the board to a flat flex connector (FFC) on edge. Each line has an NTC thermistor that grounds the line at room temperature to prevent any current injection during handing or bonding. The resistance increases significantly at cryogenic temperature, detaching the signal line from the ground. High-frequency signal is applied to the device through SMP connector and co-planar wave-guide on the board, combined with a DC line using a bias-tee. An

[10]The PCB is designed by Stephan Philips.

infrared light is assembled on the board for resetting the device at low temperature when necessary, aiming to replace the time-consuming thermal cycle to some extent.

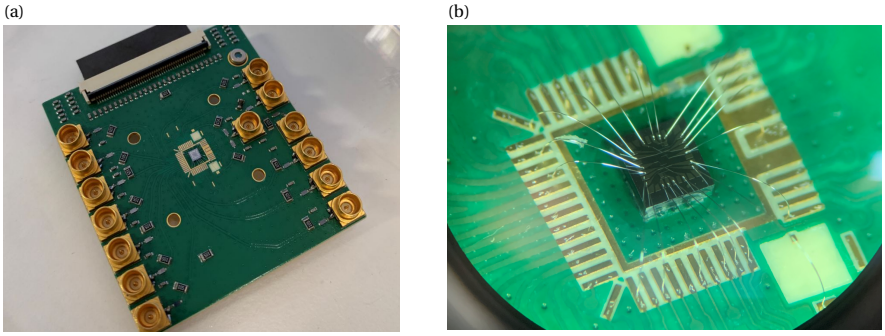

Figure 3.8: (a) The PCB to support devices testing at cryogenic temperatures (b) The device is bonded on the PCB using aluminum wires

In addition, we use the PCB shown in Fig.3.9a to measure single transistors or on-chip test structures at 4K. The sample is glued on a chip carrier which can be embedded on the PCB board. 32 DC lines are connected from the carrier to the FFC. The board is not suitable for tests in the dilution refrigerator mainly because the signal lines and adaptors in the refrigerator are designed to match FFC with 48 pins.
Another PCB designed one step further for this project is shown in Fig.3.9b[11]. It is suitable to test both on-chip and off-chip integrated samples. More importantly, there are footprint and peripheral circuits designed on the board for shift registers, which can be tested together with floating devices (We will describe the idea in Chapter 7).

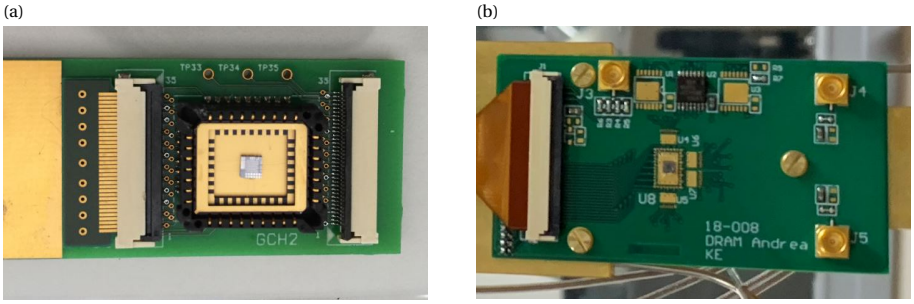

Figure 3.9: (a) PCB for simple tests at 4K (b) PCB for testing floating gate devices combined with shift registers

Dipstick

[11] the DRAM PCB designed by Andrea Corna

The PCB board is mounted at the end of a dipstick as shown in Fig.3.10 to test basic functionalities of devices at around 4 K. The stick is inserted into a liquid helium dewar to make the sample directly exposed to liquid helium. DC signals from measurement modules pass through push-pull circular connectors, wire looms inside the stick and a microD to FFC adaptor to the PCB board.

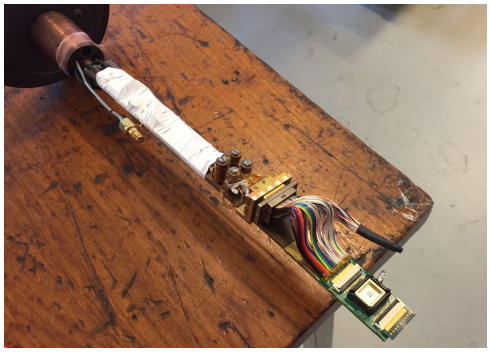

Figure 3.10: PCB board mounted on the end of the dipstick for tests at 4 K

Dilution refrigerator

A dilution refrigerator uses the heat of mixing of the two isotopes of helium, 3-He and 4-He, to obtain cooling. In this study, we use either Bluefors BF-XLD400 or Oxford TRITON400-10 to keep devices cold at temperatures below 20 mK. A dilution refrigerator consists of 3 basic components: the cryostat with cylindrical blocks for different temperature stages, the gas handling system (GHS) that contains all pumps, valves, pressure gauges, etc, and the control unit that contains all the electronics to control and read the status of the GHS. For system automation, the software ValveControl can operate the entire system by executing scripts[12].
Both refrigerators have more than 48 DC lines and more than 10 coaxial lines available at the coldest stage. As shown in Fig. 3.11, two samples are mounted on a homemade cold-finger attached to the mixing chamber (MC) plate of Bluefors XLD. Filters made of copper powder are employed to further suppress high-frequency noise on the DC signal lines in addition to the low-pass filters. Cooling down a sample from room temperature to temperatures below 20 mK usually takes around 12 hours with fast loading mechanisms (Oxford TRITON400-10). It takes about 40 hours for the whole refrigerator to warm up and cool down again without fast loaders (Bluefors BF-XLD400).

Electronic modules
The signals we deliver to or obtain from the devices consist of DC and AC components. Here we describe electronic modules operating at room temperature to supply and record these signals. The modules communicate with a control computer using optical ca-

[12]More information see BF-XLD-SERIES User manual.

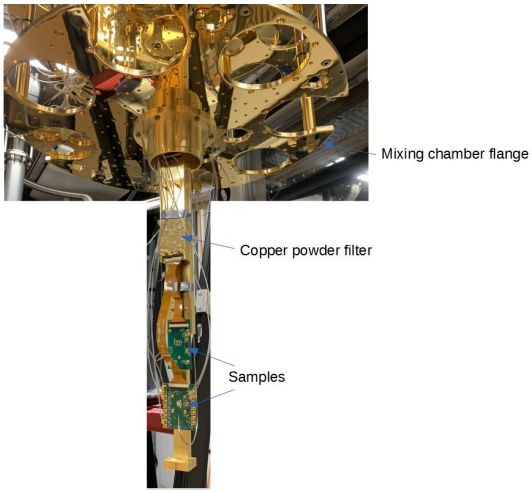

Figure 3.11: Samples mounted on the cold finger of Bluefors XLD dilution refrigerator

bles.[13]
- For DC voltages applied to the gates of quantum dots to confine electrons, we use homemade Digital to Analog Converters (DACs) that offer a resolution of 16 to 18 bit over a range of 4 V. To apply small bias voltages on the ohmics (e.g. 0.1 mV), a voltage divider is also employed to improve accuracy. The voltage sources are wired to a matrix module, which is connected to the sample via wire looms and adaptors.
- AC voltage pulses of a few hundreds Hz frequency are generated by an Arbitrary Waveform Generator (AWG, Agilent 33522A). The signal is attenuated and applied to the sample PCB through coaxial lines and SMP connectors. (more information about calibration of the attenuators is provided in Chapter 5.)
- To measure the current flowing through the quantum dots, an in-house developed transconductance amplifier is used. Its resistance is selectable between 1 MΩ and 1 GΩ. The acquisition is done with a multimeter (i.e. Keithly 2000 or Keithly 2700) or a digitizer (i.e. Keithly DMM6500).

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4

DEVICE CHARACTERIZATION

In this chapter, we report basic characterization measurements of individual transistors and quantum dots. Well-functioning separate components are a prerequisite for the proper operation of the integrated devices, which we present in the next chapter. These measurements also serve to validate the fabrication process.

4.1. EXPECTED TRANSISTOR TEMPERATURE DEPENDENCE

Characteristics of transistors at cryogenic temperature are different from those at room temperature. Here we use analytical expressions and a COMSOL simulation of a MOS device for better understanding. Although the minimum device operating temperature in COMSOL is limited to 77 K, we can still see the trend of changes from it. Software such as Silvaco is suitable for more accurate simulation of devices working at cryogenic temperatures.

The MOSFET model[1] we use here consists of a p-type Si substrate, SiO_2 dielectric and aluminium gate. Both the length and width of the channel are 1 µm. We simulate its transfer curve (source-drain current I_d as a function of the gate voltage V_g) under temperature settings of 300 K, 200 K and 100 K. The source is grounded and the drain is biased at 10 mV.

As the linear-scale plot shows in Fig. 4.1(a), the threshold voltage is shifted to the positive direction at a lower temperature. The explanation for this is not very intuitive. According to the literature [1], the threshold voltage of an NMOS transistor is given by the equation

$$V_{th} = V_{oxT} + \phi_{ms} + 2\phi_{fp}, \tag{4.1}$$

where V_{oxT} is the voltage across the gate oxide, ϕ_{ms} the work function difference between the metal and semiconductor and ϕ_{fp} the potential difference between the intrinsic level and the Fermi-level. The former two can be expressed with ϕ_{fp} as

[1] Follow the COMSOL tutorial: DC Characteristics of a MOS Transistor (MOSFET)

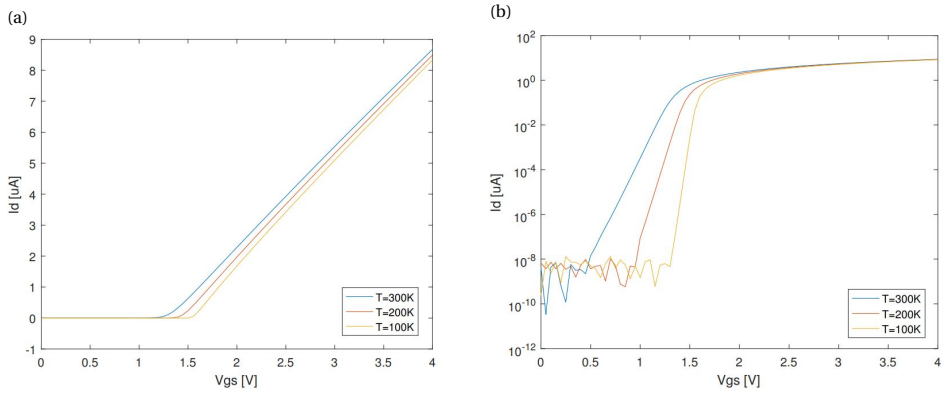

Figure 4.1: Transfer curves of a MOSFET at different operating temperatures in (a) linear scale and (b) log scale. The results are obtained by COMSOL simulation.

$$V_{oxT} = \frac{\sqrt{4eN_a\epsilon_s\phi_{fp}}}{C_{ox}} - \frac{Q_{ss}}{C_{ox}} \tag{4.2}$$

and

$$\phi_{ms} = \phi_m - (\chi + \frac{E_g}{2e} + \phi_{fp}). \tag{4.3}$$

In Eq.4.2, N_a is the acceptor concentration under the gate, ϵ_s the permittivity of the semiconductor, C_{ox} the gate oxide capacitance, Q_{ss} the fixed oxide charges staying close to the oxide-semiconductor interface. In Eq.4.3, ϕ_m and $(\chi + \frac{E_g}{2e} + \phi_{fp})$ are work functions of the metal and semiconductor, respectively. Here χ is the electron affinity and E_g the bandgap for silicon. Then, the threshold voltage can be reformed as below that among all the parameters, ϕ_{fp} is most sensitive to temperature changes[2].

$$V_{th} = \frac{\sqrt{4eN_a\epsilon_s\phi_{fp}}}{C_{ox}} - \frac{Q_{ss}}{C_{ox}} + \phi_m - \chi - \frac{E_g}{2e} + \phi_{fp} \tag{4.4}$$

Here,

$$\phi_{fp} = E_{Fi} - E_F = \frac{kT}{e}\ln\left(\frac{N_a}{n_i}\right) \tag{4.5}$$

is positive for p-type substrate. n_i is the intrinsic carrier concentration, k the Boltzmann constant, T the temperature and e the elementary charge. The Fermi level position as a function of temperature in theory is plotted in Fig. 4.2, which also takes freeze-out at low temperature into account [1]. The plot shows that with a fixed substrate doping concentration, when temperature decreases, the Fermi-level moves further from the intrinsic level. Thus, ϕ_{fp} increases and V_{th} moves to the positive direction according to Eq. 4.4.

The Log-scale plot in Fig. 4.1(b) provides more information on the subthreshold region. Here the subthreshold swing (SS) is used to represent the slope obtained under

[2] E_g is also a function of temperature, but has less influence than ϕ_{fp} on V_{th}. E_g (0K) = 1.17 eV; E_g (300K) = 1.12 eV [2].

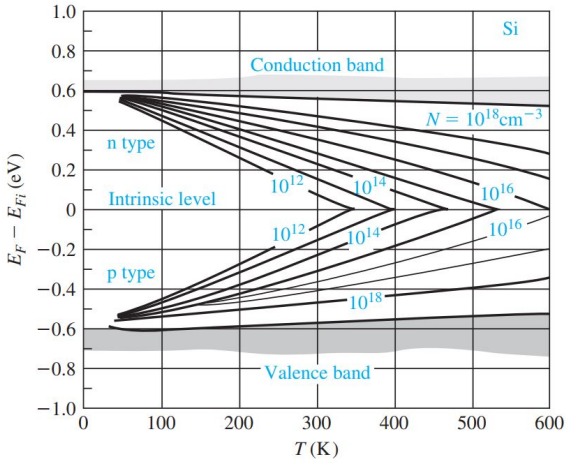

Figure 4.2: Position of Fermi-level as a function of temperature for various doping concentrations[1].

different temperature conditions. SS is defined to be the voltage required for the current to increase by a factor of 10 in the subthreshold region. It indicates the switching speed of devices. Ideally, it is expected to be

$$SS = \frac{kT}{e}\ln 10, \tag{4.6}$$

which is 60 mV/dec at 300 K and decreases with decreasing temperature. It can also be seen from the simulation in Fig. 4.1(b) that the lower the temperature, the deeper the slope, meaning less voltage is needed to make the same current change.

We can also see the trend of field-effect mobility μ_{FE} with temperature from this set of I_d-V_g curves. I_d as a function of the gate and drain voltages (V_g and V_d) in the linear region (small bias voltage on the drain) is provided by [1]

$$I_d = \mu_{FE} C_{ox} \frac{W}{L}\left((V_g - V_{th})V_d - \frac{V_d^2}{2}\right). \tag{4.7}$$

Since V_d is a constant, the transconductance g_m can be obtained by taking partial derivative of I_d as

$$g_m = \frac{\partial I_d}{\partial V_g} = \mu_{FE} C_{ox} \frac{W}{L} V_d. \tag{4.8}$$

Therefore, we can calculate the field-effect mobility corresponding to the maximum g_m. As shown in Fig.4.3(a), the maximum slope of the transfer curve (g_m^{max}) increases with decreasing temperature, so does the field-effect mobility. The physical reason for higher mobility at low temperature is the reduction of the lattice scattering effects[3].
Finally, we compare output curves (I_d versus V_d) simulated under different temperature conditions (see Fig.4.3(b)). The linear and saturation regions are clearly observed. For

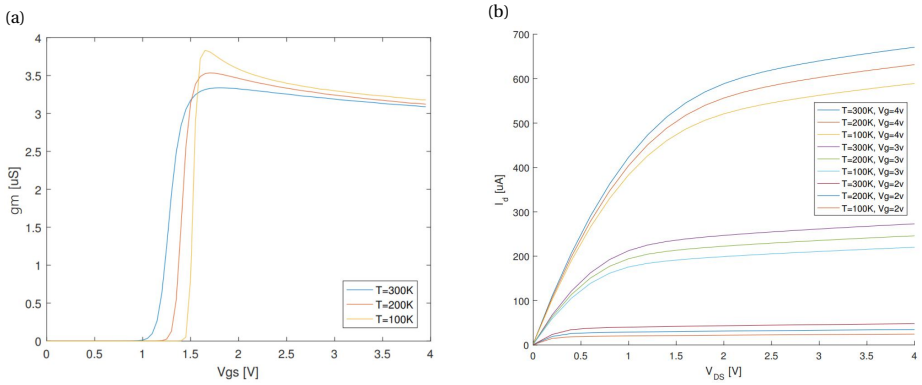

Figure 4.3: (a) Device transconductance as a function of the gate voltage (b) Output curve obtained under different temperature conditions

the same gate voltage, the current level is slightly lower for lower temperatures because of the V_{th} shift we just discussed.

In short, the simulation results in COMSOL indicate that as temperature decreases, the threshold voltage increases, the field-effect mobility increases and devices can be switched faster. We expect the same trend for devices operating at temperatures out of the simulation range (lower than 100 K).

4.2. CHARACTERIZATION OF SINGLE TRANSISTORS

When the drain of a transistor and the gate of a quantum dot are connected to form a floating gate device, the connection point is only accessible through the source after turning on the transistor. Adding additional leads and pads on the floating point for testing will introduce parasitic capacitance, and introduce the potential for leakage. Therefore, we use single transistors that are fabricated on the same chip with floating gate devices to test their current and voltage characteristics.

4.2.1. TRANSFER AND OUTPUT CURVES

The performance of transistors in practice is affected by many factors, such as material options, fabrication processes, and test conditions. In this study, we integrated several batches of transistors with quantum dots, with slight differences between the batches. We will list design considerations and test results in this section. All transistors are tested at 4 K exposed in the liquid helium.

- FET1: W/L = 10 μm/10 μm, processed in VLL

To start with, FET1 is fabricated earlier in this study[3]. It is based on a 1 by 1 cm^2 chip and all patterns are defined by ebeam lithography. The Si/SiGe substrate is provided by Intel,

[3] Fabrication process is provided in appendix A

the gate oxide of 7 nm Al_2O_3 is processed at Imec. From its transfer curve in Fig. 4.4(a) (source grounded, drain biased at 1 mV also for the following I_d-V_g tests), the threshold voltage and subthreshold swing are extracted to be 600 mV and 15 mV/dec, respectively. The field-effect mobility is calculated to be 1.3×10^4 cm^2/Vs according to Eq.4.8, with C_{ox} regarded to be a 7 nm Al_2O_3 layer and a 30 nm $Si_{0.7}Ge_{0.3}$ layer in series. The output curve in Fig. 4.4(b) shows the modulation of the drain voltage on the channel current that the linear and saturation regions can be clearly observed.

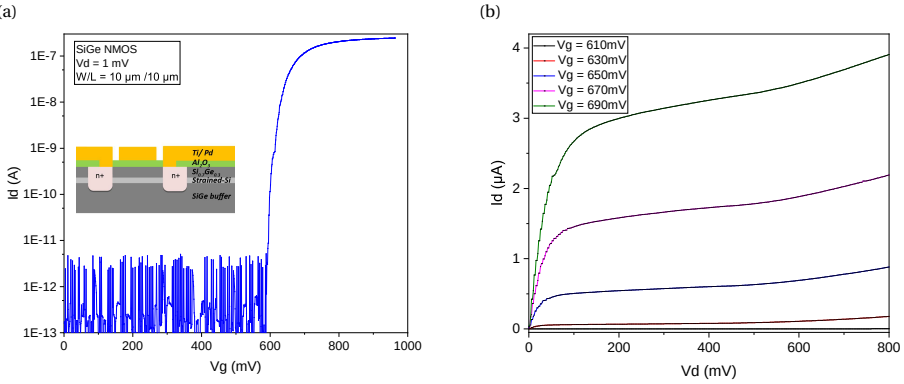

Figure 4.4: Transfer and output curve of FET1

- FET2: W/L = 10 μm/10 μm, processed in VLL and EKL

After the batch with FET1, we aimed to further improve the process reproducibility through wafer-based pre-fab processes (as explained in section 3.1). Meanwhile, Si/SiGe substrate has been successfully prepared in EKL, and the ALD system (Picosun R-200) in VLL also provided high-quality Al_2O_3 films for gate oxide. Therefore, we switched our process with the same design but follow the flowchart in appendix B (combined photolithography and ebeam-lithography). Both substrate and gate oxide are home-made. Two more differences between FET2 and FET1 are that the gate oxide is 20 nm thick instead of 7 nm, and we use Pd instead of Ti/Pd as the gate metal. The characterization result of a single transistor is shown in Fig. 4.5.

After a rearrangement of the ground lines among the measurement modules, the noise level is significantly reduced as can be seen from the off-state signal of the transfer curve. The threshold voltage is around 840 mV according to this specific measurement result. However, as discussed in more detail in the next subsection, this device, as well as other devices, showed hysteresis when sweeping the gate voltage beyond 1 V. In this experiment, V_g is swept to 1.5 V that may cause the V_{th} shifts. Nevertheless, a thicker oxide and the gate metal with larger work-function may also cause the increase of the threshold voltage. The subthreshold swing and field-effect mobility of FET2 are 3.3 mV/dec and 3.4×10^4 cm^2/Vs, respectively, indicating an improvement of the material quality and fabrication processes.

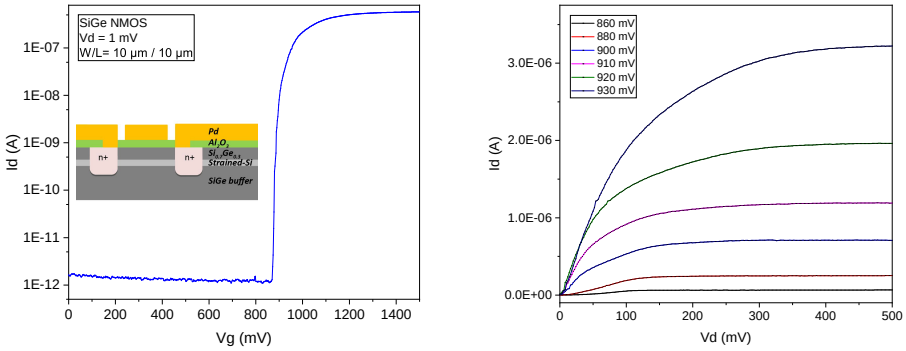

Figure 4.5: Transfer and output curve of the FET2

4

- FET3: W/L = 1 μm/10 μm, processed in VLL and EKL

So far, the device sizes are large to have a relatively reliable fabrication process, which leads to a large channel capacitance and parasitic gate-source capacitance. As explained in Chapter 2, these capacitances introduce offsets on the voltage of the floating node. Therefore, we next made devices with smaller channel sizes. The chip that comes from the same pre-fab wafer as FET2 are used, on which the implantation region (source and drain) is already defined. Thus, the channel length is kept at 10 μm, and we use the transistor gate to define the width of the channel to be 1 μm [4]. The transfer and output curves are shown in Fig. 4.6. Since the data for the output curves are obtained after a hysteresis check, the gate bias voltages are not aligned with the transfer curve.

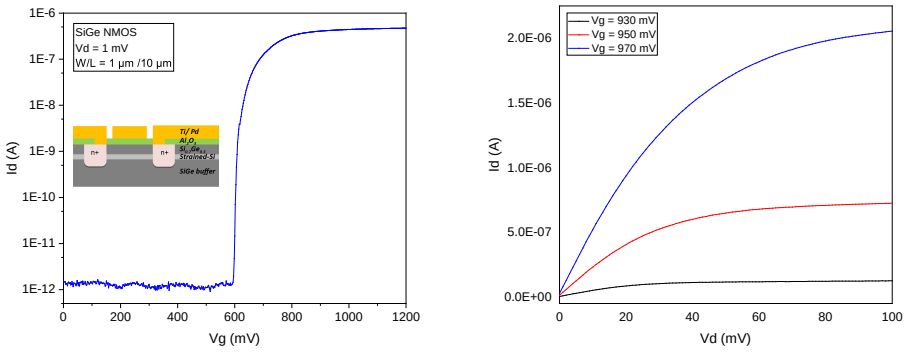

Figure 4.6: Transfer and output curve of FET3

The extracted parameters of FET3, together with parameters for FET1 and FET2, are summarized in Table 4.1. In general, the subthreshold slope is lower and the field-effect

[4] The gate metal is changed back to Ti/Pd for this batch. The reason to use only the Pd for FET2 is that Ti is suspected to react with the resist during lift-off process and leave residues on the sample surface, however, this is not the case after the optical microscope inspection of the sample.

	V_{th} (mV)	SS (mV/dec)	g_m^{max} (μS)	μ_{FE} (cm^2/Vs)
FET1	600	15 mV/dec	3.58	1.3×10^4
FET2	820	3.3 mV/dec	5.95	3.4×10^4
FET3	620	2.9 mV/dec	3.32	1.9×10^5

Table 4.1: Characteristics of the transistors from various batches

mobility is higher than room temperature MOS devices. Besides the reason of cryogenic working temperature, the strained-silicon channel that removed from the oxide-semiconductor interface also contribute to it. One observation from the table is that the field-effect mobility of FET3 is surprisingly high. More specifically, when the channel width decreased from 10 μm for FET2 to 1 μm for FET3, the source-drain current is also expected to reduce by a factor of 10 and the maximum transconductance g_m^{max} would decrease in the same scale. However, comparing the transfer curves of FET2 and FET3, the on-state currents are on the same scale, which then result in very high mobility for FET3 by calculation.

In the end, the batch with FET3 become one of the main batches of this study. The transistor that we use later to illustrate the hysteresis issue (section 4.2.2), and some integrated devices (device *B* and *C* in Chapter 5) are all from this batch.

- FET4: W/L = 3 μm/ 1 μm, processed in VLL and EKL

There is another option to reduce the channel length using the chip with source-drain distance pre-defined to be 10 μm. The device structure with 2 metal layers and 2 gates is shown in Fig. 4.7.

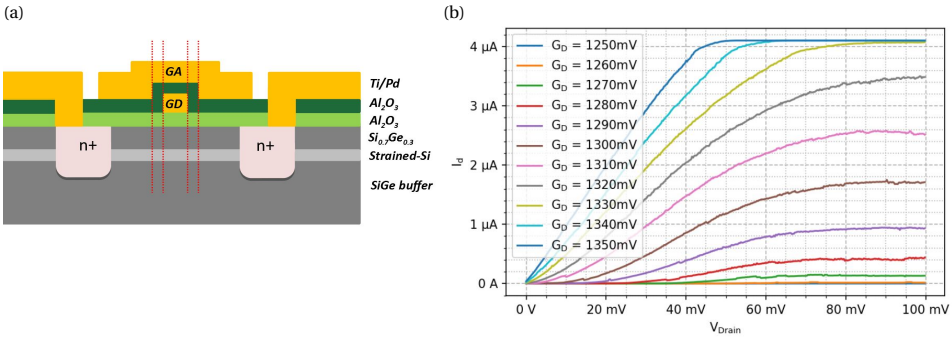

Figure 4.7: Cross section (a) and output curve (b) of FET4

The idea is to use a large gate *GA* to accumulate charges and use a fine gate *GD* to pinch-off the channel. However, this transistor requires over 1 V for both *GA* and *GD* to turn it on. Besides, as can be seen from its output curve, it is hard for a current to pass through with small source-drain bias voltages. As indicated by the red dot line in fig. 4.7(a), this is probably due to the oxide located at the wall of *GD*, which makes *GA* far from the 2DEG layer and thus creates extra barriers in the channel.

4.2.2. HYSTERESIS ISSUE

Throughout the experiments, we notice that V_{th} drifts as the sweeping range of V_g increases. Here we use a transistor fabricated in the same batch as FET3 for more explanation.

Fig. 4.8 shows a set of I_d-V_g curves (linear scale). The end value of the V_g sweeping range is increased by 50 mV after each forward and backward scans. The first curve is from 400 mV (off state) to 800 mV and the last one is from 1500 mV to 400 mV.

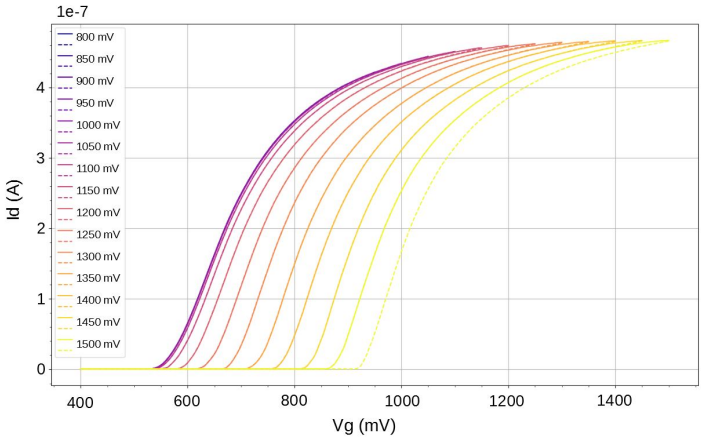

Figure 4.8: Linear scale I_d-V_g curves to check the device hysteresis. For each sweeping range of V_g, a forward and a backward scan is carried out, the results are represented in solid lines and dash lines, respectively.

The curves obtained before sweeping V_g up to 1100 mV overlap well. From the backward scan from 1100 mV to 400 mV, V_{th} starts to shift towards the positive direction. Moreover, the forward scan overlapped with the previous backward scan with 50 mV less in the V_g sweeping range, indicating that the drift occurs during the on states of the transistor. The reason for the hysteresis might be that some electrons get trapped at the substrate or interfaces and that these traps are not depleted when the transistor is switched off. Based on the experiment above, the voltage on the gate with respect to drain or source (V_{gs} or V_{gd}) should not be larger than 1 V in later experiments to avoid the hysteresis issue.

4.3. CHARACTERIZATION OF SINGLE QUANTUM DOTS

The gate pattern of the single-metal-layer quantum dots is the same for all batches as it is shown in Fig. 3.1(b). Single quantum dots without floating gate structures are first tested at 4 K to check the turn-on and pinch-off voltages for each gate. After that, we cool down an integrated device from the same batch to 20 mK in the dilution refrigerator. There we set the transistor gate voltage to be sufficiently high (0.8 V above the maximum V_{in}) to keep the transistor conducting, and we bias the single quantum dot to the few-electron regime.

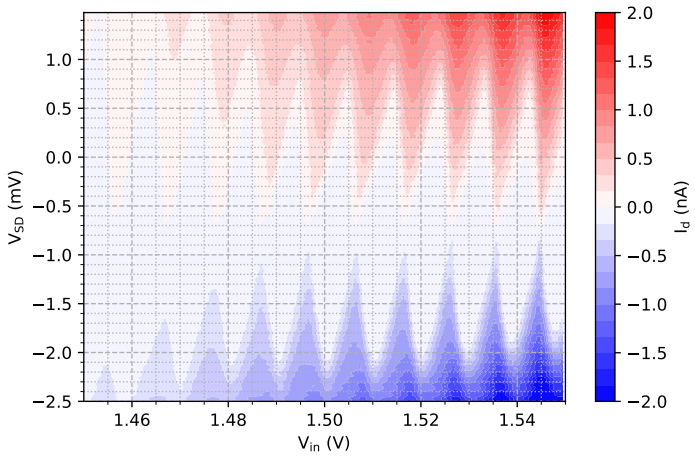

Figure 4.9: Coulomb diamond plot of an integrated device. V_{SD} is the source-drain bias across the quantum dot and V_{in} is applied directly to the plunger gate with the transistor conducting.

Fig.4.9 shows several Coulomb diamonds measured on the quantum dot [5]. The device is stable after cooling in the refrigerator for over a month. The source-drain bias voltage of the quantum dot V_{SD} has an offset of around 0.7 mV since the DAC has an offset and it is directly connected to the drain ohmic contact of the quantum dot. This offset can be reduced by first increasing the DAC output voltage 1000 times and then routing the DAC output to a 1000:1 voltage divider. The charging energy E_c and lever arm α extracted from the data close to V_{in} of 1.5 V are around 9 meV and 0.1, respectively, which are comparable to other works[4, 5].

4.4. TRANSISTOR ON-OFF VOLTAGE SET

The on and off regions of the transistor are clear on the transfer curves of discrete devices. However, there we set the source voltage to ground ($V_g = V_{gs}$) for all the measurements. When integrating with quantum dots, the source of the transistor is connected to V_{in} as indicated in Fig.1.3. Thus the potential of the transistor is lifted. Taking also the threshold voltage drifting into consideration, we make the following experiment on an integrated device to define the transistor on- and off-voltages.

We conduct a V_{in}–V_g scan while measuring the current through the quantum dot. To avoid the input voltage being maintained on the floating node, thereby resulting in no current difference between floating and non-floating mode, we discharge the capacitor before each sweep of V_g from low to high. The result is shown in Fig.4.10. We see that the gate voltage should be around 0.55 V higher than the input voltage to turn on the transistor. Since we set V_{in} to around 1.5 V, V_g^{ON} and V_g^{OFF} were set to be 2.2 V and 1.6 V for this device.

In general, we use all the experiments mentioned above to select functional devices

[5] Results of device *C* described in Chapter 5, fabricated in the same batch as FET3.

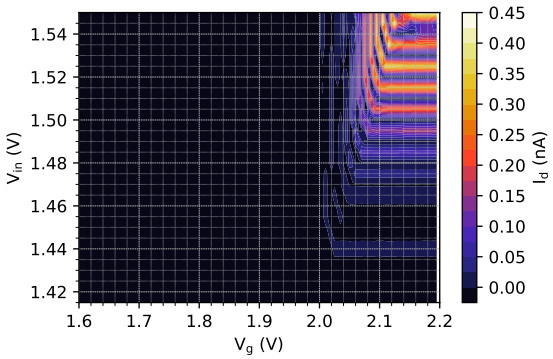

Figure 4.10: V_{in}-V_g scan to define the transistor switching range, with the colour representing the current through the quantum dot.

and define their operation voltages. We will start to investigate more on the floating gate behaviour in the next chapter.

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5

QUANTUM DOT WITH A FLOATING PLUNGER GATE

To investigate the charge-locking performance of the switched-capacitor circuit, we characterize the voltage accuracy and leakage rate on the floating node of the integrated devices. Furthermore, we demonstrate that the electrochemical potential of the quantum dot can follow a pulse signal while the dot is partially floating, which is essential for applying this strategy in qubit experiments.

5.1. VOLTAGE ACCURACY

We have discussed factors that influence the voltage accuracy on the floating node in Chapter 2. Both random errors and systematic errors are affected by the device sizes. Therefore, we make three devices (device *A*, *B* and *C*) with the same quantum dot design but different transistor and holding capacitor sizes and compare their voltage variations on the floating node. The schematic of the devices is provided in Fig.1.3 that a switched-capacitor circuit is connected to gate *P* of a single quantum dot. The device dimensions and other specifications are listed in Table 5.1. Here the 0.4 μm lateral diffusion as measured in Section 3.1.3 is also taken into consideration. The relative permittivity of ALD Al_2O_3 is discussed in Section 3.1.4. V_{in}, V_g^{ON}, V_g^{OFF} and V_{th} are set using the method provided in section 4.4. The expected random errors are calculated from Equation 2.6 and 2.7 and the expected systematic shifts are calculated according to Equation 2.14 and 2.15 in Chapter 2. We will analyse the overall voltage shifts obtained from the experiments (last line in the table) in detail in this section.
Devices *A* and *B* are mounted in the dilution refrigerator Bluefors BF-XLD400 and device *C* is mounted in Oxford TRITON400-10. Both refrigerators operate at a base temperature below 10 mK and at zero magnetic field. All current measurements through the quantum dot are performed with a 100 μV source-drain bias applied across the quantum dot.

Parts of this chapter have been published in Appl. Phys. Lett. 117 (2020)

	Device *A*	Device *B*	Device *C*
Designed C_H area	15 μm × 15 μm	15 μm × 15 μm	100 μm × 100 μm
Designed transistor channel size (L×W)	10 μm × 10 μm	10 μm × 1 μm	10 μm × 1 μm
Corrected channel size with 0.4 μm lateral diffusion (L×W)	9.2 μm × 10.8 μm	9.2 μm × 1.4 μm	9.2 μm × 1.4 μm
Corrected source-drain overlap area with 0.4 μm lateral diffusion	0.9 μm × 10.8 μm	0.9 μm × 1.4 μm	0.9 μm × 1.4 μm
Target Al_2O_3 thickness	20 nm	20 nm	20 nm
Al_2O_3 relative permittivity (measured)	7	7	7
Target $Si_{0.3}Ge_{0.7}$ thickness	30 nm	30 nm	30 nm
$Si_{0.3}Ge_{0.7}$ relative permittivity (expected)	13.05	13.05	13.05
Expected C_H	0.697 pF	0.697 pF	30.98 pF
Expected $C_{channel}$	0.171 pF	0.022 pF	0.022 pF
Expected C_{gs}	30 fF	3.9 fF	3.9 fF
V_g^{ON} - V_g^{OFF}	3.3 V - 2 V	1.98 V - 1.5 V	2.2 V - 1.6 V
V_{in}	1.14 V - 1.27 V	1.21 V- 1.24 V	1.43 V - 1.52 V
V_{th} (estimate)	1.95 V	0.55 V	0.55 V
Elementary charge limit $\Delta V = e/C_H$	0.23 μV	0.23 μV	0.0052 μV
Thermal noise $\sqrt{kT/C_H}$ at 10 mK	0.44 μV	0.44 μV	0.06 μV
Expected ΔV_c	9.3 mV - 26.4 mV	2.9 mV - 3.5 mV	0.04 mV - 0.08 mV
Expected ΔV_p	53.65 mV	2.67 mV	0.08 mV
Measured peak shift	44 mV - 48 mV	2.8 mV - 5.4 mV	0.5mV -1 mV

Table 5.1: Device specifications

5.1.1. CHANNEL CHARGE INJECTION

As a reference, we first test the devices in static mode with gate P not floating. The current through the quantum dot is experimentally measured while the transistor is conducting. In the floating mode tests, we first turn on FET_1 to charge the capacitor and then turn it off. After 10 ms, we measure the current through the quantum dot while gate P is floating. As shown in Fig. 5.1, the patterns of the Coulomb peaks measured in floating mode (orange traces) are consistent with those measured in static mode (blue traces), but shift in V_{in}. The measured voltage shifts (which are expected to contain ΔV_c and ΔV_p, the random errors are in principle orders of magnitude smaller than the systematic errors) are extracted from the shifts of the individual Coulomb peaks at different V_{in}. As can be seen from Table 5.1, the measured dependence of gate voltage shift versus dimensions matches the predicted trend very well. Device B shows smaller shifts than device A due to its smaller transistor channel size; and the voltage shift of device C is less than that of device B because of its larger holding capacitance.

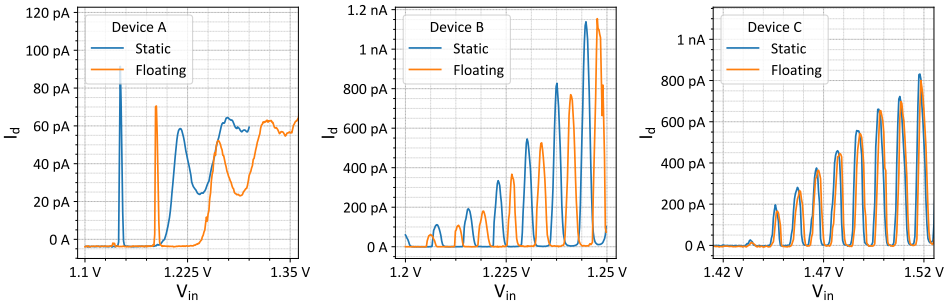

Figure 5.1: Current through the quantum dot as a function of V_{in}, with device A, B and C operating in static and floating mode. Patterns of Coulomb peaks are consistent between the blue line (static mode) and orange line (floating mode).

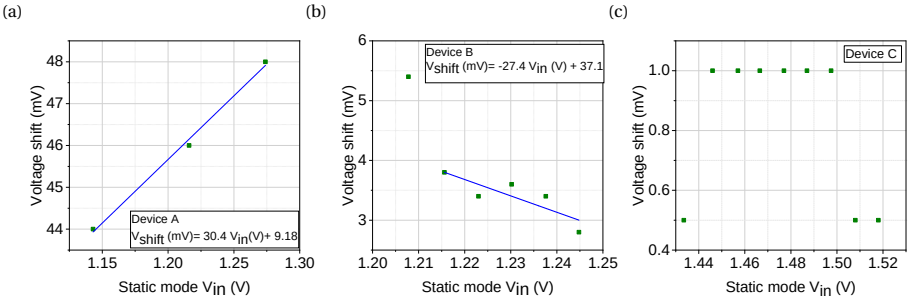

Figure 5.2: Voltage shift of each Coulomb peak as a function of the input voltage in the static mode for device A, B and C. Blue lines are linear fits of all data for device A, and the 5 points on the right for device B.

To analyse the influence of the channel charge on the voltage variation between static and floating mode, we plot the overall voltage shift of each Coulomb peak as a function of the corresponding input voltage in the static mode in Fig. 5.2. According to Equation

2.14 and 2.15, ΔV_p is independent of V_{in} and ΔV_c is inversely proportional to V_{in} with the coefficient $-C_{channel}/2C_H$. Thus, we can extract the ratio of C_H and $C_{channel}$ by linear fitting the function of the total voltage shift to the input voltage.

We see a positive slope of the fitting curve for device A in Fig.5.2 (a). The reason for it is unclear, possibly due to drifting of the quantum dot in the course of the measurements (device A is less stable). For device C shown Fig.5.2 (c), the step size for V_{in} is set to 0.5 mV in the experiment, which limited the resolution of the results.
Here we discuss in detail for Fig.5.2 (b), the negative slope of the fitting curve for device B is consistent with Equation 2.14, indicating that under a fixed V_g^{ON}, a larger V_{in} results in fewer charges in the channel and thus a smaller voltage shift upon switching off the transistor. For the five Coulomb peaks at the highest V_{in} (the leftmost peak is shifted more than expected), the fitting result is

$$V_{shift}(mV) = -27.4V_{in}(V) + 37.1 \tag{5.1}$$

Therefore, the ratio of C_H and $C_{channel}$ is extracted to be 18.2 for device B from the measurement. Substituting it into Equation 2.14, ΔV_c is calculated to be 5.1 mV to 5.9 mV corresponding to the input voltage of 1.215 V to 1.245 V. As can be seen from Fig.5.2 (b), the individual shifts fluctuate around the overall linear trend by about ±0.2 mV. By comparison, the random shifts expected from thermal noise and charge quantization (Eq. 2.7 and Eq. 2.6) are below 1 μV. However, the measured voltage fluctuations match well the measured $1/f$ noise caused by background charge fluctuations modulating the dot potential. The measurement takes a few minutes to complete and the $1/f$ noise amplitude at 0.01 Hz is indeed of order 0.2 mV/$\sqrt{\text{Hz}}$ (see noise analysis in Section 5.1.3). In addition, we will discuss in Section 5.2 that the average voltage decay rate for device B in the first 40 seconds after opening the transistor was approximately 2.8 μV/s. Therefore, the voltage shift on the floating gate due to leakage through the holding capacitor is negligible during the 10 ms interval between the moment the transistor is opened and the time of measurement.

5.1.2. GATE-SOURCE PARASITIC CAPACITANCE

The gate-source parasitic capacitor couples the switching signal on the gate of the transistor to the floating node. To measure its influence on the maintained voltage, we compare the voltage shift between static and floating mode for device B with different transistor switching ranges, as shown in Fig. 5.3. V_g^{ON} is fixed at 1.98 V and V_g^{OFF} is set to 1.5 V, 1.3 V and 1.1 V in the tests, respectively. The voltage shifts of the Coulomb peaks summarized in Fig. 5.3 (d) show that a larger switching range results in larger offsets, the trend of which is consistent with Equation 2.15. The average distance between the blue and black line in Fig. 5.3 (d) is 4.7 mV, corresponding to 0.4V difference in V_g^{OFF}. The ratio of C_{gs} and C_H is then estimated to be 84 based on the experimental data. Inserting this result into Equation 2.15, ΔV_p is calculated to be 5.64 mV in case V_g^{OFF} is 1.5 V. However, the ratio of C_{gs} and C_H is expected to be 179 based on the specifications in Table 5.1. The difference might due to overexposure during lithography for the gate metal layer, making the gate-source overlap area larger than expected.

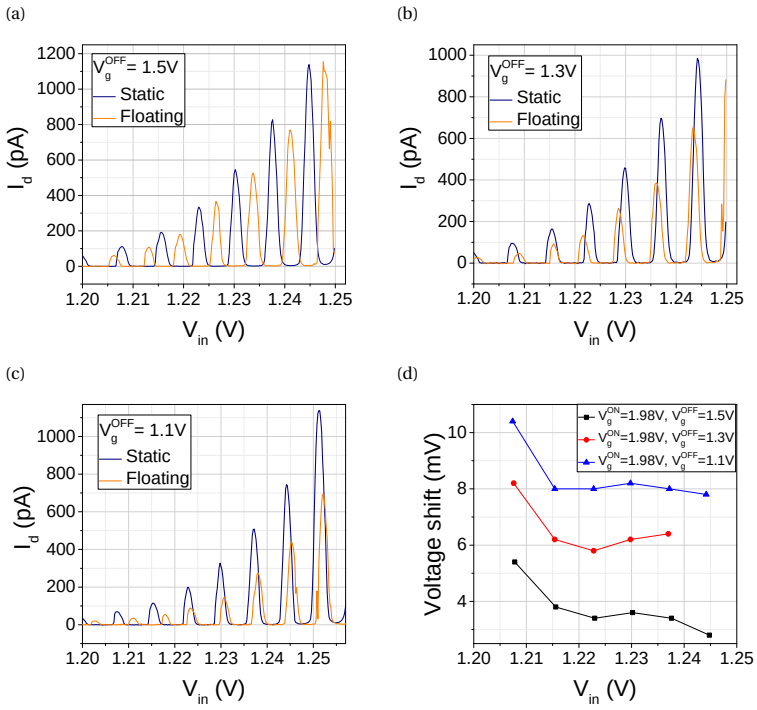

Figure 5.3: Static (blue) and floating (orange) mode Coulomb blockade peaks of device B with V_g^{ON}=1.98V and (a) V_g^{OFF}=1.5 V, (b) V_g^{OFF}=1.3 V and (c) V_g^{OFF}=1.1 V. The peak shifts are summarized in (d) as a function of the input voltage in the static mode.

5.1.3. NOISE ANALYSIS

There are basically two methods to characterise the noise level on the floating node. One is using the probability density function (PDF) to describe the distribution of the noise amplitude, which does not include the information about how fast the signal varies in the time domain. The other more common way is to characterise noise with its power spectral density (PSD), for which the sampling rate needs to be considered when processing the data. Although the latter contains more information than the former, the PDF is actually more intuitive in specific experiments. Therefore, for some earlier devices, we still use the PDF method, while many later analysis are mainly based on PSD.

We characterize the noise level of device A using the probability density function. A Coulomb peak is measured in the static mode before and after the noise test as shown in Fig.5.4(a), and no obvious shift is observed suggesting the noise measurement is reliable. During the noise measurement, we select a point on the flank of the peak (V_{in} is set to locate this point in the floating mode), turn the transistor on and off and then measure the current flowing through the quantum dot and repeat this 500 times. The inset shows the measured current values. The histogram is plotted in Fig.5.4(b) where the current is divided in 1 pA intervals. The distribution can be fit with a Gaussian function. We use the full width at half maximum (FWHM) of the peak to characterize the noise level. In

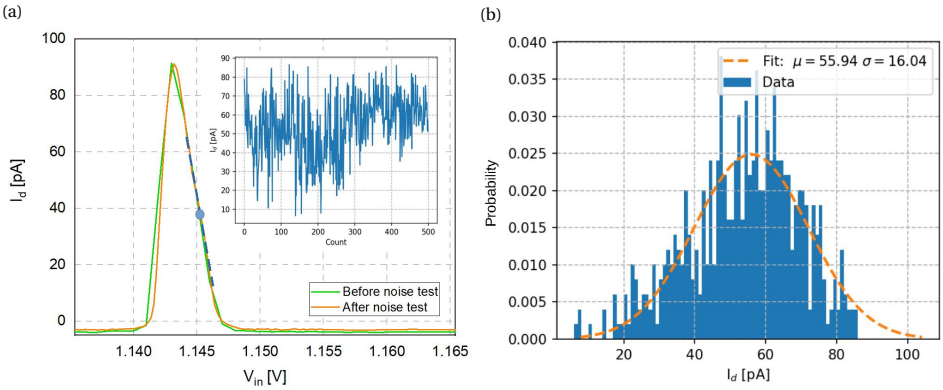

Figure 5.4: (a) A static mode Coulomb peak of device *A* before (green) and (orange) after the noise measurement. We switch the transistor and measure the current indicated by the blue point 500 times, the inset figure presents the result. (b) Distribution of the measured current fit by a Gaussian function.

this case, FWHM = 2.35σ = 38.5 pA. The current is converted into a voltage by dividing by the slope at the set point (shown in Fig.5.4(a)). Finally, the random voltage variation on the floating node for device *A* is estimated to be 0.5 mV.

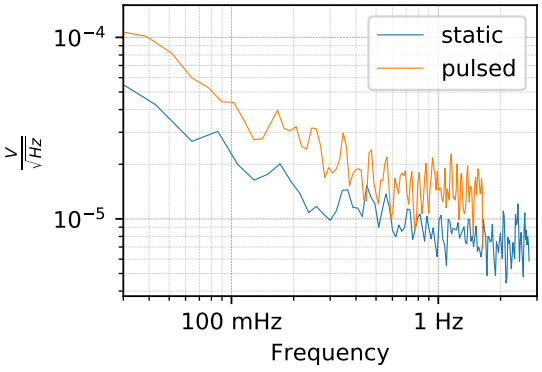

Figure 5.5: Noise spectrum referred to the plunger gate of device *B* measured with the device in static (blue) and pulsed (orange) mode.

For device *B*, we compare the noise power spectral density with and without its plunger gate floating. In the static mode, the transistor is kept on, we sample the current through the quantum dot 1000 times at a rate of 5.5 Hz. The pulsed (floating) mode measurement is the same as described for device *A*, the transistor is turned on and off and then the current through the quantum dot is measured. Limited by the switching speed in the experimental setup, the process is repeated 1000 times with a sampling rate of about 3.3 Hz. The measured current as a function of time is converted into the fre-

quency domain by Fourier transform. The noise spectrum for both modes is shown in Fig.5.5, which follows an 1/f shape at low-frequencies, as is common in quantum dot devices where background charge fluctuators dominate. Extrapolating the curve measured in pulsed mode (orange line) towards lower frequency, the noise amplitude at 10 mHz is estimated to be around 0.2 mV/$\sqrt{\text{Hz}}$.

5.2. DISCHARGING RATE AND LEAKAGE PATH

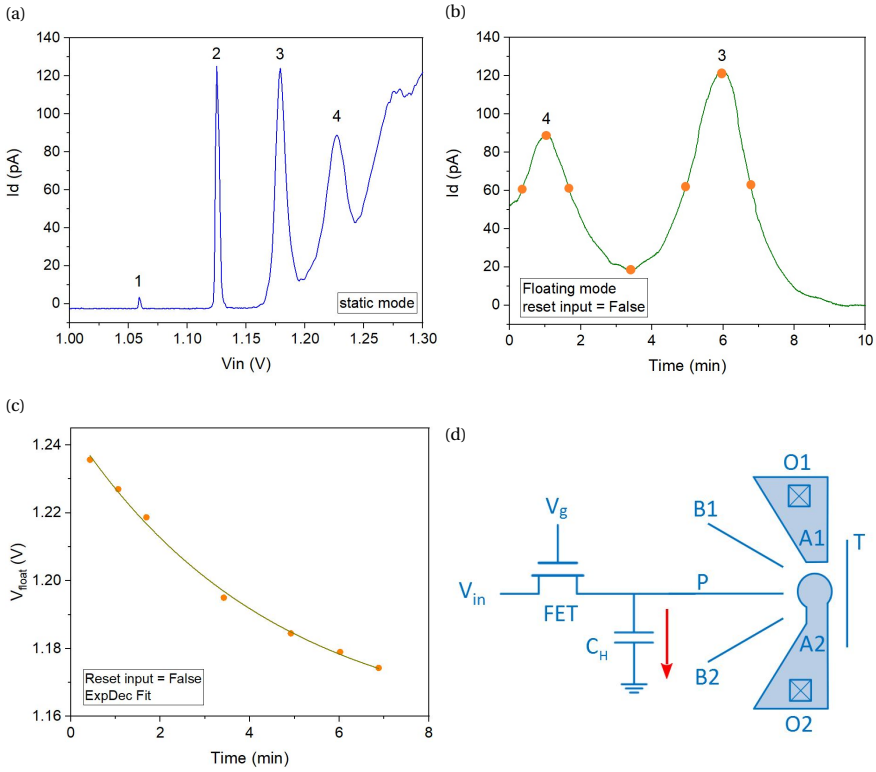

Figure 5.6: Leakage rate measurement of device *A* without reset input V_{in}. (a) A few Coulomb peaks measured in the static mode as reference. (b) Current through the quantum dot as function of time after floating its plunger gate. A few points (orange dots) are selected to relate the current level to the voltage on the plunger gate. (c) Voltage decay on the floating node fitted by an exponential function. (d) An indication of the main leakage path.

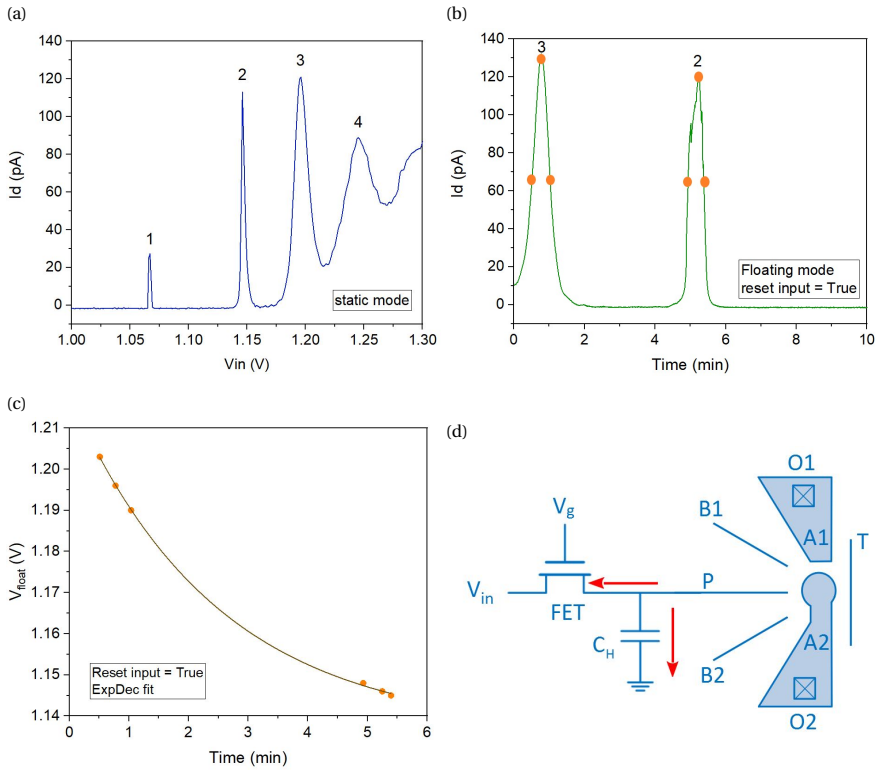

Figure 5.7: Leakage rate measurement with reset input. (a) Static reference. (b) Result of the floating mode test. (c) Exponential fitting of the voltage decay on the floating node. (d) An indication of the leakage path

There are two main paths for charges on the floating node to leak away, through the holding capacitor to ground or through the transistor channel to its drain side. The voltage on the floating node is expected to decay exponentially with time, expressed as

$$V(t) = V_0 exp(-t/\tau) + V_{final}, \tag{5.2}$$

where time constant $\tau = RC$. C is the total capacitance of the floating node to ground, dominated by C_H in this case. Both R and V_{final} depends on the the parasitic resistance of the holding capacitor and the transistor off-state channel resistance.

To measure the discharging rate of device A, a static mode test is first carried out. Fig. 5.6(a) shows 4 Coulomb peaks and their corresponding bias voltages on the plunger gate. Then V_{in} is set higher than the gate voltage of peak 4. In the floating mode test, we switch the transistor on and off and subsequently measure the current through the quantum dot as a function of time. In Fig. 5.6(b), the patterns of peak 4 and 3 appear over the course of 10 minutes[1]. We select a few data points from the figure (orange dots) and relate their current level to the potential on the plunger gate according to Fig. 5.6(a).

[1] We note that when measuring the decay rate over a period longer than a few minutes, the results could be influenced by slow drift of the quantum dot.

The data can be fitted with an exponential decay curve shown in Fig. 5.6(c). The time constant extracted from the discharging function is 270 s. During the measurement V_{in} is not changed, thus, the main leakage path is through the holding capacitor as indicated in Fig. 5.6(d). Since the holding capacitance of device A is about 0.697 pF (listed in Table 5.1), the parasitic resistance of the holding capacitor R_{cap} is estimated to be 387 TΩ.

Next, we study the influence of the transistor off-state resistance $R_{channel}$ on the decaying rate of the floating node voltage. We process the same experiment but reset V_{in} to ground after switching off the transistor. The results are shown in Fig. 5.7. Specifically, the reference Coulomb peaks should in principle be identical with that for the first test (plotted in Fig. 5.6(a)), but the peaks slightly shift to the positive direction of V_{in} as shown in Fig. 5.7(a). Then we bias V_{in} higher than the voltage required for peak 4, switch on and off the transistor, reset V_{in} to ground and start to measure the current on the dot versus time. The result is plotted in Fig. 5.7(b). We see the pattern of peak 2 and 3 in 10 minutes. However, peak 4 is missing possibly because the changes in V_{in} is coupled to the floating node through the gate-source and gate-drain parasitic capacitors, which leads to an extra voltage shift and thus a lower starting voltage in the floating mode test result. Nevertheless, the decay curve is fitted (5.7(c)) and the discharging rate is approximately 149 s. The leakage path in this case is indicated in 5.7(d) where the total resistance R is regarded to be R_{cap} and $R_{channel}$ in parallel, calculated to be 214 TΩ. Taking R_{cap} of 387 TΩ from the last experiment, $R_{channel}$ is then 480 TΩ. The results are summarized in Table 5.2.

	Discharging function	τ (s)	R_{cap} (TΩ)	$R_{channel}$ (TΩ)
Not reset V_{in}	$V_{float}(t)$= 0.09 exp (-t/270) + 1.15	270	387	-
Reset V_{in}	$V_{float}(t)$ = 0.08 exp (-t/149) + 1.14	149	387	480

Table 5.2: Discharging function and extracted parameters for device *A*

We conclude that for this device, when resetting the input to ground after switching-off the transistor, charges on the floating node leak through the holding capacitor and the transistor at a comparable rate, thus there is no dominant path. However, if we consider connecting V_{in} of multiple DRAM-like cells to one DAC line, the range of the voltages applied at the respective V_{in} is determined by the variations of gate voltages required on the quantum dots, which is probably much smaller than the whole range from V_{in} to ground. In that case, it is the resistance of the capacitor that dominates the discharging rate.

In practice, people focus more on the initial part of the voltage decay if the voltage on the node is to remain close to its target value. Comparing with the entire discharging process, the change of the floating node voltage over time in the beginning of an exponential decay is approximately linear. So for device *B* and *C*, we measure the average discharging rate in the first few seconds.

Fig. 5.8 shows the data used to estimate the discharging rate of the holding capacitor of device *B*. The dot is biased at point 1 as shown in panel (a), then the floating mode test is processed. Panel (b) shows that the current increased from roughly 590 pA to 640 pA (point 1 to 2) during the first 40 s, corresponding to a 0.11 mV drop on the floating node.

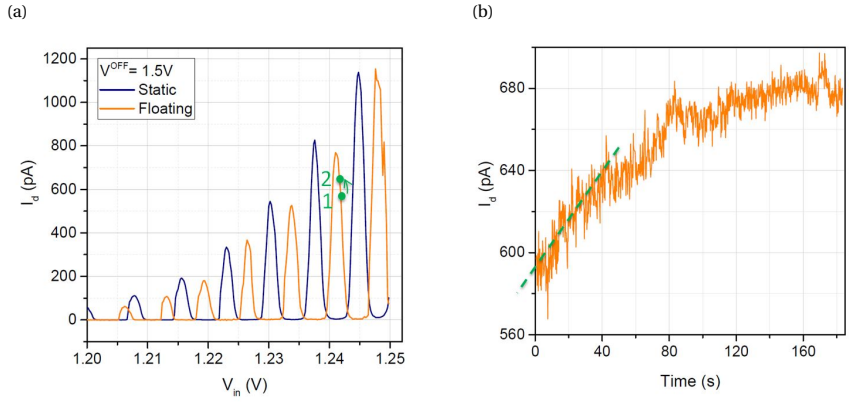

Figure 5.8: (a) Coulomb blockade trace for device *B* in static and floating mode. (b) Current through the quantum dot as a function of time in the first 180 s after switching the transistor off.

Linearizing the beginning of the exponential, the average discharging rate is estimated to be 2.8 μV/s. Applying the same method for device *C*, the average discharging rate in the first 80 s was estimated to be 5.9 μV/s with results plotted in Fig. 5.9.

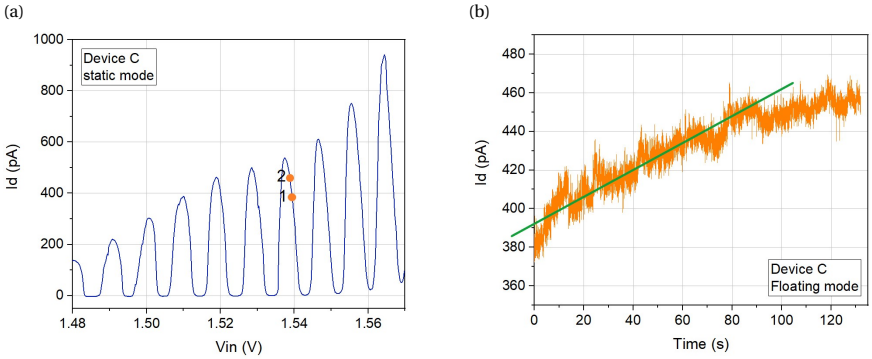

Figure 5.9: (a) Coulomb blockade trace for device *C* in static and floating mode. (b) Current through the quantum dot as a function of time in the first 120 s after switching the transistor off

Since the parasitic resistance is highly dependent on the dielectric quality and the physical structure, the discharging rate varies between devices. Nevertheless, they are all of the same order. In general, assuming a floating node requiring a 1V potential and a discharging time constant of 100 s, it will take about 0.1 ms for the voltage to drop 1 µV which would result in a refreshing frequency of 10 kHz.

5.3. FAST LINE OPERATION IN THE FLOATING PERIOD

For qubit operation and readout, gate voltage pulses must be applied to one or more of the quantum dot gates. We now test the compatibility of applying such pulses with a switched-capacitor circuit present and operated in floating mode. In principle the volt-

age pulses can be applied either to a floating gate (e.g. via the holding capacitor) or to another gate. Either way, the question is to what extent the presence of the capacitor and transistor that form the SC circuit distorts the waveform. Here we perform a preliminary test on device *C* for voltage pulses applied to a gate that is not floating.

5.3.1. CALIBRATION

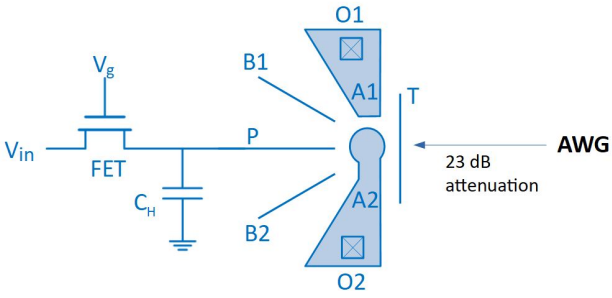

Figure 5.10: Schematic of the experiment setup. The voltage pulses generated by an AWG at room temperature is applied to gate *T* through a coaxial cable with approximately 23 dB attenuation.

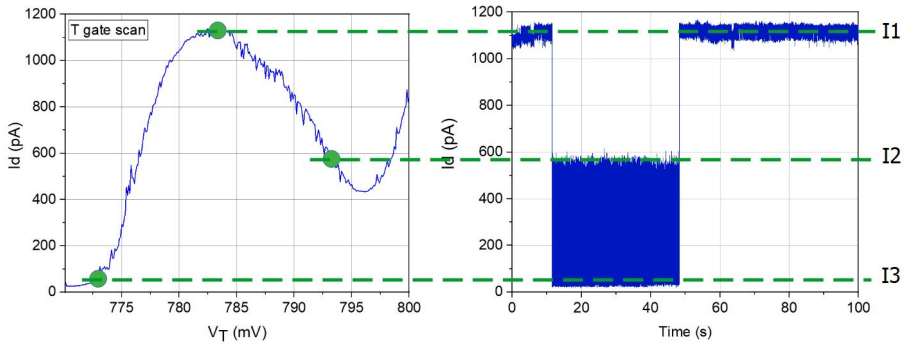

Figure 5.11: Attenuation line calibration. A 783 mV DC voltage is applied to gate *T* to make about 1050 pA current (I1) flow through the quantum dot. Then 140 mVpp, 100 Hz voltage pulses are generated by an AWG and applied to gate *T* through in total 23 dB attenuators, result in the current through the dot oscillates between I2 and I3. The current level is consist with ±10 mV voltage pulses adding to the DC bias voltage directly on gate *T* .

The output of an arbitrary waveform generator (AWG) is connected through a coaxial cable to gate *T* of the quantum dot as indicated in Fig. 5.10. Since there are a series of attenuators along the cable, we execute the following experiment to check whether the total attenuation is 23 dB as specified.

A static mode scan is made on gate *T* to locate a Coulomb peak as shown in the left panel of Fig. 5.11. Then the DC bias voltage is set to 783 mV at the current peak . Next, the AWG is enabled to send out a square wave of 140 mVpp, 100 Hz that would attenuate

to 20 mVpp to the gate and overlap with the DC bias signal. The right figure is a plot of the current flowing through the dot as a function of time, where I1 corresponds to the peak current without fast line signal. I2 and I3 correspond to the current level when the voltage on gate T is 773mV and 793mV respectively.

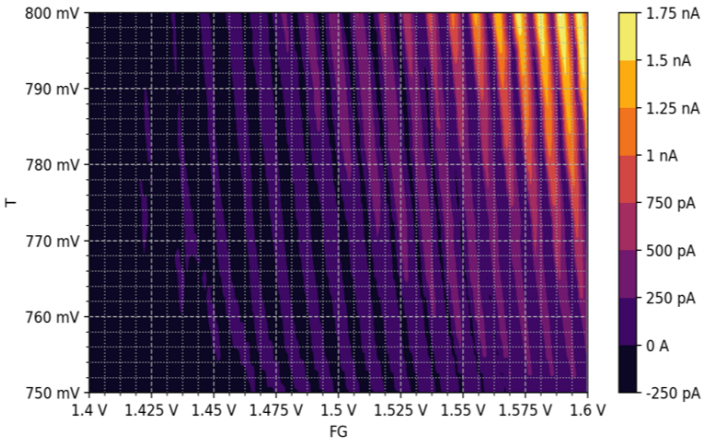

Figure 5.12: Stability diagram of gate T and the floating plunger gate

Next, we check whether a ±10 mV voltage difference on gate T is able to make an observable and stable difference in the coulomb peak patterns. Fig. 5.12 is a stability diagram of the device as a function of gate T and the floating plunger gate. After stepping the voltage on gate T to the next value in the plot, we perform the floating mode test. The colour scale represents the current through the quantum dot, which shows the modulation of the dot potential from gate T and a stable pattern of the Coulomb peaks.

5.3.2. EXPERIMENT

In this experiment, we provide voltage pulses to gate T of device C, and check if the electrochemical potential of the quantum dot is able to follow the signal while gate P is floating.

The sequence of the experiment is depicted in Fig.5.13. The input voltage is first set to 1500 mV, then the transistor is switched on and off (2200 mV for on-voltage and 1600 mV for off-voltage as described in section 4.4) to deliver V_{in} to the floating node. The holding capacitor connected with gate P maintains V_{in} for the next 200 ms. In the first 100 ms, a 140 mV_{pp}, 100 Hz square wave is provided from an arbitrary waveform generator through a 23 dB attenuator to gate T, adding to a DC bias voltage of 790 mV on the same gate. In the second 100 ms, the device is still floating but without the pulsing signal. After that, we set V_{in} to 1501 mV and repeat the procedure. The current through the quantum dot is measured as a function of time; the sampling rate is 1 kHz. The time-based results are first converted into V_{in}-based results, then we extract the current data corresponding to the high level of the voltage pulse (T=800 mV), the low level of the voltage pulse (T=780 mV) and the second 100 ms without pulses (T=790 mV), respectively. We plot these 3 groups of data separately as a function of V_{in} (solid lines, the error

bars indicate the standard deviation of each data point) and compare the shape of the Coulomb peaks to the static measurement references, which is obtained under the condition that 780 mV, 790 mV and 800 mV DC voltages are directly applied on gate T while gate P is not floating (dotted lines). The shapes of the Coulomb peaks are consistent with the respective reference measurements.

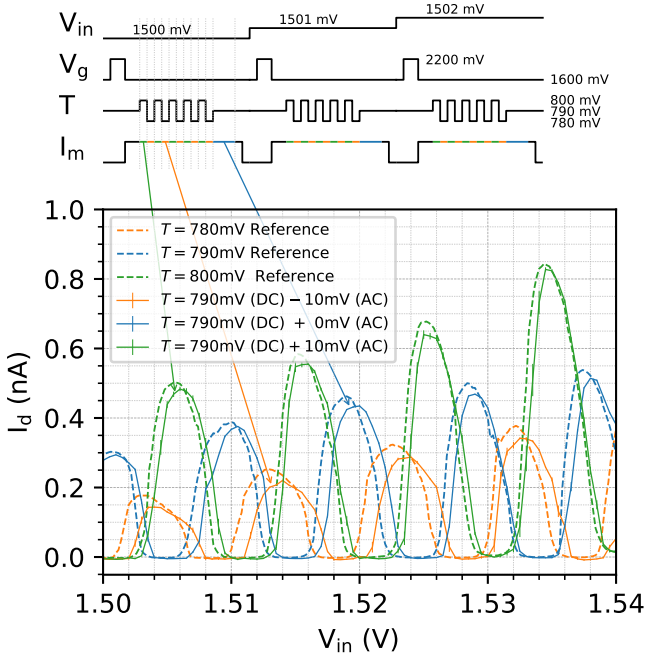

Figure 5.13: The input voltage V_{in} is stepped from 1.5 V to 1.54 V that covers several Coulomb blockade peaks. For each V_{in}, we first floated gate P by setting V_g from "high (2200 mV)" to "low (1600 mV)". Then a 100 Hz, ± 10 mV pulse signal is applied to gate T through a bias tee during 100 ms, adding to a 790 mV DC bias voltage, while we continuously measure the current flowing through the quantum dot. The current through the dot corresponding to the high (T = 800 mV, green lines) and low (T = 780 mV, orange lines) stages of the voltage pulse, as well as the current during a subsequent time interval without gate voltages pulses (T = 790 mV, blue lines), were extracted separately and compared to the static mode measurement results (dotted lines).

The 0.6-1.0 mV voltage shift of the center peaks (blue solid versus dotted traces) is in agreement with the expected shift from channel charge injection and parasitic capacitance of the transistor upon switching off. Furthermore, the peaks obtained while applying a 100 Hz square pulse overlap closely with their expected positions, see the green and orange solid and dotted lines. The 0.6 mV larger average shift for the orange versus the green solid lines indicates that the square pulse amplitude at the gate is slightly larger than the intended ±10 mV, which can be explained by a deviation (within the specified tolerance) of the values of the attenuators placed in the transmission line connected

to gate T. These results show that the voltage pulses on gate T are not affected by the switched-capacitor circuit and its floating operation on gate P.

5.3.3. AC SIMULATION

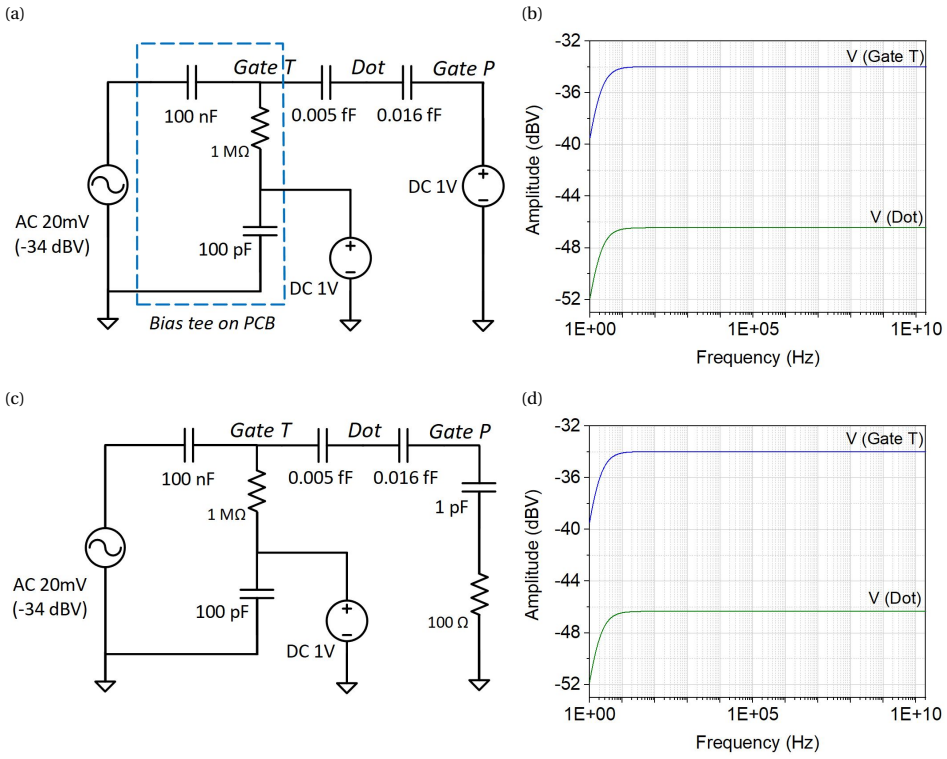

Figure 5.14: Small AC signal simulation. (a) Circuit model without switched-capacitor circuit and (b) its AC response on gate T and the quantum dot. (c) Circuit model when gate P is floating and (d) its AC response on gate T and the quantum dot.

The frequency of the voltage pulse in the experiment is limited by the 1 kHz sampling rate during the present measurement. Here we simulate the AC response on the quantum dot for higher frequencies in LT spice. Fig.5.14(a) and (c) show the circuit model used for the analysis in the static and floating mode, respectively. Gates T and gate P are capacitively coupled to the quantum dot. The gate-dot capacitances were extracted from the corresponding Coulomb blockade peak spacing. A small AC signal (20 mV_{pp}) is applied to gate T through a bias tee on the PCB that carries the sample. In static mode, gate P is connected to a DC voltage source. In floating mode, gate P is connected to a 1 pF holding capacitor in series with a 100 Ω parasitic resistor. The input frequencies range from 1 to 20 GHz. The AC response corresponding to static and floating mode conditions show the same voltage magnitude both on gate T and on the quantum dot as shown in Fig.5.14(b) and (d). Based on the results from the experiment and simulations,

we expect the large capacitor that stores the floating node voltage (on gate P) not to impact the modulation of the dot potential in response to a pulse on gate T up to 20 GHz.

So far, we demonstrated in this chapter that a switched-capacitor circuit placed on the same chip with a quantum dot can function as a local voltage source. Nevertheless, the sizes of capacitors are orders of magnitude larger compared to the quantum dot, which is not favorable for scaling. In industry, advanced processes for transistor fabrication such as FinFET or FDSOI achieve both $C_{channel}$ and C_{gs} of around 1 fF[1]. The required value for C_H is then around 1 pF (for a 1 µV voltage accuracy). Vertical/trench capacitors as used in technology achieve densities of 700 nF/mm^2[2]. This brings the area of C_H to 1.4 µm^2 per gate, which is still larger than the dot size itself. Therefore, we believe the ultimate scaling may rely on sparse quantum dot arrays that leave more space for the electronic circuits[3]. We will discuss this approach more in the next chapter.

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[3] J. M. Boter, J. P. Dehollain, G. van Dijk, T. Hensgens, R. Versluis, J. S. Clarke, M. Veldhorst, F. Sebastiano, and L. M. K. Vandersypen, *A sparse spin qubit array with integrated control electronics,* in *IEEE International Electron Devices Meeting (IEDM)* (IEEE, New York, 2019) pp. 31.4.1–31.4.4.

6

DEMULTIPLEXER AND INTERCONNECT FOR A SCALABLE INTERFACE

With the floating gate strategy described in previous chapters, we could use one voltage source to provide different voltages to multiple quantum dot gates. Although the number of DAC lines is reduced, we need extra signal lines to control the transistors in the switched-capacitor circuits. To reduce the number of wires for scaling, these control signals need to be demultiplexed on-chip and only the inputs of the demultiplexer are connected to higher temperature stages. Fig.6.1 schematically illustrates the approach.

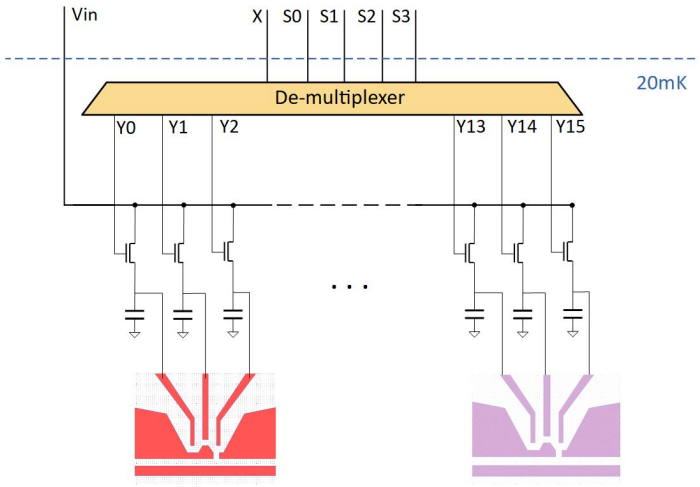

Figure 6.1: Schematic of a demultiplexer integrated with switched-capacitor circuits and quantum dots

To provide voltages to 16 quantum dot gates, one signal line (V_{in}), one input line (X) and four address lines (S0 to S3) are required from higher temperature stages. The outputs of the demultiplexer (Y0 to Y15) are connected to the transistor gates for switching. Further, adding one address line could double the output number without adding extra signal and input lines. As a purely digital operation, the on- (or off-) state voltage can be set sufficiently high (or low) to overcome the transistors' threshold voltage variation and the noise during switching.

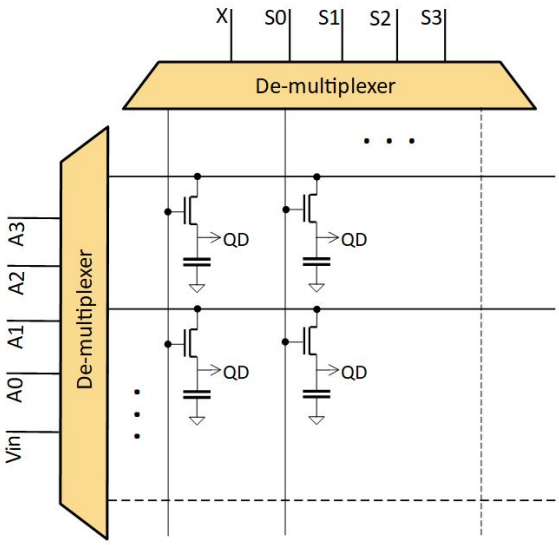

Figure 6.2: Schematic of demultiplexers, switched-capacitor circuits and quantum dots arranged in a DRAM-like matrix.

Moreover, when considering to demultiplex V_{in} from a second dimension to form a DRAM-like matrix as shown in Fig. 6.2, the output voltages that to be maintained on the holding capacitors should be precise and differ among each quantum dot gate, which brings in more challenges in the design and calibration phase. We mainly focus on demultiplexing digital signals in the following discussions.

6.1. DEMULTIPLEXER STRUCTURES AND REQUIREMENTS

There are three possible structures for making a demultiplexer:
Option 1: Demultiplexer based on the pass transistor
Option 2: Demultiplexer based on the transmission gate
Option 3: Demultiplexer based on the static CMOS logic gate
Circuit schematics of a 1 to 4 demultiplexer based on option 1 and 2 are shown in Fig.6.3[1].

The advantage of the pass transistor structure is the smallest number of transistors needed and only NMOS required. The drawback is that if the input and address signals are on the same voltage level for logic "1", there will be a drop of V_{th} on each transistor from input to output. The way to overcome the V_{th} drop is either to increase the voltage

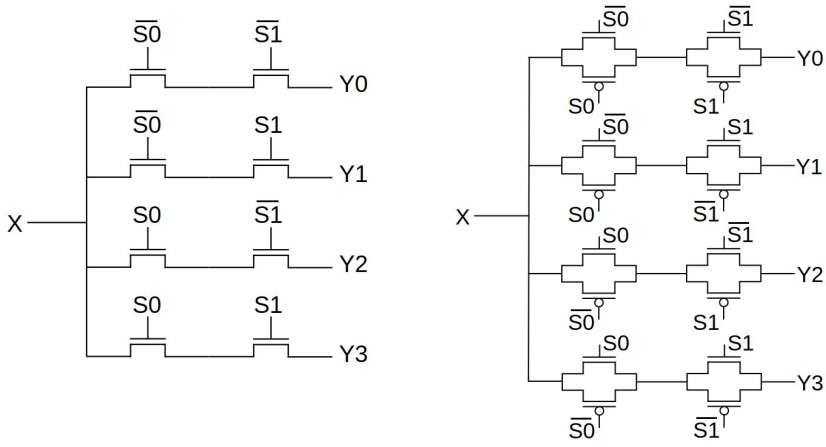

Figure 6.3: Pass transistor structure (left) and transmission gate structure (right) to make a demultiplexer

on the transistor gates (address line) or to use the transmission gate structure shown on the right. However, the transmission gate requires CMOS and integrating PMOS on the same chip with quantum dots would introduce complexities in fabrication and characterization processes. In both cases, inverters are required to generate the opposite logic level of the address signals. An inverter can be constructed using a single NMOS coupled with a resistor, or using an NMOS and a PMOS transistors. The former is easier to fabricate but consumes more power during operation.

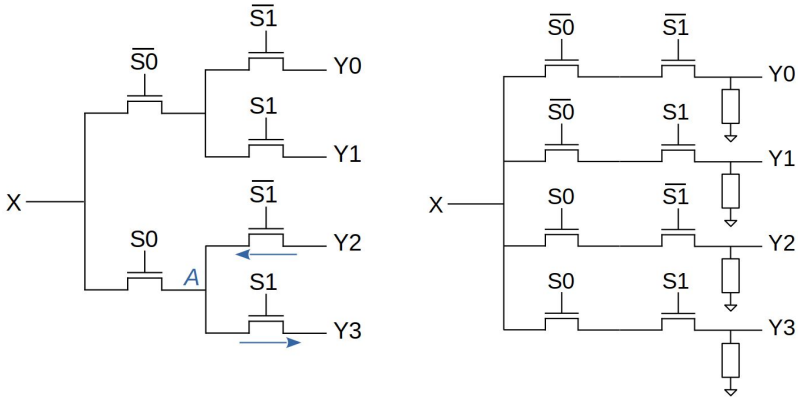

Figure 6.4: Left: a binary tree structure to form a 1 to 4 demultiplxer. The blue arrows indicating the signal paths when S0 is set to logic low and S1 is switched from low to high. Right: pull down resistors required at the outputs to define the inactive state.

Implementing a binary tree structure as shown in the left panel of Fig. 6.4 could reduce the number of transistors in the circuit[2]. (The structure can also be applied based on the transmission gate.) However, it may introduce crosstalk among the outputs. For

instance, when we set S0 to logical low and switch S1 from low to high to pass the input signal to Y1, the signal on Y2 may pass to Y3 in the meantime (as shown by the blue arrows in the figure, the signal on Y2 is first maintained on node *A* when S1 is low, it can then pass to Y3 when S1 is switched to high). Thus, the binary tree structure is feasible in specific applications that the inactive outputs are always on the same voltage level or can be random. Another remark for both option 1 and 2 is that when one path is selected by S0 and S1, the other outputs are open-circuited. Pull-down resistors may be required to set the other outputs to ground as shown in the right panel of Fig.6.4.

A more common demultiplexer design is based on logical gates. As shown in the left panel of Fig. 6.5, a 1 to 4 demultiplexer is constructed by 2 NOT gates and 4 AND gates[3]. The right panel shows a typical design of a single AND gate using complementary MOSFETs. (It is also possible to build an AND gate with NMOS only, but with higher power consumption.) One advantage of this structure is that there is no floating state, all outputs are defined either in logical high or low. However, the input X is not directly passed to the output, it is actually used to define whether the selected output is pulled to Vdd or GND.

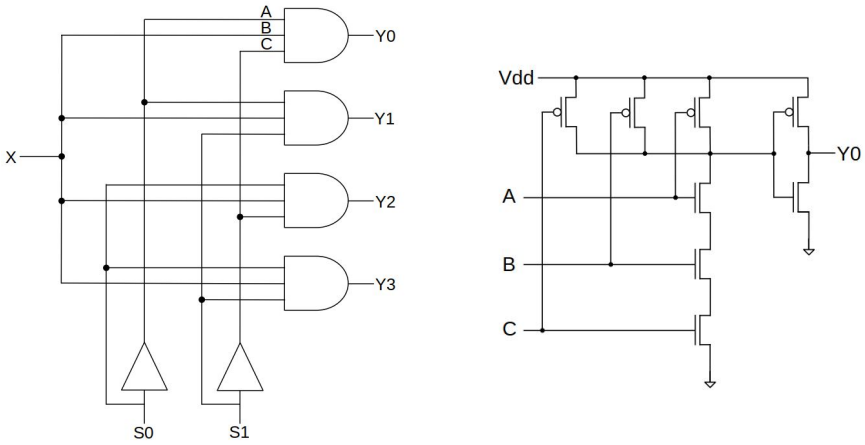

Figure 6.5: Left: 1 to 4 demultiplexer based on logical gates. Right: An AND gate made by MOSFETs

In short, the choice of the demultiplexer depends on the actual conditions. Logical gates based structure is preferable for pure digital operation when reliable on-chip integrated CMOS technology is available. In case the demultiplexer must be implemented with only NMOS, the option with pass transistors is better.

6.2. SPARSE DOT ARRAY

As mentioned by the end of Chapter 5, sizes of the holding capacitors are much larger than those of the quantum dots. To provide space within the qubit plane to integrate the switched-capacitor circuits and demultiplexers, the qubits are proposed to be placed sparsely[4].

6.2.1. ARRAY OPERATION AND LINE SCALING

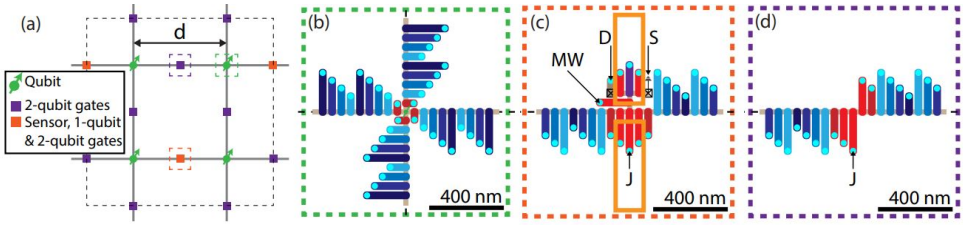

Figure 6.6: (a) Schematic of a unit cell containing four spin qubits (green) and operation regions (purple/orange) (b) Qubit idling region. Four barrier gate electrodes (red) define the confinement potential and allow qubits to shuttle into the channels (blue). (c) Qubit operation region including control gates (red), sensing dot plunger (purple), source (S)/drain (D) ohmic contacts (squares) and micromagnets (orange rectangles). The gate electrodes labelled MW and J are used for single and two-qubit operations, respectively. (d) Two-qubit operation only regions.

The basic idea of the sparse array is presented in Fig. 6.6(a). The qubits are arranged as a 2-dimensional square lattice for the surface code implementation[5]. The main difference here from the other spin-qubit architecture is that the distance between 2 adjacent qubits d is 12 μm. For the single- or two-qubit operation and readout, qubits need to be transferred to the operation regions via shuttling channels.

Gates involved in each functional area are plotted in detail in Fig.6.6(b)-(d). Electrons loaded from reservoirs are shuttled to the qubit idling region, where four barrier gates (dark red in figure 6.6(b)) are used for the electron confinement. The shuttling channel is created by the travelling wave potential. To trap and shuttle an electron, four phase-shifted sinusoidal signals are applied and repeated along the consecutive gates (shades of blue in the figures). Here, the four sinusoidal signal inputs can be shared over the entire quantum plane in case the created travelling wave potential is large enough to overcome the potential inhomogeneities (caused by the substrate or fabrication process).

To perform single-qubit operation via electric dipole spin resonance (EDSR), an electron is shuttled to the operation region and confined under the bottom red gates in figure 6.6(c). A transverse magnetic field is provided by a pair of micro-magnets. A microwave pulse is applied (labelled MW) to drive spin rotations [6]. For the two-qubit gate, two electrons from the vertices adjacent are firstly shuttled to the two-qubit operation region (purple block) or the all-qubit operation region (orange block). Then a pulsed signal is applied on the gate labelled J to activate an exchange interaction between the two electron spins[7].

Qubit readout is performed via spin-to-charge conversion based on Pauli spin blockade. A charge sensing quantum dot connected to source/drain ohmic contacts is placed next to the qubit operation region (figure 6.6(c)). The sensing dot is used to detect a spin-dependent tunnelling event, which can be mapped into a single-spin measurement of the target qubit [8].

We define a block shown in figure 6.6(a) as a unit cell of a quantum plane that contains 4 qubits, 6 two-qubit-operation regions and 2 all-operation regions in equivalent.

Based on the above descriptions, we can calculate the number of signal lines in a unit cell, summarized in Table 6.1.

	Counts per unit cell	Fine (DC, 1 μV)	Coarse (DC, 1 mV)	Pulsed signals (AC)
Qubit idling region	4 ×	-	4	4
All-operation region	2 ×	7	2	6
Two-qubit operation region	6 ×	3	3	5
Shuttling	-	-	-	4
Total per unit cell		32	32	62

Table 6.1: Summary of signal lines per unit cell.

Here two DC bias voltage resolutions ΔV are defined to accommodate different gate functionalities. For gates acting as barriers to shuttling channels (dark red gates in figure(b-d)), only a resolution sufficient to maintain an electron in a quantum dot is required. Therefore we can afford a coarse resolution ΔV = 1 mV. A fine resolution ΔV = 1 μV is required for all other plunger and barrier gates[9]. As shown in the table, there are in total 64 gates requiring DC biasing, with an equal split between gates requiring 1 mV and 1 μV resolution. Next we implement the floating gate scheme to provide these local DC bias voltages.

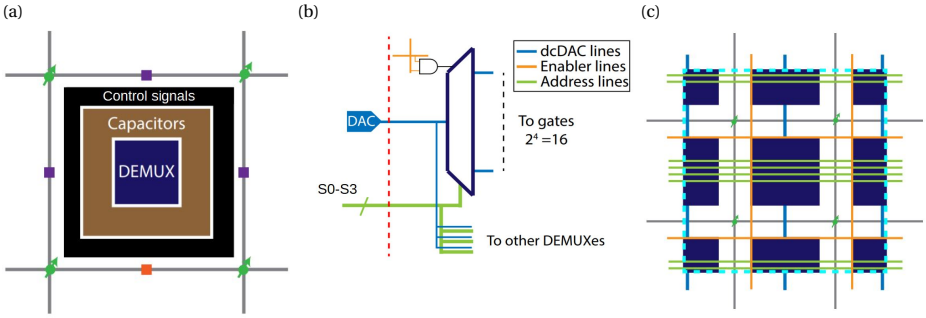

Figure 6.7: (a) Schematic of sparsely placed qubits integrated with electronics on-chip. (b) A 1 to 16 demultiplexer with 4 address lines and 2 enable lines. The input is provided by a DAC module. (c) Schematic of a unit cell (in the dashed light blue square) as part of the sparse array. The signal lines are shared among many demultiplexers.

As shown in Fig.6.7(a), the space between the qubits allows switched-capacitor circuits and demultiplexers to be placed on-chip close to the qubits. Fig.6.7(b) is the schematic of a 1 to 16 demultiplexer with two enable lines (orange), four address lines (green) and one input line (blue). Aligned with the unit cell definition in Fig.6.6(a), there are in equivalent 4 demultiplexers per unit cell as depicted in Fig.6.7(c), which provides 64 outputs with in total 9 signal lines (1 input + 4 enable + 4 address lines). Scaling up to N unit cells, the address lines and the input lines can be shared among many unit cells. Only the enable lines scale with the number of unit cells. Therefore, the number of DC lines

required off-chip becomes around $4\sqrt{N}+5$. The 62 pulsed and microwave control signals (as shown in Table 6.1) can be shared across all unit cells in the array, irrespective of the total number of qubits. [1]
In short, here we show that by demultiplexing DC lines and sharing some of the control signals, the number of interconnects can be scaled more efficiently with the number of qubits. In addition, there are more practical things to consider when assessing the feasibility of such a scheme. In the following subsection, we will focus on one specific element namely heat dissipation.

6.2.2. HEAT DISSIPATION OF A UNIT CELL

It is necessary to ensure that the device heat dissipation meets the requirement set by the cooling power of a dilution fridge. Here we consider two main sources that dissipate heat: on the electronic devices and on the metallic signal lines.

As calculated in Chapter 2, the heat generated during charging and discharging the holding capacitor is negligible compared to the dynamic power consumption of transistor switches. In other words, among the electronic devices integrated on-chip, heat is mainly dissipated in the demultiplexers. It is reported in the literature that a 1 to 8 demultiplexer dissipates around 100 μW power at 400 MHz[10]. In our case, it is estimated at the end of section 5.2 that the refresh frequency for a single switched-capacitor circuit is 10 kHz. For a unit cell that uses 1 DAC line to provide voltages to 64 outputs, the refresh frequency of the demultiplexers needs to be 640 kHz. Since the power consumption is proportional to the operating frequency and the number of outputs, we roughly estimate that four 1 to 16 demultiplexers cycling through 64 gates with 640 kHz refresh rate dissipate 1.28 μW power per unit cell.

Next, we discuss the heat dissipation on the signal lines. It is in principle determined by the parasitic capacitance among the metallic lines and layers. Although software simulations based on a specific design could give more accurate calculation, we currently use a simplified model for estimation. In general, there would be six or more metal layers for interconnection. Here we mainly focus on the first two layers with the densest signal lines. Metal layers higher up would have signal lines separated widely, thus bringing in less parasitic capacitance. Vias that make connections between layers introduce a parasitic capacitance as well, while it would be reduced through proper layout design that avoids placing vias close together.

Assuming the size of a unit cell is 24 μm by 24 μm (since the distance between 2 neighbouring qubits is designed to be 12 μm, the side length of a unit cell is twice the distance according to Fig. 6.6(a)), 150 signal lines in the first and second layers each are placed orthogonally with each other as shown in Fig.6.8. The length L, width W and height H of each line is 24 μm, 80 nm and 50 nm, respectively [2]. Lateral distance d between lines is 80 nm. The dielectric between the layers is assumed to be SiO_2 with the relative permittivity ϵ_{Si} of 3.9 and the thickness t of 500 nm. The capacitance between

[1] J. M. Boter et al, The spider-web array - a sparse spin qubit array, in preparation
[2] The line does not stop after the unit cell, the continuation of the line capacitance is included in the next unit cell.

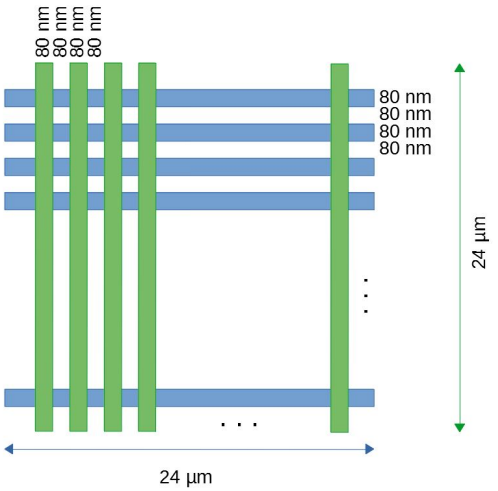

Figure 6.8: Schematic of signal lines in a 24 μm by 24 μm unit cell. Line width and lateral distance in between are both 80 nm. The first layer (blue) and second layer (green) are separated by presumably 500 nm SiO_2 (not shown in this figure of top view).

two parallel signal lines in the same layer is

$$C_1 = \epsilon_0 \epsilon_{Si} \frac{LH}{d} + \frac{\epsilon_0 \epsilon_{Si} L}{377\pi v_0 ln(-\frac{2}{\sqrt{\frac{d}{d+2W}-1}}(\sqrt{\frac{d}{d+2W}}+1)}, \tag{6.1}$$

with ϵ_0 the permittivity of air and v_0 the speed of light in vacuum. The first term in Eq. 6.1 is the parallel-plate capacitance between the side-wall of two lines, and the second term calculates the fringe capacitance from wire-top to wire-top and wire-bottom to wire-bottom[11][3]. Next, the capacitance between the first and second layers is formed by overlapping areas and also fringe effects. We use the formula below to estimate the capacitance of each node of line crossing [12].

$$C_2 = \epsilon_0 \epsilon_{Si} [\frac{3.285 \times W^2}{t} + 2W(4.505 \times \frac{H}{H+0.2\times t} - 4.348 \times (\frac{H}{H+0.2\times t})^2)]. \tag{6.2}$$

Here we add the capacitance of the crossover area, the fringe capacitance from the top of the lower line to the side-wall of the upper line and the fringe capacitance from the bottom of the upper line to the side-wall of the lower line together. The total power dissipation on the signal lines can be calculated as [13]

$$P = (N_{lines} C_1 + N_{nodes} C_2) V_{dd}^2 f, \tag{6.3}$$

where $N_{lines}C_1 + N_{nodes}C_2$ is the total capacitance, with number of signal lines N_{lines} to be 300 and number of overlapping nodes N_{nodes} to be around 22500 on a unit cell.

[3]There is an online calculator: https://www.emisoftware.com/calculator/coplanar-capacitance/

V_{dd} and f are the switching range and frequency of the signal. Assuming a 100 kHz, 3V amplitude signal for each line, P is estimated to be 632 nW. Note that this calculation is based on the worst-case scenario, and its result should not be the main limiting factor for the circuit design. Nevertheless, the power consumed on the signal lines is on a comparable scale with that consumed on the electronic devices.

With these discussions, We discussed a few aspects of a proposed design for a sparse quantum dot array with integrated electronics for distributing signals and locally storing voltages. Additional considerations to assess the feasibility of this design are discussed in [4] and Boter et al, in preparation.

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7

CONCLUSION AND OUTLOOK

7.1. CONCLUSION

This project focuses on making a scalable interface for Si/SiGe based quantum dot arrays. We implement a switched-capacitor circuit for charge-locking and use it to float the gate of quantum dots, combined with demultiplexers to overcome the wiring bottleneck for scaling.

As presented in Chapter 3, we fabricate prototypes of a single quantum dot with the plunger gate connected to a switched-capacitor circuit. All devices are integrated on a Si/SiGe-based substrate to eliminate the need for wire bonding. A general rule during the process development is to incorporate the steps for making electronic circuits without affecting the fabrication flow of quantum dots. For instance, to prevent strain relaxation in the quantum well, we use rapid thermal annealing at 700 °C for 15 s instead of high-temperature (>1000 °C) annealing in conventional processes to activate the implanted phosphorus dopants. Another example is for the dielectric layer, we follow the choice of the quantum dots that use thermal ALD Al_2O_3 as the gate oxide material. For both quantum dots and transistors, Al_2O_3 has a good compromise among leakage, disorder and a reliable process.

The testing results showed in Chapter 4 and 5 imply the success of the fabrication process. Here we first characterize discrete transistors from several batches. Due to the cryogenic working temperature and the larger lattice constant for strained-silicon, we observe a lower subthreshold slop and higher field-effect mobility than those of room temperature MOS devices, which is consistent with the simulation results based on silicon modules. In addition, to avoid the hysteresis issue, the gate-source/drain voltage is limited to be less than 1 V in the following experiments. Single quantum dots without a floating gate show stable Coulomb peaks and Coulomb diamonds at 20 mK. The charging energy and lever arm extracted are comparable to other works.

In Chapter 5 we report measurements of devices combined with a switched-capacitor circuit and a single quantum dot. The results show that the floating gate circuit does not

affect the Coulomb peaks of the quantum dot dramatically. The discharging time constant for an around 1 V bias voltage on the floating node is in the scale of 100 s, which results in a re-charging frequency of approximately 10 kHz if a voltage accuracy of 1 μV is required. Besides, we observe an offset on the sampled voltage, which contains a systematic part and a random part. The systematic part is introduced by channel charge injection and gate-source capacitive coupling, which can be reduced by using a larger holding capacitor and a smaller transistor. For the random part, although thermal noise and electron charge quantization may also be the reasons, the random offsets are dominated by $1/f$ noise in the dot potential in the present measurements. Furthermore, we demonstrate that the electrochemical potential of the quantum dot can follow a 100 Hz pulse signal while the dot is partially floating. Together with the simulation results, we expect that floating a quantum dot gate does not impact the effect of voltage pulses up to 20 GHz applied to another quantum dot gate.

Since the transistor switching signals need to be demultiplexed to finally reduce the number of wires going off-chip, we discuss designs of demultiplexers connected to a quantum dot array in Chapter 6. For demultiplexer structures, transmission gate with on-chip integrated CMOS technology holds the advantage of a larger input voltage range compare to the pass transistor structure with only NMOS, but brings complexities in fabrication. Implementing a binary tree structure can reduce the number of transistors. Furthermore, since the holding capacitor size is much larger than a quantum dot even using the advanced deep-trench technique, the quantum dot arrays are proposed to be placed sparsely to leave more space for the electronic circuits. Here we take a unit cell of 4 qubits in specific, we estimate the heat dissipation on the signal lines to be 632 nW in the worst case. There are many aspects, from the device footprint to qubit control, to be considered in detail when building a physical qubit system, which is out of the scope of this thesis.

There exist alternative approaches for biasing a large number of quantum dot gates. Below we discuss preliminary work we performed using off-chip switched capacitor circuits. We also present design considerations and initial preparations for future experiments aiming to perform a single-shot spin readout of a partly floating quantum dot and the use of a shift register instead of a demultiplexer to update locally stored voltages.

7.2. ON-GOING WORK AND OUTLOOK

7.2.1. OFF-CHIP INTEGRATION

It is widely accepted that an interface circuit needs to work at the same temperature as the quantum dots. However, there is no conclusion on whether on-chip or off-chip integration is the best approach. The latter allows optimization of each individual part. Meanwhile, additional engineering is required to bond chips together.

We carried out the following experiment to show that the floating gate strategy is also applicable in terms of off-chip integration[1]. As shown in the left panel of Fig. 7.1, a square chip is placed in the carrier holder, which includes a switched-capacitor circuit fabricated on a crystalline silicon substrate. The transistor channel size is 1μm by 1μm and the MOS capacitor is 50 pF. A Si/SiGe based chip with a single quantum dot is firstly

[1] Presented by M. Trifunovic at FTQC werkbespreking, 2017.

glued on top [2]. Then, the devices are wire-bonded according to the circuit shown in the right panel of Fig. 7.1.

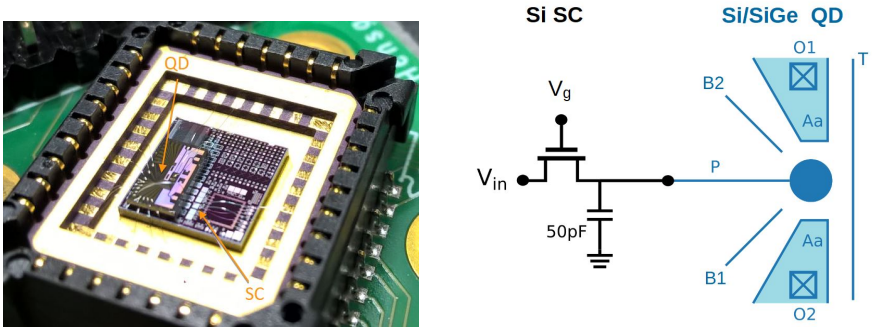

Figure 7.1: Left: the quantum dots and switched-capacitor circuits are fabricated on the Si/SiGe heterostructure and crystalline silicon substrates, respectively. They are wire-bonded and placed in a chip carrier on the PCB board for the cryogenic tests. Right: device schematic showing that the SC circuit is used to float the plunger gate of a single quantum dot.

The sample is cooled down to 10 mK in the dilution refrigerator. We test the device in the static and floating mode in the same way as described in Chapter 5. The results are shown in Fig. 7.2. The device is first biased without the gate floating and a few Coulomb blockade peaks are observed (the inserted figure of the left panel). Then we switch the transistor to float the plunger gate of the quantum dot and measure the current flowing through the dot. We see coulomb peaks reappearing in the next 2 hours due to a slow discharge of the capacitor. The discharging time constant extracted from this experiment is around 2800 s (using the method described in section 5.2). The pulsed mode test result is given in the right panel, the Coulomb blockade peaks obtained in the pulsed mode follow the same trend as the static reference but shift in V_{in}. The approximately 12 mV systematic shift can also be explained by the channel charge injection and gate voltage coupling. Furthermore, the random voltage variation is around 0.18 mV on average (extracted from the probability density function, the method is described in section 5.1.3).

Compared with on-chip integrated samples, the discharge performance for the off-chip integrated device is better since each individual component can be optimized. For example, the dielectric layer for the quantum dot is Al_2O_3 prepared using ALD, while for the transistor and capacitor, the dielectric later is made of SiO_2 grown at temperatures higher than 1000 °C, which results in fewer defects and lower leakage current. The systematic shift and noise level of the current device can be further engineered since the channel size is still large and the switching voltage is relatively high (over 5V for the on-state). Nevertheless, making dense and high-quality interconnections is always a challenge to apply off-chip integration to a large number of qubits. Below we explore some considerations for the interconnections.

First of all, to avoid the complexity in routing all the I/O ports to chip edges for wire

[2]The chip with a SC circuit is prepared by M. Trifunovic in EKL, the quantum dot chip is prepared by N. Samkharadze in VLL.

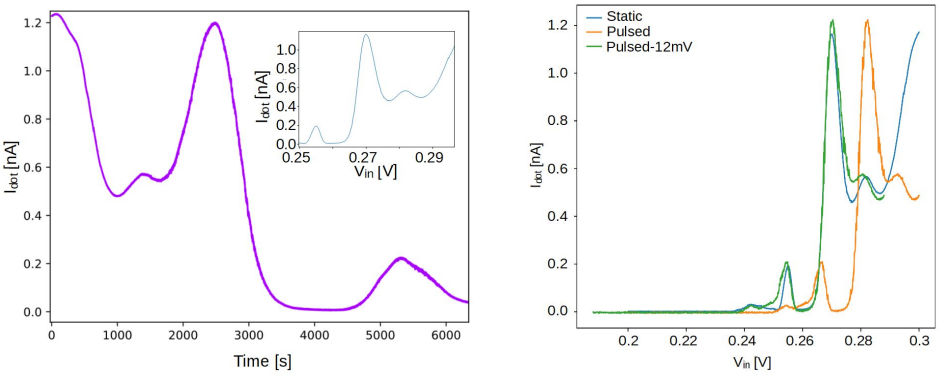

Figure 7.2: Experiment results of the off-chip integrated device. Left: current flowing through the quantum dot as a function of time after switching off the transistor. The static mode Coulomb peak pattern (insert) reappearing. Right: Coulomb blockade peaks obtained in the static (blue line) and pulsed (orange line) mode follow the same trend, with V_{in} shifts. The green line is the result of a negative shift of the orange line by 12 mV, which overlapped well with the blue line.

bonding, signal from electronic circuits could approach the quantum dot plane through the third dimension. Existing techniques for the 3D integrated circuit include making through-silicon vias (with the top chip facing up) and flip-chip bonding with ball grid arrays (BGA)[1]. Either way, joints are critical at the interface to connect two chips. The connection should be mechanically stable and have low resistance at cryogenic temperature to avoid local heating. Researchers have shown a superconducting connection between two planar chips with aluminium signal lines using indium bumps [2]. Indium is selected here as an adhesive layer because of its relatively high critical temperature of 3.4K. Besides, indium bump bonding also exists for the industrial CMOS process at room temperature[3]. The softness of indium is also an advantage of making good connections. However, it may have potential issue on the alignment accuracy, especially for applications with small pitches. An optional method is direct-bonding with the assistance of additional heating and force. NbN is used here because it is also superconducting at temperatures below 4K and has a relatively simple composition. High-quality NbN films need to be fabricated and the bonding parameters need to be optimized before making high-density NbN-NbN joints [3].

7.2.2. SINGLE-SHOT READOUT OF A PARTIALLY FLOATING QUBIT

Turning back to the on-chip integration approach, the devices we fabricated so far are all based on a single quantum dot and we mainly focus on their function of electron confinement. As a next step, we want to explore the feasibility of making qubit experiments with floating gates. So we propose to fabricate a prototype to execute single-shot spin readout with a partially floating quantum dot. We therefore need a smaller quantum dot, which can be depleted until only one electron is left on the dot. A sensing dot close to the qubit dot is used to detect the spin state of the electron on the qubit dot using

[3] Y. Li, et al, Wafer-level direct bonding of optimized superconducting NbN for 3D chip integration, Physica C: Superconductivity and its Applications, 582 (2021)

Elzerman readout[4] [4].

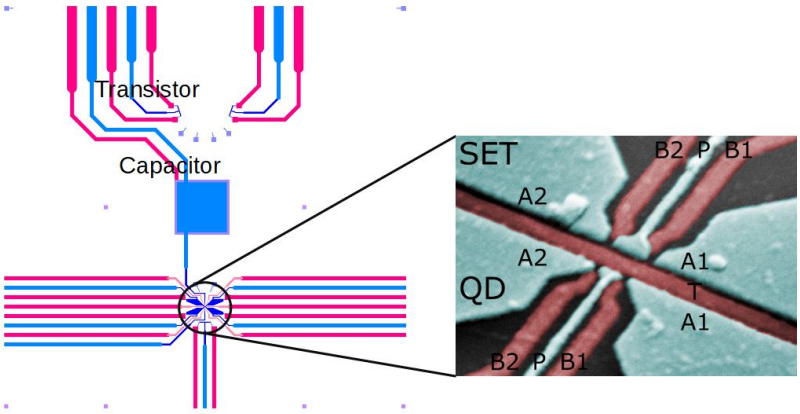

Figure 7.3: Left: device design that integrate the transistor, capacitor, qubit and sensing dot on the same substrate. The pink and blue color represent two metal layers. Right: SEM image of the quantum dots part. The area defined for qubit is smaller than that defined for the sensing dot in opposite.

We make a start to design and prepare the device. The left panel of Fig. 7.3 presents the design that integrates the transistor, capacitor and quantum dots (for the qubit and sensing) on a Si/SiGe based substrate. It is not yet a mature design with two remarks here. Firstly, instead of a single-metal-layer process described in Chapter 3, this device has two metal layers. Therefore, both electrodes of the capacitor are made from metal rather than using the implantation area to define one electrode as in the earlier design. This gives some flexibility to alter the capacitor size and the dielectric thickness. Secondly, the design doesn't contain mesas, so there is a potential issue of leakage from the drain of the transistor to the plunger gate of the quantum dot. A quick solution is wire-bonding the switched-capacitor circuit to the quantum dot. It is still under discussion whether mesa is necessary for the long term. The right panel of Fig. 7.3 shows the SEM image of the quantum dot part. The small plunger gate is around 80 nm by 40 nm that define the qubit area, the dielectric below is 7 nm Al_2O_3 produced by thermal ALD. The larger quantum dot placed opposite the qubit dot will be operated as a single-electron transistor (SET). To use the SET as a charge sensor, the SET needs to operate on the flank of a coulomb peak, where it is extremely sensitive to fluctuations in the electrostatic environment.
Elzerman readout uses the difference in energy between the spin states for spin-to-charge conversion, the principle is illustrated in Section 2.1.3. Since it relies on the precise positioning of the spin levels with respect to the reservoirs, variations of the electrochemical potential on the quantum dot are required to be smaller than the energy splitting of the spin states, which is typically around 100 μeV. Taking the lever arm of 0.1 for example, the voltage variation on the floating gate needs to be less than 1 mV when attempting to perform this read-out scheme.

[4] See master thesis from Florian Unseld for more information.

7.2.3. A FULLY FLOATING SINGLE QUANTUM DOT WITH GATE ADDRESSING

A single floating gate cannot solve the wiring bottleneck in scaling up the number of qubits. We could make prototypes with many floating gates, combined with an addressing circuit, to experimentally demonstrate that the scheme is able to reduce the number of wires connected to higher temperature stages. The device schematic is presented in Fig.7.4 [5].

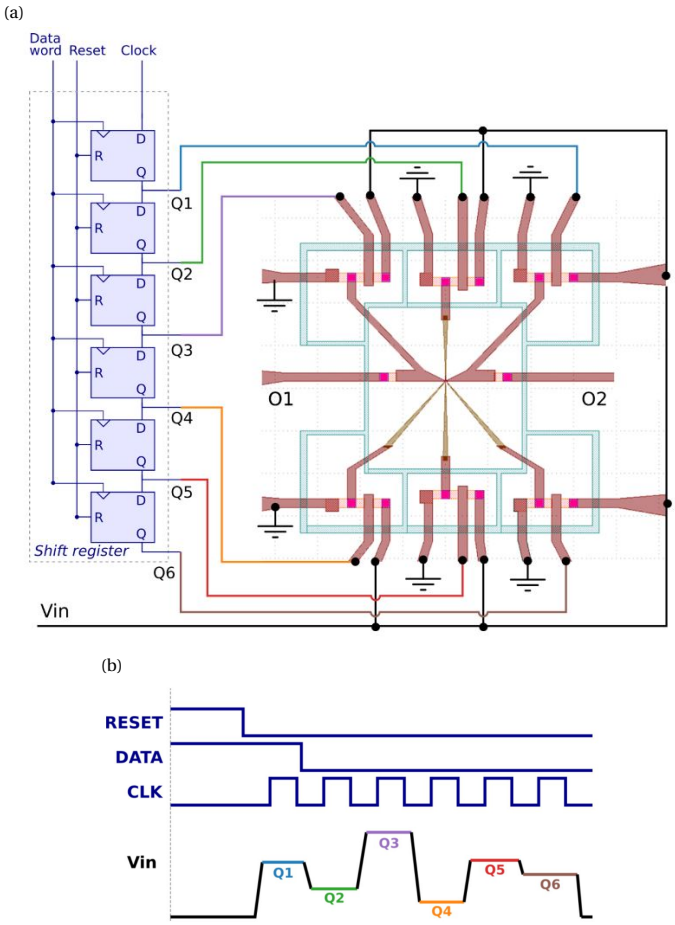

Figure 7.4: (a) Layout of a single quantum dot with all gates floating. The switched-capacitor circuits connected to two accumulation, two barrier, one plunger and one T gates of a quantum dot are separated by trenches (colored in sky-blue). The floating gates are addressed by a shift register made of D-type flip-flops presented on the left. The output (Q) from each flip-Flop is connected to the input (D) of the next flip-flop. (b) Working sequence of the fully floating quantum dot addressed by a shift register, details described in the text.

As shown in Fig. 7.4(a), six switched-capacitor circuits are applied to float the plunger, barrier and accumulation gates of a single quantum dot. Each transistor gate is con-

[5] Presented at 13th Workshop on Low Temperature Electronics (WOLTE-13) by Andrea Corna, 2018.

nected to an output of a shift register (Q1 to Q6). The working sequence of the system is presented in Fig. 7.4(b). After enabling the shift register (RESET from logical high to low), a logical high signal is provided on the DATA line to set the output Q1 high. Thus, the transistor of the first switched-capacitor circuit is switched on, and the voltage required for the corresponding quantum dot gate is provided through V_{in}. In the next clock cycle, the logical high signal is shifted to the output of Q2 and the voltage at V_{in} is set to update the second quantum dot gate. In this case, four signal lines are required to provide voltages to six gates of the quantum dot. Adding one floating gate with a switched-capacitor circuit would reduce the updating frequency, but does not increase the number of signal lines needed from higher-temperature stages[6]. We use a shift register here for addressing instead of de-multiplexers we discussed in Chapter 6. It is applicable when there is no need for random access, and a sequential updating is sufficient.

7.2.4. SUMMARY

In conclusion, the proposals mentioned in this chapter indicate on-going work that allow to take step forward in the future. In the long term, it is important to show that the interface electronics structure can be integrated with a large number of quantum dots. In addition, an experimental demonstration that universal qubit control initialization and measurement are compatible with the use of floating gates is essential. Together, these two advances can help overcome the wiring bottleneck which is currently one of the biggest practical obstacles to large-scale quantum computers based on electron spin quantum dots.

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[6] The PCB board introduced in section Fig. 3.9b is designed for this experiment.

ACKNOWLEDGEMENTS

I would like to thank prof. Lieven Vandersypen for receiving me and giving me a warm welcome to join your group. Thank you for arranging people and resources to support this project. Thank you for maintaining an excellent group so I can always reach people for help, from understanding physics to device measurement details. Thanks a lot for the many valuable instructions and suggestions you provide on this project and for editing my paper and thesis sentence by sentence. Thank you for tolerating my delay in writing the thesis. Thank you for letting me join the trip to Iceland. It was also fun to have fencing with you on the strategy day.

I would like to thank dr. Ryoichi Ishihara for giving me the opportunity of being a PhD candidate. Thank you for the initial ideas for this project. Thank you for giving me the opportunity as an exhibitor in the delft technique event and teaching assistant for your courses. Thank you for many useful discussions and suggestions on the project. Thank you for the encouragement and understanding along the way. I also enjoyed time for the sushi dinners and summer bbq with the group.

I would like to thank prof. Lina Sarro for being my promoter for the first two years of my PhD life. Thank you for giving positive feedback on my interview for the PhD vacancy, and also positive feedback on my go/no go meeting.

I would like to acknowledge financial support from Intel Corporation. I would like to thank dr. Jim Clarke and his colleagues for coming to Qutech and listening to our report on the project progressing. Thank you Jim for always showing interests in this project and sharing the industrial capacitor characterization scheme with me. Thank you Jeanette for providing SiGe substrates for us. Thank you Kanwal for making the dielectric layer of the samples.

I would like to thank prof. Edoardo Charbon, dr. Fabio Sebastiano and the Quantum integrated circuits group for useful discussions on the electronic specifications for supporting qubits. Thank you for sharing experiences of measuring cryo-CMOS.

I would like to thank prof. Koen Bertels for maintaining good cooperation between the QC&E department and the physics department. Thank you for encouraging Ryoichi's group when we were facing difficulties. I would like to thank prof. Said Hamdioui for organizing and letting me join the summer school in Beijing.

Next, I would like to thank Andrea for joining this project. Thank you for developing and naming Big-woop and Julia, and writing the script for the measurement. Thank you for making the device testing plan, which became the basis of our paper. Thank you for the knowledge sharing on quantum physics, analogue electronics, mechanics for the dilution fridge and the common sense of being a physics student. Thank you also for sharing the feeling about life and family with me.

I would like to thank Anne-Marije for supporting me with the device measurement. Thank you for explaining many technical details to me with your nice drawings. Besides, I appreciate your concern for me very much and I was always inspired by your vitality.

I would like to thank Gautham and Florian for choosing this topic for your master theses, and Shuting for the undergraduate internship. Gautham, thank you for taking over the fabrication work when I got pregnant. Thanks for your nice work on the Raman test and dielectric characterizations. Florian, thank you for the data processing and for making nice pictures for our paper. Thank you for being brave to select the difficult topic of single-shot readout with floating gate to work on.

Next, I would like to thank people who trained and supported me in the fabrication processes. Thank you Silvana for being my mentor in the Else Kooi Laboratory (EKL). I would also like to thank members of the facility team and the engineering team of EKL: Johannes, Henk, Gregory, Koos, Mario, Tom, Wim, Alex, Johan, Hugo and Cassan. Thank you all for your hard work to keep the cleanroom up and running. Thank you Nodar and Nima for sharing the quantum dots recipe and fabrication experience with me. Thank you Nodar for being my mentor in the Van Leeuwenhoek Laboratory (VLL). Thank you for guiding me in every detail of the fabrication process. I would like to thank Delphine for arranging people for my module training. Thank Jelmer and Gabriel for training me on the ebeam-lithography. Thank Elfi for training me on the wet-bench and evaporator. Thank Diego for training me on ALD. Thank JP for training me on the AJA evaporator. Thank Nima for training me on RTP and thank Delphine for training me on the dry etcher, sputter machine and SEM. I would like to thank technicians from VLL for your kind support and maintenance: Anja, Arnold, Charles, Eugene, Ewan, Hozanna, Marco and Marc.

I would furthermore thank Amir and Delphine for developing pre-feb processes and delivering samples with improved uniformity. Thank you Amir for making excellent SiGe substrate for us, thank you for checking my flowcharts step by step carefully. Thank you Francisco for your assistance with the sample fabrication. I would like to thank all of you in the weekly fabrication meeting for exchanging the latest results and having many useful discussions: Sergey, Patrick, Will, Stephan, Nodar, Anne-Marije, Florian, Lucas, Brian, Zhongyi, Marcel, Mario, Menno and Giordano.

I would like to thank Stephan and Anne-Marije for the design of PCBs onto which the samples were mounted. Thank Kees and Hans from DEMO for the PCB assembling. Thank you Miki and Guoji for refurbishing the Julia dipstick. Thank you Andrea for designing the cold finger of the dilution fridge. Thank you Olaf for maintaining the cryostats and thank you Remond for maintaining the electronics.

Thank you all from Lieven's group for always being so kind to me and helped me a lot: Erika, Pasquale, Christian, Udit, Xiao, Floor, Guoji, Jelmer, JP, Oriol, Jurgen, Sjaak, Pablo, Max, Mateusz, Tobias, Tzu-Kan, Patrick, Sergey, Sander and Pieter.

I would like to thank all members of Ryoichi's group: Miki, Pengfei, Paolo, Oscar, Gautham, Juan, Aniello and Ramin. I felt so cheerful to work together with you.

Almost to the end, I would like to thank Joyce, Lindwina and Laura for letting me join the ladies activities in QC&E department. It was very relaxing to have lunch or make jewellery with you. Thank Marian from ECTM, Marja and Chantal from Qutech for your daily support and the arrangement of many great activities. Thank teachers from the graduate school that providing many attractive PhD courses. Thank secretaries from the international office for arranging visa and certificates for us.

Finally, I would like to thank my parents and grandparents for always supporting me

unconditionally. Thank my parents, mother in law and aunt Li for flying all the way from China to the Netherlands to look after my son. Thank my husband who is facing all the challenges in life together with me and thank the little one who open a new window for me to view the world.

A

FLOWCHART OF QUANTUM DOTS WITH FLOATING GATES, PROCESSED IN VLL

Substrate material: crystalline Si with <100> crystal orientation/ 500 nm $SiGe_x$ buffer/ 10 nm Strained-Si/ 30 nm $Si_{0.7}Ge_{0.3}$/ 1 nm Si/SiO_2 cap, provided by Intel. More information on the database[1], run number SQ17-68.

1. **Surface treatment**
   - Cleave a 3 cm by 3 cm Si/SiGe chip
   - Rinse in acetone for 1 min
   - Rinse in isopropanol (IPA) for 1 min, dry with N_2 gun
2. **Alignment Markers**

   Lithography:
   - Prebake on hot plate at 175 °C for 1 min
   - Spin coat MMA/MAA 17.5 EL11, spinning speed: 2500 rpm
   - Bake on hot plate at 175 °C for 10 min
   - Spin coat PMMA 950 A4, spinning speed: 4000 rpm
   - Bake on hot plate at 175 °C for 10 min
   - E-beam exposure, dose: 1150 $\mu C/cm^2$, beam step size: 40 nm
   - Develop, MIBK:IPA 1:3 for 1 min
   - Rinse in IPA, dry with N_2 gun

[1] https://qtechserv2.tnw.tudelft.nl/

Tungsten deposition [2] and lift-off:

- Sputter ~100 nm Tungsten (W) on Alliance sputter
- Rinse in acetone for 1 hour with ultrasound, chip placed vertical in a holder, spray with acetone when take out
- Rinse in IPA, dry with N_2 gun

3. **Ion implantation**

Lithography:

- Prebake on hot plate at 175 °C for 1 min
- Spin coat MMA/MAA 17.5 EL11, spinning speed: 2500 rpm
- Bake on hot plate at 175 °C for 10 min
- Spin coat PMMA 950 A4, spinning speed: 4000 rpm
- Bake on hot plate at 175 °C for 10 min
- E-beam exposure, Dose: 1150 μC/cm^2, beam step size: 80 nm
- Develop in MIBK:IPA 1:3 for 1 min
- Rinse in IPA, dry with N_2 gun
- O_2 plasma descum in Tepla etcher, chip placed in a Faraday cage, oxygen flow: 200 ml/min, plasma energy: 600 W, etching time: 1 min

Implantation:

- Glue to a 4-inch carrier wafer with a drop of PMMA A2, leave overnight in a vacuum desiccator
- Transfer to EKL[3]
- Implant 31P+ (phosphorous) at 20 keV, 5×10^{15} ions/cm^2, chip tilt: 7°

Resist removal:

- Transfer to VLL
- Cover the sample with AZ9260 (photoresist)
- Bake on hot plate at 90 °C for 10 min
- Remove the sample from carrier wafer with acetone
- Without drying put the sample in a holder in acetone and sonicate full power for 1 hour
- Repeat sonication a few times over the next 2-3 days (sample stays in acetone this whole time)
- Rinse in IPA, dry with N_2 gun

[2] Sputtered tungsten is not an optimal material for the markers in ebeam-lithography, but is one of the few material options allowed in the implanter.

[3] When transferring between VLL and EKL, the chip /wafer box is sealed in an ESD shielding bag.

4. **Dicing**

   - Spin coat S1813 (photoresist), spinning speed: 2000 rpm
   - Bake on hot plate at 100 °C for 1min
   - Dice into 9 chips of 1 cm × 1 cm, tape thickness: 140 µm (ESD compliant), NBC blade
   - Remove S1813 by acetone, rinse in IPA, dry with N_2 gun

5. **Annealing**

   - Rapid thermal annealing in forming gas at 700 °C for 15 sec

6. **Trench etching**

   Lithography:

   - Prebake on hot plate at 150 °C for 1 min
   - Spin coat CSAR62 09, spinning speed: 4000 rpm (target resist thickness: 200 nm)
   - Bake on hot plate at 150 °C for 3 min
   - E-beam exposure, dose: 300 µC/cm^2, beam step size: 50 nm
   - Develop, Pentylacetate 1 min, MIBK:IPA 1:1 1 min
   - Rinse in IPA, dry with N_2 gun

   Etching:

   - Etch in Feybold F1 etcher, SF6 flow: 12.5 sccm, He flow: 10 sccm, pressure: 10 µbar, forward power: 25 W, etching time: 45 sec
     (target trench depth: 100 nm)

   Resist removal :

   - NMP (N-Methyl-2-Pyrrolidone) at 80 °C for 1 hour
   - Rinse in IPA, dry with N_2 gun

7. **Ohmic contacts**

   Lithography :

   - Prebake on hot plate at 175 °C for 1 min
   - Spin coat MMA/MAA 17.5 EL11, spinning speed: 2500 rpm
   - Bake on hot plate at 175 °C for 10 min
   - Spin coat PMMA 950 A4, spinning speed: 4000 rpm
   - Bake on hot plate at 175 °C for 10 min
   - E-beam exposure, dose: 1150 µC/cm^2, beam step size: 80nm

- Develop, MIBK:IPA 1:3 for 1 min
- Rinse in IPA, dry with N_2 gun

Surface treatment (native oxide removal) :

- Bake on hot plate at 120 °C for 10 min
- Dip in BHF 1:7 for 30 sec, rinse in deionized (DI) water and dry with N_2 gun, load in the evaporator quickly

Metalization and lift-off :

- Evaporate 5 nm Cr, rate 0.5 Å/s
- Evaporate 45 nm Au, rate 1 Å/s
- Lift-off in 50 °C acetone for 1 hour
- Spray with syringe in acetone a few times, rinse in IPA, dry with N_2 gun

8. **Al_2O_3 deposition**

   - Dip in BHF 1:7 for 30 sec, rinse in DI water and dry with N_2 gun, load in the ALD quickly
   - Thermal ALD of Al_2O_3 in Oxford Flexal ALD system, process temperature: 300 °C, number of cycles: 150 (target thickness: 15 nm)
   - OR: transfer the device to Imec, thermal ALD Al_2O_3 at 300 °C, number of cycles: 70 (target thickness: 7 nm)

9. **Fine gates**

   Lithography :

   - Prebake on hot plate at 150 °C for 1 min, take off and wait for ~20 sec
   - Spin coat CSAR62 04, spinning speed: 4000 rpm
   - Bake on hot plate at 150°C for 3 min
   - E-beam exposure, dose: 420 $\mu C/cm^2$, beam step size: 4 nm
   - Develop, Pentylacetate 1 min, MIBK:IPA 1:1 1 min
   - Rinse in IPA, dry with N_2 gun

   Metallization and lift-off :

   - Evaporate 5 nm Cr, rate 0.5 Å/s
   - Evaporate 15 nm Au, rate 1 Å/s
   - Lift-off in 80°C NMP for 1 hour
   - Spray with syringe in NMP a few times, rinse in IPA for ~5 min, dry with N_2 gun

10. **Contact openings**

Lithography :

- Prebake on hot plate at 150 °C for 1 min
- Spin coat CSAR62 09, spinning speed: 2500 rpm
- Bake on hot plate at 150 °C for 3 min
- E-beam exposure, dose: 300 μC/cm^2, beam step size: 20 nm
- Develop, Pentylacetate 1 min, MIBK:IPA 1:3 1 min
- Rinse in IPA, dry with N_2 gun

Al_2O_3 etching:

- Etch in Oxford ICP etcher, BCl_3 flow: 20 sccm, forward power: 1250 W, etching time: 15 sec

Resist removal :

- Lift-off in 80 °C NMP for 1 hour
- Rinse in IPA for ~5 min, dry with N_2 gun

11. **Large gates and bonding pads**

Lithography :

- Prebake on hot plate at 175 °C for 1 min
- Spin coat MMA/MAA 17.5 EL11, spinning speed: 2500 rpm
- Bake on hot plate at 175 °C for 10 min
- Spin coat PMMA 950 A4, spinning speed: 4000 rpm
- Bake on hot plate at 175 °C for 10 min
- E-beam exposure of coarse pattern, dose: 1150 μC/cm^2, beam step size: 80 nm
- E-beam exposure of fine pattern,dose: 1400 μC/cm^2, beam step size: 20 nm [4]
- Develop, MIBK:IPA 1:3 1 min
- Rinse in IPA, dry with N_2 gun

Metallization and lift-off :

- Evaporate 5 nm Cr, rate 0.5 Å/s
- Evaporate 245 nm Au, rate 2 Å/s
- Lift-off in acetone sonicate full power for 1 hour
- Rinse in IPA, dry with N_2 gun

[4] We expose two ebeam-images in this step, the coarse pattern mainly contains large bonding pads, the fine pattern mainly contains transistor gates and capacitor plates.

B

FLOWCHART OF QUANTUM DOTS WITH FLOATING GATES, PROCESSED IN EKL AND VLL

Substrate material: 4-inch diameter, crystalline Si <100> wafer/ 1 μm grading SiGe (0-30%) + 300 nm $Si_{0.7}Ge_{0.3}$/ 10 nm Strained-Si/ 30 nm $Si_{0.7}Ge_{0.3}$/ 1 nm Si/SiO_2 cap, produced in EKL. More information on the database[1], run number SQ18-175, optical mask set: Qutech-prefab DC floating gates-reticle1-v1-3.

1. **Optical markers and trench etching**

   Photo lithography:

   - Spin coat photoresist in EVG120, recipe: 1-CO-3012-1.4 µm
   - Lithography energy density: 150 mJ/cm^2, mask: COMURK
   - Lithography energy density: 140 mJ/cm^2 mask: Image 1
   - Develop in EVG120, recipe: 1-Dev-sp

   Dry etching:

   - Pre-conditioning (run the same recipe with standard Si wafers, etching time set to 2 min)
   - Dry etching (with only process wafers, see table 3.1 in main text for detailed gas flow and etching time)
   - Resist removal with O_2 plasma in Tepla, power: 1000 W, O_2 flow: 400 ml/min, etching time: end point detected

[1] https://qtechserv2.tnw.tudelft.nl/

- Trench depth check with Profilometry

2. **Ion implantation**

   Cleaning:

   - 10 minutes in 99% HNO_3 at room temperature
   - 5 minutes rinsing in DI water
   - 10 minutes in 69.5% HNO_3 at 110 °C
   - 5 minutes rinsing in DI water
   - Spin dry under N_2 treatment

   Photo lithography:

   - Spin coat photoresist in EVG120, recipe: 1-CO-3012-1.4 µm
   - Lithography energy density: 150 mJ/cm^2 mask: Image 2
   - Develop in EVG120, recipe: 1-Dev-sp

   Ion implantation:

   - Dopant: Phosphorus; acceleration voltage: 20keV, dose: 5×15 ions/cm^2, wafer tilt: 7 °

   Resist removal:

   - Resist removal with O_2 plasma in Tepla, power: 1000 W, O_2 flow: 400 ml/min, etching time: end point detected

3. **Annealing**

   - Transfer to VLL
   - Rapid thermal annealing in forming gas, 700 °C for 15 s
   - Transfer to EKL

4. **Al_2O_3 deposition**

   Cleaning:

   - 10 minutes in 99% HNO_3 at room temperature
   - 5 minutes rinsing in DI water
   - 10 minutes in 69.5% HNO_3 at 110 °C
   - 5 minutes rinsing in DI water
   - Marangoni dry (dip in 0.55% HF for 4 min, rinse in DI water and dry with N_2)
   - Transfer to VLL

   Al_2O_3 deposition:

- Thermal ALD of Al_2O_3 in Picosun R-200 system, process temperature: 300 °C, number of cycles: 200 (target thickness: 20 nm)

Post-annealing:

- 450 °C in forming gas for 20 minutes
- Transfer to EKL

5. **Ohmic contacts and EBPG markers**

Cleaning [2]:

- 10 minutes in 99% HNO_3 at room temperature
- 5 minutes rinsing in DI water
- Spin and dry under N_2 treatment

Lithography:

- Spin coat photoresist in EVG120, recipe: 1-CO-Nlof-1.5 µm
- Lithography energy density: 40 mJ/cm^2, mask: Image 4
- Lithography in contact aligner EVG420, lamp intensity: 15 mWatt/cm^2; exposure time 6.3 s, mask: PF-H-CONTACT-ALIGNER-MASK-V2-3
- Develop in EVG120, recipe: Only-X-link bake
- Develop in EVG120, recipe: xDelphine-Dev-lift-off
- Post bake in Fusion DUV, recipe: lift-off
- Resist discuum in Tepla, O_2 flow: 250 ml/min, power: 600 W, time: 1 min

Metallization and lift-off:

- Dip in BHF 1:7 for 40 sec, rinse in DI water and dry with N_2
- Evaporate 5 nm Ti, rate 0.5 Å/s
- Evaporate 55 nm Pt, rate 2 Å/s
- Lift-off in 70°C NMP for 40 min
- Rinse in IPA for 5 min, dry with N_2 gun
- Inspection under optical microscope

6. **Dicing**

- Transfer to VLL
- Spin coat S1813 at 2000 rpm, target thickness: 2μm
- Baking on a hot plate at 100 °C for 1 min
- Dicing into 1cm × 1cm dyes on Disco dicer, use the blade for silicon (NBC blade)

[2] 69.5% HNO_3 at 110 °C dissolve Al_2O_3, should be skipped

- Remove S1813 by acetone, rinse in IPA, dry with N_2 gun

7. **Fine gates**

   Lithography :

   - Prebake on hot plate at 150 °C for 1 min, take off and wait for ~20 sec
   - Spin coat CSAR62 04, spinning speed: 4000 rpm
   - Bake on hot plate at 150°C for 3 min
   - E-beam exposure, dose: 450 $\mu C/cm^2$, beam step size: 4 nm
   - Develop, Pentylacetate 1 min, MIBK:IPA 1:1 1 min
   - Rinse in IPA, dry with N_2 gun

   Metallization and lift-off :

   - Evaporate 5 nm Ti, rate 0.5 Å/s
   - Evaporate 15 nm Pd, rate 1 Å/s
   - Lift-off in 80°C NMP for 1 hour
   - Spray with syringe in NMP a few times, rinse in IPA for ~5 min, dry with N_2 gun

8. **Large gates and bonding pads**

   Lithography :

   - Prebake on hot plate at 175 °C for 1 min
   - Spin coat MMA/MAA 17.5 EL11, spinning speed: 2500 rpm
   - Bake on hot plate at 175 °C for 10 min
   - Spin coat PMMA 950 A4, spinning speed: 4000 rpm
   - Bake on hot plate at 175 °C for 10 min
   - E-beam exposure of coarse pattern, dose: 1150 $\mu C/cm^2$, beam step size: 80 nm
   - E-beam exposure of fine pattern,dose: 1400 $\mu C/cm^2$, beam step size: 20 nm [3]
   - Develop, MIBK:IPA 1:3 1 min
   - Rinse in IPA, dry with N_2 gun

   Metallization and lift-off :

   - Evaporate 5 nm Ti, rate 0.5 Å/s
   - Evaporate 195 nm Pd, rate 2 Å/s
   - Lift-off in acetone sonicate full power for 1 hour
   - Rinse in IPA, dry with N_2 gun

[3] We expose two ebeam-images in this step, the coarse pattern mainly contains large bonding pads, the fine pattern mainly contains transistor gates and capacitor plates.

CURRICULUM VITÆ

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LIST OF PUBLICATIONS

3. J. M. Boter, J. P. Dehollain, J. P. G. van Dijk, **Y. Xu**, T. Hensgens, R. Versluis,H. W. L. Naus, J. S. Clarke, M. Veldhorst, F. Sebastiano and L. M. K. Vandersypen , *The spider-web array - a sparse spin qubit array*, in print, arXiv: 2110.00189

2. Y. Li, A. M. Gheytaghi, M. Trifunovic, **Y. Xu**, G. Q. Zhang and R. Ishihara, *Wafer-level direct bonding of optimized superconducting NbN for 3D chip integration,*, Physica C: Superconductivity and its Applications, **582**, 1353823 (2021).

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