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# Superconducting Funnelled Through-Silicon Vias for Quantum Applications

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# Superconducting Funnelled Through-Silicon Vias

For quantum applications

# SUPERCONDUCTING FUNNELLED THROUGH-SILICON VIAS

FOR QUANTUM APPLICATIONS

## Proefschrift

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus Prof.dr.ir. T.H.J.J. van der Hagen,
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op
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door

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Dit proefschrift is goedgekeurd door de promotoren

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*To God and my family.*
*The words printed here are concepts. You must go through the experiences.*

Saint Augustine

# CONTENTS

**Summary** ix

**Samenvatting** xi

**1 Introduction** 1
- 1.1 Quantum Technologies . . . 2
- 1.2 Interconnects for Quantum Computer . . . 3
  - 1.2.1 Superconductivity . . . 4
  - 1.2.2 Requirements for superconducting TSVs interconnects . . . 4
  - 1.2.3 Requirements for Superconductive Materials . . . 5
  - 1.2.4 State of the art of superconducting vias . . . 6
- 1.3 Research question . . . 7
- 1.4 Thesis Outline . . . 7

References . . . 7

**2 HAR TSVs development: layout** 11
- 2.1 Introduction . . . 12
- 2.2 Through-Silicon Vias . . . 12
- 2.3 Masks design . . . 15
  - 2.3.1 DRIE test structures . . . 16
  - 2.3.2 Test structures for electrical characterization . . . 19
- 2.4 Summary . . . 20

References . . . 21

**3 HAR TSVs development: etching** 23
- 3.1 Introduction . . . 24
- 3.2 TSVs etching by DRIE . . . 24
- 3.3 Bosch Process . . . 24
  - 3.3.1 Shortcomings of Bosch DRIE . . . 26
- 3.4 Etching of Straight Vias . . . 27
- 3.5 Wineglass Vias . . . 29
- 3.6 Hourglass Vias . . . 31
- 3.7 Surface smoothening . . . 33
- 3.8 Insulation layers . . . 35
- 3.9 Conclusion . . . 36

References . . . 36

**4 HAR TSVs development: metallization** **39**
4.1 Introduction . . . 40
4.2 TSVs filled by VALM method . . . 40
4.2.1 Why Indium? . . . 40
4.2.2 VALM tool . . . 41
4.2.3 Doctor Blade coating technique . . . 41
4.2.4 VALM procedure . . . 41
4.2.5 Results . . . 42
4.3 TSVs coated by Physical Vapor Deposition . . . 44
4.3.1 Aluminum Metallization . . . 45
4.3.2 Sputtering of Niobium . . . 47
4.4 Discussion . . . 49
4.5 Conclusion . . . 52
References . . . 52

**5 HAR TSVs development: Electrical characterization** **55**
5.1 Introduction . . . 56
5.2 Measurement set-ups . . . 56
5.2.1 two-point probe resistivity measurement . . . 56
5.2.2 Four-point probe resistivity measurement . . . 56
5.2.3 Cryogenic measurement setup . . . 58
5.3 Measurements at room temperature . . . 58
5.3.1 Indium TSVs . . . 58
5.3.2 Niobium and Niobium Titanium TSVs . . . 60
5.3.3 Aluminium TSVs . . . 61
5.4 Measurement at cryogenic temperature . . . 61
5.4.1 Niobium TSVs . . . 62
5.4.2 Aluminum TSVs . . . 62
5.5 Discussion . . . 65
5.6 Conclusion . . . 66
References . . . 67

**6 Conclusions and Recommendations** **69**
6.1 Conclusions . . . 69
6.2 recommendations . . . 70

**Acknowledgements** **73**

**Curriculum Vitæ** **75**

**List of Publications** **77**

# SUMMARY

System downscaling, 3D integration, and increasing functionalities are the main challenges that integrated circuits and MEMS technology have dealt with in the past decade. Advanced packaging schemes and interconnect technologies are some of the successful approaches to tackle the challenges. These issues also extend to modern designs such as terahertz applications and quantum technologies, particularly the solid-state quantum computer.

In-demand instances of the latter are *e.g.* high-density quantum computing systems, where the layer implementing quantum bits (qubits) needs to be bridged to the microelectronic control layer. The latter typically requires CMOS-based circuitry compatible with cryogenic temperatures (*i.e.*, cryo-CMOS) for the control and readout of the many physical qubits needed to implement error-tolerant logical qubits. In order to scale the number of qubits, a more efficient way for the interconnection of the qubits is necessary. In line with such a three-dimensional (3D) integration approach, an interposed layer featuring superconducting vertical interconnections such as through-silicon vias (TSVs) represents a crucial element in the fabrication and assembly of large, scalable, and densely integrated superconducting systems.

This thesis aims to design, fabricate and characterize TSVs filled or coated with superconductive material to integrate multiple quantum devices. First, it is necessary to establish the quantity, dimension placement and characteristics of the interconnects and the required microtechnologies for its fabrication. Therefore the process starts by defining the layout, mask design of the test structures used during the etching, and for the electrical characterization of the TSVs. This is described in Chapter 2.

Extensive investigation and testing of TVS etching is then described in Chapter 3. Initially, traditional straight TSVs with a 50 $\mu$m diameter were fabricated on 300 $\mu$m and 500 $\mu$m thick silicon substrates. The most straightforward scheme chosen was traditional straight sidewall TSVs and the manual deposition of Indium as superconductive material. Indium melts at 156 C, which allows the filling of the TSVs by a developed method called VALM (Vacuum Assisted Liquified Metal). However, it is shown that this method had reproducibility, etching, and patterning problems due to the manual metal spreading. Therefore, it was decided to try an already known but unsuccessful method of filling high-aspect ratio (HAR) TSVs known as metal sputtering. For this, aluminium and niobium were used as superconductive materials. Partially successful results were obtained with straight vias, but the deposited layer had a thickness in the order of tens of nanometers leading to undesired high electric resistivity.

The found solution was the redesign of TSVs to increase the thickness of the superconductive material deposited on the sidewall of the TSVs. Two technologies were consequently developed, the latter improving on the former. First,cavities in the shape of funnels were added on top and bottom of the straight vias, wineglass TSVs to enable efficient coating of the sidewalls of the TSVs with thicker and thus obtaining continuous

metal layers. The final TSV design presented in this thesis is a modification of the wine-glass design, where the top and bottom cavities are broader and a smaller diameter in the center, in the shape of an hourglass. In Chapter 4 are explained the metallization methods, including the Vacuum Assisted Liquified Metal (VALM) together with blade coating, and metallic sputtering for straight and funneled TSVs. Metallic layers as thick as 430 nm in the center of the TSVs were obtained in funneled TSVs.

In Chapter 5 reports the electrical characterization at room temperature and at cryogenic temperature of the TSVs. The measurement setup and the results obtained are presented. A sharp superconducting transition at 1.27 K was obtained for hourglass TSVs coated with aluminum. Conclusions and recommendations are discussed in Chapter 6.

# SAMENVATTING

Systeem verkleining, 3D integratie, en meer functionaliteiten zijn de voornaamste uitdagingen in geïntegreerde schakelingen en MEMS technologie van het afgelopen decennium. Geavanceerde verpakkingsontwerpen en interconnectie technologie zijn een paar van de succesvolle benaderingen om deze uitdagingen te overkomen. Deze problemen reiken ook tot moderne ontwerpen zoals terahertz toepassingen en quantum technologie, in het bijzonder de vaste-staat quantum computer.

Gewilde gevallen van dit laatstgenoemde zijn *d.w.z.* hoge-dichtheid quantum computer systemen, waar de laag die de quantum bits (qubits) implementeerd wordt verbonden met de microelectronica bestuur laag. Dat laatste vereist doorgaans op CMOS gebaseerde schakelingen die compatibel zijn met cryogene temperaturen (*d.w.z.* cryo-CMOS) voor de besturing en uitlezing van de vele fysieke qubits die nodig zijn om error-tolerante logica qubits te implementeren. Om het aantal qubits te verhogen is het noodzakelijk om een efficiëntere manier te vinden om ze te verbinden. In lijn met een dergelijke driedimensionale (3D) integratie aanpak, een tussenlaag met supergeleidende verticale verbindingen zoals door-silicium-vias (TSVs) vertegenwoordigt een cruciaal element in de fabricage en assemblage van grote, schaalbare, en dicht geïntegreerde supergeleidende systemen.

Dit proefschrift heeft als doel om TSVs gevuld of bedekt met een supergeleidende materiaal te ontwerpen, fabriceren en te karakteriseren voor de integratie van meerdere quantum apparaten. Ten eerste is het noodzakelijk om vast te stellen wat de hoeveelheid, dimensie plaatsing en karakteristieken van de verbindingen en de vereiste microtechnologieën zijn voor de fabricage. Het proces start daarom met het definiëren van het ontwerp, het masker ontwerp van de test structuren voor het etsen, en de elektrische karakterisatie van de TSVs. Dit is beschreven in hoofdstuk 2.

Uitgebreid onderzoek en testen van het TSV etsen is daarna beschreven in hoofdstuk 3. Aanvankelijk werden traditionele rechte TSVs met een 50 $\mu$m diameter gefabriceerd op 300 $\mu$m en 500 $\mu$m dikke silicium substraten. Het gekozen meest eenvoudige ontwerp was de traditionele rechte zijmuur TSVs en de handmatige depositie van indium als supergeleidend materiaal. Indium smelt bij 156 C, wat het vullen van de TSVs toelaat met een ontwikkelde methode genaamd VALM (vacuum geassisteerd vloeibaar metaal). Het is echter aangetoond dat deze methode reproduceerbaarheid-, ets-, en patroonvormingsproblemen heeft door de handmatige metaal spreiding. Het was daarom besloten om een bekende, doch onsuccesvolle, methode te gebruiken voor het vullen van hoge aspect-ratio (HAR) TSVs genaamd sputteren. Hiervoor werden aluminium en niobium gebruikt als supergeleidend materialen. Gedeeltelijk succesvolle resultaten zijn behaald met rechte vias, maar de gedeponeerde laag had een dikte in de ordegrootte van tientallen nanometers, wat leidde tot ongewenste hoge elektrische weerstand.

De gevonden oplossing was het herontwerpen van de TSVs om de supergeleidende laag te verdikken op de zijdes van de TSVs. Twee technologieën werden daarop on-

twikkeld, de laatste als verbetering op de eerste. Eerst werden trechtervormige uitsparingen aan de boven- en onderkant van de rechte vias toegevoegd: wijnglas TSVs om een dikkere laag beter op de zijkanten van de TSVs aan te brengen en zo een continue metaal laag te krijgen. Het laatst gepresenteerde TSV ontwerp in dit proefschrift is een modificatie van dit wijnglas ontwerp waar de bovenste en onderste uitsparingen breder zijn en smaller in het midden, als een zandloper. In hoofdstuk 4 worden de metallisatie methoden uitgelegd, zoals vacuüm geassisteerde vloeibaar metaal (VALM) met blad coating, en metaal sputteren voor rechte en trechtervormige TSVs. Metallische lagen tot 430 nm in het midden van de TSVs zijn behaald in de trechtervormige TSVs.

In hoofdstuk 5 wordt gerapporteerd over de elektrische eigenschappen van de TSVs bij kamer temperatuur en op cryogene temperatuur. De meetopstelling en de behaalde resultaten worden gepresenteerd. Een scherpe overgang tot supergeleiding bij 1.27 K was behaald voor de zandloper TSVs gecoat met aluminium. Conclusies en aanbevelingen worden besproken in hoofdstuk 6.

# 1

# INTRODUCTION

1

## 1.1. QUANTUM TECHNOLOGIES

In the last two decades, research on quantum technologies has caught the interest of the scientific community, particularly after the great contribution of scientists that received a Nobel Price in this emerging field. In 1997, Steven Chu, Claude Cohen-Tannoudji, and William D. Phillips were awarded for the development of methods to cool and trap atoms with laser light. In 2001, Eric A. Cornell, Wolfgang Ketterle, and Carl E. Wieman were awarded the Nobel Price for achieving Bose-Einstein condensation in dilute gases of alkali atoms and for early fundamental studies of the properties of the condensates. The most recent one was in 2012, awarded to Serge Haroche and David J. Wineland who have independently invented and developed methods for measuring and manipulating individual particles while preserving their quantum-mechanical nature in ways previously thought unattainable. [1]. These and related achievements have encouraged the expansion of the quantum technology field into several application areas: quantum communication, focused on network security and cryptography; quantum computing, promising unprecedented processing capacity by making use of qubits as elemental unit, those can be represented by trapped ions, superconducting circuits, electronic semiconductor qubits, impurity spins and linear optics; quantum simulation of quantum systems that are practically impossible using classical computers and algorithms due to exponential slow down of computation speed with system size, like quantum Monte Carlo sampling for computing of ground state properties in certain situations and quantum metrology, wide range of precise sensing, that goes from the sub-nano scale to the galactic scale [2].

However, the technology available in the last years was not advanced enough to pursue the envisioned applications. The technology required for the perfect control and manipulation of quantum states demanded the use of new materials, new fabrication methods, and new systems that were not available back then. According to Acín *et al* [2], there are newly developed technologies that can explicitly address individual quantum states and use quantum properties such as superposition and entanglement. Among the leading quantum technologies currently under investigation, communication, simulation, sensing and metrology, quantum computation is gaining particular relevance.

Quantum computing's fundamental logic element is the quantum mechanical bit, i.e. the qubit. Qubits are microwave resonant structures that store and manipulate quantum information, they are represented by the Bloch sphere. In the sphere the qubits are represented by a oriented unit vectors and denoted using Dirac's quantum mechanical notation or "bra-ket". The figure Fig. 1.1, shows the states of a qubit on the Bloch sphere [3].

Qubits can present interference, which is related to the superposition of their wave functions. This means that qubits can drive transitions between the quantum states, the quantum equivalent of bit-flip operations. The quantum bits can also be entangled, which means that the quantum states of two or more qubits are related, keeping the system reference (information) even if the objects are physically separated [4]. This is what makes quantum computers so powerful. Unfortunately, the smallest interference from the outside world can break the entanglement (decoherence), making this also the weak point of quantum technologies. During the computation, qubits can assume any value on the Bloch sphere [4]; traditional computation is instead only based on 0 or 1. This means that classical computers can calculate with binary digits, one at a time, while

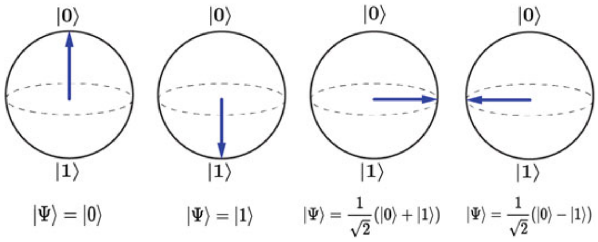



Figure 1.1: Representation of the qubit states in the Bloch sphere[3]

quantum computers can perform two calculations at once, for a two-level system. In theory, n-level systems are possible in quantum computation. Physically, qubits can be realized by any two-level quantum system, such as excited states of an atom, nuclear and electron spins, positions of a crystalline defect, states of a quantum dot, or energy levels of a superconducting circuit.

To take full advantage of quantum computing in desktop-size devices, at least $10^4$ physical qubits have to be integrated and interconnected (necessary for the error correction) on the same mm-sized platform [5]. For example, one single transmon qubit (a superconducting charge qubit) requires an approximate area of 100 $\mu$m by 100 $\mu$m, while one traditional transistor has an approximate size of 90 nm by 90 nm. The technological gap between both technologies is considerable in terms of micro-fabrication. Consequently, it is necessary to explore intermediary technologies that combine the required number of physical qubits and the qubits readout in the same platform. A possible approach is to remove the wires used for the connections between the qubits and use this space to place more qubits. In this context, we propose to connect the qubits and the driving and readout circuitry through 3D interconnection schemes.

## 1.2. INTERCONNECTS FOR QUANTUM COMPUTER

Silicon-based quantum computers currently operate at temperatures lower than 1K [5]. CMOS circuitry, generally working between room temperature and 150°C, is required for the control and readout of the many qubits[6]. Therefore, a scheme for interconnects among qubits and between qubits and cryo-CMOS circuitry is essential (Fig.1.2), hence the need for superconducting interconnects.

Through-Silicon Vias (TSVs) are vertical conductive structures used to connect integrated circuits (ICs) or microelectromechanical devices (MEMS) on the top surface of a silicon wafer with others at the bottom of the same wafer or to use the wafer as an interposer layer between two separate substrates. TSVs increase functional density and device performance while reducing interconnection-related parasitic effects [7–11].

Copper, doped polysilicon, and tungsten are the most used materials for interconnections and filled vias in the semiconductor industry, thanks to their excellent electrical conductivity or thermal stability [12]. However, none of these materials is superconductive. Moreover, prior works on superconducting interconnections (i.e., indium bumps and TSVs with polymer-filled metallic liner [13, 14] rely on materials or fabrica-

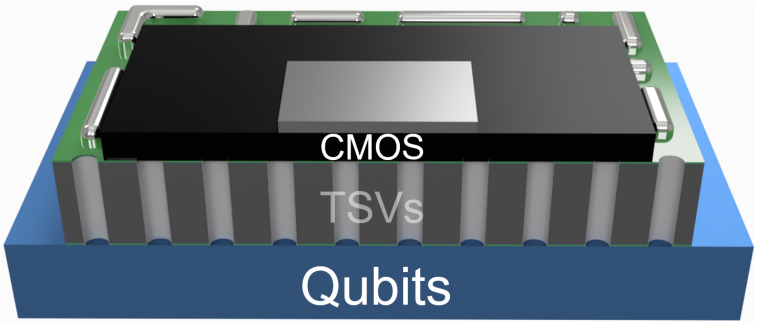



Figure 1.2: Sketch of the three TSV designs.

tion methods that are not CMOS compatible or not easily scalable [15]). Thus, several requirements for material and configuration choice need to be addressed to provide 3D interconnects operating at cryogenic temperatures.

### 1.2.1. SUPERCONDUCTIVITY

In 1911 H. Kamerlingh Onnes discovered superconductivity, in Leiden(The Netherlands). He made experiments with mercury in liquefying helium, and noticed the "vanishing" of the electrical resistivity when merecury reached the 4.2 Kelvin. Since then, there is ever growing search for materials that have superconducting properties and the exploration of their use in diverse applications. The superconductivity in materials was explained in 1957 by a theory developed by John Bardeen, Leon Cooper and John R. Schrieffer. They found that the electrons form pairs (Cooper pairs) in superconducting materials, when they are exposed to temperatures close to 0 Kelvin. The electrons were able to move through the crystal lattice without any obstruction to the flow (resistance), when a electric potential difference is applied. In this state electrons keep moving even when the voltage is removed, the current continues to flow indefinitely. The resistance increases when the temperature is raised. This is because the lattice of atoms starts vibrating again [16]. In superconductors, the drop of the electrical resistance to zero ohm varies per material. The temperature at which the sharp transition occurs is the critical temperature (Tc). The critical temperature is determined by many factors, such as the crystal structure, bond lengths, the electron-phonon coupling among others. [17] [3].

### 1.2.2. REQUIREMENTS FOR SUPERCONDUCTING TSVS INTERCONNECTS

Moore's law underlines the field of integrated circuits. This empirical law states that the number of transistors on IC doubles approximately every two years. This model has ruled for the last five decades, but the cost and development time associated with following this path are becoming unsustainable. The microelectronics industry is therefore looking for alternatives. According to Burkett *et al* [18], heterogeneous integration and advanced packaging approaches, such as three-dimensional (3D) integration, have been identified as paths for continuing the push for increased bandwidth and functionalityof electronic systems while decreasing the cost per system volume. The heterogeneous in-

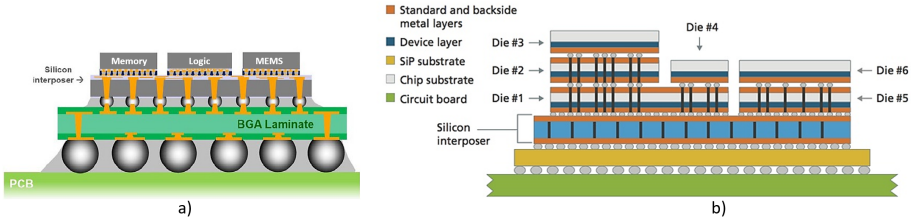



Figure 1.3: Sketches illustrating the heterogeneous integration concept including ICs and MEMS [20] (a) and TSVs integration (b) [21].

tegration relies on the use of TSVs as enabling technology for 3D stacking to connect device layers from the front to the backside of the wafer, Fig. 1.3a) or to create interposer chips to be placed between separate chips Fig. 1.3b).

TSVs also contribute to improving the general performance by reducing the delay in long wiring. This is an essential factor to consider for the scalability of chips or microsystems. However, TSV technology is still at an early stage of development. Lietaer *et al.* [19] mentioned some of the possible challenges for the integration of TSVs with MEMS: 1) TSVs needs to be realized in a 300 $\mu$m or more substrate thickness; 2) TSVs fabrication should be compatible with silicon-on-insulator (SOI) substrate; 3) Wet processing steps are problematic due to the presence of inlets or released structures in MEMS; 4) TSVs with very fine pitch are required for the interconnection of multiple devices. Additionally, they need to result in homogeneous, highly reproducible, and conformal metallic coatings. It is also imperative that the compatibility of the fabrication processes with conventional CMOS technology is preserved. For superconducting vias, as indicated by Foxen *et al.* [14], it is also important to maintain compatibility with the qubit architecture and to satisfy some additional requirements: 1) the fabrication yield must be high, particularly for routing control signa; 2) the interconnects must continue to perform electrically and mechanically after cooling from 300 K to 10 mK; 3)interconnects must be superconductive to provide a no loss connection between chips and avoid local heating and 4) The critical current (current when superconductivity is achieved) must exceed 5mA to keep the stability and precision of the qubit.

### 1.2.3. REQUIREMENTS FOR SUPERCONDUCTIVE MATERIALS

Among the various strategies, superconducting qubits are the most promising for the realization of a quantum computer [22]. Superconducting qubits are fabricated with materials that exhibit different electrical behavior at cryogenic temperatures. As mentioned, the critical temperature $T_c$ is the temperature at which the electrical resistivity of a metal drops to zero. The transition is sudden and sharp as it is a transition to a different phase of matter. There are several materials with different $T_c$ values. There are 27 superconducting pure materials. However, only a few have interesting properties for quantum; for example, high $T_c$ (above 1 K), or have already been implemented in IC fabrication, such as Indium, Aluminum, and Niobium.

Indium can reach superconductivity at 3.4 K, and it is mechanically stable at cryogenic temperatures (not brittle), has low electrical loss at microwave frequencies, it is

compatible with standard lithographic techniques (though not compatible with CMOS standards), and has good bonding capabilities [23]. Additionally, indium has a melting temperature of approximately 156°C.

Aluminum is a well-known material in IC and MEMS. It has a superconducting transition at 1,2 K. It is compatible with CMOS fabrication and can be deposited using well-established physical vapor deposition methods, such as sputtering and evaporation. Josephson junctions, which are the base of qubits and Rapid Single Flux Quantum (RFSQ), are fabricated with Aluminum and Niobium (Nb) [24]. This is convenient because it simplifies the fabrication process in the case that the TSVs are required.

Niobium and Niobium alloys such as Niobium Titanium Nitride(NbTiN) can achieve superconducting transitions at 9 K (Nb) and 16 K (NbTiN). They have little microwave phase noise and microwave loss, desirable properties for photodetectors, and circuit quantum electrodynamic experiments [25]. It is compatible with CMOS fabrication and with sputtering and Atomic Layer Deposition (ALD)techniques.

### 1.2.4. STATE OF THE ART OF SUPERCONDUCTING VIAS

Several works in literature have reported a variety of approaches to deploying superconducting interposers [13–15, 22, 26–32]. To mention some, Foxen *et al* [14] used indium bumps as electrical interconnects between two planar devices with aluminum wiring. They could get a superconducting transition at 1.1 K. Since Indium is classified as contaminating metal in conventional CMOS technology, the proposed process limits the possibility of integration with qubits.

Vahidpour *et al* [13] worked on the fabrication of 250 $\mu$m deep Al TSVs. The vias were etched on the backside by inductively coupled plasma and isotropic etching, obtaining a sloped wall via geometry. The hole is about 200 $\mu$m diameter and shrinks to 50 $\mu$m in the top part of the wafer. Al was evaporated from the backside to take advantage of the sloped profile, and Parylene C sputtered as via fill. Then the oxide (landing layer) was removed from the top side, and the metallization step was repeated. The size of the openings and the proposed complex process limit the integration of many devices per wafer. However, the opened profile facilitates the Al electron-beam evaporation and Parylene-C sputtering. Unfortunately, Parylene-C processing is not compatible with conventional CMOS technology. They achieved a superconducting transition below 1.2 K.

Grigoras *et al* [30] fabricated arrays of 60 $\mu$m diameter TSVs, coated by ALD TiN, in 495 $\mu$m thick silicon wafers. They achieved superconducting transition at around 1.6 K. To achieve superconducting vias, a layer thicker than 50 nm, according to the London penetration depth to effectively shield radiation [31], is required. ALD deposition is a prolonged process and consequently less preferable when thicker layers are needed. Rosenberg *et al* [22] developed blind vias, in a 725 $\mu$m thick silicon wafer. The vias were lined with TiN using chemical vapor deposition, and the wafers thinned down to 200 $\mu$m. They achieved superconducting transition around 2.5-3 K without a clear and sharp transition. Although these approaches result in fully coated and functional TSVs, they often require fabrication methods that are not compatible with conventional CMOS micro-fabrication, and more importantly, they all lack a sharp superconducting transition.

## 1.3. RESEARCH QUESTION

In this thesis, the possibility to fabricate high aspect-ratio superconducting through-silicon vias is investigated. The fabrication process should be CMOS compatible, provide high TSVs density, and allow wafer-scale manufacturing with high yield and low cost. Moreover, the superconducting vias should present a sharp transition at the critical temperature and without hysteresis.

## 1.4. THESIS OUTLINE

The thesis is organized as follows:

Chapter 2 describes the TSVs design and the mask layout used for the test structures to monitor the fabrication process and perform electrical characterization.

Chapter 3 presents the TSV microfabrication, the tools required, the shortcomings observed, and the solutions to overcome them towards an optimization of the process.

Chapter 4 describes the TSVs metallization using Indium, Aluminium, Niobium, and Niobium alloys. It also includes the use of straight TSVs filled with Indium as superconductive material, the development of the filling tool VALM, and recipes developed for sputtering.

Chapter 5 reports the electrical characterization of the TSVs, the measurement setup, the measurements at room temperature of In, Nb, and Al TSVs, and the measurements at cryogenic temperatures of Al TSVs.

Chapter 6 summarizes the main findings and gives suggestions for future work.

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# 2

# HAR TSVs DEVELOPMENT: LAYOUT

## 2.1. INTRODUCTION

IC planar connections are based on 2D wiring. Conventional 2D interconnects are characterized by long wire connections that need to be accommodated in a limited chip area. With the increase in device density and diverse functionalities integrated in a chip that needs to be interconnected and addressed, conventional 2D interconnect schemes have reached their limit [1]. System-on-Chip (SOC) technologies offer the option to integrate different systems or functionalities in the same chip, decreasing the wire length used for the interconnections. However, integrating such diverse technologies on a single chip increases the chip area, the materials required, and the complexity of the fabrication process. Furthermore, there is a growing interest in the integration of several non-electric functionalities, *i.e.* MEMS, which require different 'wiring' schemes [2]. Electronic devices such as smartphones, wearables, or sensor systems demand an increase of heterogeneous functions to be performed simultaneously, and they should fit in smaller areas.

The technologies used at the system-level and device-level are System-in-Package (SiP), 2.5D integration, and 3D integration [3]. SiP is a low-cost integration solution containing more than one active electronic component and optionally passive devices, MEMS components, or optical devices encapsulated together in a single standard package. It offers a small form factor and reduces time-to-market development, and it is easy to redesign [4]. Figure 2.1 illustrates the cross-section of a gas sensor system implemented under the SiP scheme.

The 2.5D integration uses silicon interposer and micro-bumps. Silicon interposer is an electrically conductive structure that allows electrical signals to pass through. Micro-bumps are micro metallic spheres, usually made of indium, attached to the interposer to connect two chips. Together they are a strong candidate to deliver low power/high-performance connections and high chip densities [5]. A successful example of the implementation of this technology is the Xilinx 2.5D based through silicon via and interposer (Virtex-7HTFPGA) (Fig. 2.2). However, the 2.5D approach presents technical challenges related to the difficulties in the fabrication, design, and heat dissipation, among others.

Finally, 3D integration requires TSVs (usually HAR TSVs). The two distinct configurations implemented are 3D integrated circuits (3D-IC) with a sophisticated architecture including different transistor layers and 3D system-on-chip (3D-SOC) with a less complex design [6]. The use of 3D stacking may seem like a good solution; however, it must guarantee a highly conductive connection between the different levels and sub-levels of the system. Specific technologies required to implement 3D integration are TSVs, wafer thinning, and wafer/chip bonding [7]. TSVs are considered the heart of 3D integration technologies as they offer the possibility of shortening interconnection paths. It can be implemented at wafer-level (Fig. 2.3a) or as 3D stacking of multiple devices (Fig.2.3b).

## 2.2. THROUGH-SILICON VIAS

TSVs are formed by a combination of drilling and filling techniques. High aspect ratio openings are etched in a substrate, then coated by a liner (which has insulating or adhesion enhancement purpose), and finally metalized to electrically interconnect the top and bottom of the substrate. There are several methods for the TSVs formation: Plasma etching, laser drilling, electrochemical etching, and sandblasting [10]. The most attrac-

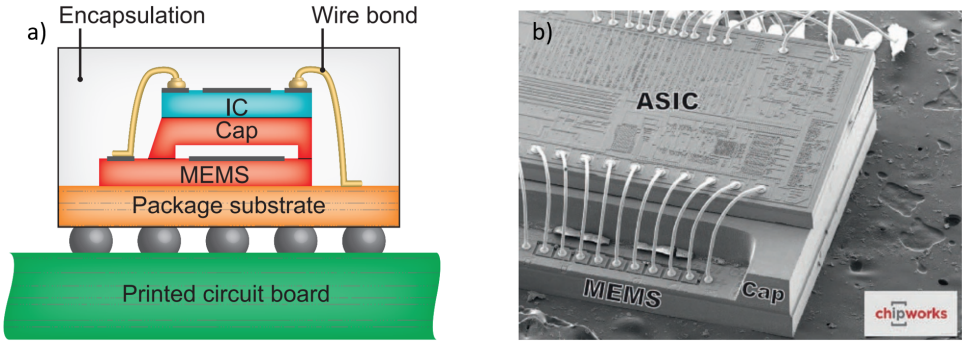



Figure 2.1: Cross-section of a SiP solution a) and SEM image of a SiP 3-axis accelerometer [2].

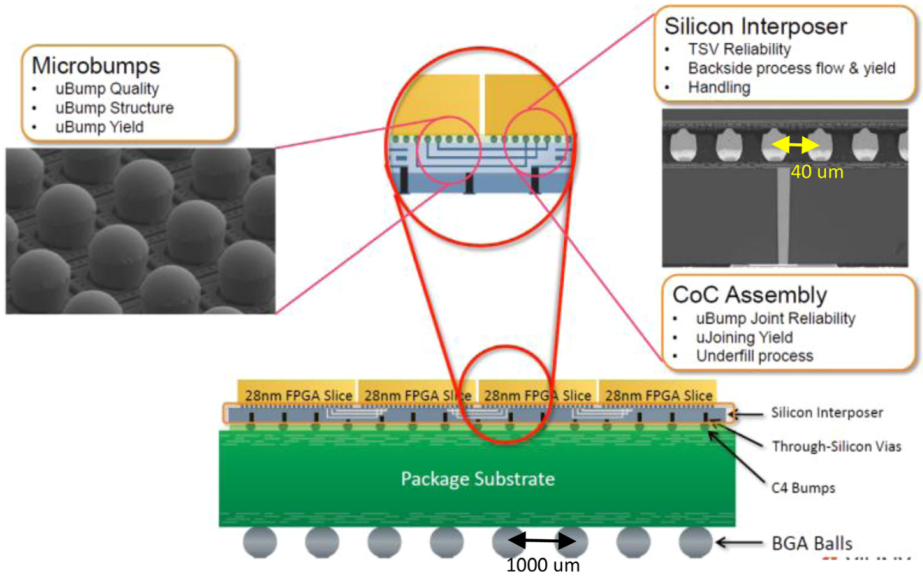



Figure 2.2: Cross-section of the Xilinx 2.5D TSI based Virtex-7HT FPGA [8].

tive in terms of achievable high aspect ratio and smooth sidewalls is plasma etching. This etching method is going to be described and discussed in Chapter 3. Laser drilling is a technology that etches the material through vaporization or sublimation [7]. It is an attractive option for the fabrication of HAR TSVs on glass substrates. It can reach via aspect ratios as high as 70 [11] without the need of a masking layer. However, there are still issues related to the remaining bulges around the holes [12]. Electrochemical etching is based on wet chemistry, using an electrolyte solution, an anode, a cathode, and a source of direct electric current. The technology promises aspect ratios around 35 with small diameter through-holes (few micrometers) [13]. Unfortunately, mechanical grinding and

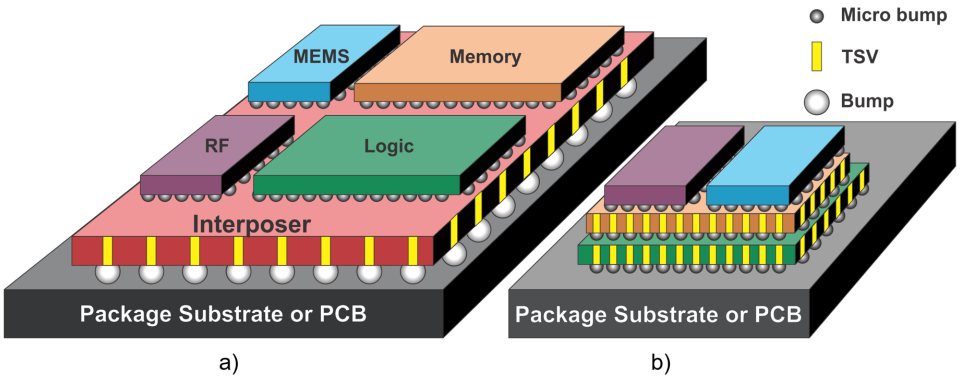



Figure 2.3: Schematic of 3D interconnects a) wafer lavel b) 3D stacking [9].

polishing are required. Sandblasting or abrasive jet machining is a technology that uses fine particles (<100 $\mu$m) that are launched by compressed air to the wafer; the silicon is then mechanically removed by chipping. It is possible to obtain feature sizes down to 30 $\mu$m and aspect ratios up to 2.5 [13]. However, the surface is rough after etching, and the technology is not viable for processing inside a cleanroom environment [14].

There are different ways to manufacture TSVs. They can be formed at the top of the wafer as via-first, via middle, and via-last (also possible at the bottom of the wafer) (Fig.2.4). In the via-first approach, the TSV is fabricated before the active devices. Doped polysilicon is often employed as conductive material as it can withstand the high temperatures (higher than 650 ° C) used during the deposition or annealing of other materials. TSVs made of polysilicon and tungsten have an average electric resistance in the order of tens of ohms [15].

TSVs can be filled or coated by different methods such as electroplating or electroless plating, physical vapor deposition, and atomic layer deposition. Electroplating is the deposition on a cathode of metallic ions from the electrolyte; an external electric source is required (voltage or current). Cu electroplating is the most common way of filling TSVs. Copper offers high conductivity, good resistance against electromigration, and stress migration [**?** ]. However, the filling process is slow (20 hours for 300 $\mu$m long TSVs). In addition, many other steps are required; backside seed layer wet etch, double-sided seed layer sputter deposition, and through-resist mold electroplating, among others [**?** ]. In physical vapor deposition (PVD), the material is vaporized from a target, pellets, or liquid source in the form of ions through an environment in vacuum or low pressure to be deposited over a substrate [17]. Vacuum evaporation, sputter deposition, and ion plating are some of the PVD techniques available. They are not often implemented in TSVs, except the seed layer deposition for electroplating. The sidewall coating of HAR vias with PVD is not trivial, non-homogeneous, and generates defects in the deposited layer. Atomic layer deposition (ALD) is a vapor phase technique capable of depositing a variety of thin layers at modest temperatures (below 350 ° C). It is possible to achieve excellent conformality in HAR 3D structures. The process is based on a sequence of steps forming a cycle. Several cycles are needed to deposit a thin layer, generally from a few

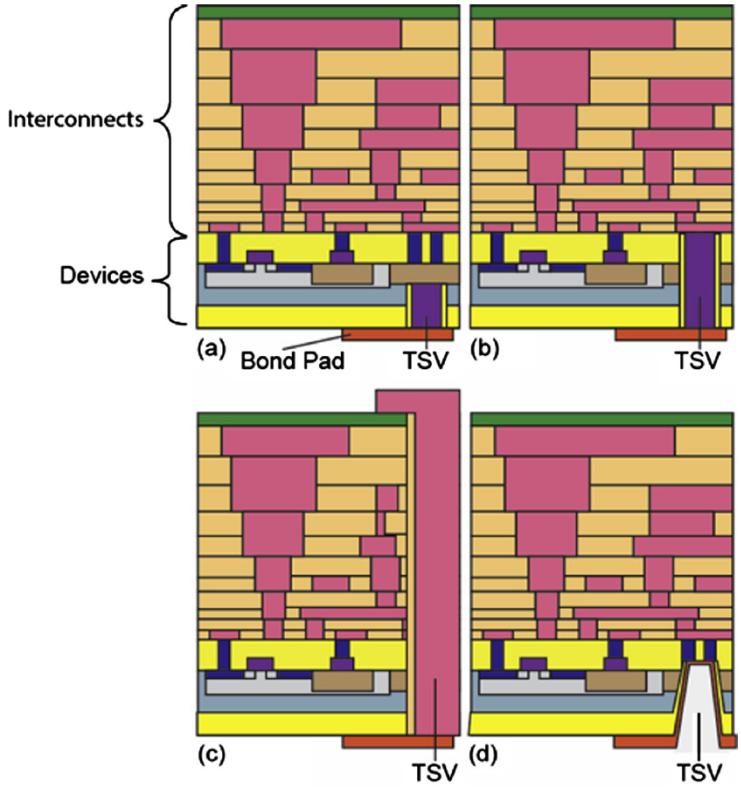



Figure 2.4: Schematic drawing illustrating different approaches to manufacture TSVs a) via-first b) via-middle, c) via-last, and d) via last (backside) [16]

nanometers to a few tens of nanometers. The first step is the functionalization of the substrate obtained by introducing a chemical precursor (gas) into a vacuum chamber. After a selected time sufficient to complete the reaction between precursor and surface, the chamber is purged with nitrogen or argon to remove unreacted precursor molecules. Then a counter-reactant precursor is pulsed, which reacts with the surface creating a monolayer of the desired material [18]. A new purge step completes the cycle. HAR TSVs coated by ALD require several hours or, depending on the material, days to achieve the desired layer thickness for achieving an electrical conductivity in the order of Ohms or higher. Considering all the advantages and drawbacks of the mentioned techniques, and to comply with the requirements discussed in chapter 1, we selected a modified DRIE to 'drill' the vias and PVD deposition for the metallization (see Chapter 3).

## 2.3. MASKS DESIGN

To optimize the TSVs fabrication and to characterize the electrical performance, a mask set was designed containing two sets of test structures. The first set was designed to optimize the DRIE process concerning uniformity, aspect ratio dependence, reproducibil-

Table 2.1: Selected geometrical parameters for DRIE test

| Block | Via diameter [$\mu$m] | Pitch (Center to center) [um] |
|---|---|---|
| **1** | 10-20 | 40 |
| **2** | 25-55 | 80 |
| **3** | 60-85 | 160 |

ity and to study possible configurations to achieve the maximum TSVs density without compromising the mechanical strength of the wafer. The second set contained several resistivity measurement structures for the electrical characterization of the materials and the TSVs.

### 2.3.1. DRIE TEST STRUCTURES

The first set of experiments was designed to determine the aspect ratio dependent etching rate (ARDE), an essential test as patterns with different sizes are generally present on the wafer, especially when MEMS components are implemented, and the silicon etch-rate reduces when the opening size reduces. We thus studied the etching depth for a fixed number of etching cycles for different size openings. Another aspect to investigate is related to the mechanical stability of the wafer. It is, in fact, important to determine the maximum density of vias that can be implemented without jeopardizing the mechanical stability of the wafer, especially considering the remaining process steps that need to be performed after the DRIE to complete the metallization.

The design of the first mask for this test is depicted in Fig. 2.5and the geometrical parameters summarized in Table 2.1. It consists of 3 blocks of circular openings with diameters varying from 10 $\mu$m to 85 $\mu$m. The vias were not equally distributed on purpose, mimicking the possible space distribution variations for IC and MEMS. Each block has a fixed separation (center-to-center distance) among the vias which increases from 40$\mu$m for the first block to 160 $\mu$m for the last one. This mask helped to find the optimal etching parameters for highly dense vias with straight sidewalls.

Once the etch rate and uniformity were determined, a second test, for which a second mask was needed, was carried out to determine the ARDE effect, so to assess if it was possible to fabricate TSVs for different connections schemes on the same substrate. The second mask, shown in Fig.2.6, has openings with different diameters (70 $\mu$m, 80 $\mu$m and 90 $\mu$m) and a fixed spacing of 300 $\mu$m (center to center).The layout is divided into three regions with different numbers of TSVs, going from only one to an array of 700. The denser structures at the bottom of each block are van der Pauw structures where many vias are connected in series. This allows to know the total resistance in a possible design that requires multiple TSV interconnections.

Based on the findings from the first round of experiments, a second layout that allowed for different sizes and shapes of the TSV at the surface was conceived. This mask was used to investigate the profile and uniformity of both wineglass and hourglass vias (see later chapters). This layout also contains the openings related to the test structures for electrical characterization. Another two masks with different size openings were also

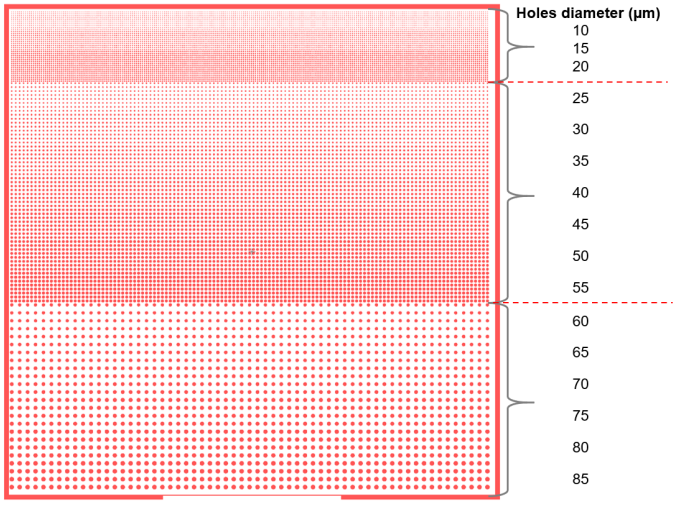



Figure 2.5: First mask design: 3 blocks of circular openings with sizes varying form 10 $\mu$m to 85 $\mu$m to determine the aspect ratio dependent etching rate

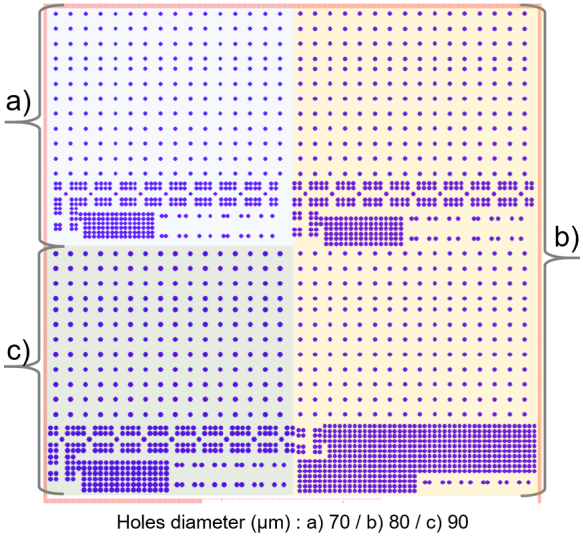



Figure 2.6: Second mask design: openings with different diameters (70 $\mu$m, 80 $\mu$m and 90 $\mu$m) and a fixed spacing of 300 $\mu$m (center to center)

used. Both are identical to the one shown in Fig. 2.7, the only difference being the diameter of the openings, 20 $\mu$m in one case and 100$\mu$m in the other. In addition to the masks used for the etching of the TSVs, other two masks (see Fig. 2.8), one for the top side and the other for the bottom side of the wafer, were necessary to pattern the metal and complete the TSVs. The full mask set for the case with 100 $\mu$m diameter openings

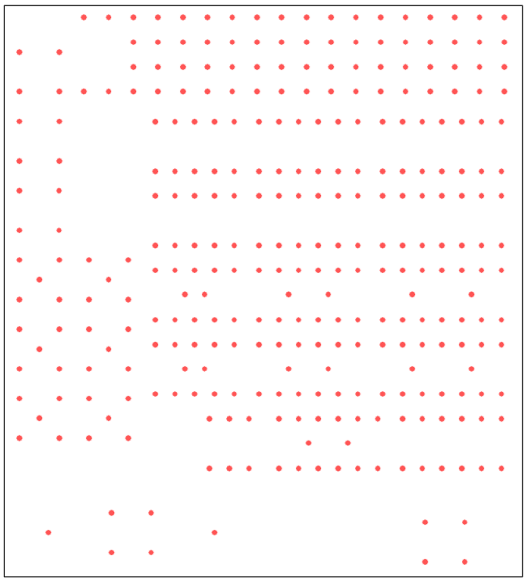



Figure 2.7: Mask design used on the fabrication of TSVs for the electrical characterization Mask design for vias distribution as required for the electrical characterization: vias are 50 $\mu$m in diameter and spaced at 200 $\mu$m.

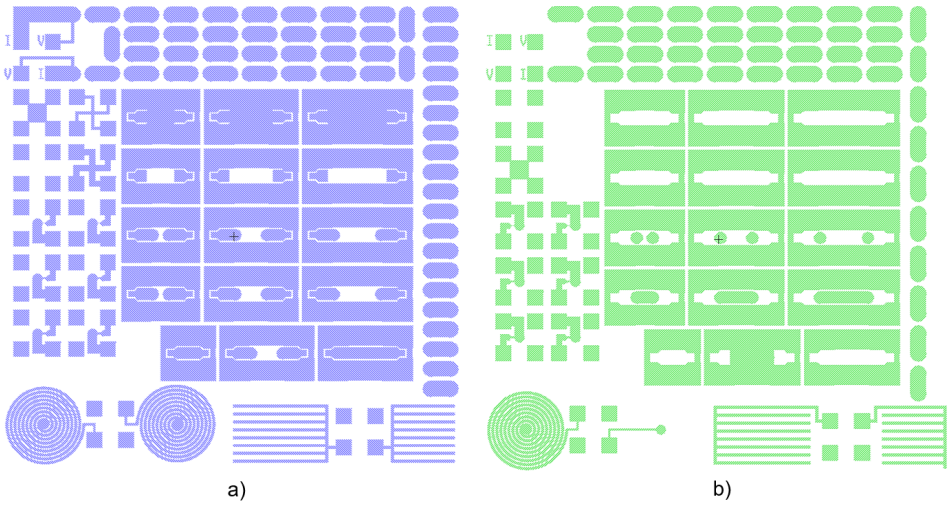



Figure 2.8: Mask set for the metallic patterning on the a) top and b) bottom of the wafer.

is shown in Fig. 2.9. The mask set is part of a multi-project design and contains several structures, not all related to this work. In the next section, we will discuss only the ones used in this thesis.

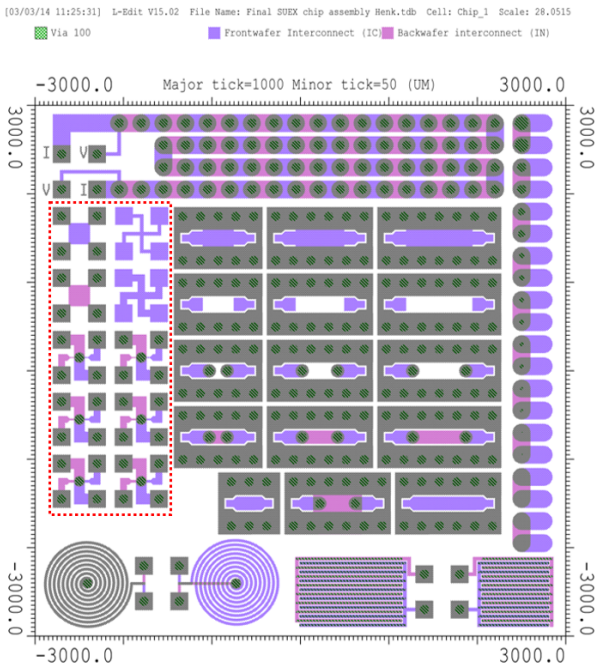



Figure 2.9: Mask set including the design for openings with a diameter of 100$\mu$m and the patterning of the metal. Only the marked structures were used (van der Pauw structures).

### 2.3.2. TEST STRUCTURES FOR ELECTRICAL CHARACTERIZATION

The electrical resistance of the TSVs was characterized using van der Pauw structures, see Fig. 2.10. These structures will be explained in detail in Chapter 5. For the electrical characterization of superconducting TSVs, it is important to define the material electrical resistance in planar structures and then compare it with the electrical resistance measured on the structures that include TSVs. The structure shown in Fig. 2.10a) corresponds to a traditional four-point probe van der Pauw structure. The bond pads are 200 $\mu$m by 200 $\mu$m and the wires that interconnect them are 80 $\mu$m wide. To measure the electrical resistance of the TSVs, a modified version of the van der Pauw structure was used. The structure is called Cross-Bridge Kelvin Resistor structure [19], (Fig. 2.10b)). The bond pads are 200 $\mu$m by 200 $\mu$m, the wires that interconnect them have different widths, 120 $\mu$m, 80 $\mu$m and 30 $\mu$m. Fig. 2.10c) is a simpler version of a four-probe measurement for electrical resistance. An array with 72 TSVs is shown in Fig. 2.10d). The purpose of this structure was to determine the reliability of the fabricated TSVs by checking continuity and the electrical resistance on a series configuration. The bond pads are 200 $\mu$m by 200 $\mu$m and the wires width vary from 40 $\mu$m to 200 $\mu$m.

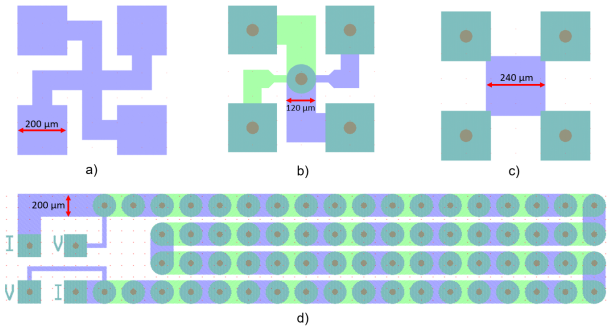



Figure 2.10: Test structures used for the electrical characterization of all types of TSVs, a) van der Pauw structure, b)Cross-Bridge Kelvin Resistor structure, c) Simple four probe measurement structure for TSVs, d) Array of TSVs with modified version of the cross-bridge Kelvin resistor structure.

## 2.4. SUMMARY

Interconnect technologies are necessary to increase density and reduce the footprint for IC and MEMS devices. TSVs are considered the heart of 3D integration technologies as they offer the possibility of shortening interconnection paths, thus reducing chip size while allowing the integration of more functionalities. The TSVs subject of this study were fabricated by DRIE since this allows to achieve high aspect ratio trenches. Several structures with different openings and spacings were designed and implemented to test the potential and limitations during the fabrication of TSVs by DRIE technology and provide test structures for the electrical characterization of the TSVs.

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# 3

# HAR TSVs DEVELOPMENT: ETCHING

## 3.1. INTRODUCTION

Realizing HAR TSVs over wafer-sized substrates requires a robust, reproducible process suitable for large-scale area manufacturing. This poses several challenges. The first is the etching of high aspect ratios (HAR) structures with suitable sidewalls profiles, and sizes.

Several fabrication methods were reported in the literature; some of them were briefly presented in Chapter 2. One of the most suitable processes for HAR etching in silicon substrates is deep reactive ion etching (DRIE). DRIE can achieve HAR structures with complete control of the process (reproducibility), employing anisotropic or isotropic etching or a combination of both. This chapter describes the etching of HAR TSVs with three different profiles (straight, wineglass, and hourglass). The encountered issues and the results obtained are presented and discussed in detail.



## 3.2. TSVs ETCHING BY DRIE

DRIE is a technology applied in micro-manufacturing, based on the use of plasma as an etchant. DRIE combines physical and chemical etching. The ions in the plasma react with the solid surface on which they impinge, forming volatile products (chemical part) and physically remove atoms from the substrate surface if they have enough energy (physical part). It allows the fabrication of deep trenches and TSVs in silicon substrates with high selectivity (greater than 70:1)to masking materials generally employed in IC technology, such as silicon dioxide. DRIE etches bulk silicon regardless of crystal orientation. This characteristic makes it possible to achieve deep structures with excellent control of the vertical profile and etching rates up to 3µm per minute [1] [2]. There are two main types of DRIE technologies: the cryogenic process and the "Bosch" process. [3] Both processes are based on the use of fluorine plasmas as etching agent, for example $SF_6$, $CF_4$, $SiF_4$, $NF_3$, $XeF_2$ or $F_2$. The fluorine radicals reactivity and the high volatility of the silicon fluorides make this plasma etching method intrinsically isotropic. Therefore, to achieve anisotropy in this case, vertical directionality passivation layer during the etching is required.

The cryogenic process was developed by Tachi *et al.* [4]. In this process, the wafer is cooled down at temperatures around −100°C. The passivation layer on the sidewall is formed after the addition of Oxygen gas to the etching plasma ($SiO_xF_y$), creating a thin protective layer of $SiO_2$ (Fig. 3.1). The concentration of $O_2$ added to the plasma also controls the anisotropy during the etching, the tapering (negative or positive), and undercutting.[1]. Cryoetching is a clean process where no deposition occurs at the reactor walls. It is a one-step process where no alternations are needed, and there is no visible scalloping effect. However, ARDE is very significant, and the process is susceptible to crystal orientation, oxygen and temperature. Even a slight temperature change (a few degrees) significantly affects the profile slopes. In addition, limiting the undercut is not easy[5].

## 3.3. BOSCH PROCESS

The Bosch process, also called "pulsed etching" [6], consists of three repetitive and consecutive steps, forming cycles, in which passivation and etching gases are introduced

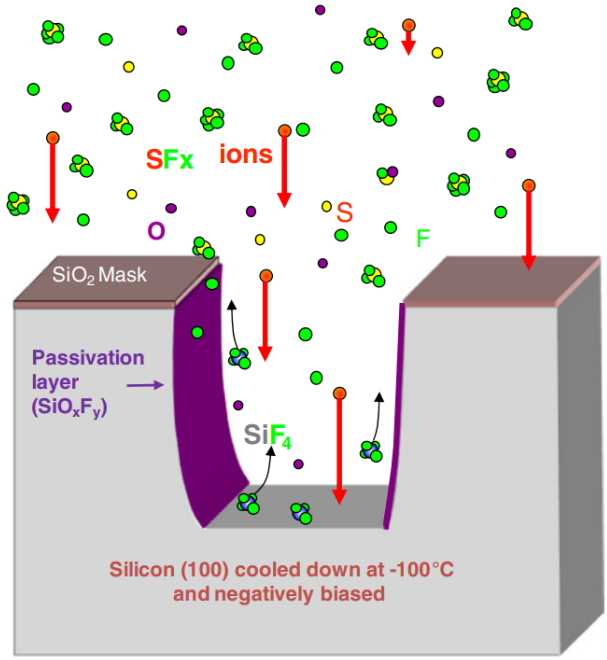



Figure 3.1: A schematic drawing of the physical and chemical mechanisms involved in cryoetching [5]

into the reaction chamber separately (Fig. 3.2). At the beginning of each cycle, the etching gas $SF_6$ is introduced to the plasma, which etches silicon isotropically. Then in the passivation step, a thin layer of octofluorocyclobutane $C_4F_8$ is deposited across all the surfaces. Applying a DC bias to the wafer plate supplies the ions from the plasma with sufficient energy to remove the polymer layer from the top surface (breakthrought step). At the same time, no significant removal of the polymer on the sidewalls takes place due to ion directionality, which relies on the ion incidence angle distribution. Increasing the energy in the vertical direction, keeping the lateral component low, improves the $C_4F_8$ removal over the wafer. The exposed silicon surface is etched again by the reactive fluorine-based plasma. By repeating this cycle, deep trenches can be etched in the silicon substrate. The $C_4F_8$ deposited on the sidewalls protects them from being etched during the further silicon etch steps. This permits to achieve and maintain vertical profiles of the etched structures. The Bosch process is prone to scalloping, a periodical peak and valley on the etched surface caused by the fast alternating sequence of etching and passivation cycles (Fig. 3.3). Factors such as plasma power, gas flow, temperature, pressure distribution, and switching speed need to be tuned in order to achieve smooth surfaces. The smoothness of the surface is highly relevant in many cases, and is essential for TSVs as thin insulation and metal layers need to be deposited on the side walls to achieve void-free trench refilling or coating.

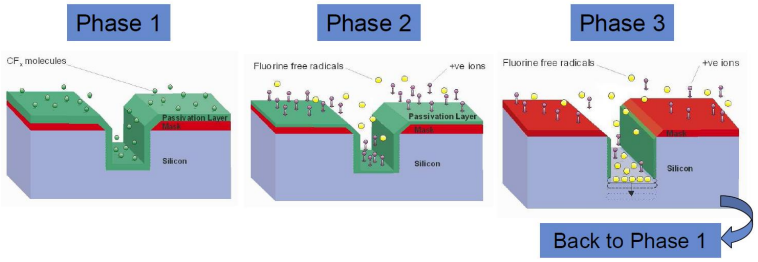



Figure 3.2: A schematic drawing of DRIE steps sequence [7].

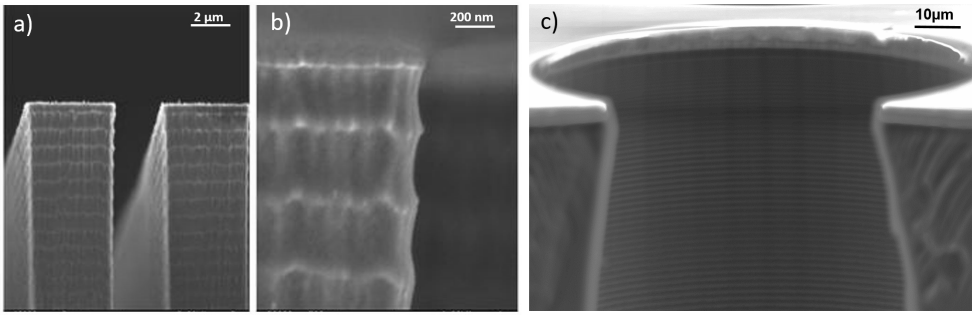



Figure 3.3: SEM image showing the scallops on the sidewalls after the Bosch process [8].

### 3.3.1. SHORTCOMINGS OF BOSCH DRIE

High etch rates are required to reduce the fabrication time for TSVs. Furthermore, to avoid using extra steps such as wafer thinning, complete etching through the wafer is desired. However, fast etching could alter the quality of the TSVs sidewalls (Fig. 3.4). Smooth sidewalls are necessary to ensure optimal coverage of the conducting material and a homogeneous coating or growth of the liner material such as SiO2. The achievement of the optimal TSVs involves optimization of the process concerning etch rate, selectivity to the masking layer, profile, and Aspect-Ratio Dependent Etching.

The first variable to be determined during the etching of TSVs is the silicon etch rate. During the etching of small feature sizes, the process is slowed down since it is more difficult for the reactive gases to get inside the cavity or hole, as well for reaction products to evacuate. The etching is mainly controlled by the plasma pressure, the RF power density, the reactive gases, and the substrate temperature. Increasing pressure increases etch rate. However, a pressure higher than 75 mTorr will decrease the etch rate.[6] [9]. Increasing the substrate temperature improves the etch rate, but it lowers the $C_4F_8$ deposition, giving as result sidewall erosion and undercuts (Fig. 3.6 a)). The etch selectivity is relative to the mask used during the etching. It depends on the quality of the mask in terms of material density and uniformity. Thermally-grown silicon oxide offers better protection and homogeneous coverage compared to photoresist (PR). Unfortunately, thermal oxidation is a long process, and high temperatures (> 1000°C) are required. Similar to thermally growing silicon oxide, Plasma Enhanced Chemical Vapor Deposition (PECVD)

of silicon oxide can also be used. It provides a very good masking layer; although the deposition is less conformal than thermal oxidation as reported in the literature, up to 10 $\mu$m of $SiO_2$ could be deposited by this method. However, these layers introduce some stress that can cause wafer bending. Photoresist offers a more straightforward solution with good masking properties. However, PR suffers significantly by the plasma during the etching. So the PR thickness is the limiting factor. However, there are new types of photoresists developed to overcome, in part, this thickness limitation, making it possible to reach 20$\mu$m and thus providing a masking layer sufficient for the etching of 500$\mu$m of silicon.



Generally, straight profiles are expected after HAR silicon etch, as often required for the realization of 3D MEMS devices such as resonators or accelerometers [10]. For HAR TSVs, sometimes, a sloped sidewall could help a conformal deposition of the seed, metallic and dielectric layers. Ideally, a sidewall slope of around 85 degrees is preferred [9]. The via tapering is controlled by the etching and deposition times. Longer etching cycles compared to passivation cycles give negative tapered vias. Opposed to this, longer passivation cycles compared to etching cycles end with positive tapered vias (i.e., with diameter of the bottom section smaller than the top one). In TSVs application, an etch stop layer is required (commonly silicon dioxide or aluminum). It protects the chuck where the wafer lays and prevents leakage of the cooling helium. This etch stop often causes notching. This effect is related to the charge accumulation at the edge of the via. It happens once the etching radicals are in contact with the dielectric barrier. A charge accumulation generates a strong electric field, changing thus the direction of the incoming etching ions at the bottom of the trench. A possible way to avoid this is by increasing the duration of the $C_4F_8$ deposition cycle in the last steps of the process (Fig. 3.4d).

It often occurs that structures with different sizes need to be etched at the same time. As mentioned earlier, this results in etch rate difference between small and large openings. This phenomenon is called aspect ratio dependent etching (ARDE). It is caused by the depletion of reactive species (fluorine content) at the trench bottom, due to the limited Knudsen transport of the gas species, as well as by the reaction of ion bombardment.[9]. Consequently, if the size of the trench or cavity is small, this effect is more pronounced, slowing down the etch in a more significant measure for smaller structures. This will result in a large variety of etch depths across the wafer. This effect can, in part, be compensated (or can be mitigated) by either implementing some design features or adjusting the etching parameters. Generally, for TSVs, this problem is less significant as they are typical of the same diameter. The density, though, could vary, and some loading effect may occur that needs to be addressed.

## 3.4. ETCHING OF STRAIGHT VIAS

In order to reduce the space needed and keep flexibility in positioning vias, the first option explored is the one using straight sidewalls. The etching was performed on 300 $\mu$m and 500 $\mu$m-thick 4-inches Si wafers. A layer around 6 $\mu$m-thick of silicon dioxide was deposited on both wafer sides by a combination of thermal wet oxidation (1100 °C) and PECVD (400 °C). The layer was used as a hard mask during vias fabrication by DRIE. The $SiO_2$ layer is patterned with circular structures, 50 to 100 $\mu$m in diameter (Fig. 2.7 and Fig 2.9), by reactive plasma etching with landing on the Si substrate. The TSVs were formed

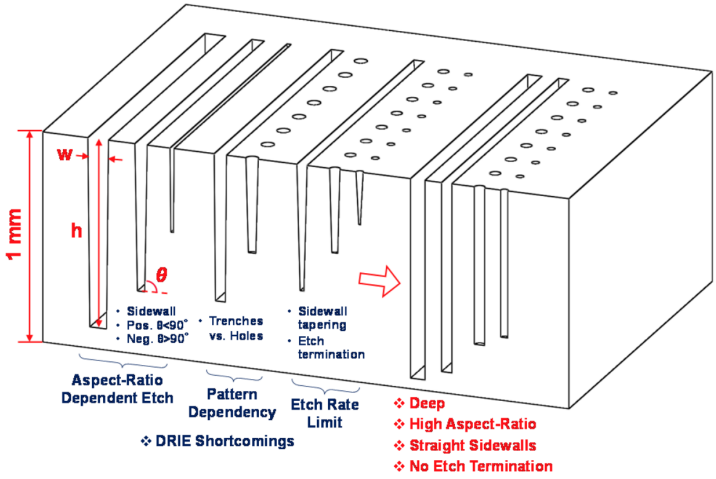



Figure 3.4: Sketch showing the DRIE shortcomings [11].

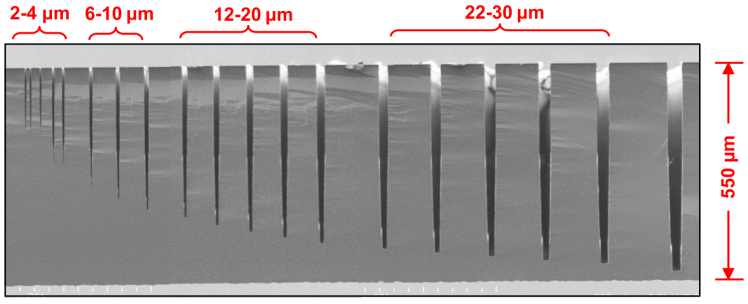



Figure 3.5: Aspect-ratio dependent etching (ARDE) [12].

by DRIE of the silicon, landing on the silicon oxide at the wafer backside, and subsequent removal of the silicon dioxide left on both wafer sides by immersion in a 40 percent HF solution for 20 minutes.

As mentioned, sidewall slope is a common issue during the etching of straight vias. Particularly, negative sidewall taper is obtained when a high $SF_6$ / $O_2$ or an inadequate process pressure is employed. Figure 3.7a) shows the results obtained using an etch pressure of 35 mTorr. This is inconvenient for high-density arrays of TSVs. If there is an evident negative slope, the TSVs could overlap during the etching or end with a fragile separation wall between them. This might limit the use of the TSVs during the next steps in the process, since metallization would be impossible. To avoid this, we investigated various etching pressures and achieved satisfactory results with 20mTorr, as shown in Fig. 3.7b). Cross-section images of the achieved HAR TSVs for both 300 and 500 $\mu$m-thick wafers are reported in Fig.3.8, showing the smooth sidewalls and straight profile of the vias.

As metallization of straight vias might be complex or problematic, other profiles are

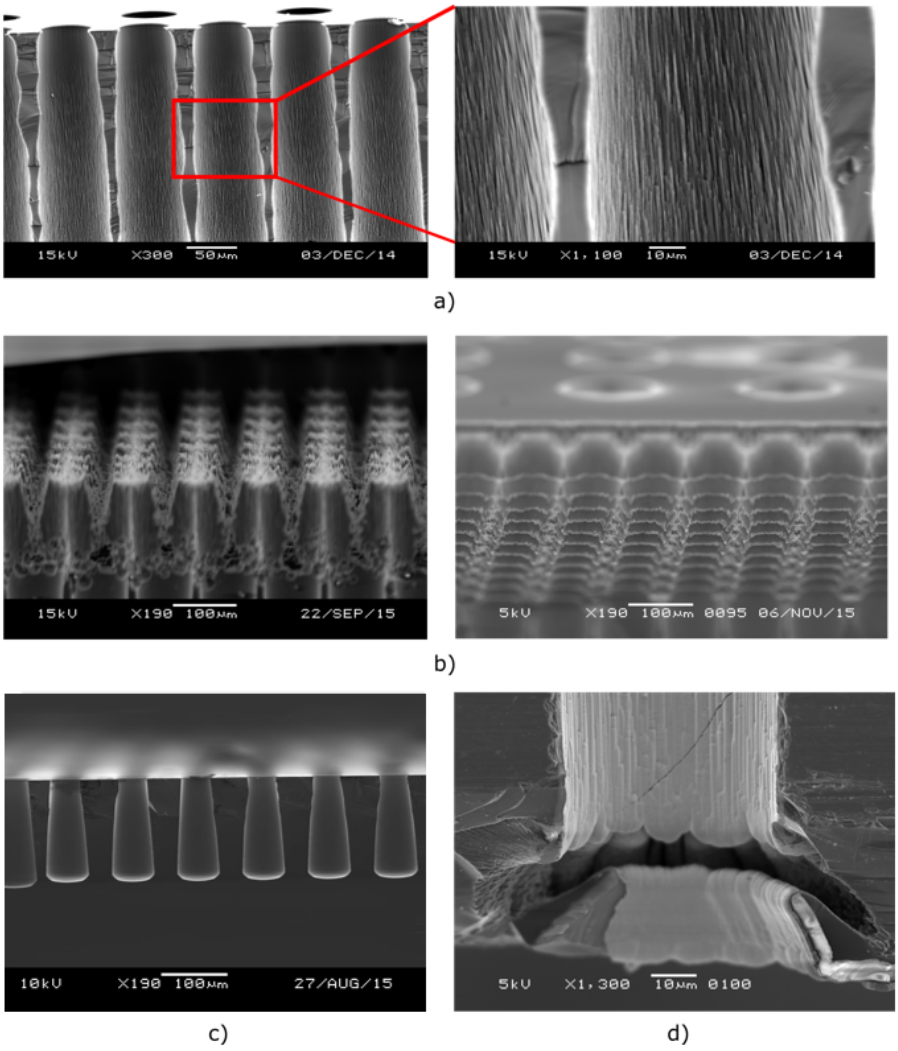



Figure 3.6: Possible TSVs etching defects: a) side wall erosion, b) poor selectivity, c) side wall slope (when straight vias are desired) and d) notching .

explored as well. First, a so-called wineglass and next a so-called hourglass via profile were explored. The results are reported in the following sections.

## 3.5. WINEGLASS VIAS

The etching of the wineglass TSVs builds on the results achieved for straight vias. In particular, cavities in the shape of funnels were added on top and bottom of the vias. This novel TSV geometry was introduced to enable efficient coating of the sidewalls of

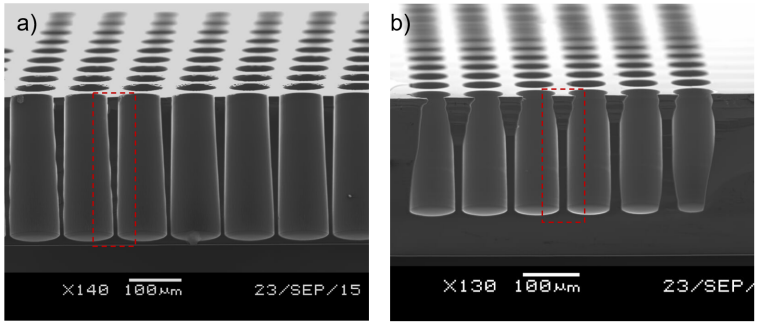



Figure 3.7: SEM images of TSVs showing the effects of using an etching pressure at a) 35 mTorr and b) 20 mTorr.

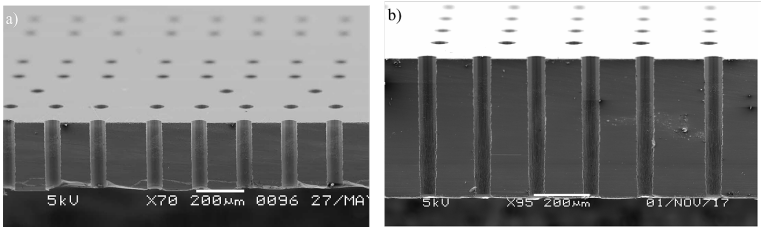



Figure 3.8: SEM images of TSVs cross-section after DRIE for a) 300 $\mu$m deep and b) 500 $\mu$m deep vias.

the TSVs with thicker and more continuous metal layers.

The general etching process is schematically represented in Fig. 3.9. The process started with thermal growth over a 4", double-side-polished, 300 $\mu$m-thick silicon wafer of a 2.6 $\mu$m-thick layer of silicon dioxide, used as a hard mask for the ensuing steps. Aligned hemispherical cavities (funnels in the following, representing the open extremities of the vias) were then etched on both sides of the Si substrate. To achieve this, the $SiO_2$ layer was first photo-lithographically patterned with circular windows on one side of the wafer (Fig. 3.9a). After that, isotropic deep reactive ion etching (DRIE) was introduced for 130 s at 25 °C using inductively-coupled $SF_6$ plasma. The plasma was generated near the coils in the upper part of the reactor chamber (Rapier Omega i2l). This step etched wine glass-shaped funnels with pronounced undercuts. The funnels were subsequently plasma-etched anisotropically using an $SF_6$- and $CH_8F_8$-based plasma generated in closer proximity of the substrate. This step removed the undercuts mentioned above and broadened the openings of the funnels. The aligned funnels at the other side of the wafer were fabricated in the same way. A protective layer of silicon oxide deposited by plasma-enhanced chemical vapor deposition (PECVD) was then added on the bottom side of the wafer (Fig. 3.9b). The inner, 50 $\mu$m-wide cylindrical section of the vias was drilled by anisotropic Bosch-type etching, landing on the previously deposited $SiO_2$ layer (Fig. 3.9c). The wafer was then thoroughly cleaned through exposure to oxygen plasma and immersion in HF and $HNO_3$ solutions (Fig. 3.10).

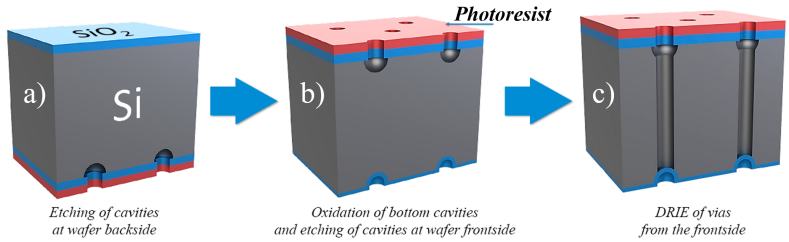



Figure 3.9: Sketched cross-sections of a Si substrate illustrating the via fabrication and coating process flow: a) etching of bottom side funnels: isotropic DRIE followed by anisotropic DRIE; b) $SiO_2$ deposition over bottom side funnels and etch of top side funnels; c) DRIE of straight section of the vias



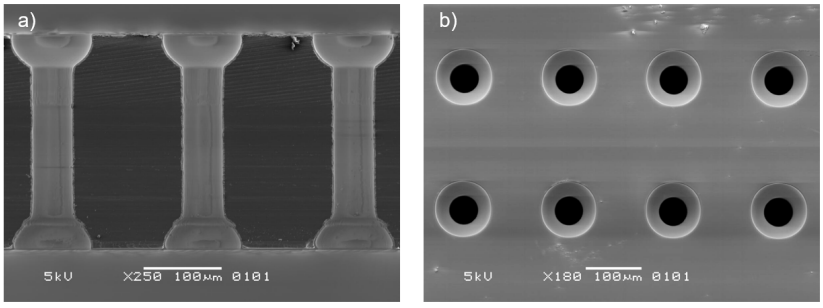



Figure 3.10: SEM image of etched wineglass vias a)cross section and b) top view.

## 3.6. HOURGLASS VIAS

For the hourglass vias, the fabrication process started with the thermal growth of a 300 nm-thick silicon dioxide layer on a 4" double-polished 500 $\mu$m thick silicon wafer. A protective layer of 5 $\mu$m of silicon oxide was deposited by PECVD on the top and bottom side of the wafer to be used as a hard mask for the ensuing steps (Fig. 3.11a-b). Two-level cavities were then patterned on the backside of the wafer utilizing two sequential process steps of photolithography and oxide etching. First, a 4$\mu$m-thick photoresist (AZ 3027) was coated on the backside of the wafer, and 100 $\mu$m diameter holes were exposed with a dose of 500 mJ/cm$^2$ and developed. Then the silicon oxide was partially etched by plasma for 6 min, leaving around 2 $\mu$m of oxide for the following (etch) step. After this, a standard cleaning procedure was performed, including an oxygen plasma treatment (400 ml/min of $O_2$ at 1000 W) followed by immersion in $HNO_3$ (99 % concentration) at room temperature and then in $HNO_3$ (69% concentration) at 110 °C. The backside of the wafer is then again coated by 4 $\mu$m-thick photoresist (AZ 3027), and 50 $\mu$m diameter holes are exposed with a dose of 650 mJ/cm$^2$, developed and etched by plasma for 7 minutes until the silicon oxide was removed. This was also performed on the front side of the wafer, as shown in Fig. 3.11b, which also includes a close-up view of the two-level etched cavity.

The TSVs were etched by DRIE. To achieve the hourglass shape, the vias were etched using different DRIE configurations, varying the power, gases, and temperature (see Ta-

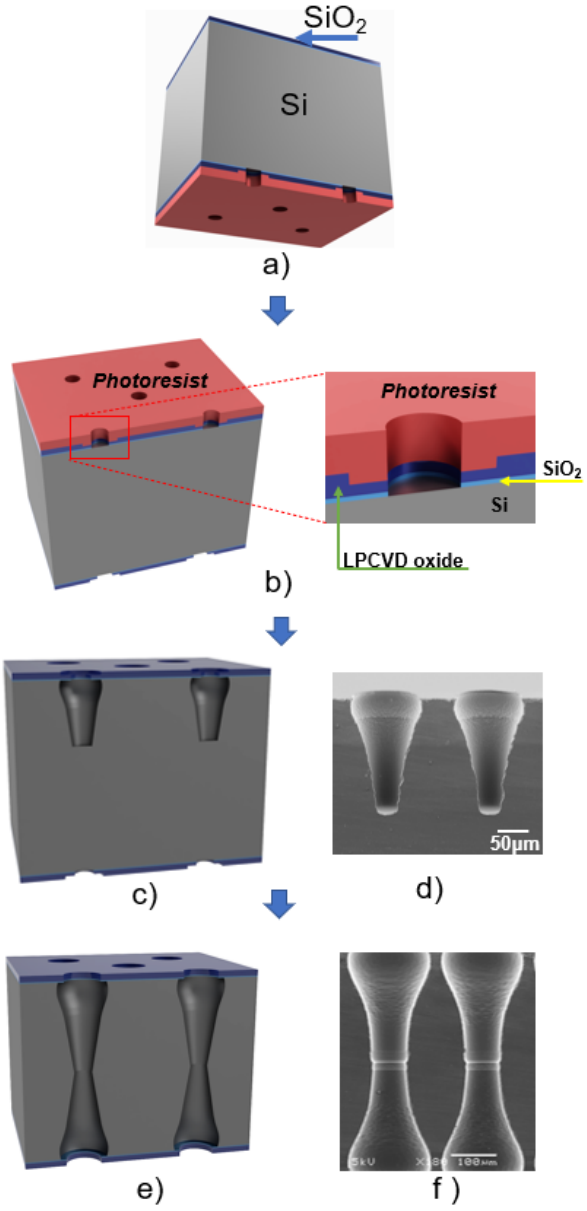



Figure 3.11: Sketched cross-sections of a Si substrate illustrating the TSV fabrication process flow: a) etching of bottom side two-level cavities; b) etching of top side two-level cavities; c) etching of top side funnels: anisotropic DRIE followed by isotropic DRIE; d) SEM cross-sectional view of TSVs after step c); e) Etching of top and bottom side funnels: anisotropic DRIE; f) SEM cross-sectional view of TSVs after step e)

ble 3.1). The etching process started by anisotropic Bosch-type etching at 20 °C during 360 cycles on the front side of the wafer. Immediately after, isotropic DRIE was applied

for 260 s at 20 °C. This particular type of etching uses inductively coupled $SF_6$ plasma, which is generated near the coils in the upper part of the reactor chamber (Rapier Omega i2l). This step etched hemispherical cavities that, in this case, ended as funnels due to the previous etching step (Fig. 3.11c). Fig. 3.11d shows a SEM picture of a TSVs etched after the first two etching steps (the silicon oxide mask was removed before dicing). The wafer is then etched from the backside. A deep cleaning of the wafer was performed. This is necessary to remove any possible residue of the octafluorocyclobutane [$C_4F_8$] passivation layer introduced during anisotropic DRIE. Firstly, an oxygen plasma stripper is used. The recipe has two steps. The first step operates with a mixture of $CF_4$ (200 ml/min) and $O_2$ (35 ml/min) at 400 W for 3 minutes. The second step uses pure $O_2$ (500 ml/min) at 1000 W for 10 minutes. Next, a cleaning procedure with $HNO_3$ was performed, and lastly, the wafer was immersed in a solution containing a non-ionic surfactant (Triton) dissolved in water for 3 minutes and in buffered hydrofluoric acid (BHF, 7:1) for approximately 1 minute. This last step partially removed the silicon oxide, leaving only the 100 $\mu$m openings in the remaining hard mask. The final part of TSV etching was performed by a so-called "Pseudo KOH" etching step which mimics the effects produced by (wet) KOH etching. The anisotropic plasma, in this case, was a mixture of $SF_6$ and $CH_8F_8$ gases. It was generated in closer proximity to the substrate to obtain a significant impact on the edges of the already partially etched funnels. As a result, this step broadened the openings and smoothed the TSV sidewalls. This step is performed for 520 seconds on both sides of the wafer (Fig. 3.11e). A transport wafer was necessary during the etching of the backside of the wafer because of the absence of a landing layer and to prevent the backside helium pressure in the etching machine from dramatically increasing and consequently arresting the process. A transport wafer added extra height to the process wafer, which changed the etching performance. This is the reason for the minor mismatch between the etching on the front side and the etching on the backside, which is visible in Fig. 3.11f.

Several etching tests were performed before obtaining the desired Hourglass form. Some of the tests were conducted in parallel; for this reason, some of the selected etching parameters are not related. However, all the tests were based on the same recipes reported in Table 3.1. Only the time or number of cycles was varied. The related results are shown in Fig. 3.12 and the corresponding etching times or cycles reported in Table 3.2. In Fig. 3.12 are shown the etching configurations: a) was etched only by anisotropic etching, b) was etched initially by isotropic etching for 260 seconds, the longest isotropic etching of all these tests. The vias is c) d) and e) were etched in a similar way, only different anisotropic etching times in step 3, 1920, 1620, and 960 seconds respectively.

## 3.7. SURFACE SMOOTHENING

The etching of TSVs by DRIE generally leaves small imperfections such as scalloping, sidewall roughness, or erosion. Scalloping is the most common, it is formed due to the switching between the etching and passivation steps, and it is in the range of hundred nanometers [13]. Rough sidewalls create problems in insulation and seed layer deposition and also cause serious leakage current[3]. This roughness is usually not a problem for MEMS devices, but a perfectly smooth surface is critical for superconducting applications. Any small imperfection on the surface could induce ruptures during the metalliza-

Table 3.1: Main parameters for the DRIE etching steps for hourglass TSV fabrication.

| **Etch type** | Step 1: Bosch (anisotropic) | Step 2: isotropic | Step 3: anisotropic (PseudoKOH) |
|---|---|---|---|
| **Time [sec]** | 360 cycles: D1: 2 E1: 1,5 E2: 5,5 | 260 | 520 |
| **Power [W]** | Primary coil: 2200 | Primary coil: 2500 | Primary coil: 500 Secondary coil: 2000 |
| **Platen temperature [C]** | 20 | 20 | 50 |
| **Gas flow [sccm]** | D1: $C_4F_8$ = 280 E1: $SF_6$ = 350 E2: $SF_6$ = 350 | $SF_6$ = 500 | $SF_6$ = 350 $C_4F_8$ = 210 $O_2$ = 210 |

Table 3.2: Tested parameters for the DRIE etching before obtaining hourglass TSVs. The corresponding images in Fig. 3.12 are indicated.

| **Via type** | **Wafer Thickness [um]** | **Openings diameter [um]** | **Step 1 [s]** | **Step 2 [cycles]** | **Step 3 [s]** |
|---|---|---|---|---|---|
| **a)** | 300 | 20 | Anisotropic (PseudoKOH): 960 | Anisotropic (Bosch): 260 | Anisotropic (PseudoKOH): 600 |
| **b)** | 300 | 20 | Isotropic: 260 | Anisotropic (Bosch): 225 | Anisotropic (PseudoKOH): 960 |
| **c)** | 300 | 20 | Isotropic: 70 | Anisotropic (Bosch): 300 | Anisotropic (PseudoKOH): 1920 |
| **d)** | 300 | 20 | Isotropic: 70 | Anisotropic (Bosch): 260 | Anisotropic (PseudoKOH): 1620 |
| **e)** | 300 | 50 | Isotropic: 70 | Anisotropic (Bosch): 300 | Anisotropic (PseudoKOH): 960 |

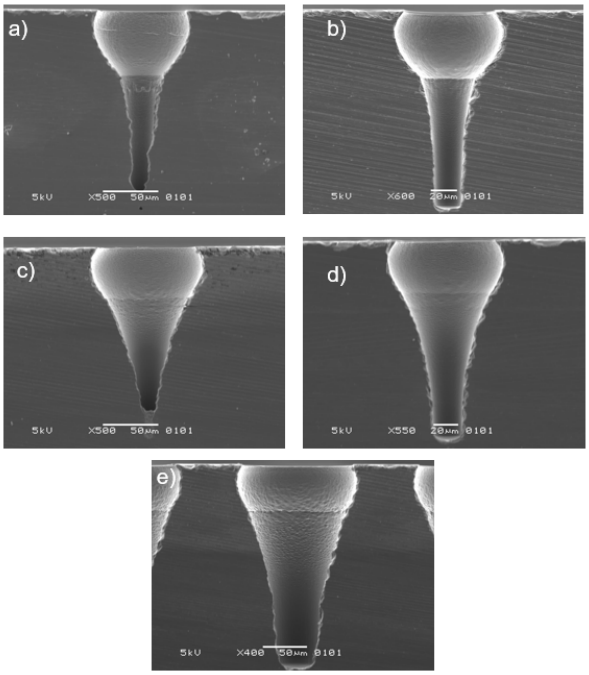



Figure 3.12: SEM images of different etching configurations achieved during the development and optimization of the hourglass vias.

tion, ending as nanometric cracks in the metallic surface. The solution to this problem was the growth of "wet" silicon oxide. Repeated sequential steps (two) of oxidation and oxide removal were performed for smoothening the sidewalls; as rough surfaces have a larger exposed area, they oxidize faster, thus consume more silicon upon etching and the result is a smoothening of the surface. In each step, a 2 $\mu$m-thick layer of thermal silicon oxide was grown on the etched silicon wafer and then removed by HF 40%. This procedure was implemented in all etched TSVs mentioned before.

## 3.8. INSULATION LAYERS

Insulation layers are not required for superconducting devices. At cryogenic temperatures, the bulk silicon behaves almost as an insulator. However, during the electrical characterization at room temperature, a necessary step for monitoring the quality of the metal layer deposited on the wafer and through the vias, a good insulating layer is necessary. A layer of around 2 $\mu$m of thermal $SiO_2$ was grown as electric-via-insulation as this guarantees good isolation, high breakdown voltage, and a smooth surface. Other layers that have good insulation properties are LPCVD $SiO_2$ or SiN, or ALD aluminum oxide.

## 3.9. CONCLUSION

The three etching schemes described in this chapter use different DRIE etching parameters, such as time, substrate temperature, and gas flow, to achieve high-quality HAR vias and thus achieve high quality through silicon interconnects. They all give satisfactory results and are suitable for further processing. The slented shape of the wineglass and hourglass vias will facilitate coverage by thin films deposited by sputtering while requiring more surface area. The straight vias will allow more dense arrays, but different filling techniques are more indicated in this case. The choice is thus determined by the type of application envisioned or the selected metallization method.



In the next chapter, possible metallization alternatives for filling these HAR vias will be presented and discussed.

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# 4

# HAR TSVs DEVELOPMENT: METALLIZATION

## 4.1. INTRODUCTION

System downscaling, 3D integration and increasing functionalities are the main challenges that both IC and MEMS technology are facing. Advanced packaging schemes, low-cost materials and reliable interconnect technologies are therefore required.

Although for 3D interconnects the TSV technology using copper as vias filling material is quite established, it still presents reliability issues such as mismatch among the coefficient of thermal expansion of the materials involved. TSV filling by electroplating and electroless plating is typically time-consuming and is hardly void-free, especially for high aspect ratio (HAR) vias [1]. Silver inkjet printing [2] and magnetic assembly of Ni rods [3, 4] have been reported to improve vias filling. However, these filling methods show limitations in substrate choice, via depth, processing time or temperature budget. In addition, when moving towards quantum technology applications additional requirements have to be taken into account.The TSVs should achieve superconductivity to be suitable for the operation of quantum devices at cryogenic temperatures [5].



In Chapter 3 the microfabrication techniques for the etching of HAR TSVs were explained. In order to complete the fabrication of the superconducting TSVs a proper metallization is necessary. According to the type of TSVs, we utilized two different techniques. The first technique fills straight TSVs with indium by a new and non-standard method called Vacuum Assisted Liquified Metal(VALM). The other technique coats non-straight (funelled) TSVs with aluminum and niobium by means of physical vapor deposition (Sputtering). In this chapter, these two techniques are explained and the results obtained are discussed. Both advantages and limitations of each of them will be addressed.

## 4.2. TSVs FILLED BY VALM METHOD

Vacuum Assisted Liquified Metal (VALM)is a new method based on the combination of a novel filling material for vias, Indium, and a straightforward via filling technique. In this section the motivation for selecting indium as metal layer, the tool designed and the process developed are described, followed by an evaluation of the filling characteristics of this method.

### 4.2.1. WHY INDIUM?

Indium is a soft, ductile and malleable material that keeps its plastic properties at cryogenic temperatures [6]. Indium is widely used as semiconductor compound in diverse applications: indium antimonide (InSb) for infrared detectors, indium arsenide (InAs) for photovoltaic photodiodes and terahertz applications and indium phosphide(InP) lately used in the fabrication of quantum dots for photoluminescent applications [7]. Indium is also used in IC soldering, since it has a melting temperature approximately of 156 °C. Indium has been already implemented in the integration of superconducting qubits by means of bumps [8]. The attractiveness of this material in quantum technology is due to the possibility of reaching superconductivity at higher temperatures (3.37 K) compared with other materials such as titanium and tungsten (< 0.5 K). The TSVs are filled using pure beads (6.35 mm diameter, trace metal basis higher than 99.99, Kurt J. Lesker Co. Ltd).

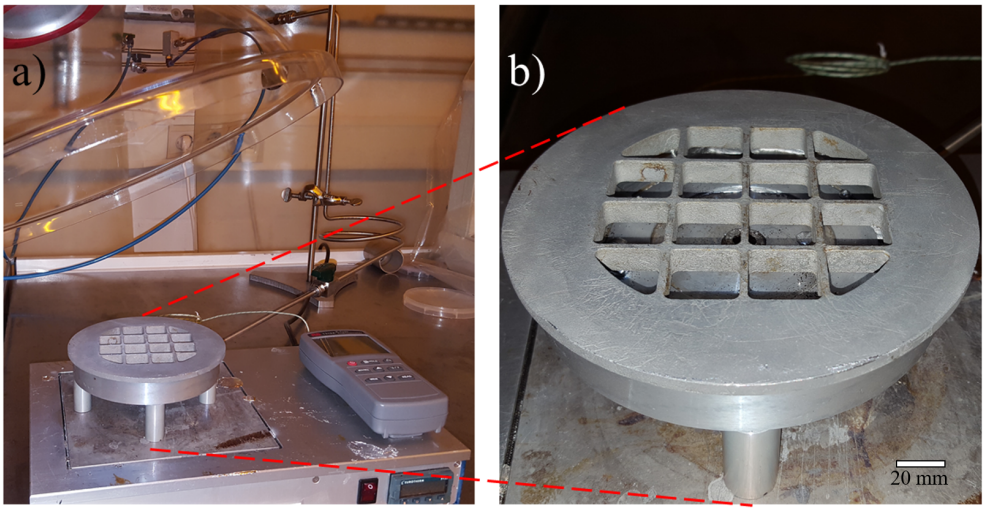



Figure 4.1: Custom-made setup for the VALM process. It is over a hotplate, thermocouple is placed on top of the vacuum tool(a), close-up of the custom-made vacuum tool (b)



### 4.2.2. VALM TOOL

The VALM method designed to fill the TSVs is based on the combination of vacuum and heat supply using a custom-made tool (Fig. 4.1). The vacuum is generated in the tool by the Venturi effect and reaches a maximum value of -0.85 bar with an induced air flow of 28 nl/min. The vacuum tool is placed on a hotplate which provides the heat to fully melt the In beads(previously cleaned in a HF solution) and lower as much as possible its viscosity in the fluid state. The temperature should not raise above 160 °C, to avoid an accelaration of In oxidation.

### 4.2.3. DOCTOR BLADE COATING TECHNIQUE

Doctor blade, or tape casting, is used for the production of thin films on large area surfaces. It was developed in the 40's for the fabrication of piezoelectric films and capacitors. In the doctor blading process, schematically depicted in Fig. 4.2, a well-mixed slurry consisting of a suspension of ceramic particles along with other additives (such as binders, dispersants or plasticizers) is placed on a substrate. When a constant relative movement is established between a blade and the substrate, the slurry spreads on the substrate to form a thin sheet which results in a gel-layer upon drying. The doctor blading can operate at speeds up to several meters per minute and it is suitable to coat substrates with a very wide range of wet film with thicknesses ranging from 20 to several hundred microns.

### 4.2.4. VALM PROCEDURE

The wafer with the already etched TSVs was placed on the chuck of the vacuum tool. After waiting for temperature stabilization, the In beads were deposited on top of the wafer. (Fig. 4.3a). The In melts and was spreaded across the wafer surface. Subsequently

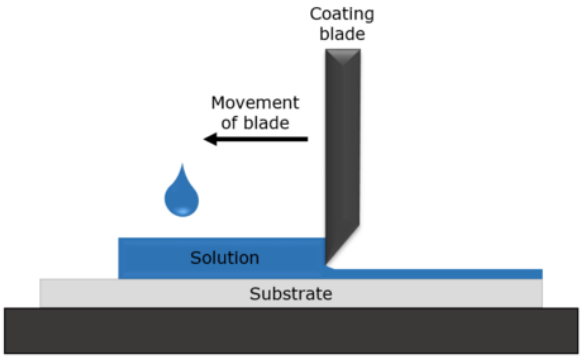



Figure 4.2: Schematic drawing illustrating the doctor blade coating technique [9].

the vacuum was activated. As a consequence, a pressure difference between the opposite openings of the vias causes the molten In to flow inside the vias in a laminar flux regime with a specific velocity pattern, which is higher at the center of the via and lower towards its contour. According to the Stokes flow law, such pressure difference is a function of the center liquid velocity, liquid density, via dimeter and via length.

A blade, covered with a thin Kapton film, is then used to repeatedly scan the top wafer surface (Fig. 4.3b) to spread around the molten In into the vias until they are filled and a thin layer (few tens of $\mu$m-thick) is left on the surface (Fig. 4.3c). After blade coating, the vacuum is stopped, the wafer is covered with Kapton film for protection and turned upside down, so that the same procedure can be performed on the back side of the wafer (Fig. 4.3d). After complete filling of the vias, the In layer is patterned on both wafer sides using a conventional photolithographic process.

A thick layer of photoresist is required to conformally coat the metal surface which presents topographical irregularities, caused by the manual blade coating and micrometric In oxide clumps which form upon exposure to air of the In surface. A 35 $\mu$m-thick photoresist layer (AZ9260, Microchemical GmbH) was obtained by sequentially spray coating 32 layers of diluted photoresist (2 $\mu$L per layer). Finally, after resist exposure and development, the exposed In is etched in a solution of hydrochloric acid, hydrogen peroxide and water in a ratio of 8:1:1 for around 7 minutes. (Fig. 4.3e).

### 4.2.5. RESULTS

The VALM process allows to successfully fill HAR TSVs for both the 300 $\mu$m and 500 $\mu$m wafer thicknesses tested, as shown by the cross-section images reported in Fig. 4.4. Optical images of the wafer after patterning are shown in Fig. 4.5. The voids-free filling of TSV has been obtained at wafer level in just 10 minutes, irrespective of the depth of the vias. In comparison, conventional via-filling methods such as electroplating and electroless plating require around 20 hours and 2 hours, respectively [11]. The results achieved show the effectiveness of the proposed VALM method for filling HAR TSVs, and open up the possibility of applying the method to other low melting point metals such as gallium, tin, eutectic alloys for soldering, and micro/nano suspension pastes.

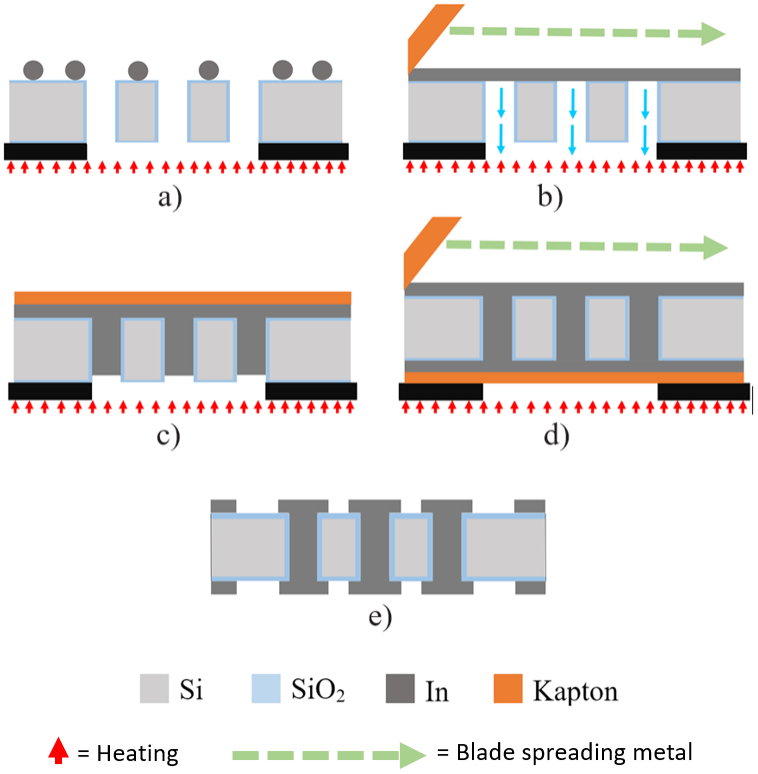



Figure 4.3: Main process steps for the fabrication of In-filled HAR TSVs: a) Application of In beads over the DRIE etched wafer placed over the heated vacuum tool. b) Blade coat-ing of melted In with activated vacuum. c) Vias filling with In, and coverage of top wafer side with Kapton film. d) In blade coating on bottom wafer side. e) Patterning of top and bottom In layers after complete vias filling.

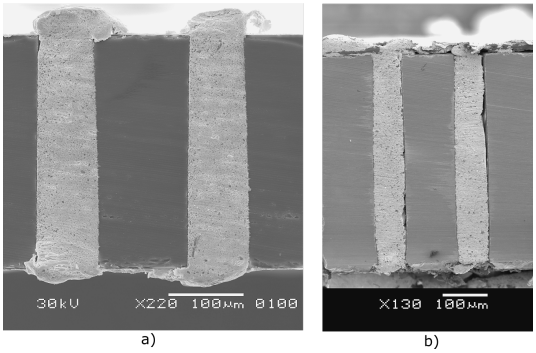



Figure 4.4: SEM images of TSVs cross section after filling with indium a) 300$\mu$m deep vias b) 500 $\mu$m deep vias. The voids and delamination in (b) were caused by the sawing used to obtain the cross-sections of the samples.

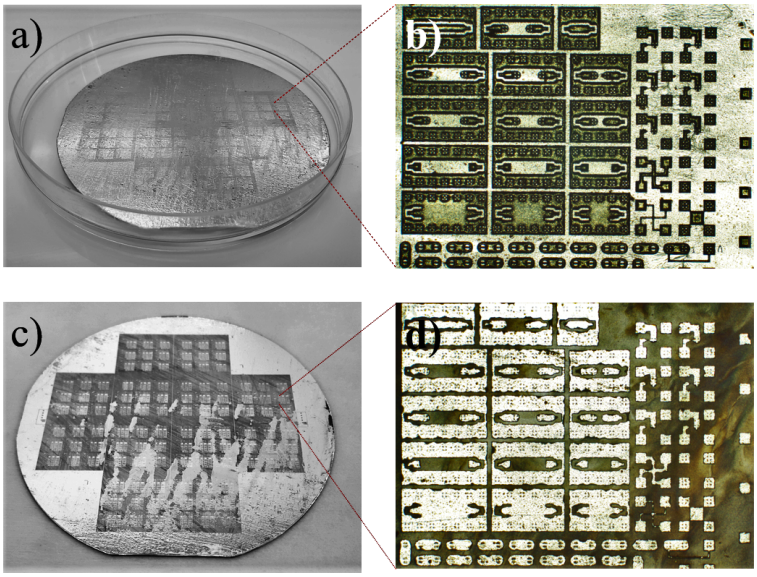



Figure 4.5: Patterning of indium after blade coating. Top view (a) and close-up (b) of the In-coated 4-inch wafer after photoresist patterning. Top view (c) and close-up (d) of patterned In test structures.

Currently, the major challenge facing the fabrication process regards the etching of the In layers after via filling to define the interconnection lines and bond pads. The challenge arises from the residual non-uniformity of the In layer after blade coating. The wet etching step takes longer where the In is thicker, ending with under-etched and over-etched regions (Fig. 4.5c). It is thus very important to achieve a good thickness uniformity of the In layer, after spreading the molten material across the wafer, to render the etching process more controllable. An ideal set-up would feature spin coating of molten In; a blade that could be actively heated, precisely aligned to the wafer surface and mechanically moved; and an oxygen free or forming gas environment to avoid In oxidation, such as a glove box. The process yield is around 90 percent.

## 4.3. TSVs COATED BY PHYSICAL VAPOR DEPOSITION

Sputtering is defined as a physical ejection of particles (atoms, ions, and clusters) from a solid surface (target) which is attacked by energetic ions. The term sputtering is used more generally to denote erosion processes induced by the impact of atoms, molecules, neutrons, or electrons [10, 11]. During the collisions, the target is transformed into atomic particles which are deposited over the substrate in conditions of gaseous plasma in a vacuumized chamber (Fig. 4.6).

The vacuumized chamber is filled with a high purity gas, argon. Argon has an inert relative mass and the property of transmit its kinetic energy during the collisions in the plasma, creating the ions. The ions are the main force during the sputtering of thin films. The range of pressures during the sputtering are from 0.5 mTorr to 100 mTorr. A negative bias is applied to the cathode, target material, typically between -2 to -5 KV. A positive

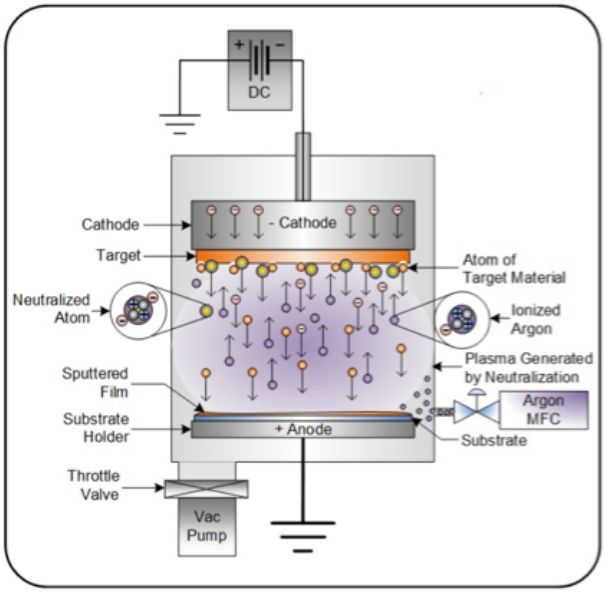



Figure 4.6: Diagram of the DC sputtering process [12]

charge is then applied to anode the substrate where the material is going to be deposited. The electrically neutral argon gas atoms are first ionized as a result of the collision of these gas atoms onto the surface of the negatively charged target[]. Then, the substrate attracts the ionized gas ions together with the vaporized target coating ions, forming a thin film on the substrate.

### 4.3.1. ALUMINUM METALLIZATION

Uniform and void-free metallization of HAR TSVs presents several difficulties. To assess if it is possible to coat TSVs by sputtering of a metal layer, the different types of vias fabricated as described in Chapter 3 were coated by a 2$\mu$m-thick layer of pure aluminum on both sides of the wafers. The first test was done using double-side polished 280 $\mu$m thick wafer, the thinnest wafers available without extra thinning steps. The first tests were performed on straight vias with 20 $\mu$m and 50 $\mu$m of diameter.

As shown in the cross section of Fig. 4.7a the aluminum was not able to penetrate inside the vias beyond some tens of microns below the wafer surface. Similarly, for 50 $\mu$m diameter vias, the sputtered aluminum was not able to cover the central part of the via, Fig. 4.7b. This indicates that by conventional sputtering methods it is not possible to coat completely HAR straight vias. Next, funneled TSVs were tested. TSVs with the same diameters and a small funnel on the top part, were also coated with 2 $\mu$m of pure aluminum. In Fig. 4.7c the cross section of a 20 $\mu$m diameter via with a funnel is shown. In this case the via was not successfully coated, however, there is an improvement compared to the straight vias. The via was totally coated for the case of 50 $\mu$m diameter vias with funnel at the top (Fig. 4.7d). Given these encouraging results, we developed the

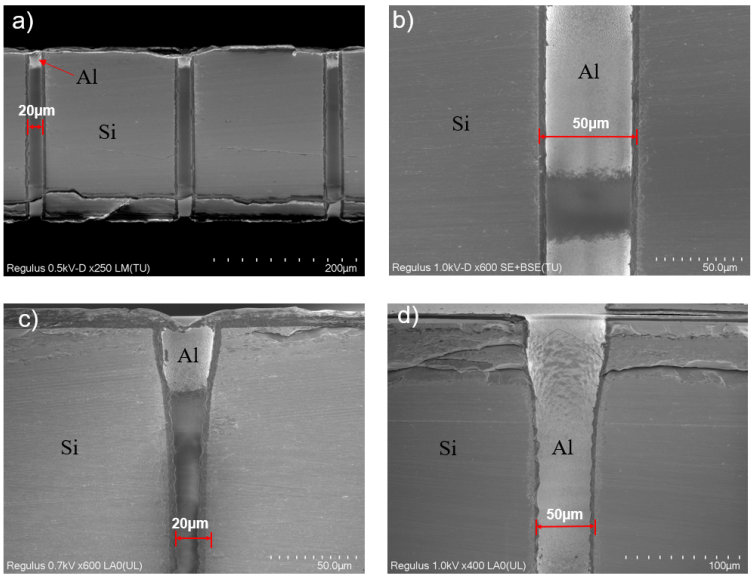



Figure 4.7: SEM micrograph of the test wafers cross-section showing the aluminum penetration inside the Si vias after sputtering: a) Straight vias with 20 $\mu$m diameter, b)Straight vias with 50 $\mu$m diameter, c) Funelled vias with 20 $\mu$m diameter, d) Funelled vias with 50 $\mu$m diameter.

process further using the funneled and hour glass profile vias.

The metallization of the vias was performed by sequential sputter deposition of Al and TiN on both sides of the wafer using a cryo-pumped Trikon Sigma 204 sputter-coater with a base pressure of $10^{-6}$ Pa. A 4.5 $\mu$m-thick layer of pure aluminum, as measured on the flat wafer surface, was first sputtered over the TSVs as superconducting layer. The deposition took 34 minutes and was performed with a substrate temperature of 25 °C, 20 sccm of argon gas flow and a DC power of 1.3 kW on the 16 Al target. The chamber pressure was set to 244 mPa, obtaining a deposition rate of approximately 2.25 nm/s. Subsequently, a 20 nm-thick layer of titanium nitride was sputtered over the aluminum, acting as a capping layer. TiN was deposited at 350 °C for 58 s. During the TiN deposition, the pressure was tuned to 569 mPa by using 20 sccm of argon and 70 sccm of nitrogen, and the power was set to 6 kW. Micrographs of the resulting vias after the metallization are shown in Fig. 4.8a-c.

### PATTERNING

The Al and TiN layers were patterned by optical lithography and plasma etching. AZ 12xt-20PL photoresist was spin coated to a thickness of 12 $\mu$m using a holder that has vacuum only at the edge, soft baked at 110 °C for 240 s, exposed with 300 mJ/cm$^2$, post-exposure baked at 90 °C for 60 s and developed with AZ 300MIF developer per 60 s using a double puddle develop process. Then, the metallic layers were etched by inductively-coupled plasma at 25 °C using HBr (30 sccm) and Cl (20 sccm) as reaction gases and 500 W of RF power.

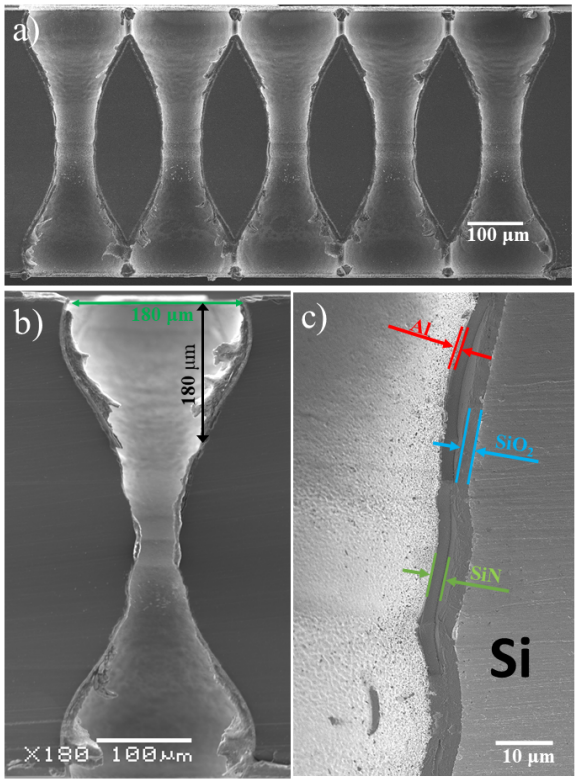



Figure 4.8: SEM micrograph of the cross-section of 500 $\mu$m-deep TSVs after Al/TiN sputtering. (a) Array of TSVs. (b) Single via (hanging Al flakes due to saw dicing). (c) Central section of the via showing the layers stack (the TiN capping layer is not visible).



#### RESULTS

The cross-sections shown in Fig. 4.8 evidence successful, fully conformal and void-free coating of the TSVs with sputtered Al/TiN in a hourglass via. In particular, a metallic layer as thick as 430 nm could be deposited in the center of the TSV (Fig. 4.9). The metal thickness measured in the center of a wineglass via is in the range of 330nm (Fig. 4.10). A poly-crystalline microstructure of the Al layer is observed. The hourglass shape allowed the deposition of a thicker layer of Aluminum compared with the wineglass shape.

### 4.3.2. SPUTTERING OF NIOBIUM

This metallization was performed using Niobium (Nb) and Niobium alloys, such as niobium nitride (NbN), niobium titanium (NbTi) and niobium titanium nitride (NbTiN). The deposition of Nb and NbN was done using the same system as the one utilized during the Al sputtering. A Nordiko 2000 system was used for NbTi and NbTiN deposition. Wineglass and hourglass vias were coated with metallic layers varying from 1$\mu$m to 4$\mu$m in thickness, as measured on the flat wafer surface. The Nb deposition took around 5

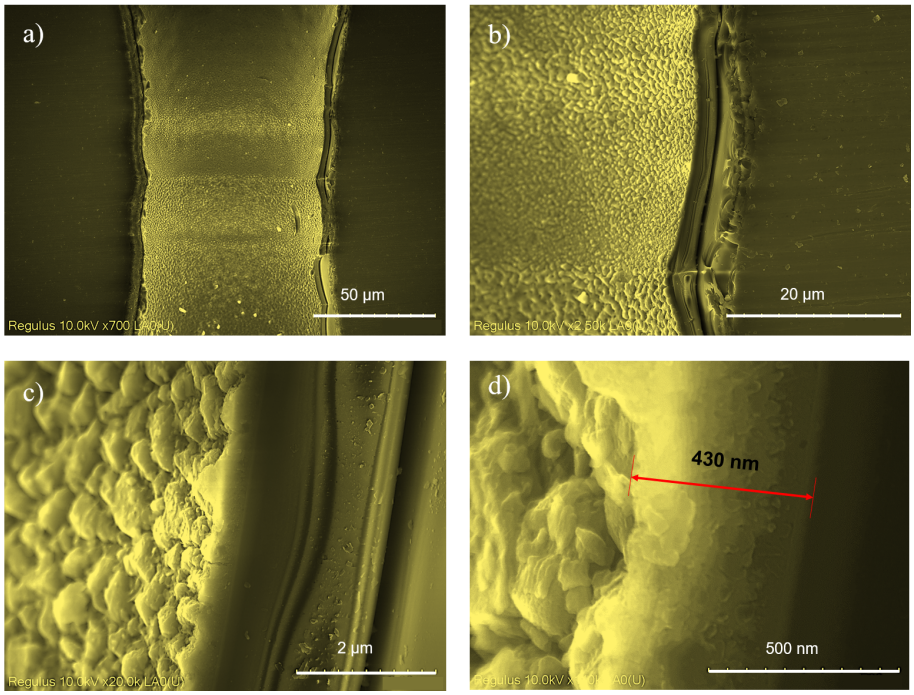



Figure 4.9: SEM micrographs of the cross-section of the middle section of an hourglass TSV after Al sputtering and imaged at increasing magnifications. (a) 50 $\mu$m scale. (b) 20 $\mu$m scale. (c) 2 $\mu$m scale. (d) 500 nm scale, evidencing the measured thickness and the poly-crystalline microstructure of the Al layer (no TiN capping layer observed).

minutes, for 4$\mu$m thickness with a substrate temperature of 25 °C, 150 sccm of argon gas flow and a DC power of 5 kW on the 16 Nb target. The chamber pressure was set to 11,4 Pa, obtaining a deposition rate of approximately 12 nm/s. NbN was deposited with substrate temperature of 25 °C and 350°C, 150 sccm of argon gas flow, 5 or 7 sccm of nitrogen gas flow and a DC power of 5 kW. The chamber pressure was set to 1.15 Pa, and a deposition rate of approximately 14 nm/s. NbTi and NbTiN were deposited at room temperature 100 sccm of argon gas flow, 5.3 sccm of nitrogen gas flow(NbTiN) and a DC power of 0.44 kW. The chamber pressure was set to 0.88 Pa, and a deposition rate of approximately 1.38 nm/s.

### PATTERNING

The niobium layers were patterned by optical lithography and plasma etching. Following the same procedure used for Al, the AZ 12xt-20PL photoresist was patterned. The metallic layers of Nb and NbN were etched by inductively-coupled plasma at 25 °C using $SF_6$ (30 sccm) as reaction gas, 125 W of RF power, chamber preasure of 660mPa and 20°C substrate temperature. NbTi and NbTiN layers were etched using the same raction gases and power as the one used for Al and TiN layers.

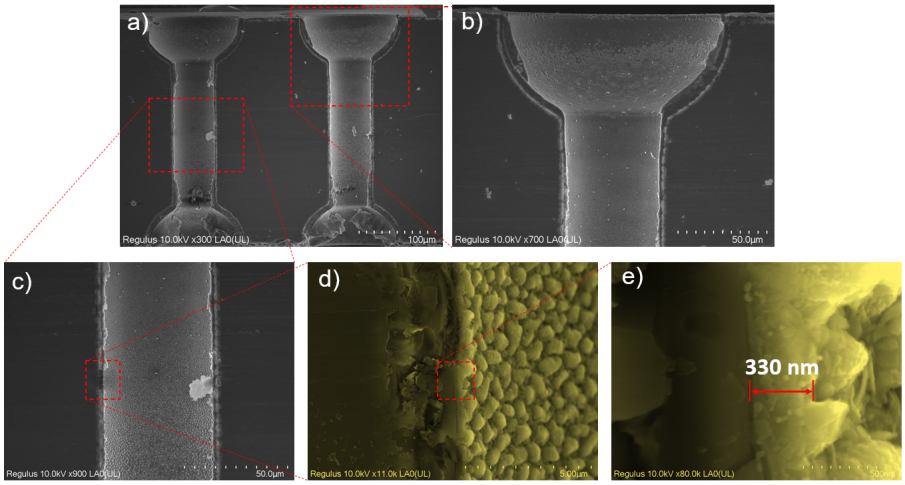



Figure 4.10: SEM micrographs of an wineglass TSV after Al sputtering and imaged at increasing magnifications. (a) 100 $\mu$m scale. (b) Only top part, 50 $\mu$m scale. (c)Only middle part, 50 $\mu$m scale. (d)5 $\mu$m scale. (e) 500 nm scale, evidencing the measured thickness and the poly-crystalline microstructure of the Al layer (no TiN capping layer observed).



### RESULTS

The cross-sections shown in Fig. 4.11 evidence the conformality of Nb sputtering in winglass vias. A metallic layer as thick as 180 nm could be deposited in the center of the TSV. The layer thickness measured at the center of a wineglass via sputterd with NbTi is in the range of 340 nm(Fig. 4.12). The cross-sections of Hourglass vias are shown in Fig. 4.13. A layer of approximately 314 nm was achieved in the center of the TSVs.

## 4.4. DISCUSSION

An effective and versatile method for filling high aspect ratio through silicon vias at wafer level with In, i.e. a low melting point and cryogenically superconductive material was studied. HAR TSVs fabricated on both 300 $\mu$m and 500 $\mu$m-thick Si wafers have been used as test structures. The novel filling method, VALM, has been applied to fill void-free TSVs in only 10 minutes irrespectively of vias depth. The TSVs filling yield is around 90 percent for all diameter vias tested. Moreover, filling of high density TSVs is not an issue for this method, though via surface density is inherently restricted by the DRIE process. Indium patterning is challenged by the current non-uniformity of the blade coated In layer at the wafer surface. A dedicated tool designed to guarantee a uniform thickness of the molten layer is currently under construction. This filling method is practical for MEMS when a simple interconnect is required and sputtering is not an option.

To facilitate the penetration of the plasma within the TSVs during the sputtering process, a funneled TSV profile in the shape of a wine glass was introduced in 300 $\mu$m-thick Si wafers. It was tested and there were some progress but the technology required further development. The idea of funnels was deeply tested using different shapes, sizes and wafer thickness. This pseudo-hemispherical funnel was 50 $\mu$m deep and had a di-

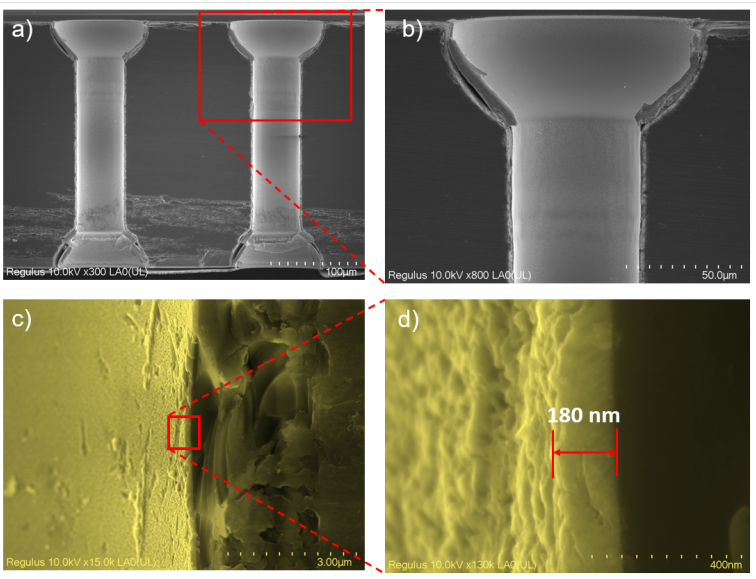



Figure 4.11: SEM micrographs of the cross-section of an wineglass TSV after 4$\mu$m Nb sputtering and imaged at increasing magnifications. (a) 100 $\mu$m scale. (b) Only top part, 50 $\mu$m scale. (c)Only middle part, 3 $\mu$m scale. (d) 400 nm scale.

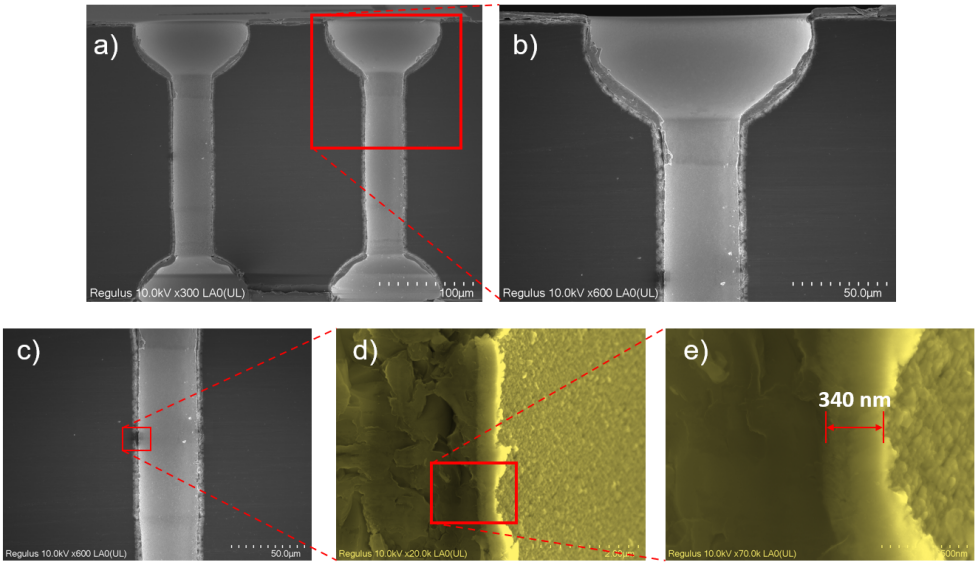



Figure 4.12: SEM micrographs of the cross-section of an wineglass TSV after 2$\mu$m NbTi sputtering and imaged at increasing magnifications. (a) 100 $\mu$m scale. (b) Only top part, 50 $\mu$m scale. (c)Only middle part, 50 $\mu$m scale. (d)2 $\mu$m scale. (e) 500 nm scale.

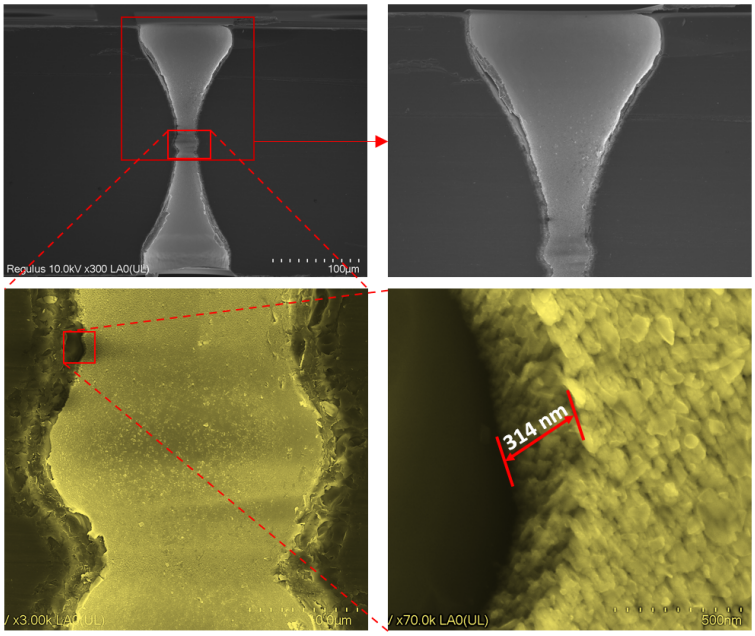



Figure 4.13: SEM micrographs of the cross-section of an Hourglass TSV after 2$\mu$m NbTi sputtering and imaged at increasing magnifications. (a) 100 $\mu$m scale. (b) Only top part. (c)Only middle part, 10 $\mu$m scale. (d) 500 nm scale.



ameter of 120 $\mu$m at the wafer surface side. The central section of the TSV was cylindrical with a diameter of 50 $\mu$m and a length of about 200 $\mu$m. They were succesfully coated with Al, Nb and NbTi achieving a metal thickness up to 340 nm in the center of the TSVs.

The hourglass TSV profile features relatively wide access holes (180 $\mu$m) to enhance plasma funneling into the core of the via, as well as a smooth tapering which exposes the entire length of top and bottom halves of the sidewall to the molecular flux incoming from the closest access hole. The progressive shrinking of the diameter of the via (down to 50 $\mu$m in its middle section) promotes lateral physical deposition of molecular species from the plasma to the sidewalls even in the center of the via, as it compensates for the decreased lateral mobility of the reactive molecules in that most remote via section. By virtue of these features and in combination with a suitable configuration of the sputtering process, the proposed via geometry overcomes the issues related to inconsistent, insufficiently thick or non-uniform metal coating that persist in prior examples of superconducting TSVs.

The versatile TSV technology allows to achieve a minimum inner diameter of 20 $\mu$m and a maximum diameter for the outer openings on top and bottom wafer surfaces of 250 $\mu$m for a wafer thickness of 500 $\mu$m. Thicker and thinner wafers are also compatible with our TSV fabrication process. Moreover, it is readily possible to sputter and pattern additional superconducting materials in hourglass vias, such as *e.g.* niobium, titanium and their alloys [13]. More generally, it is in principle possible to introduce any sputter

material inside the proposed TSVs, including *e.g.* copper or gold, the limitations residing rather in the patterning of the metal layers.

## 4.5. CONCLUSION

The VALM method allows to keep the temperature of the via filling process below 160 °C, and achieves approximately 90 percent yield, and low resistivity interconnects without the need of additional thermal treatments. The proposed method thus enables the effective use of In as TSVs filling material, allowing 3D MEMS integration for superconductive devices. Indium achieves superconductivity at higher temperatures in comparison with Aluminum [14]. This is important in quantum engineering to ease the realization of a prototype of a quantum computer. The microfabrication process for 500 $\mu$m-deep Al-based and Nb-based TSVs is fully compatible with conventional CMOS fabrication processes. A high conformality and superior uniformity of the metallic coating of the vias was obtained employing the tailored hourglass and wineglass sidewall profile in combination with low-pressure DC-sputtering. In the next chapter, the results of electrical characterization at room and cryogenic temperatures will be presented.



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# 5

# HAR TSVs development: Electrical characterization

## 5.1. INTRODUCTION

In Chapter 4, different metallization methods were presented for straight, wineglass, and hourglass TSVs. Hourglass vias coated with sputtered aluminum show, so far, proper characteristics in terms of layer thickness and homogeneous sidewall coating to achieve highly conductive TSVs. However, to confirm this, electrical characterization is necessary.

The TSVs electrical resistance was measured by the four-point probe method employing a 3D cross-bridge Kelvin resistor structure. The resistance was measured at room temperature to determine the quality and continuity of the metal deposition. For the In-filled vias, electrical measurements were performed with a different set of test structures, this due to the difficulties encountered during the patterning. The TSVs with the best electrical performance at room temperature were also measured at cryogenic temperature to determine whether they could reach superconductivity.

## 5.2. MEASUREMENT SET-UPS



The electrical characterization was performed at room temperature for all types of vias and at cryogenic temperature only for wine glass and hourglass TSVs. The characterization of the TSVs at room temperature was made through I-V measurements by means of a precision semiconductor parameter analyzer (Keysight 4156C) and a multi-probe station (Cascade Microtech). Cryogenic DC resistance through the vias was measured as a function of temperature with a standard 4-point probe method using a commercial adiabatic demagnetization refrigerator (ADR, Entropy GmbH). Only the In TSVs were measured by a two-point prove resistivity measurement. This is because the structures necessary for the four-point probe measurement were not successfully patterned during the etching of indium.

### 5.2.1. TWO-POINT PROBE RESISTIVITY MEASUREMENT

To characterize the In-filled vias, electrical measurements were performed on the set of test structures shown in Fig. 5.1. A path of 200 $\mu$m width by 200 $\mu$m length was used for single via measurement. The same length was used for measurements with two vias in parallel and two vias in series with a separation between the vias of 180 $\mu$m . The width of the path was 445 $\mu$m for the parallel configuration and 945 $\mu$m for the TSVs in series. The measurements were performed by providing a stepwise voltage, from -15 mV to +15 mV, for all three different vias configurations: single via, two vias in parallel, and two vias in series (Fig. 5.2).

As mentioned in Chapter 4, straight vias were not successful in terms of coating during the sputtering of Al and Nb/NbTi layers. For this reason, straight vias were not used anymore for these metals.

### 5.2.2. FOUR-POINT PROBE RESISTIVITY MEASUREMENT

For the Al and Nb wineglass and hourglass TSVs, the resistance was measured using a four-point probe method by means of a 3D cross-bridge Kelvin resistor structure (Fig. 5.3) [1]. A current was applied across one pair of diagonally opposite terminals (indicated by $I$ and $GND$ in Fig. 5.3b) and the resulting voltage drop across the central single

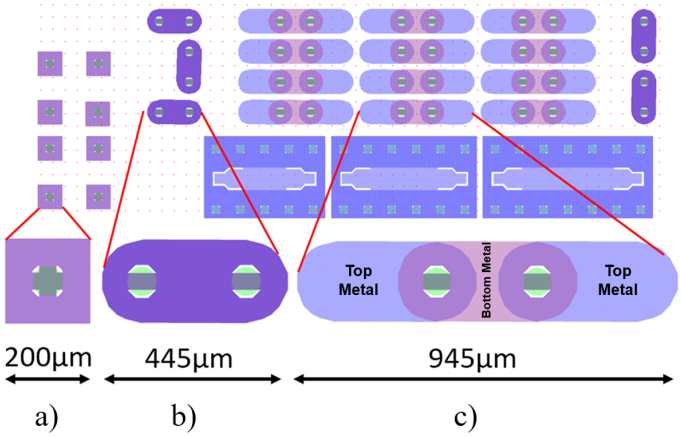



Figure 5.1: Layout of the test structures for the electrical characterization of the indium vias : a) single via; b) two vias in parallel; c) two vias in series.



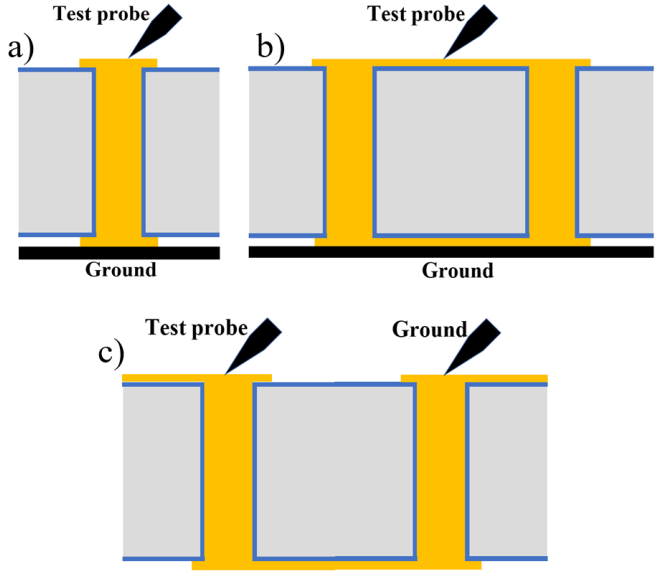



Figure 5.2: Configuration for the electrical characterization of the In-filled vias: a) single via; b) two vias in parallel; c) two vias in series.

via was measured across the other pair of terminals ($V_1$ and $V_2$). The value of the single-via resistance can be approximated using the following formula:

$$R = \frac{\pi}{\ln(2)} \frac{\Delta V}{I}$$

where $\frac{\pi}{\ln(2)}$ is used as geometric correction factor since the TSVs are coated with thin metallic layers and the probes are equidistant [2].

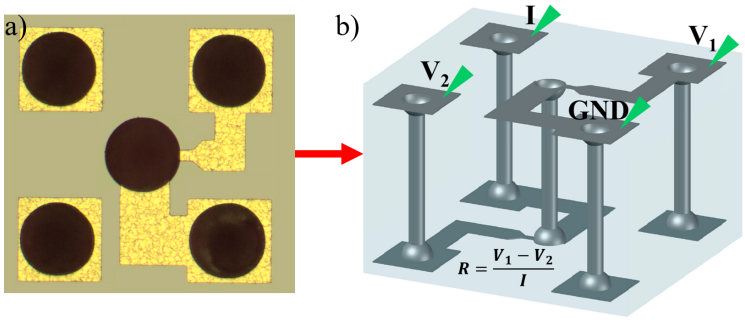



Figure 5.3: a)Top view of a single cross-bridge Kelvin resistor structure used during the electrical characterization of the TSVs. b) Sketch of the 3D geometry of a single cross-bridge Kelvin resistor structure.



### 5.2.3. CRYOGENIC MEASUREMENT SETUP

Cryogenic DC resistance through the vias was measured as a function of temperature with a standard 4-point probe method. The sample was mounted on a copper block weakly coupled to the Gadolinium Gallium Garnet stage of the ADR (Fig. 5.4). A thermometer and a resistive heater allowed to change the temperature down to 600 mK. The holder has a usable area of 20mm x 5mm, so only two structures at the same time can be inserted. The holder was coated by kapton tape before mounting the sample, as the chips have a conductive layers on the back side. The samples were glued with Ge varnish, which is thermally conductive down to approximately 100 mK to 200 mK.

## 5.3. MEASUREMENTS AT ROOM TEMPERATURE

### 5.3.1. INDIUM TSVs

The measurements for 75 $\mu$m diameter vias in a 300 $\mu$m -thick wafer are reported in Fig. 5.5. A resistance of 0.16 Ω was measured for the parallel configuration, and 3.60 Ω for two vias connected in series (Fig. 5.2). All the measured configurations show an ohmic behavior of the In-filled vias over the investigated voltage range. The obtained resistivity for a single via is as low as 593.6 $\mu$ Ωcm, which is in line with prior works [3, 4]. It was not possible to pattern properly van der Pauw structures due to the irregularities in the topography of In layers. Because of this, it was also not possible to perform electrical measurements at cryogenic temperatures.

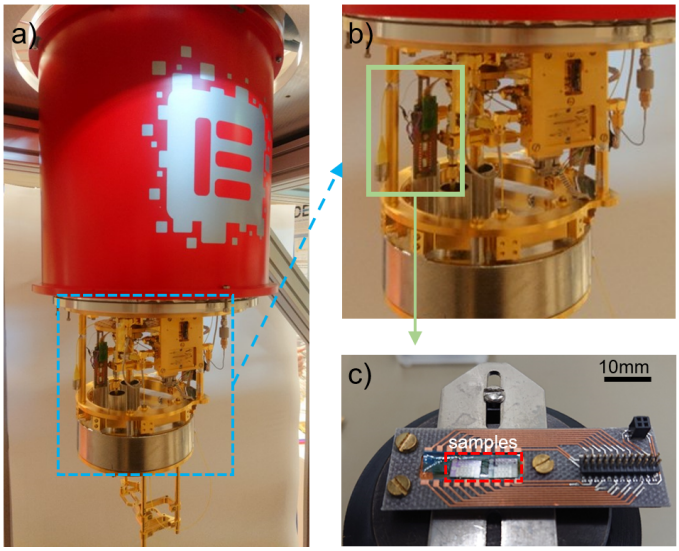



Figure 5.4: Adiabatic demagnetization refrigerator (ADR) at SRON a) full cryogenic system, b) zoom showing where the sample holder is placed and c) sample holder (Courtesy of SRON).

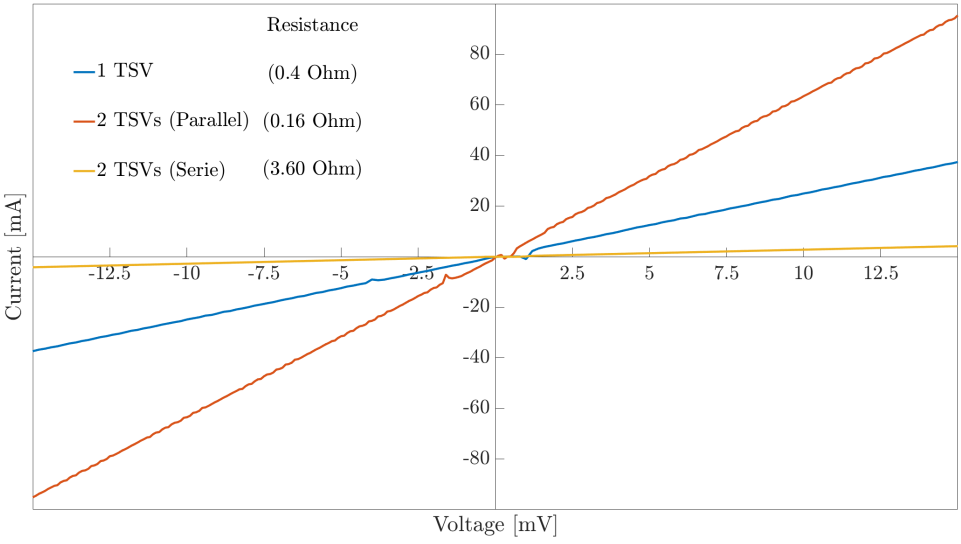



Figure 5.5: I-V curve of straight vias: single TSV, two TSVs measured in parallel and two TSVs measured in series. An ohmic behavior is observed for the investigated voltage range.

| Metal | Metal thickness (Nominal) [$\mu$m] | Deposition temperature [C] | Via Resistance [Ω] | Annealed | Via design |
|---|---|---|---|---|---|
| Nb | 4 | 25 | 13.31 ± 0.62 | No | Wineglass |
| Nb | 4 | 25 | 504.75 ± 1.11 | Yes (550°C) | Wineglass |
| Nb | 4 | 25 | 867.17 ± 2.15 | Yes (550°C) | Hourglass |
| NbN | 4 | 350 | 169.2 ± 1.33 | No | Wineglass |
| NbTi | 2 | 25 | 29.36 ± 1.04 | No | Wineglass |
| NbTi | 2 | 25 | 34.8 ± 1.79 | No | Hourglass |
| NbTiN | 1 | 25 | 100041.62 ± 5.91 | Yes(550°C) | Hourglass |

Table 5.1: Summary of the electrical measurements of Nb and NbTi TSVs

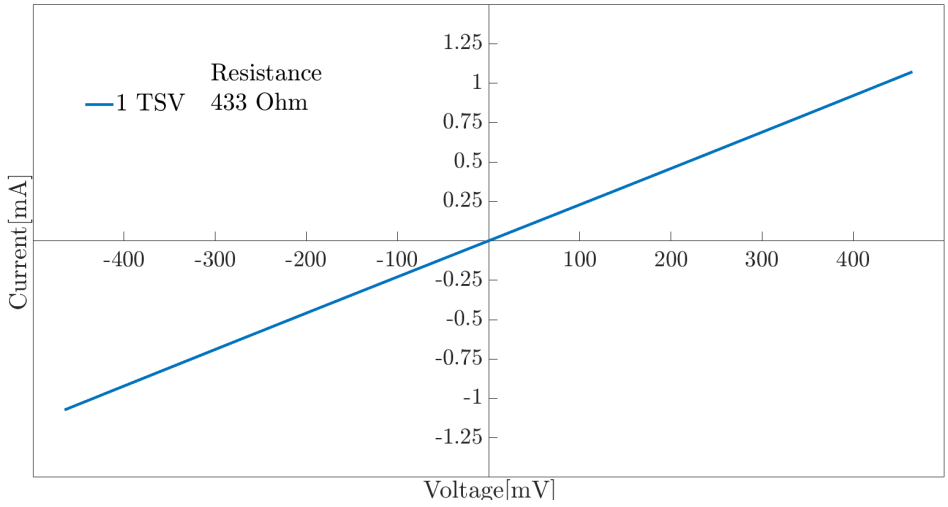



Figure 5.6: I-V characterization of a single Nb-coated TSV (Hourglass) at room temperature. An ohmic behavior is observed for the investigated voltage range

### 5.3.2. NIOBIUM AND NIOBIUM TITANIUM TSVS

Niobium (Nb) and Niobium Titanium (NbTi) TSVs were characterized using the test structures presented in Chapter 2 (Fig. 2.10 a) and 2.10 b)). The wineglass design was mostly used during the test. The vias had 50 $\mu$m diameter and were fabricated in a 300$\mu$m thick substrate. Several measurements were performed according to the different Nb metallizations presented in Chapter 4. Table. 5.1 summarizes the measurements of Nb, NbTi and some alloys. The lowest via resistance was achieve by using 4$\mu$m of pure Nb deposited at 25°C. Annealing at 550°C in argon (6 liters/min) for 20 minutes, did not improve the electrical resistance, possibly because the annealing was performed in a furnace without high vacuum. For NbTiN a higher resistance value compared to the other deposited metals was measured. It is also the thinnest metal thickness. It was annealed at 550°C (middle range temperature). The electrical resistance measured in a single hourglass via was as low as 433± 24 Ω (Fig. 5.6).

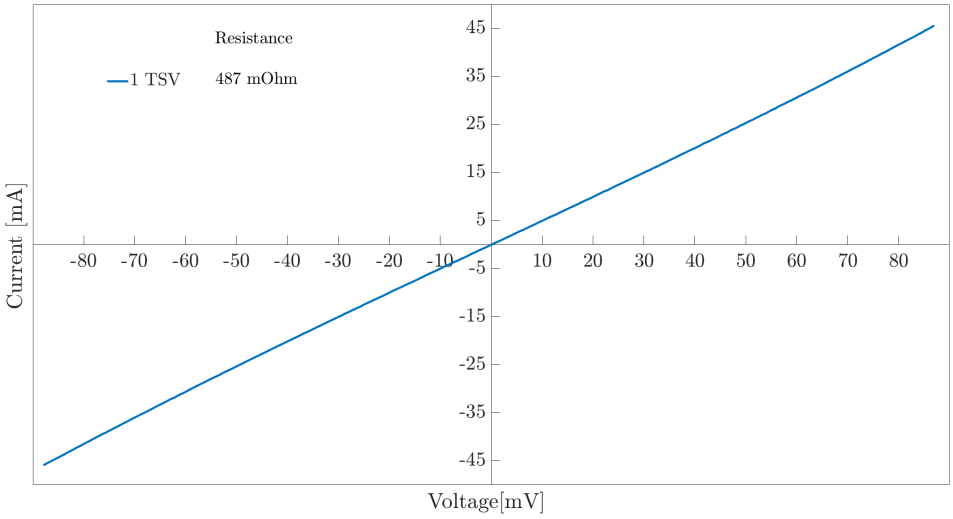



Figure 5.7: I-V characterization of a single Al-coated TSV at room temperature. An ohmic behavior is observed for the investigated voltage range



### 5.3.3. ALUMINIUM TSVS

Aluminum TSVs were electrically measured for all types of vias described in chapter 4. For all measured straight vias, with diameters from 30 $\mu$m to 100 $\mu$m and for substrate thicknesses of 200$\mu$m, 300$\mu$m and 525 $\mu$m, the electrical resistance values were in the range of MΩ to open circuit. The sputtered layer of Al did not reached the center of the via or the layer was possibly extremely thin or not continuous. Wine glass TSVs in 200, 300 and 500 $\mu$m-thick wafers were tested. The electrical resistance of a single via, located in the center of the cross-bridge Kelvin resistor structure, measured as low as 487± 68 mΩ. The ohmic behavior of one single wine glass TSV is shown in Fig. 5.7).

Hourglass vias of the same diameter but only for the 500 $\mu$m-thick wafers were tested. The single-via electrical resistance measured at room temperature was in the range of hundreds of mΩ for most of the TSVs (Fig. 5.8), with the lowest measured value of 160 mΩ. The measurements also evidenced the ohmic behavior of the TSVs, as shown in Fig. 5.9. The wafer-scale yield for the fabrication of electrically conductive TSVs was close to 90 percent (Fig. 5.10).

## 5.4. MEASUREMENT AT CRYOGENIC TEMPERATURE

During the cryogenic measurements the current was kept constant at 30 $\mu$A, and the temperature was repeatedly changed in cycles of upward and downward sweeps between 1.1 K and 1.6 K for Al and 1.1 K and 20 K for Nb/NbTi. The measurements were repeated over a period of several minutes and sometimes several days to check for stability, and to test deterioration over the time.

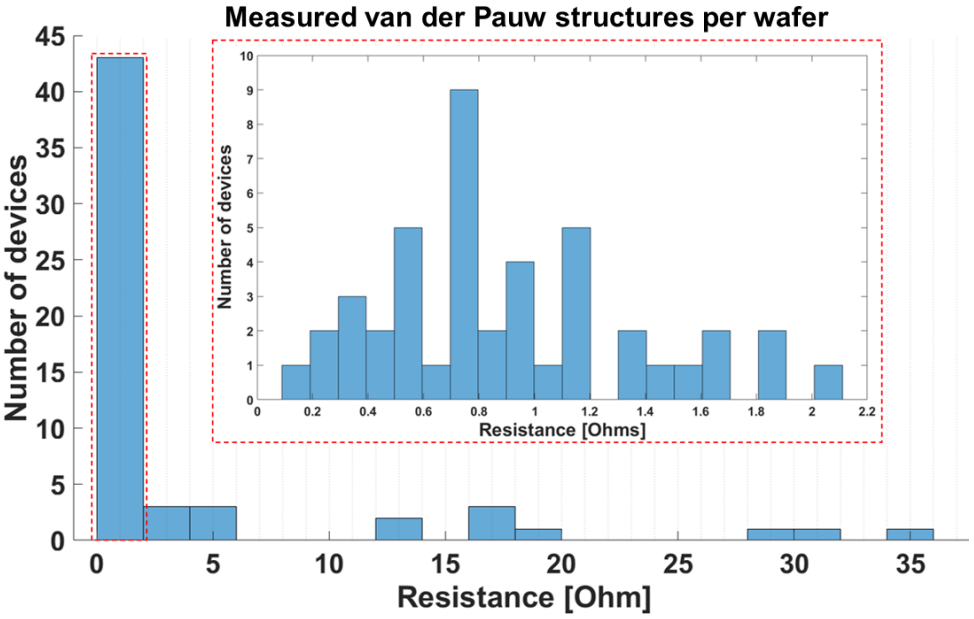



Figure 5.8: Distribution of room temperature electrical resistance values measured for single hourglass TSVs using the 3D Van der Pauw structures. Includes a sub-plot of the distribution between 0 and 2 Ohm.

### 5.4.1. NIOBIUM TSVS

In theory Nb can achieve superconductivity at a critical temperature of 9K, a relatively high temperature that is highly desirable as explained in chapter 4. Measurements were performed on planar structures (van der Pauw structures) of Nb layers deposited at different conditions. The parameters varied are argon and nitrogen flow, and deposition temperature. Table 5.2 shows the obtained results. All the configurations have a transition at the expected Tc (9K), however two of them were not able to reach the 0Ω.

The obtained results for the Nb vias are shown in Fig. 5.11. All the vias showed a suggestive transition, but they were not able to reach absolute superconductivity. As it is mentioned above the planar structures were superconducting, however the same type material deposited in the TSVs was not superconductive. This is possibly because the deposited layers close to the center of the via were not thick enough. Additionally, the cristallization of the sputtered materials in the center of the vias might not be optimal, probably because of the use of inadequate substrate temperature, gas flow, or pressure during the material deposition. The stoichiometry of the gases has a important role when nitrogen is used for the formation of matal-nitride layers, such as NbN or NbTIN. More research has to be done in this direction.

### 5.4.2. ALUMINUM TSVS

The results for wineglass vias are presented in Fig. 5.12. Two superconducting transitions are observed, one at around 1.25 K and the other at around 1.32 K. The sharper transition at around 1.36 K originates from the Al of the planar and funnel sections of the Kelvin

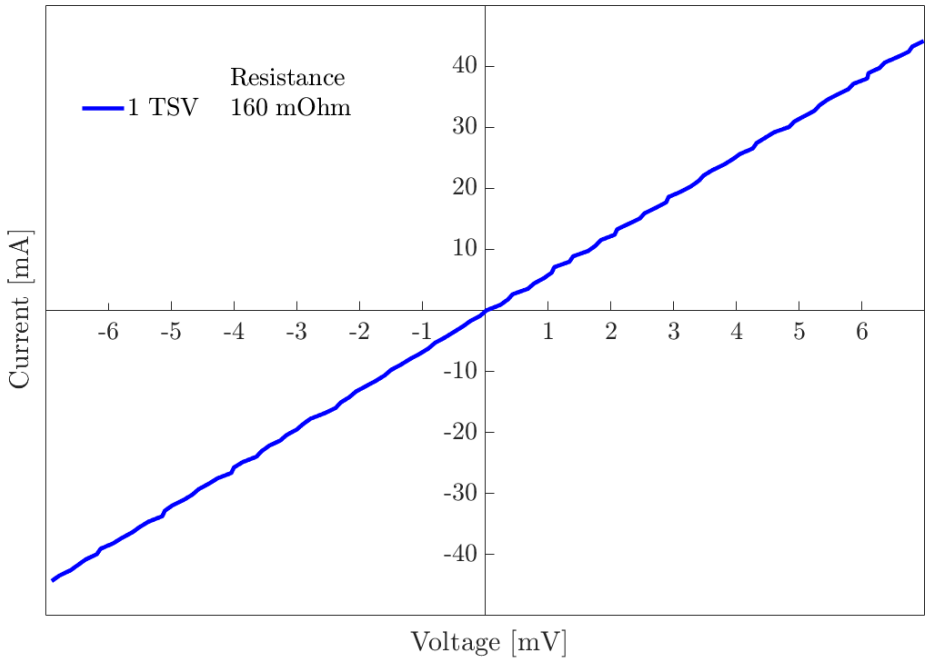



Figure 5.9: Ohmic behavior of a single Al-coated hourglass TSV evidenced by I-V characterization at room temperature. The measured electrical resistance is 160 mΩ.

| **Ar (sccm)** | **N (sccm)** | **Deposition temperature [C]** | **Resistance (Planar structure) [Ω]** | **Tc [K]** | **Superconductivity (0 )** |
|---|---|---|---|---|---|
| 150 | 5 | 25 | 0.3157 ± 0.0391 | 9.09 | No |
| 50 | 7 | 350 | 0.3169 ± 0.0546 | 9.17 | No |
| 150 | 7 | 350 | 0.3254 ± 0.0691 | 9.11 | Yes |
| 50 | 7 | 25 | 0.3767 ± 0.0532 | 8.69 | Yes |
| 150 | 5 | 350 | 0.3206 ± 0.0197 | 9.23 | Yes |
| 300 | 7 | 25 | 0.3713 ± 0.1247 | 8.91 | Yes |
| 150 | 7 | 25 | 0.3399 ± 0.0685 | 8.79 | Yes |

Table 5.2: Summary of the electrical measurements performed on Nb planar structures

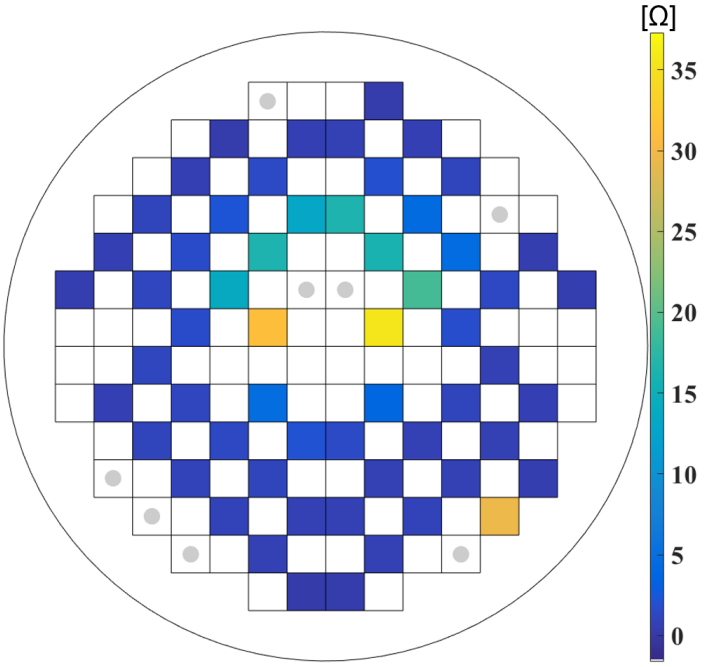



Figure 5.10: Wafer map showing the fabrication yield and color-coded single-via sheet resistance for 4-inch wafer-level TSVs. Grey dots indicate the locations of electrically non-conductive TSVs.

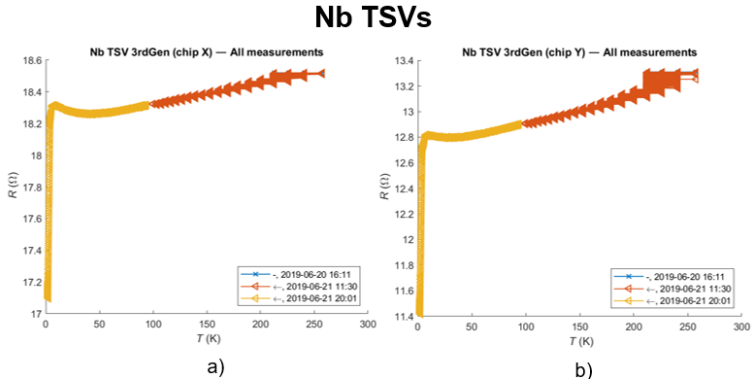



Figure 5.11: Superconductive transition for Nb TSVs(Wineglass)a) chip X and b) chip Y

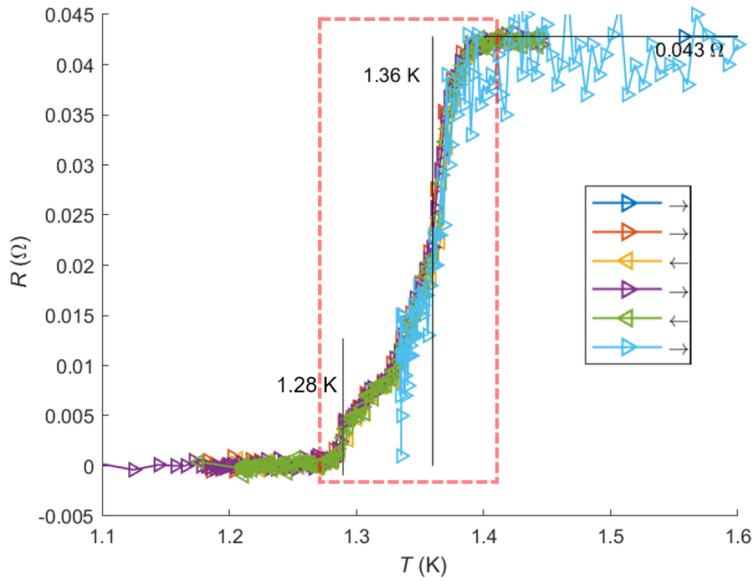



Figure 5.12: Superconductive transition measured for a single cross-bridge Kelvin structure with 300 $\mu$m-deep Al/TiN-coated TSVs. The overlapping curves represent consecutive upward (→) and downward (←) temperature sweeps, and confirm the repeatibility of the measurements.



resistor structure, where the sputtered Al film is thicker. The broader transition at 1.32 K is associated to the transition of the Al film in the via, where the film is thinner than in the funnels. This is consistent with prior reports, as the superconducting transition temperature of Al increases for thinner films with higher sheet resistance.

In hourglass vias a single, sharp and hysteresis-free Al superconducting transition was measured at 1.27 K (Fig. 5.13). We consider this result as conclusive proof of the quality and uniformity of the Al layer sputtered inside the hourglass TSVs. Since the ADR at our disposal could not measure I-V curves, we reserve to quantify the TSVs critical current in future work.

## 5.5. DISCUSSION

The TSV technology here successfully demonstrated shows promise for application as vertical interconnection technology for physical qubit layers and superconducting MEMS devices. The sharp superconductive transition proves the high purity of the sputtered materials and the quality of the poly-crystalline layer formed during the deposition over the TSVs side-walls. Without expectedly loosing signal quality or decreasing electrical performance, the TSVs can be densely packed, particularly when implemented in thin Si substrates. In this respect, we remark that the smallest pitch in closely-packed arrays of hourglass TSVs is bounded by the diameter of their access holes at the wafer surface; and that the latter is roughly proportional to the wafer thickness, as deeper TSVs require wider funnels to be properly coated by sputtering. As a result, the outer via diameter of hourglass TSVs can be downscaled to *e.g.* less than 100 $\mu$m for 300 $\mu$-thick wafers. Dense

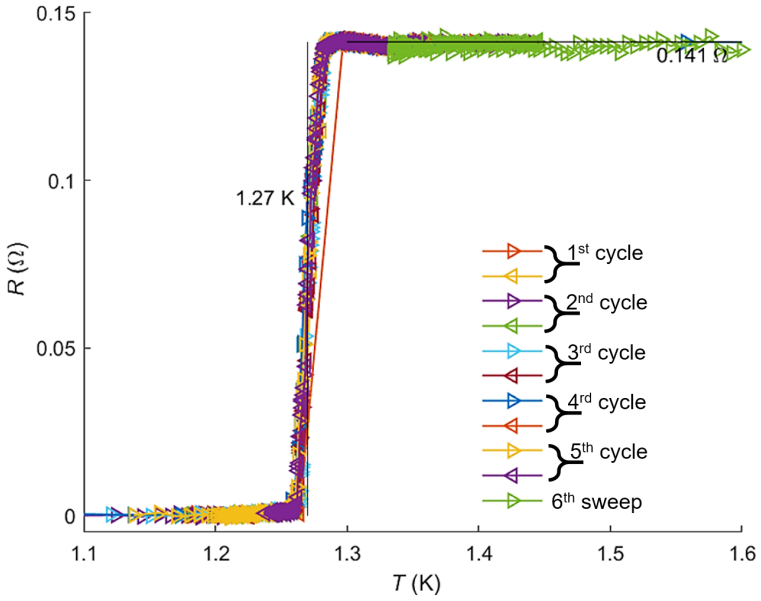



Figure 5.13: Superconductive transition measured for a single cross-bridge Kelvin structure with 500 $\mu$m-deep Al/TiN-coated TSVs. The overlapping curves represent consecutive upward (→) and downward (←) temperature sweeps, and confirm the high repeatibility of the measurements.

arrays of superconducting TSVs are especially relevant in 3D integration to reduce signal latency, dissipate power more efficiently, and address dense arrays of coherent qubits.

Some minor modifications in TSV design and implementation, such as a relaxation of the geometrical transition from the wafer surface to the funnel and sputtering of other types of materials, could suffice to enable applications in support of *e.g.* photodetectors and other superconducting astronomical instruments exploiting the THz range of the electromagnetic spectrum [5, 6].

## 5.6. CONCLUSION

Indium TSVs were completely filled by a dedicated tool designed to guarantee a uniform thickness. Two-terminal In-filled TSV-based structures were electrically characterized. A single via resistance of 0.40 Ω is measured for 300 $\mu$m deep TSV and 75$\mu$m in diameter. This type of vias is especially attractive for compact superconducting interconnects supporting quantum computing devices operating below 4 K. Highly conformal TSVs coated with Nb and NbTi for both wineglass and hourglass designs achieved an electrical resistance as low as 13 Ω. However, superconductivity was not achieved, more test are necessary to determine the reason. High conformality and superior uniformity of the Al coating of the vias obtained by means of the tailored hourglass sidewall profile in combination with low-pressure DC-sputtering of Al was confirmed by a remarkably sharp superconducting transition measured at 1.27 K.

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# 6

# CONCLUSIONS AND RECOMMENDATIONS

## 6.1. CONCLUSIONS

The successful implementation of a quantum computer sufficiently powerful to be at least of practical use if not capable of unprecedented performance, depends on the amount of physical qubits that can be located in an small chip area. Space as a limiting factor is not new for IC and MEMS, where 3D integration has been explored and implemented as possible solution. Increasing demand of large-scale and high-density silicon-based quantum computing systems is pushing the development of 3D interconnect technologies to adapt to new and challenging requirements. The use of 3D interconnections with superconducting materials is one posible path to solve the space problem for qubits, and the one that was choosen in this thesis.

Three different types of TSVs to achieve superconducting interconnects were presented: Straight sidewall TSVs filled with indium by VALM and, funelled TSVs (Wineglass and Hourglass) coated with aluminium and niobium(Fig. 6.1a-c).

Indium HAR TSVs offer a good solution for a simple interconnection. The novel filling method, named Vacuum Assisted Liquified Metal has been applied to fill void-free TSVs in only 10 minutes irrespectively of vias depth. The TSVs filling yield is close to 90 percent for all diameter vias tested. Moreover, filling of high density TSVs is not an issue for this method, though via surface density is inherently restricted by the DRIE process. Indium patterning is challenged by the non-uniformity of the blade coated In layer at the wafer surface. A dedicated tool designed to guarantee a uniform thickness of the molten layer is currently under construction.

To facilitate the penetration of the plasma within the TSVs during the sputtering process, a funneled TSV profile in the shape of a wineglass and hourglass were introduced. By means of this technologies superconductive Al-sputtered TSVs were achieved. However, for wineglass vias single and sharp superconducting transition could not be observed. Non-uniformities in thickness of the sputtered Al layer across the wineglass

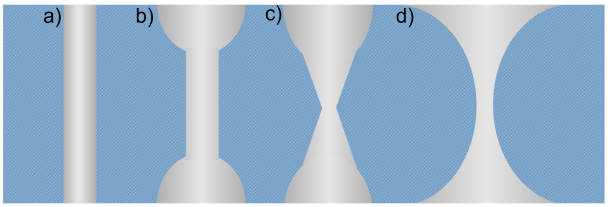



Figure 6.1: Sketch illustrating the different shapes of TSVs: a) straight, b) wineglass, c) hourglass and d) smooth transition(proposed for application in the terahertz domain).

sidewalls could be the cause. As indication of this, via sections with differing metal thicknesses were associated with multiple differing transition temperatures. Specifically, the Al layer was systematically thicker at the junction of the planar and funnel sections than in the cylindrical section of the vias. To reduce the unevenness of sputtered metal thickness between top and middle sections of the TSVs, a novel TSV sidewall profile (Hourglass via) was tested. TSVs with relatively wider access holes and smoother and elongated transition towards the center of the via were fabricated. A single, sharp and hysteresis free Al superconducting transition was measured at 1.27 K. This result was considered as conclusive proof of the quality and uniformity of the Al layer sputtered inside the hourglass TSV. Test with Nb, NbN and NbTi were also performed. However, it was not possible to achieve a superconducting transition in wineglass or hourglass TSVs.



## 6.2. RECOMMENDATIONS

The results achieved in this thesis provided insights about the fabrication process, materials and possible implementation of an interposer suitable for potential architectures of solid-state quantum computers. There is nevertheless still a lot o space for improvement in the fabrication of the wineglass and hourglass TSVs, as it will be briefly elaborated in the following. During the DRIE etching the process is not a continuous process, the vias are fabricated in halves.

### NON-CONTINUOUS METALLIC LAYERS

It is advised to not make use of a transport wafer, this will never give equal results in non-continuous etching. In order to minimize the etching issues, the process should have a longer overlapping in the etching of the central part of the via, this will also help to have a smoother transition, which is also desirable. A wider via funnel with a smaller central part of the via is ideally the best approach for other type of applications, particularly in terahertz transmission lines. So that, the transition from one plane (horizontal) to the other (vertical) is minimized as much as possible. Figure 6.1 shows an illustration of the vias presented in this thesis and a possible design for high frequency applications.

This gives room to defects in the central part of the vias, if the etching is varied a bit in terms of gas flow or RF power or substrate temperature the defects are going to be more pronounced.

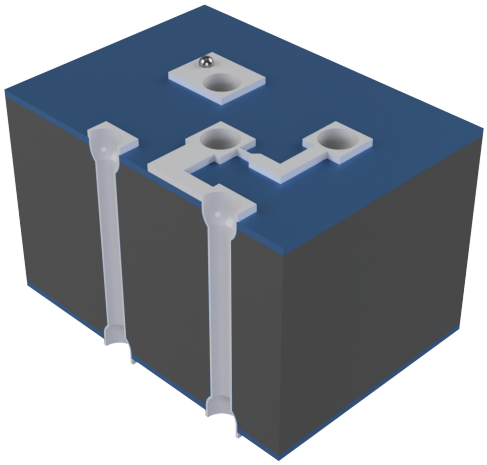


Figure 6.2: Sketch illustrating the metallic micro bump over the TSV bond pad for the 3D wafer stacking



### THERMAL BUDGET

In order to broaden the use of funneled TSVs in more applications for IC and MEMS, it is recommended to perform test in the tuning of the DRIE etching recipes. This to diminish as much as possible the scallops and avoid the consecutive use of thermal oxidation steps at high temperatures to remove the imperfections in the TSVs sidewalls.

### METAL DEPOSITION

It is advisable to investigate the use of more materials or deposition techniques such as atomic layer deposition. A broader comparison will give more information about the design and possible improvements. From the sputtering point of view, more tests are necessary. Parameters such as deposition angle and target-substrate proximity were not tested. Additionally, it is necessary to find a balance between the deposition rate and time required for the deposition. From the experience, lower deposition rates normally give better coverage.

### MICRO BUMPS AND BONDING

The implementation of micro bumps is an essential part of the design of the TSVs as interposer. They are necessary for the connection of quantum devices or qubits with the TSVs (and Cryo CMOS). The standard In bumps have a 150 $\mu$m to 200 $\mu$m pitch, the bond pads require at least the same size, this could be a limiting factor for the implementation of many qubits. It is recommended as a possible alternative, the use of spray-coating with negative resist and lift-off of evaporated indium to fabricate them with pitch ten times smaller. Figure 6.2 shows an sketch of where to place the micro bump for the 3D connection. The micro bumps can be as small as 5 $\mu$m if they are fabricated over the substrate.

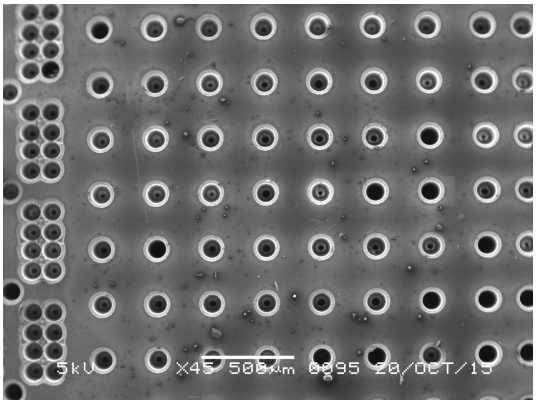



Figure 6.3: SEM image of TSVs coated with the polymer PPC. The coating clogs in the center in most of the TSVs.

### APPLICATIONS OF VALM

The use of VALM is not limited to Indium TSV filling only. Polymers, conductive nanoparticle pastes and other low-melting point metals can be used with this tool. As possible application the partial filling of TSVs with polymers such as Poly(vinyl Acetate) (PVA), Polypropylene carbonate (PPC) or Poly(acrylic acid) (PAA) as sacrificial layers. This polymers have the property of dissolving in water and resist at temperatures between 300 and 360 Celsius(PVA and PPC only). This means that the TSVs can be coated with PVA, then over the PVA performed the metallization. Once the the metal is patterned the layer of PVA can be dissolved in hot water, obtaining in this way TSVs with an air gap as dielectric. Preliminary work along this lines was conducted in this thesis, though with limited success (fig.6.3).

### METAL COMPOSITIONS

To further verify superconducting funneled TSVs using Nb as coating material, it is necessary to investigate sputtering parameters such as deposition rate, reacting gasses, substrate temperature and RF power. In addition, it is necessary to perform more analysis of the composition of the metallic microstructure by means of a TEM and XPS. This may help to clarify whether the composition of the material is different along the TSV (top , center and bottom parts), and to detect if there are additional impurities that may alter the Tc or preclude the possibility of achieving superconductivity with the TSVs.

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# LIST OF PUBLICATIONS

4. **J.A. Alfaro, M. Mastrangeli, D.J. Thoen, S. Visser, J. Bueno, J.J.A. Baselmans, P.M. Sarro.**, *Highly-Conformal Sputtered Through-Silicon Vias With Sharp Superconducting Transition*, IEEE Journal of Microelectromechanical Systems **30**, No. 2, p. 253 - 261 (2021).

3. **J.A. Alfaro, M. Mastrangeli, D.J. Thoen, S. Visser, J. Bueno, J.J.A. Baselmans, P.M. Sarro.**, *Superconducting High-Aspect Ratio Through-Silicon Vias With DC-Sputtered Al for Quantum 3D Integration*, IEEE Electron Device Letters **41**, No. 7, p. 1114 - 1117 (2020).

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