Characterization and Modeling of Self-Heating in Nanometer Bulk-CMOS at Cryogenic Temperatures

't Hart, P.A.; Babaie, M.; Vladimirescu, A.; Sebastiano, F.

Citation (APA)
't Hart, P. A., Babaie, M., Vladimirescu, A., & Sebastiano, F. (2021). Characterization and Modeling of Self-Heating in Nanometer Bulk-CMOS at Cryogenic Temperatures. *IEEE Journal of the Electron Devices Society*, *9*, 891-901. https://doi.org/10.1109/JEDS.2021.3116975

Important note
To cite this publication, please use the final published version (if applicable).
Please check the document version above.

Characterization and Modeling of Self-Heating in Nanometer Bulk-CMOS at Cryogenic Temperatures

P. A. 'T HART [1,2], **M. BABAIE** [1] **(Member, IEEE), A. VLADIMIRESCU** [1,2,3,4] **(Life Fellow, IEEE),
AND F. SEBASTIANO** [1,2] **(Senior Member, IEEE)**

1 QuTech, Delft University of Technology, 2628 CD Delft, The Netherlands
2 Department of Quantum and Computer Engineering, Delft University of Technology, 2628 CD Delft, The Netherlands
3 Department of Micro-Nano Electronics and Radio Communications, ISEP, 75006 Paris, France
4 Berkeley Wireless Research Center, UC Berkeley, Berkeley, CA 94708 USA

CORRESPONDING AUTHOR: P. A. 'T HART (e-mail: p.a.thart@tudelft.nl)

ABSTRACT This work presents a self-heating study of a 40-nm bulk-CMOS technology in the ambient temperature range from 300 K down to 4.2 K. A custom test chip was designed and fabricated for measuring both the temperature rise in the MOSFET channel and in the surrounding silicon substrate, using the gate resistance and silicon diodes as sensors, respectively. Since self-heating depends on factors such as device geometry and power density, the test structure characterized in this work was specifically designed to resemble actual devices used in cryogenic qubit control ICs. Severe self-heating was observed at deep-cryogenic ambient temperatures, resulting in a channel temperature rise exceeding 50 K and having an impact detectable at a distance of up to 30 μm from the device. By extracting the thermal resistance from measured data at different temperatures, it was shown that a simple model is able to accurately predict channel temperatures over the full ambient temperature range from deep-cryogenic to room temperature. The results and modeling presented in this work contribute towards the full self-heating-aware IC design-flow required for the reliable design and operation of cryo-CMOS circuits.

INDEX TERMS CMOS, cryogenic electronics, modeling, MOSFET, self-heating.

I. INTRODUCTION

Quantum computers have the potential to solve certain computational problems that would otherwise take a prohibitive long time to complete using classical computers. For proper operation, the quantum bits (qubits) –the basic unit of information in quantum computers– need to be cooled down to deep-cryogenic temperatures, around a few Kelvin in some cases [1] but typically below 100 mK [2]. Since state-of-the-art quantum computers comprise only a handful of qubits, each qubit can be individually wired to equipment placed at room temperature (RT) [3]. However, to be of any practical use, future quantum computers require thousands to even millions of physical qubits, making today's approach unworkable due to the need for thousands of cables going from the cryogenic qubits to the RT equipment. The

problems associated with scalability, manufacturability and reliability of these systems could be solved by placing integrated control electronics in close vicinity to the qubits, thus requiring electronic circuits operating at cryogenic temperatures. Such electronics are typically operated at liquid helium (LHe, 4.2 K) temperature, as commonly-adopted dilution refrigerators can offer significant cooling power ($\approx$ 1 W) [4] only at those temperatures.

The technology of choice for the cryogenic controller is nanometer CMOS, for its high speed, maturity, integration density and its potential to operate down to 30 mK [5], [6], all required for handling a large number of qubits.

It has been shown that core device parameters, such as threshold voltage, mobility, subthreshold slope, mismatch and leakage, can shift significantly from their RT values at
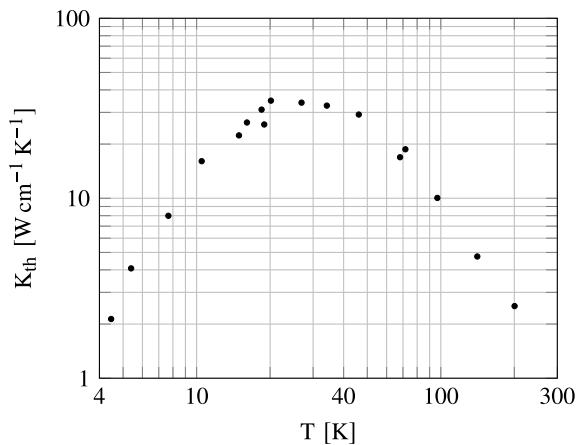
FIGURE 1. Thermal conductivity of silicon over temperature, replotted from [11].

low ambient temperatures (T_{amb}) [5], [7]–[10]. The incorporation of device temperature in compact models extended to the cryogenic environment is thus paramount to guarantee reliable circuit simulations and hence, robust circuit operation under these conditions. However, self-heating (SH) can raise the device temperature (T_{chan}) significantly above T_{amb}. This effect is amplified at cryogenic temperatures, as thermal properties of silicon, such as thermal conductivity (K_{th}), vary almost over 1.5 orders of magnitude in the temperature range from RT down to 4.2 K, as shown in Fig. 1. For instance, a recent cryo-CMOS microwave driver for spin qubits operating at $T_{amb} = 3$ K was subjected to SH exceeding 10 K for a dissipated power above 400 mW [12].

SH does not only impact the characteristics of the device itself, it can also propagate through the surrounding silicon forming thermal feedback loops with neighboring devices [13]. While this can be already critical in electronic cryogenic circuits, it will become crucial in future system-on-chip (SoC), integrating both electronics and qubits, which are extremely sensitive to any thermal crosstalk [1].

SH at RT has received much attention in literature, specifically focused on silicon-on-insulator (SOI) technologies as the buried oxide (BOX) poses a thermal impedance 2 orders of magnitude higher compared to that of bulk silicon at this temperature [11], [14].

Far less attention was devoted to studies on SH at cryogenic temperatures. Early work dates back to the beginning 1970s [15] and has been extended more recently by investigations on bulk MOSFETs [13], [15]–[18], resistors [19], [20] and SOI [21], [22]. SH was investigated both by measurements of the device temperature itself [20]–[22] and by placing temperature sensors in the vicinity of on-chip heaters [13], [19], [20], [23]–[25]. All these works show that SH is exacerbated at cryogenic temperatures and that the effect is highly dependent on device geometry (size, aspect ratio) and power density. This variability is clearly observed in recent cryo-CMOS integrated circuits for qubit interfacing, as SH ranged from 1 to 3 K in a 40-nm bulk-CMOS high-speed ADC with low power density [26] to more than 10 K

in a 22-nm FinFET microwave driver [12]. As device geometry and power density differ considerably between advanced bulk CMOS nodes and the previously studied mature technologies, it is necessary from a modeling perspective to characterize SH on devices better resembling those employed in practical cryo-CMOS designs [26]–[29], both in geometry and power density. Understanding the impact of SH is especially crucial for the cryo-CMOS low-noise amplifiers (LNA) necessary for the detection of the weak signals from quantum processors, as an increase of the device temperature of only a few Kelvin can strongly affect the noise performance, e.g., in a thermal-noise-limited amplifier in which the noise is directly proportional to the device temperature.

This paper bridges this gap by characterizing and modeling the effects of SH on the device itself and on the surrounding silicon, using a typical NMOS device.

It is found that SH can have a severe impact on both the device operating temperature and the temperature of the surrounding silicon at deep-cryogenic temperatures, and, that the former effect can be successfully predicted using a simple modeling approach.

This paper is structured as follows. Section II describes the test chip, measurement setup and the device calibration. Section III presents the measurement results, which are discussed and modeled in Section IV. Finally, conclusions are drawn in Section V.

II. TEST STRUCTURES AND MEASUREMENT SETUP

A test chip was taped-out, specifically designed for the characterization of SH at deep-cryogenic temperatures. The chip was manufactured in the TSMC 40-nm bulk-CMOS process. Fig. 2 and Fig. 3e show a simplified overview of the test structures and a die micrograph, respectively.

Three NMOS devices are employed as heaters (H1, H2 and H3), formed by a 5 fingered device with fingers measuring $W/L = 12$ μm/40 nm each, individually selectable (separated gates and drains) and able to dissipate ≈ 7 mW of power (P_H). The gates of the two MOSFETs separating H1 and H3 from H2 are connected to V_{SS} in order to electrically isolate the heaters from each other (Fig. 2 top). The center heater (H2) has additional connections available, enabling the measurement of the gate resistance, further discussed in Section II-A. The choice for NMOS over a PMOS device was motivated by its higher current driving capability (and thus power), as no significant thermal differences are expected between both types.

In addition to the MOSFETs, a linear array comprising 52 diodes, whose functionality was demonstrated in a previous experiment, is placed perpendicular to the channel, along a line through the center of the heaters (Fig. 2 top). These diodes act as temperature sensors, enabling the detection of the spatial thermal profile in the heaters' vicinity, further discussed in Section II-B.

A. GATE TEST STRUCTURE

To enable T_{chan} characterization through a range of T_{amb}, gate thermometry is employed, in which the calibrated
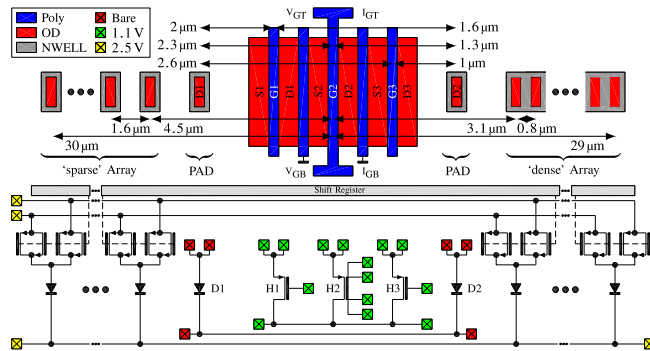
FIGURE 2. Simplified layout (top) and schematic overview (bottom) of the gate and diode test structures. H2 has Kelvin connections to its gate, comprising the V_{GT}, I_{GT}, V_{GB} and I_{GB} contacts. D1 and D2 are the two pad-accessible diodes (PAD). The different bond pad voltage domains are indicated. All digital blocks have been omitted for clarity.

FIGURE 3. Measurement setup: a) dipstick in LHe dewar; b) dipstick in climate chamber; c) PCB at the end of the dipstick; d) climate chamber internal view; e) die micrograph.

temperature dependence of the gate resistance (R_G, see Section II-D) is used as a temperature sensor [22], [30]. Kelvin connections to both top (V_{GT}, I_{GT}) and bottom (V_{GB}, I_{GB}) side of the H2 gate are therefore available to mitigate the impact of temperature dependence of back-end metals and parasitics on the resistance measurement (see Fig. 2).

The assumption was made that the gate and the channel are tightly thermally coupled, since only a thin ($< 3\,$nm) insulating layer separates them, similar to other works [18], [22], [30], [31]: $T_G \approx T_{chan}$.

B. DIODE TEST STRUCTURES

For the measurement of the thermal profile around the heaters, the substrate temperature is sensed by measuring the calibrated thermal dependency of the voltage drop (V_A) across P$^+$/NWELL silicon diodes operated at a constant current I_0. A graphical representation of this structure can be seen in Fig. 2, comprising pad-accessible diodes and a multiplexed diode array.

Pad-accessible diodes: Two diodes (D1 and D2 in Fig. 2) are placed in close vicinity to the heaters (one on each side), with connections directly available via bond pads, to measure the substrate temperature at small distances from the heaters with high spatial resolution (300 nm). Different combinations of heaters (H1/H2/H3) and diodes (D1/D2) allow for a total set of 6 distances: $d = \{1, 1.3, 1.6, 2, 2.3, 2.6\}\,\mu$m.

Because of the direct connection to the pads, these diodes have been used as benchmark to verify the correct operation of the pass gates in the multiplexed diode array.

Multiplexed diode array: A multiplexed array comprising 50 diodes to characterize the substrate temperature over larger distances, up to 30 μm from the heaters, enables automatic characterization. Thick-oxide pass gates were employed to allow the diode potential to rise above the nominal supply voltage (1.1 V), required as $V_A|_{I_0}$ increases with decreasing temperature.

An array was placed on both sides of the heaters. The 'dense' array (Fig. 2 top right) comprises diodes placed at the minimum allowed distance, resulting in a spatial resolution of
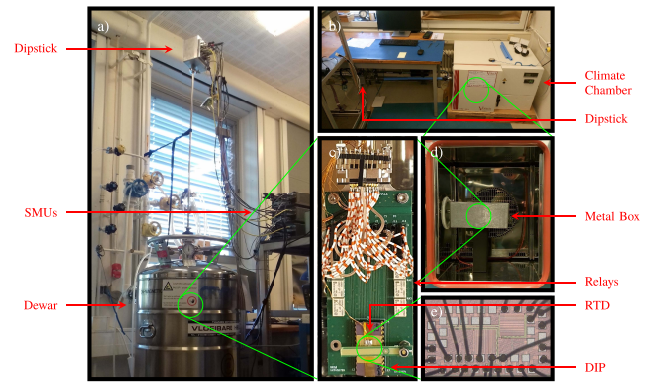
0.8 μm and is used for the actual measurements. The 'sparse' array (Fig. 2 top left) is a copy of the 'dense' array with every other device removed, resulting in less contact/metal density compared to the latter array. By comparing the results from the two arrays, it can be verified if the metal/contact density significantly impacts the thermal profile due to heat-leakage via the biasing metal lines.

C. MEASUREMENT SETUP

A photographic overview of the measurement setup can be seen in Fig. 3. The dies were glued and wire-bonded to ceramic DIP packages, which were fitted in a socket on a PCB mounted at the end of a dipstick (Fig. 3c). The PCB contains relays, enabling different configurations to be switched in and out during characterization. A Cernox type Resistance Temperature Detector (RTD) clamped to the package was used to measure T_{amb}.

Measurements at $T_{amb} \geq$ RT were carried out by inserting the end of the dipstick into a Vötsch VTM7004 climate chamber (Fig. 3b). The PCB inside the climate chamber was enclosed by a metal box to improve thermal stability, thus reducing temperature drift/gradients over time (Fig. 3d).

The dipstick was inserted into a dewar containing LHe for the cryogenic measurements (Fig. 3a). The height of the sample above the LHe level modulates T_{amb}.

Electrical characterization was carried out by 3 Keithley 2636B SMUs.

D. CALIBRATION

The temperature characteristics of both the gate resistor and the silicon diodes need to be calibrated before they can serve as temperature sensors. During calibration, the parameters of interest (R_G and $V_A|_{I_0}$) as a function of T_{amb} are characterized while T_{amb} is slowly varied with all heaters disabled.

For $T_{amb} \geq$ RT, the climate chamber is used to generate a slowly varying T_{amb}: after warming up to $\approx 350\,$K, the climate chamber is switched off and allowed to (slowly) cool down while calibration takes place. Cryogenic calibration was carried out by manually lowering the dipstick into the dewar, cooling down the sample.
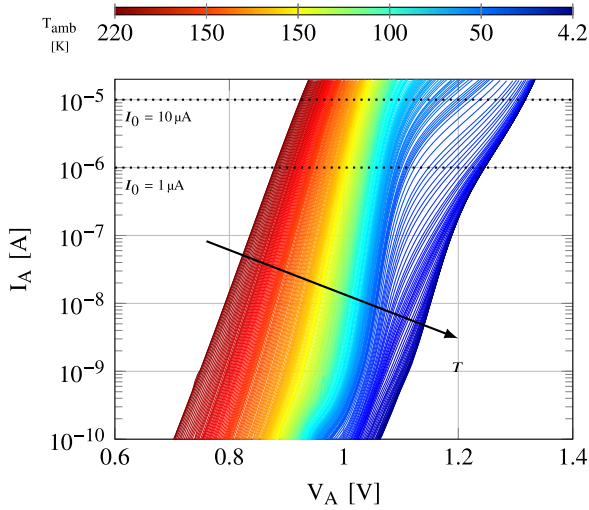
FIGURE 4. I_A-V_A curves of pad-accessible diode D1 at ambient temperatures (T_{amb}) ranging from 220 K down to 4.2 K. The two horizontal cuts along $I_A = I_0$, from which the calibration curves are extracted, are indicated.
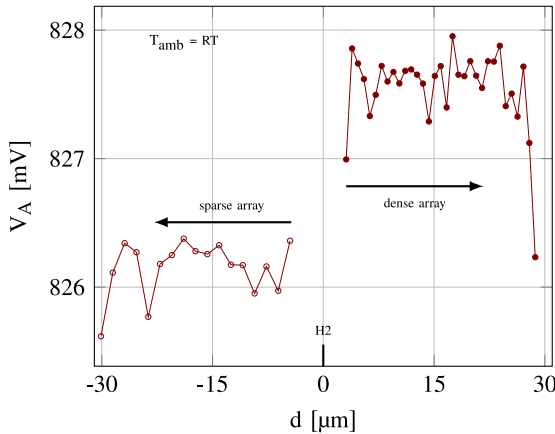

FIGURE 5. Voltage drop (V_A) measured at $I_0 = 10\,\mu$A for diodes in the 'dense' (filled dots) and 'sparse' (open dots) array operated at RT with $P_H = 0$ as a function of distance from center heater (d).
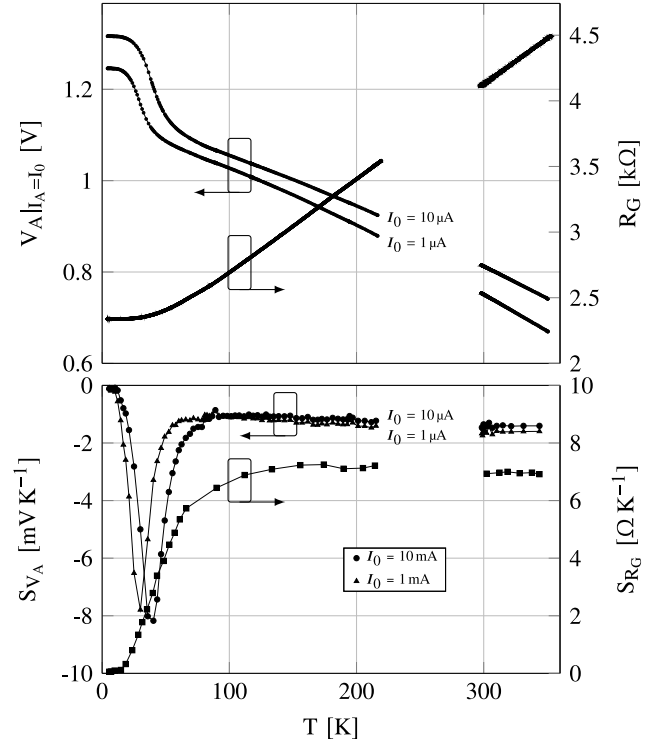

FIGURE 6. Calibration details. Top) calibration curves for the gate resistance (R_G) and the voltage drop across one of the pad-accessible diodes (V_A), the latter extracted at two different I_0 values, see also Fig. 4. Bottom) temperature sensitivity of the gate resistance (S_{R_G}) and diode voltage (S_{V_A}) as a function of temperature (T) extracted from the calibration curves. The gap between 220 K and 300 K results from limitations in the maximum and minimum attainable temperature of the LHe dewar and climate chamber, respectively.

Diode Calibration: For the 2 pad-accessible diodes, the I_A-V_A curves are measured as a function of T_{amb}. Deviation from ideal exponential behavior at cryogenic temperatures can be observed in Fig. 4. From these curves, V_A as a function of T_{amb} is subsequently extracted by a horizontal cut along the line $I_A = I_0$ as indicated in the figure. As recording the full I_A-V_A characteristics for all 50 diodes in the array would take a prohibitive amount of time, V_A is directly measured by forcing $I_A = I_0$ for these devices. Since there is some variability present among different diodes, all diodes need to be calibrated individually, see Fig. 5.

An example of a diode calibration curve and the resulting temperature sensitivity can be observed in Fig. 6 top and bottom, respectively. The minimum measurable channel temperature change ΔT_{min} was calculated as per [22] to be 0.05 K and 2 K at $T_{amb} = 50$ K and 11 K, respectively.

The de-facto standard value (for commercial diode temperature sensors) of $I_0 = 10\,\mu$A was used for $T_{amb} \geq$ RT. To increase the sensitivity at deep-cryogenic temperatures, the current bias was reduced to $I_0 = 1\,\mu$A for $T_{amb} < 300$ K. The temperature drift (T_{drift}) was monitored and the calibration was repeated in case of excessive values. The maximum T_{drift} during a single I_A-V_A characterization was 0.6 K ($T_{amb} \geq$ RT) and 1 K ($T_{amb} <$ RT).

Gate Calibration: R_G is measured by setting $V_{GB} = 0$ V and simultaneously sweeping V_{GT} from 0 to 50 mV, see Fig. 2, while recording the current through the gate (I_G). Note that V_D was left open to avoid any current and consequent heating in the device. R_G is extracted from the slope of a first-order fit of the I_G-V_{GT} characteristic. The full gate calibration curve can be observed in Fig. 6 top. The maximum T_{drift} during a single R_G characterization was 0.25 K ($T_{amb} \geq$ RT) and 0.4 K ($T_{amb} <$ RT).

The gap between 220 K and 300 K results from limitations in the minimum and maximum attainable temperature of the climate chamber and LHe dewar, respectively.

III. EXPERIMENTAL RESULTS

This section presents the measurement results, focusing on the experimental methods and discussing data validity.
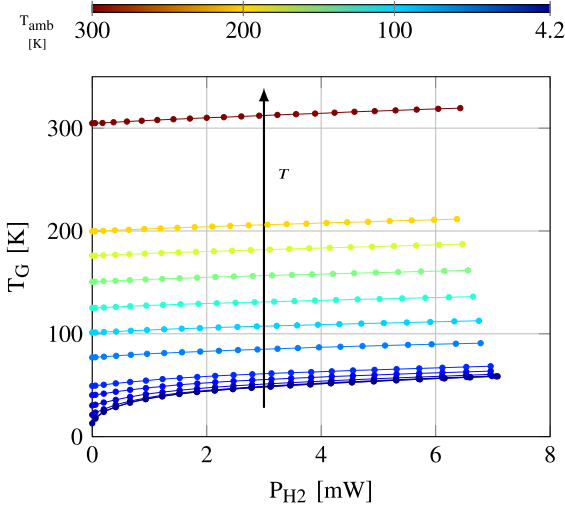
FIGURE 7. Absolute channel temperature (T_G) as a function of dissipated heater power (P_{H2}) at different ambient temperatures: T_{amb} = {4.2, 10, 20, 30, 40, 50, 75, 100, 125, 150, 175, 200, 300} K.

FIGURE 8. Channel self-heating (ΔT_G) as a function of dissipated heater power (P_{H2}) for different ambient temperatures (T_{amb}). Inset indicates interpolated SH at fixed heater power (P_{H2} = 6 mW, see dashed line) as a function of T_{amb}. Plot derived from data in Fig. 7.

In-depth analysis and discussion of the reported data is given in Section IV.

A. GATE-RESISTANCE MEASUREMENTS

In the first step of the T_{chan} characterization, the sample is brought to the target T_{amb} by placing it at a certain height above the LHe level, or for RT measurements, by keeping it inside the (switched-off) climate chamber. When T_{amb} stays within $\pm$ 0.2 K of the set point, thermalization is assumed and different power levels are dissipated in the center heater (P_{H2}) by stepping V_D in a staircase pattern: $V_D = \{0, 0.05, 0.1, \ldots, 1.1\}$ V, while V_{GB} and V_{GT} are both set to 1.1 V. Following each step in V_D, a 10 s delay was added to allow the structure to reach thermal equilibrium. V_{GT} is subsequently swept from 1.1 to 1.15 V, while both I_D and I_G are recorded. Finally, the routine described above is repeated for multiple T_{amb}.

R_G is extracted from the I_G-V_{GT} data as per the calibration routine described in Section II-D. The T_{chan} is inferred from these extracted R_G values by local Taylor-expansion of the calibration curve (Fig. 6 top) around that operating point.

As one side of the gate (V_{GT}) experiences a voltage change of 50 mV during measurement, I_D increases slightly. The dissipated power is therefore calculated using the mean I_D, $P_{H2} = V_D \cdot \bar{I}_D$, resulting in a maximum error of 2.5 % in power.

The absolute T_{chan} as a function of P_{H2} for different T_{amb} is plotted in Fig. 7. The channel self-heating, ΔT_{chan}, is derived from these data by subtracting the extracted temperature at $P_{H2} = 0$ for each T_{amb} from the corresponding curve, as shown in Fig. 8. As the temperature sensitivity of R_G drops to very low values for $T_{chan} < 11$K, the RTD temperature reading was used for compensation instead of $T_{chan}|_{P_{H2}=0}$ for these curves.

In order to protect against sudden temperature changes in the helium vapour (caused by varying pressure in the
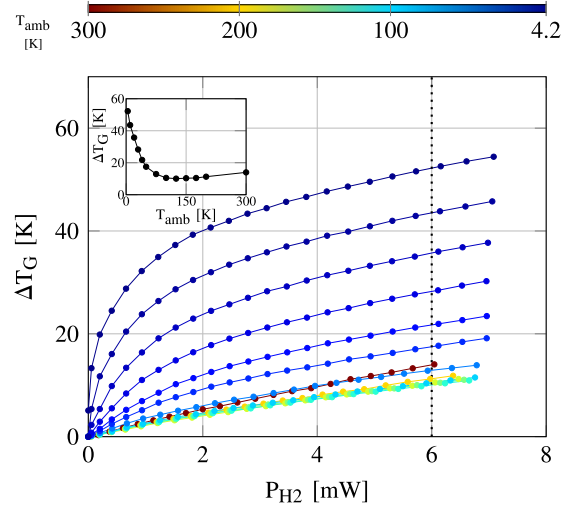
building's helium recovery system), the T_{amb} readings of the RTD are monitored: measurements are discarded when T_{drift} exceeds $\pm$ 0.5 K during a gate measurement at a single V_D set point. In addition, these readings are also cross-checked with the extracted $T_{chan}|_{P_{H2}=0}$ as an additional safeguard.

B. DIODE MEASUREMENTS

The diode characterization is very similar to that of the gate (Section III-A); however, apart from H2, in this case, H1 and H3 can additionally be used as heaters.

The characterization and analysis of the diode measurements can again be split into two groups:

Pad-accessible diodes: T_{amb}, power dissipation and thermalization are handled as per the gate measurements. For each V_D set point, V_A is swept while I_A and I_D are recorded. These data are collected for all 6 combinations of H1, H2 or H3 with D1 or D2 over all T_{amb} targets. From the I_A-V_A data, $V_A|_{I_A=I_0}$ is extracted in the same manner as during diode calibration and the diode temperature (T_D) is inferred with the use of the individual diode calibration curves (Fig. 6 top).

The absolute T_D for T_{amb} = RT and 4.2 K as a function of the enabled heater and the heater power can be seen in Fig. 9.

Finally, the substrate heating (Fig. 10) is calculated by compensating each absolute temperature curve in Fig. 9 with the corresponding temperature extracted at $P_{Hn} = 0$, identical to the procedure followed in the channel SH analysis, while for $T_{amb} < 10$ K the temperature reading of the RTD was used.

Multiplexed diode array: The measurement and analysis of the diode array follow the same routine as the pad-accessible diodes described above; however, due to the large number of devices (50), resulting in an increased measurement time, some adaptions were implemented to mitigate long-term
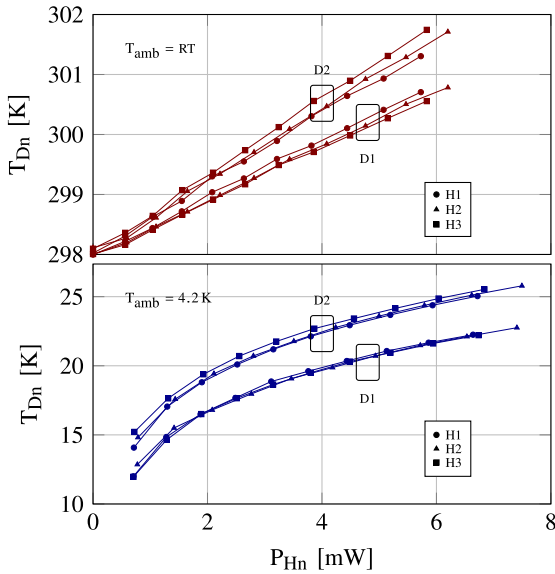
FIGURE 9. Absolute diode temperature (T_{Dn}) measured with all 6 heater/diode combinations as a function of heater power (P_{Hn}) at both T_{amb} = RT (top) and 4.2 K (bottom). At 4.2 K for P_{Hn} below 700 μW, readings are discarded due to limited temperature sensitivity, as explained in Section IV-A.
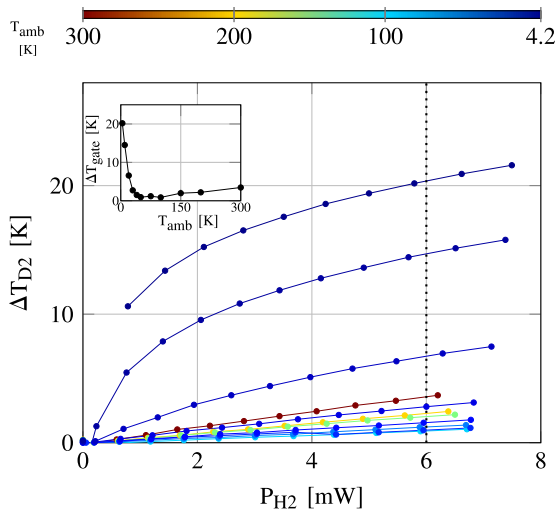

FIGURE 10. Diode temperature rise (ΔT_{D2}) of D2 as a function of heater power (P_{H2}) at different ambient temperatures: T_{amb} = {4.2, 10, 20, 30, 40, 50, 75, 100, 150, 200, 300} K. Inset indicates interpolated temperature rise at fixed heater power (P_{H2} = 6 mW, see dashed line) as a function of T_{amb}.

T_{drift}: since sub-μm resolution is not required, only H2 was enabled; V_A of each diode is directly measured by forcing $I_A = I_0$ and the number of V_D set points was reduced to the set V_D = {0, 0.1, 0.2, . . . , 1.1} V. With these measures in place, characterization of the full array still consumes a considerable amount of time, therefore T_{drift} needs to be taken into account.

Long-term temperature drift is only present for samples in helium vapour, caused by time-varying pressure in the building's helium recovery system.
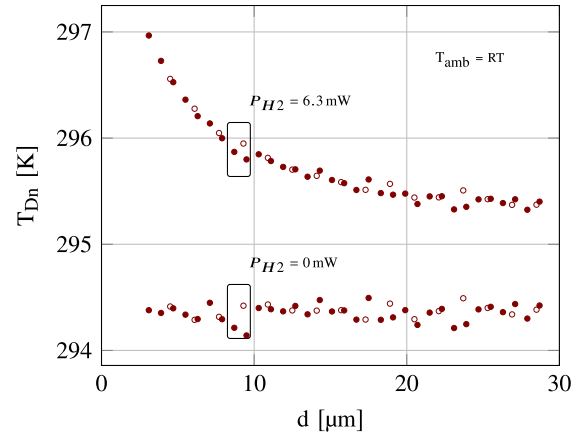

FIGURE 11. Substrate temperature measured by the diode arrays (T_{Dn}) as a function of distance from the center heater (d) at low (P_{H2} = 0) and high (P_{H2} = 6.3 mW) heater power at T_{amb} = RT. Data from the 'dense' (filled dots) and 'sparse' (open dots) arrays have been overlaid.

To further minimize T_{drift} impact, each diode in an array is fully characterized over all V_D set points (power levels), before switching to adjacent devices. During characterization of a single diode, T_{drift} is assumed to be small (comparable to that of the pad-accessible diodes) as the characterization time is relatively short: $\approx$ 115 s. However, there is still a long-term T_{drift} present between diode measurements, since a full array characterization takes $\approx$ 97 min. Therefore, the same compensation employed in the channel and pad-accessible diode characterization is applied here, which in this case, additionally auto-zeros the drift component between individual diode measurements.

The long-term drift is assumed to be small enough to maintain T_{amb}, however, large enough to distort the SH measurement, the effect of which is dependent on the height above the LHe. During the full array characterization, the RTD readings are therefore used to guard against too large short- and long-term T_{drift}. The allowed short-term drift (during single-diode measurements) is as per the pad-accessible diode characterization, while the long-term drift must stay within $\pm$0.5 K of the target T_{amb} for the data not to be discarded.

Extracted absolute substrate temperatures as a function of distance for P_{H2} = 0 and P_{H2} = 6.3 mW measured at T_{amb} = RT are plotted in Fig. 11.

Substrate heating as a function of distance at P_{H2} = 6 mW measured at different T_{amb} can be observed in Fig. 12. The corresponding measured temperatures of the pad-accessible diodes and the channel have been added to the figure.

The temperature profiles associated with different heater powers at a fixed T_{amb} = 160 K are plotted in Fig. 13, exemplifying the effect of T_{drift} on a single diode measurement.

IV. SELF-HEATING: DISCUSSION, MODELING AND TAKE-AWAYS
A. DIODE-BASED TEMPERATURE SENSING
Deviation from exponential behavior in cryogenically operated diodes shown in Fig. 4, are compatible with previous
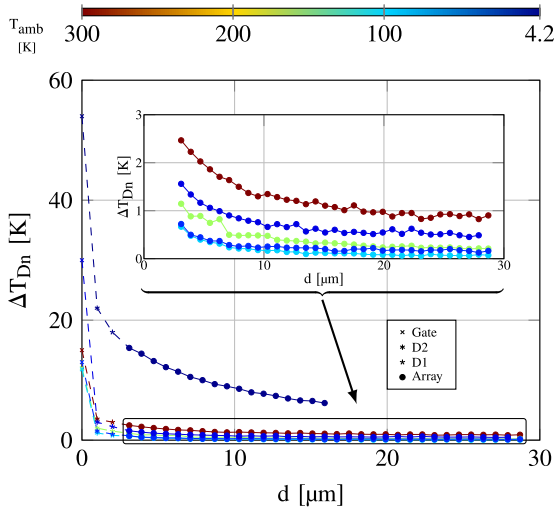
FIGURE 12. Substrate heating (ΔT_{Dn}) measured by the 'dense' array as a function of distance from the center heater (*d*) at high heater power (P_{H2} = 6.3 mW) and different ambient temperatures: T_{amb} = {4.2, 30, 50, 100, 160, 300} K. Data from the gate and pad-accessible diode structures are also plotted. The inset indicates a zoomed-in plot of the diode array measurements with the 4.2 K curve omitted for increased visibility.
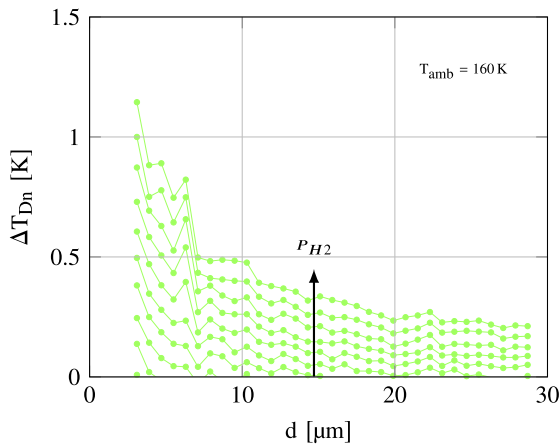

FIGURE 13. Substrate heating measured by the 'dense' array (ΔT_{Dn}) as a function of distance to the center heater (*d*) at different heater power levels: P_{H2} = {0.6, 1.2, 1.7, 2.3, 3.0, 3.6, 4.3, 5.0, 5.8, 6.6} mW. T_{amb} = 160 K. Only curves corresponding to P_{H2} values causing significant heating are plotted. T_{amb} was selected for clearly showing the effects of T_{drift}, similar curves were found at other T_{amb}.

observations in literature [32], [33]. The sharp V_A increase for $T_{amb} < 50$ K can be attributed to carrier freeze-out [33]–[35], also present in diodes specifically designed for cryogenic temperature sensing [36].

Consistently and significantly lower $V_A|_{I_0=const}$ were found for diodes in the 'sparse' array compared to the 'dense' array as indicated in Fig. 5. Most likely these differences can be ascribed to a combination of two effects: 1) diodes in the 'dense' array lie in a single continuous NWELL, while each 'sparse' diode sits in its own well. This causes differences in doping densities, and subsequent electrical characteristics, through the Well Proximity Effect (WPE) [37]. 2) the different Shallow Trench Isolation (STI) widths between diodes

in the two arrays cause different mechanical stress to be present, altering the carrier transport parameters through the piezo-junction effect [38].

The calibration curves of V_A and R_G in Fig. 6 show a near-constant temperature sensitivity of -1.2 mV/K and 0.18 %/K for $T_{amb} > 50$ K, respectively. Freeze-out causes a large increase in V_A sensitivity below this temperature, however, sensitivity drops to a very low value for $T_{amb} < 10$ K, compatible with measurements in [35]. I_0 was reduced to 1 μA during cryogenic measurements to mitigate the latter effect [32], the value being a trade-off between improved sensitivity and increased impact of array leakage at deep-cryogenic temperatures [39]. The temperature sensitivity of R_G decreases to a value close to zero for $T_{amb} < 11$ K, in-line with metal-like behavior [40]. For $T_{amb} > 50$ K, carrier transport is limited by phonon scattering, exhibiting a positive temperature coefficient (PTC), while below this temperature transport becomes increasingly limited by impurity scattering, which being temperature independent, prevents further resistance decrease.

Due to the diminishing temperature sensitivity of both the diodes and gate resistance, the reading of T_D and T_G have been excluded for temperatures below 10 K and 11 K, respectively. However, due to the rapid temperature increase to values above 10 K already at low P_H for $T_{amb} = 4.2$ K, this results in the loss of only a small part of the data (see Figs. 7 and 9).

SH due to biasing of the temperature sensors (inducing a power dissipation below 8 μW) is insignificant for the range of interest ($P_H > 1$ mW), as it has been simulated in COMSOL to cause a SH below 20 mK in the diodes.

B. CHANNEL TEMPERATURE SENSING

From the T_{chan} measurements in Fig. 7, an agreement between the RTD temperature reading and extracted $T_{chan}|_{P_{H2}=0}$ was found, indicating the correct operation of the setup through the full temperature range. Larger SH at equal P_{H2} can be observed for lower temperatures in Fig. 8: $\Delta T_{chan} \approx 14$ K (RT) vs $\Delta T_{chan} \approx 52$ K (4.2 K) at $P_{H2} = 6$ mW. For $T_{amb} < 100$ K, ΔT_{chan} is highly non-linear with respect to dissipated power, resulting in large SH for low P_{H2} in this temperature range, also observed by [18] and [24]. As shown in the inset of Fig. 8, the SH behavior from RT down to 4.2 K for a given P_{H2} shows a decrease down to 125 K, below which its effect starts to increase again, exhibiting a dramatic increase below $T_{amb} = 75$ K. This behavior hints to a temperature-dependent R_{th}, with a minimum at ≈ 100 K, also shown in other works [20], [24]. Previously reported values of the minimum lie between 77 K and 250 K and have been attributed to the impact of parasitic R_{th} (package, glue, etc.) dominating at these low temperatures in bulk CMOS [20]. Although the adopted test setup does not exactly reproduce prior work's experimental conditions, e.g., the chips are in direct contact of gaseous/liquid Helium unlike the vacuum environment used in [20], the shift in the minimum from the expected value is attributed

to the parasitic thermal resistance of the measurement setup. A more precise estimation of the effect of R_{th} may require additional experimental effort and its outside the scope of this work. The crowding of T_{chan} between 40 K and 60 K for deep-cryogenic temperatures, visible in Fig. 7 for heating power above 1 mW, is a direct consequence of this R_{th} behavior: below the R_{th} minimum, R_{th} has a negative temperature coefficient (NTC), which impedes SH more and more as T_{chan} approaches the minimum. The implications of this observed effect are further discussed in Section IV-E.

Comparing the SH magnitude extracted in this work with literature, much higher SH was found in SOI technology at comparable power densities [22]. As the main R_{th} in such technology is determined by SiO_2, which exceeds that of Si by ≈ 2 orders of magnitude, a large difference in SH is expected. Regarding bulk technology, in which no BOX exists, the geometry and area of MOSFET devices significantly impact SH. Far lower SH was observed in a large square heater in bulk technology [20], which has significantly more enclosing area and hence a much lower R_{th} to the surrounding silicon compared to the wide/short devices measured in this work. Also, the power density is orders of magnitude less compared to that in this work. The values published on a bulk device with an aspect ratio better resembling the structures characterized in this work, but with much larger W and L, show a slightly smaller SH effect. The structure in question had $\approx 100\times$ larger area [13] and considerably lower power densities. The preliminary work done by [18] shows values that compare very well with the measurements presented here, although no geometrical details are given.

These results stress the importance of geometry on SH, which is why in this work a transistor geometry comparable to the ones employed in practical cryo-CMOS circuits was chosen.

C. SPATIAL THERMAL MEASUREMENTS

Observations in line with the previous two sections can be made for the pad-accessible diodes. Both diodes show a smaller ΔT_D compared to the ΔT_{chan} at identical conditions, as the effect of heating falls off rapidly with a $1/d^n$-law (with d the distance to the heater and n a factor between 1 and 2): at $T_{amb} = 4.2$ K, 30 K less ΔT_D was measured 1 μm from the heater compared to ΔT_{chan} itself, see Figs. 9 and 10. Again, larger ΔT_D at cryogenic temperatures compared to RT was observed: $\Delta T_D \approx 3.5$ K (RT) vs $\Delta T_{diode} \approx 21$ K (4.2 K) at $P_H = 6$ mW, measured at 1 μm from the heater.

All 6 diode/heater combinations are distinguishable at both RT and 4.2 K in Fig. 9, with $T_{D2} > T_{D1}$, as D2 is closer to the heater than D1. The ΔT_D as a function of the enabled heater is flipped between D1 and D2, reflecting the mirror symmetry of the structure (see Fig. 2 top).

In Fig. 10, a similar behavior as in the T_{chan} measurements can be observed in the pad-accessible diodes below 30 K. The inset clearly shows the same behavior: a decreasing ΔT_D with decreasing T_{amb} with a minimum at ≈ 100 K, which compares well with the channel measurement.

Additional cryogenic effects were observed in the heaters, see Fig. 9. At $T_{amb} = 4.2$ K, the power in H1-H3 increases by 17 % to 20 % at equal bias conditions compared to RT, attributed to the improved mobility, resulting in an increased I_D and P_H. At equal T_{amb}, H2 was able to dissipate consistently more power compared to H1 and H3. H2 is effectively shielded from STI stress by adjacent devices (H1 and H3), which alters carrier transport parameters (and thus I_D and P_H) through the piezo-resistive effect [38].

Another interesting observation on the SH structure is the heat propagation from the heaters to the 'dense' and 'sparse' diode arrays. As seen in Fig. 11, there is good agreement between the T_D in both arrays, indicating no significant effects of metal/STI density on the thermal transport for these measurements, as was described in Section II-B. The readings at $P_{H2} = 0$ correlate well with the RTD readings and an agreement within ± 0.25 K between both 'dense' and 'sparse' diodes was found at both low and high P_{H2}; the latter indicates a stable T_{amb} and a successful calibration. The temperature mismatch between the two arrays is mainly due to the large time span between individual measurements, as each array is fully characterized before switching to the other. Compatibility of the array data with both channel and pad-accessible diode measurements can be seen, the shape corresponding to simulations shown by [20].

The substrate ΔT falls off with the distance d from the heater for all measured T_{amb}, following a similar shape to ΔT measured at RT, see Fig. 12. At $T_{amb} = 4.2$ K, the observable d range is limited as the substrate temperature drops below 10 K for $d > 15$ μm, as discussed previously. The ΔT_D evolution over T_{amb} matches the pad-accessible diode data, e.g., a minimum at ≈ 100 K. At $T_{amb} = 4.2$ K severe substrate heating was observed, as much as 7 K, measured 15 μm from the heater dissipating $P_{H2} = 6.5$ mW.

Substrate heating at $T_{amb} = 160$ K as a function of P_{H2} (Fig. 13) uncovers detectable substrate heating 30 μm from the heater at $P_{H2} > 3.6$ mW, while negligible heating is observed at $P_{H2} \leq 0.6$ mW. A 0.1 K short-term T_{drift} is visible, impacting the diode measurement at $d = 6.3$ μm.

D. ULTRA-WIDE-TEMPERATURE SELF-HEATING MODEL

In order to make the IC design work-flow cryo-SH aware, SH was modeled via a similar approach as in [22], but for bulk CMOS. First, the differential thermal resistance ($R_{th}^* = d\Delta T_{chan}/dP_H$) has been calculated from data in Fig. 8, and plotted as a function of absolute channel temperature ($T_{chan} = T_{amb} + \Delta T_{chan}$) in Fig. 14. The extracted R_{th}^* at $T_{amb} < 50$ K partially overlap, proving the validity of the measured channel SH. Since SH in bulk is far less pronounced compared to SOI, and even less at higher temperatures, the T_{chan} range for $T_{amb} > 50$ K is limited and gaps appear in the R_{th}^* curve. The previously discussed minimum and rapid increase in SH at deep-cryogenic temperatures are also reflected in this curve. The shape of the R_{th}^* curve, and in particular the deviation from the expected R_{th}^* valley around 40 K, is compatible with the one shown in [20]. This
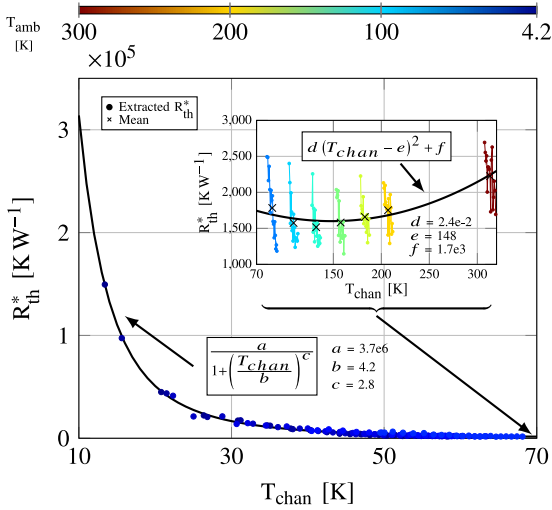
FIGURE 14. Extracted differential thermal resistance (R_{th}^*) as a function of channel temperature (T_{chan}) derived from data shown in Fig. 7. Data from different ambient temperatures (T_{amb}) are indicated by colors. The inset shows the extracted data at $T_{chan} > 75$ K for visibility. Fitting parameter values are indicated in the figure.

curve illustrates that a single function is able to describe the complete R_{th}^* behavior of this structure over the full temperature range from RT down to 4.2 K, and can thus be employed to model SH over P_H and T_{amb}. As the data at deep-cryogenic temperatures are similarly shaped to those in [22], but deviates at higher temperatures (containing a minimum, not monotonically decreasing), R_{th}^* was split into two regions, only to aid fitting. For $T_{chan} \leq 70$ K Eq. (1) [22] was used:

$$R_{th}^* = \frac{R_{th0}^*}{1 + (\frac{T}{T_0})^n}, \tag{1}$$

where R_{th}^*, n and T_0 are fitting parameters, the first being geometry dependent whose modeling is beyond the scope of this work. For $T_{chan} > 70$ K a simple parabolic function was fitted to the data to capture the minimum and the PTC behavior, both shown in Fig. 14. Finally, these two fitted functions and Eq. (2) [22] were used to predict SH as a function of T_{amb} and P_H.

$$P = \int_0^{\Delta T} \frac{d\Delta T'}{R_{th}^*(T_{amb} + \Delta T')}. \tag{2}$$

The resulting models for various T_{amb} are plotted in Fig. 15. These plots show that the very simple Eq. (2) is capable of successfully predicting SH over the full T_{amb} range from 4.2 K up to RT, including both the linear and square-root-like behavior, with < 3 K error in the 0 to 7 mW P_H range.

E. SH IMPACT ON CRYO-CMOS CIRCUITS
While the cryo-SH data and modeling presented above could enable the next steps in reliable cryo-CMOS design, conclusions on the impact of circuit behavior can already be drawn. Although SH is indeed severe for T_{amb} below 50 K
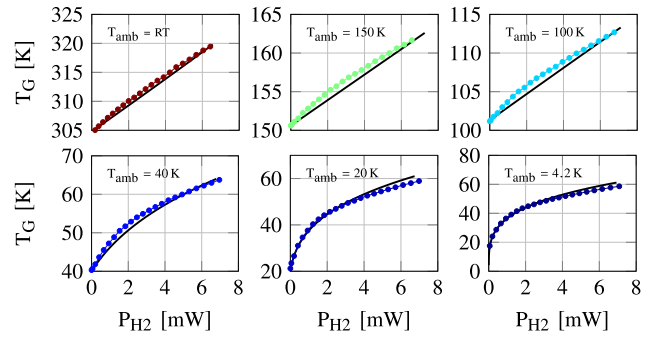

FIGURE 15. Absolute gate temperature (T_G) as a function of heater power (P_{H2}) at different ambient temperatures (T_{amb}). Model prediction (solid lines) vs measured data (dotted lines). Note: y-axes not equally scaled.
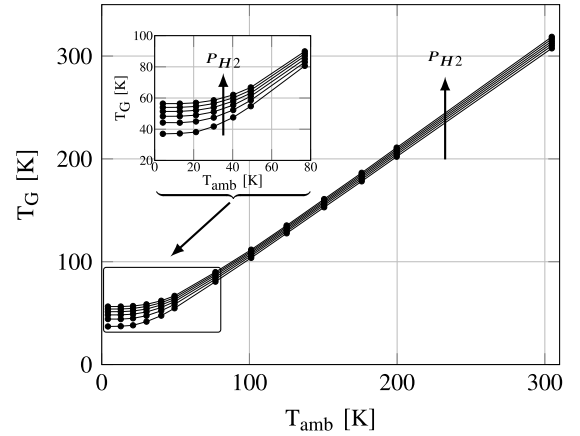

FIGURE 16. Gate temperature (T_G) as a function of ambient temperature (T_{amb}) for different H2 power levels: $P_{H2} = \{1, 2, \ldots, 6\}$ mW. These data are interpolations based on data shown in Fig. 7. A zoomed-in plot of the saturation region is shown in the inset.

(see Fig. 8), T_{chan} will not exceed an absolute temperature above 60 K even for a dissipated power of a few mW's, due to the minimum in the thermal resistance, as clearly highlighted by replotting the data from Fig. 7 in Fig. 16. Since the key transistor parameters, such as threshold voltage, current factor and subthreshold slope, as well as passive-device characteristics, such as R_G (see Fig. 6), show little variation at temperatures below 50 K [8], [9], SH would not significantly impact the circuit bias conditions and its dynamic performance, causing a relative temperature insensitivity in this regime. This effect can also explain the absence of the negative output conductance characteristic of self-heating in cryo-CMOS devices [41]. However, the increase in circuit temperature by tens of degree Kelvin above T_{amb} can significantly degrade the noise performance for a thermal-noise-limited circuit, although it is still unclear whether temperature-independent shot-noise may be the main limitation in transistor's noise performance at deep-cryogenic temperatures [42]. Moreover, since the exact position of the thermal-resistance minimum cannot be fully attributed to the thermal properties of silicon, but heavily depends on the die thermalization, such as the package, the T_{chan} may vary

due different positions on the die or boundary conditions of the die with the surrounding enclosure. Devices at tens of µm distance from each other can still experience significant thermal cross-talk at deep-cryogenic temperatures even at moderate power levels ($P > 4\,\text{mW}$) within at least a radius of 30 µm (see Figs. 12 and 13). This directly translates into layout guidelines to properly space power-hungry devices from noise-sensitive circuits and precision circuits for which matching is a major consideration.

V. CONCLUSION

A 40-nm CMOS test structure was fabricated and characterized for a comprehensive evaluation of self-heating in bulk CMOS technology in the ambient temperature range from 300 K down to 4.2 K. The temperature rise was measured both in the MOSFET channel through the change in the gate resistance, and in the surrounding silicon substrate by a linear array of diodes operating as sensors.

Severe self-heating was observed at deep-cryogenic ambient temperatures, resulting in a channel temperature rise exceeding 40 K for a dissipated power of only 2 mW at a 4.2 K ambient temperature. Although the thermal conductivity of silicon is relatively low at very low temperatures, the absolute channel temperature does not exceed 60 K even for significantly higher power, due to the thermal resistance for a typical MOSFET, which has minimum above 70 K. This effect was confirmed by extracting the device thermal resistance from measured data at different temperatures and modeling it with a simple analytical expression able to predict channel temperatures over the full ambient temperature range from deep-cryogenic to room temperature.

The spatial propagation of SH results in a rise in substrate temperature detectable and quantifiable at a distance of 30 µm from the heater.

The thorough characterization of nanometer bulk-CMOS devices at cryogenic temperatures is of paramount importance for the design of the integrated control electronics for quantum processors. For achieving first-time-right silicon, it is imperative to simulate the circuit at the actual operating temperature rather than assume the ambient temperature. Towards that goal, the results and modeling presented in this work will contribute towards the full self-heating-aware IC design-flow required for the reliable design and operation of cryo-CMOS circuits.

REFERENCES

[1] L. M. K. Vandersypen *et al.*, "Interfacing spin qubits in quantum dots and donors—Hot, dense, and coherent," *NPJ Quantum Inf.*, vol. 3, pp. 34–44, Sep. 2017.

[2] J. P. G. Van Dijk, E. Charbon, and F. Sebastiano, "The electronic interface for quantum processors," *Microprocess. Microsyst.*, vol. 66, pp. 90–101, Apr. 2019.

[3] F. Arute *et al.*, "Quantum supremacy using a programmable super-conducting processor," *Nature*, vol. 574, pp. 505–510, Oct. 2019.

[4] F. Sebastiano *et al.*, "Cryo-CMOS electronic control for scalable quantum computing," in *Proc. 54th ACM/EDAC/IEEE DAC*, 2017, pp. 1–6.

[5] R. M. Incandela, L. Song, H. Homulle, E. Charbon, A. Vladimirescu, and F. Sebastiano, "Characterization and compact modeling of nanometer CMOS transistors at deep-cryogenic temperatures," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 996–1006, 2018.

[6] S. R. Ekanayake, T. Lehmann, A. S. Dzurak, R. G. Clark, and A. Brawley, "Characterization of SOS-CMOS FETs at low temperatures for the design of integrated circuits for quantum bit control and readout," *IEEE Trans. Electron Devices*, vol. 57, no. 2, pp. 539–547, Feb. 2010.

[7] A. Beckers, F. Jazaeri, and C. Enz, "Characterization and modeling of 28-nm bulk cmos technology down to 4.2 K," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 1007–1018, 2018.

[8] P. A. 'T. Hart, M. Babaie, E. Charbon, A. Vladimirescu, and F. Sebastiano, "Characterization and modeling of mismatch in cryo-CMOS," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 263–273, 2020.

[9] P. A. 'T. Hart, M. Babaie, E. Charbon, A. Vladimirescu, and F. Sebastiano, "Subthreshold mismatch in nanometer CMOS at cryogenic temperatures," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 797–806, 2020.

[10] B. Patra, M. Mehrpoo, A. Ruffino, F. Sebastiano, E. Charbon, and M. Babaie, "Characterization and analysis of on-chip microwave passive components at cryogenic temperatures," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 448–456, 2020.

[11] C. J. Glassbrenner and G. A. Slack, "Thermal conductivity of silicon and germanium from 3°K to the melting point," *Phys. Rev.*, vol. 134, pp. A1058–A1069, May 1964.

[12] J. P. G. Van Dijk *et al.*, "A scalable cryo-CMOS controller for the wideband frequency-multiplexed control of spin qubits and transmons," *IEEE J. Solid-State Circuits*, vol. 55, no. 11, pp. 2930–2946, Nov. 2020.

[13] E. Gutierrez-D, L. Deferm, and G. Declerck, "Experimental determination of self-heating in submicrometer MOS transistors operated in a liquid-helium ambient," *IEEE Electron Device Lett.*, vol. 14, no. 3, pp. 152–154, Mar. 1993.

[14] M. Asheghi, M. Touzelbaev, K. Goodson, Y. Leung, and S. Wong, "Temperature-dependent thermal conductivity of single-crystal silicon layers in SOI substrates," *J. Heat Transf.*, vol. 120, no. 1, pp. 30–36, 1998.

[15] S. S. Sesnic and G. R. Craig, "Thermal effects in JFET and MOSFET devices at cryogenic temperatures," *IEEE Trans. Electron Devices*, vol. ED19, no. 8, pp. 933–942, Aug. 1972.

[16] D. P. Foty and S. L. Titcomb, "Thermal effects in n-channel enhancement MOSFET's operated at cryogenic temperatures," *IEEE Trans. Electron Devices*, vol. ED34, no. 1, pp. 107–113, Jan. 1987.

[17] D. Foty, "Thermal effects in p-channel MOSFETs at low temperatures," *IEEE Trans. Electron Devices*, vol. 36, no. 8, pp. 1542–1544, Aug. 1989.

[18] A. Artanov *et al.*, "Self-heating effect in 65nm CMOS technology (poster)," in *Proc. 14th WOLTE*, 2021, pp. 20–21.

[19] E. A. Gutiérrez D, L. Deferm, and G. Declerck, "Selfheating effects in silicon resistors operated at cryogenic ambient temperatures," *Solid-State Electron.*, vol. 36, no. 1, pp. 41–52, 1993.

[20] F. De la Hidalga, M. J. Deen, and E. A. Gutierrez, "Theoretical and experimental characterization of self-heating in silicon integrated devices operating at low temperatures," *IEEE Trans. Electron Devices*, vol. 47, no. 5, pp. 1098–1106, May 2000.

[21] J. Jomaah, G. Ghibaudo, and F. Balestra, "Analysis and modeling of self-heating effects in thin-film SOI MOSFETs as a function of temperature," *Solid-State Electron.*, vol. 38, no. 3, pp. 615–618, 1995.

[22] K. Triantopoulos *et al.*, "Self-heating effect in FDSOI transistors down to cryogenic operation at 4.2 K," *IEEE Trans. Electron Devices*, vol. 66, no. 8, pp. 3498–3505, Aug. 2019.

[23] F. J. De la Hidalga-W and E. A. Guttierrez-D, "The n-MOS transistor as a low temperature thermometer," in *Proc. 4th Symp. Low Temperature Electron. High Temperature Supercond.*, 1997, pp. 387–394.

[24] E. A. Gutierrez-D, L. Deferm, S. Decoutere, and G. Declerck, "Experimental determination of selfheating in silicon resistors operated at cryogenic temperatures," *Microelectron. Eng.*, vol. 19, no. 1, pp. 865–868, 1992.

[25] E. A. Gutierrez-D., J. De la Hidalga-W, M. J. Deen, and S. V. Koshevaya, "An alternative method to monitor and control the IC temperature in the 4.2-77 K range," in *Proc. 27th ESSDERC*, 1997, pp. 436–439.

[26] G. Kiene *et al.*, "A 1GS/s 6-to-8b 0.5mW/qubit cryo-CMOS SAR ADC for quantum computing in 40nm CMOS," in *Proc. IEEE ISSCC*, vol. 64, 2021, pp. 214–216.

[27] B. Prabowo *et al.*, "A 6-to-8GHz 0.17mW/qubit cryo-CMOS receiver for multiple spin qubit readout in 40nm CMOS technology," in *Proc. IEEE ISSCC*, vol. 64, 2021, pp. 212–214.

[28] A. Ruffino, Y. Peng, T.-Y. Yang, J. Michniewicz, M. F. Gonzalez-Zalba, and E. Charbon, "13.2 a fully-integrated 40-nm 5-6.5 GHz cryo-CMOS system-on-chip with I/Q receiver and frequency synthesizer for scalable multiplexed readout of quantum dots," in *Proc. IEEE ISSCC*, vol. 64, 2021, pp. 210–212.

[29] J.-S. Park *et al.*, "13.1 a fully integrated cryo-CMOS SoC for qubit control in quantum computers capable of state manipulation, readout and high-speed gate pulsing of spin qubits in Intel 22nm FFL FinFET technology," in *Proc. IEEE ISSCC*, vol. 64, 2021, pp. 208–210.

[30] G. Pavlidis, S. Pavlidis, E. R. Heller, E. A. Moore, R. Vetury, and S. Graham, "Characterization of AlGaN/GaN HEMTs using gate resistance thermometry," *IEEE Trans. Electron Devices*, vol. 64, no. 1, pp. 78–83, Jan. 2017.

[31] P. G. Mautry and J. Trager, "Self-heating and temperature measurement in sub-μm-MOSFETs," in *Proc. ESSDERC*, 1989, pp. 675–678.

[32] Y. M. Shwarts, M. M. Shwarts, and S. V. Sapon, "A new generation of cryogenic silicon diode temperature sensors," in *Proc. ASDAM*, 2008, pp. 239–242.

[33] C. D. Matthus *et al.*, "Feasibility of 4H-SiC p-i-n diode for sensitive temperature measurements between 20.5 K and 802 K," *IEEE Sens. J.*, vol. 19, no. 8, pp. 2871–2878, Apr. 2019.

[34] Y. Shwarts, V. Borblik, N. Kulish, V. Sokolov, M. Shwarts, and E. Venger, "Silicon diode temperature sensor without a kink of the response curve in cryogenic temperature region," *Sens. Actuators A, Phys.*, vol. 76, no. 1, pp. 107–111, 1999.

[35] R. Ward *et al.*, "Power diodes for cryogenic operation," in *Proc. IEEE 34th PESC*, vol. 4, 2003, pp. 1891–1896.

[36] S. S. Courts, "A standardized diode cryogenic temperature sensor for aerospace applications," *Cryogenics*, vol. 74, pp. 172–179, Mar. 2016.

[37] T. B. Hook, J. Brown, and X. Tian, "Proximity effects and VLSI design," in *Proc. Int. Conf. Integr. Circuit Design Technol.*, 2005, pp. 167–170.

[38] J. F. Creemer, F. Fruett, G. C. M. Meijer, and P. J. French, "The piezojunction effect in silicon sensors and circuits and its relation to piezoresistance," *IEEE Sensors J.*, vol. 1, no. 2, p. 98, Aug. 2001.

[39] Y. Shwarts, V. Sokolov, M. Shwarts, I. Fedorov, and E. Venger, "Advanced silicon diode temperature sensors with minimized self-heating and noise for cryogenic applications," in *Proc. ASDAM*, 2000, pp. 351–354.

[40] A. R. Alt and C. R. Bolognesi, "Temperature dependence of annealed and nonannealed HEMT ohmic contacts between 5 and 350 K," *IEEE Trans. Electron Devices*, vol. 60, no. 2, pp. 787–792, Feb. 2013.

[41] J. S. Brodsky, R. M. Fox, D. T. Zweidinger, and S. Veeraraghavan, "A physics-based, dynamic thermal impedance model for SOI MOSFET's," *IEEE Trans. Electron Devices*, vol. 44, no. 6, pp. 957–964, Jun. 1997.

[42] X. Chen, H. Elgabra, C.-H. Chen, J. Baugh, and L. Wei, "Estimation of MOSFET channel noise and noise performance of CMOS LNAs at cryogenic temperatures," in *Proc. IEEE ISCAS*, 2021, pp. 1–5.
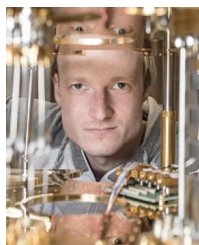
P. A. 'T HART received the M.Sc. degree in electrical engineering from the Delft University of Technology, The Netherlands, in 2014. He is currently pursuing the Ph.D. degree in characterizing and modeling cryogenic MOSFETs with the Group of Edoardo Charbon. For his thesis, he worked with the Electronic Components, Materials and Technology Department and the Electronic Instrumentation Laboratory, where he did characterization of the piezojunction effect in bipolar transistors. In 2017, he joined the Group of Edoardo Charbon. His research interests include low temperature electronics, modeling, and characterization.

M. BABAIE (Member, IEEE) received the Ph.D. degree *(cum laude)* in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 2016. In 2006, he joined the Kavoshcom Research and Development Group, Tehran, Iran, where he was involved in designing wireless communication systems, where he was a CTO, from 2009 to 2011. From 2014 to 2015, he was a Visiting Scholar Researcher with the Berkeley Wireless Research Center, Berkeley, CA, USA. In 2016, he joined the Delft University of Technology, where he is currently an Assistant Professor (tenured). His current research interests include RF/millimeter-wave integrated circuits and systems for wireless communications, and cryogenic electronics for quantum computation. In 2019, he received the Veni Award from the Netherlands Organization for Scientific Research. He was a co-recipient of the 2015–2016 IEEE Solid-State Circuits Society Pre-Doctoral Achievement Award, and the 2019 IEEE ISSCC Best Demo Award. He has been a Committee Member of the Student Research Preview of the IEEE International Solid-State Circuits Conference (ISSCC) since 2017. He is currently serving on the Technical Program Committee of the IEEE European Solid-State Circuits Conference.

A. VLADIMIRESCU (Life Fellow, IEEE) received the M.S. and Ph.D. degrees in EECS from the University of California at Berkeley, where he was a Key Contributor to the SPICE simulator, releasing the SPICE2G6 production-level SW in 1981. He pioneered electrical simulation on parallel computers with the CLASSIE simulator as part of his Ph.D. For many years, he was the R&D Director leading the design and implementation of innovative software and hardware electronic design automation products with Analog Devices, Inc., Daisy Systems, Analog Design Tools, Valid Logic, and Cadence. He is currently a Professor involved in research projects with the University of California at Berkeley, Delft University of Technology, and the Institut Supérieur d'Électronique de Paris, ISEP, as well as a Consultant to industry. He has authored *The SPICE Book* (Wiley). His research activities are in the areas of ultra-low-voltage CMOS, design, simulation, and modeling of circuits with new devices and circuits for quantum computing.

F. SEBASTIANO (Senior Member, IEEE) received the B.Sc. and M.Sc. degrees *(cum laude)* in electrical engineering from the University of Pisa, Italy, in 2003 and 2005, respectively, the M.Sc. degree *(cum laude)* from the Sant'Anna school of Advanced Studies, Pisa, Italy, in 2006, and the Ph.D. degree from the Delft University of Technology, The Netherlands, in 2011. From 2006 to 2013, he was with NXP Semiconductors Research, Eindhoven, The Netherlands, where he conducted research on fully integrated CMOS frequency references, deep-submicron temperature sensors, and area-efficient interfaces for magnetic sensors. In 2013, he joined the Delft University of Technology, where he is currently an Associate Professor and the Research Lead of the Quantum Computing Division, QuTech. He has authored or coauthored one book, 11 patents, and over 80 technical publications. His main research interests are cryogenic electronics, quantum computing, sensor read-outs, and fully integrated frequency references. He was a co-recipient of the 2008 ISCAS Best Student Paper Award, the 2017 DATE Best IP Award, and the ISSCC 2020 Jan van Vessem Award for Outstanding European Paper. He is on the Technical Program Committee of the ISSCC, the IEEE RFIC Symposium, and the IMS, and he is currently serving as an Associate Editor of the of IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION. He has served as a Distinguished Lecturer of the IEEE Solid-State Circuit Society.