Supply-Insensitive Frequency Synthesis for an LDO-Free Powering Scheme in SoCs

Chen, Y.

DOI
10.4233/uuid:2a66f780-cfc3-4749-a704-ffac3d267d02

Publication date
2022

Document Version
Accepted author manuscript

Citation (APA)
Chen, Y. (2022). *Supply-Insensitive Frequency Synthesis for an LDO-Free Powering Scheme in SoCs*. [Dissertation (TU Delft), Delft University of Technology]. https://doi.org/10.4233/uuid:2a66f780-cfc3-4749-a704-ffac3d267d02

Supply-Insensitive Frequency Synthesis for an LDO-Free Powering Scheme in SoCs

Yue CHEN

Supply-Insensitive Frequency Synthesis for an LDO-Free Powering Scheme in SoCs

Dissertation

for the purpose of obtaining the degree of doctor
at Delft University of Technology
by the authority of the Rector Magnificus Prof.dr.ir. T.H.J.J. van der Hagen,
chair of the Board for Doctorates
to be defended publicly on

Wednesday 30 March 2022 at 15:00 o'clock

by

Yue CHEN

Master of Engineering in Electronic Science and Technology, Xi'an Jiaotong University, China
born in Xi'an, China.

This dissertation has been approved by the promotor:
Prof. dr. R. B. Staszewski

Composition of the doctoral committee:

Rector Magnificus	chairperson
Prof. dr. R. B. Staszewski	Delft University of Technology, promotor
Dr. M. Babaie	Delft University of Technology, copromotor

Independent members:

Prof. dr. P. Andreani	Lund University, Sweden
Prof. dr. S. Levantino	Politecnico di Milano, Italy
Prof. dr. ir. B. Nauta	University of Twente
Dr. Y.-H. Liu	IMEC Netherlands
Prof. dr. ir. W. A. Serdijn	Delft University of Technology
Prof. dr. C. S. Vaucher	Delft University of Technology, reserve member

Yue Chen,
Supply-Insensitive Frequency Synthesis for an LDO-Free Powering Scheme in SoCs
Ph.D. Thesis Delft University of Technology.

Keywords: frequency synthesizer, digital phase-locked loop (DPLL), LC oscillator, ripple replication and cancellation, slope generator (SG), SAR ADC, divider resample, ripple pattern estimation and cancellation, DC-DC converter, supply ripple, supply pushing, LDO, power management unit (PMU), system-on-chip (SoC).

ISBN xxx-xx-xxxx-xxx-x

Printed in the Netherlands.

"What we know is not much. What we do not know is immense."

Pierre-Simon Laplace, 1749-1827

Contents

Chapter

1

Introduction

In this introductory chapter, necessary background information on power management units of integrated circuit (IC) systems and a brief overview of frequency synthesis based on phase-locked loops are presented. This facilitates the development of this dissertation in the following chapters. Moreover, the main objectives and structure of this dissertation are also summarized at the end of the chapter.

1.1 System Power Management

In the past few decades, the CMOS process technology has been continuously advancing towards the ever finer feature size. Following this scaling trend, which has been mainly propelled by digital circuits, the thickness of oxide layer keeps on reducing with each technology node. The nominal supply voltage has also been scaling down accordingly, as shown in Fig. 1.1 [1], to maintain a reasonable electric field intensity inside the device and to prevent reliability issues, such as a time-dependent breakdown of the gate dielectrics (TDDB) and hot carrier injection [2]. The nominal supply voltage of the submicron CMOS technology is already around 1 V, which is much lower than the voltage levels provided by available energy sources such as batteries. Meanwhile, energy harvesting techniques are maturing to significantly extend the system lifetime of devices for applications such as the Internet-of-Things (IoT) and wireless sensor networks (WSN), and may even realize batteryless operation of these devices. However, the output voltage of the commonly used harvester types (i.e., ∼0.25–0.75 V) [3–5] is typically much lower than the nominal 1 V supply of the submicron CMOS, making it also unsuitable to power the devices directly. Therefore, additional blocks should be inserted between the energy sources, whether batteries or energy harvesters, and the devices they power, in order to bridge that voltage gap.

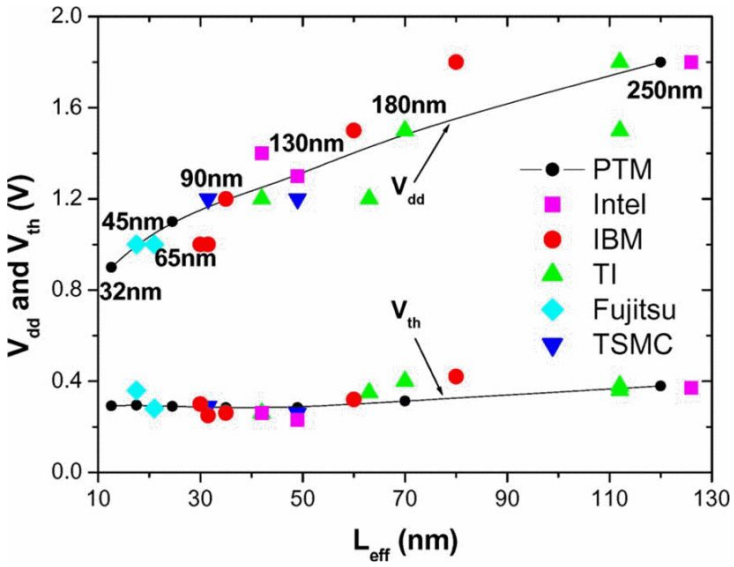


Figure 1.1: Trend of V_{dd} and V_{th} scaling from 250- to 32-nm nodes [1].

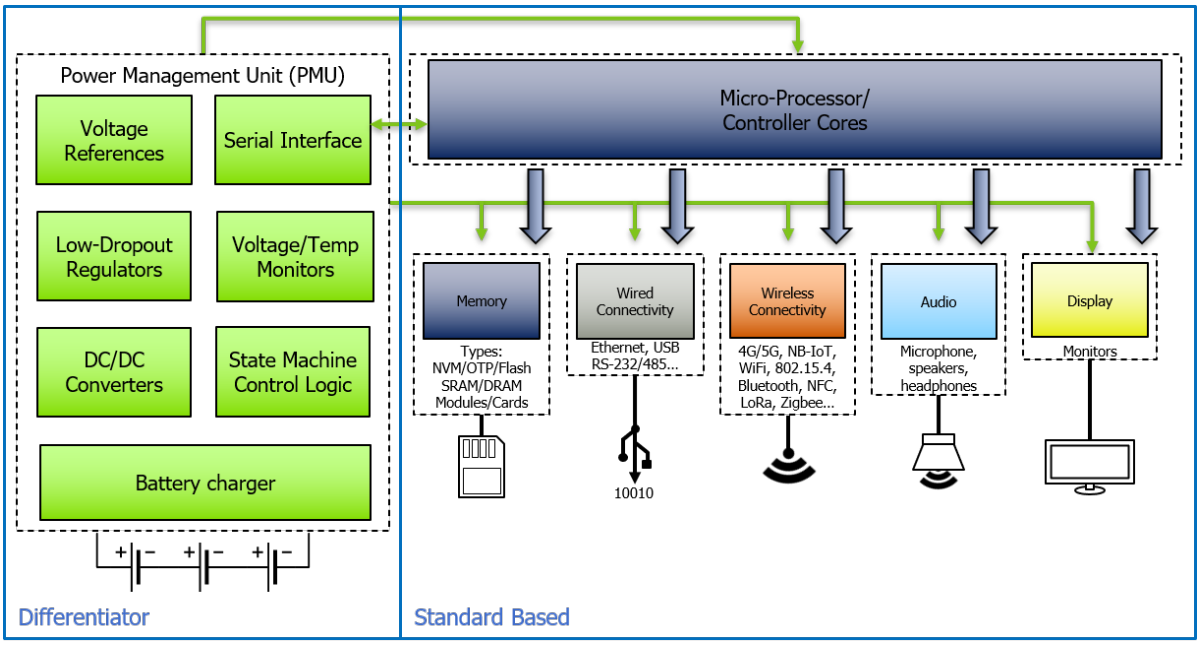


Figure 1.2: Example SoC block diagram with integrated power management [11].

Aside from the aforementioned voltage difference, an integrated system, especially a mixed-signal one, may also require multiple supply levels to power different functional blocks inside the system in order to achieve both the satisfying performance and lower power consumption [6, 7]. For example, RF and analog blocks inside the system are typically powered at the nominal supply voltage to maintain their desired performance, while the voltage levels supplying digital blocks may be lowered to reduce their power/energy consumption. Techniques that dynamically adjust the supply voltages of functional blocks are also attracting research interests [8, 9]. By varying the voltage level of certain functional blocks based on their operating circumstances, the power consumed by a particular block can be further reduced when the instant requirement on its performance is relaxed, thereby improving the system efficiency. Considering all these factors, together with other necessary control functions, power-rail sequencing [10] as an example, a dedicated power management unit (PMU) should be designed to guarantee that the integrated system is properly powered.

An example of the PMU integrated in a system-on-chip (SoC) is illustrated in Fig. 1.2 [11]. Generally, the PMU contains several voltage regulators (e.g., DC-DC converters and low-dropout linear regulators) to convert the output of the energy source to proper supply voltages required by the functional blocks. Besides, a control block is implemented to su-

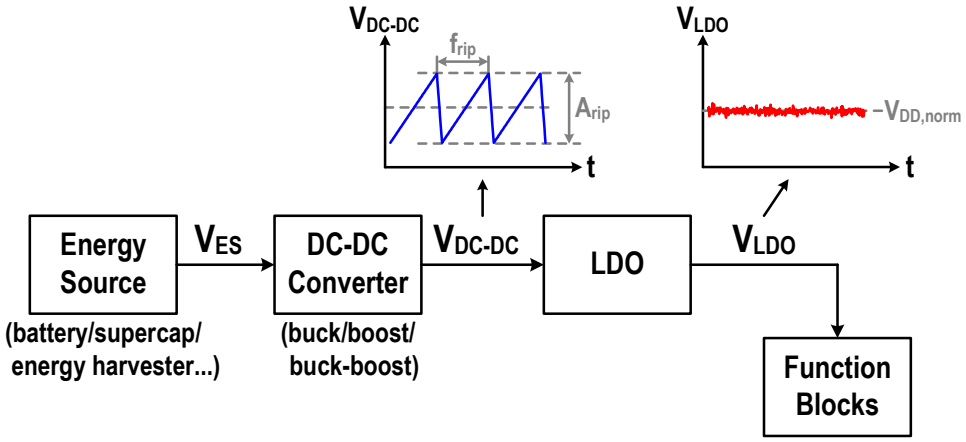


Figure 1.3: Cascading of the DC-DC converter with the LDO to generate stable supply voltage for sensitive modules inside the system.

pervise the correct behavior of the PMU outputs. Other blocks, such as voltage monitors and temperature sensors are also commonly employed in the PMU to guarantee the proper performance of the SoC [11].

1.1.1 Voltage Regulation in PMU

At the heart of the PMU are voltage regulators performing the conversion between different voltage levels. Two types of regulators are normally employed: DC-DC converters (or sometimes referred to as "switching regulators" in contrast to the linear regulators) and low-dropout (LDO) linear regulators.

A DC-DC converter transforms with high efficiency the output level of the energy source to a proper value determined by the circuits it powers. Depending on the required voltage difference between its input and output, the DC-DC converter can operate in a certain mode (i.e., buck or boost), or a combination of the two modes (i.e., buck-boost) could be adopted to accommodate different input situations (see Fig. 1.3). Conventionally, the converter tends to be designed with inductor-based topologies. However, these topologies typically require external inductors of high quality factors, impeding their full SoCs integration. In contrast, the switch-capacitor-based DC-DC converters could be implemented with on-chip capacitors and are favored for from the standpoint of full system integration [12, 13].

Although a high efficiency could be achieved by the DC-DC converter, a ripple at its output originating from the switching operation of the converter could severely degrade the performance of supply-sensitive blocks. To solve

this problem, an LDO is generally used in a cascade with the converter to suppress the ripple and to generate a 'clean' supply voltage for the functional blocks, as shown in Fig. 1.3. Besides the power supply rejection (PSR), efficiency is another important performance metric of the LDO. Many integrated LDO designs with good PSR and efficiency performance could be found in the literature. However, these designs only focus on the LDO itself, and a detailed analysis that would also take the requirements imposed by the load circuitry into consideration is still lacking.

1.2 Frequency Synthesis Overview

Frequency synthesis is widely employed in various types of applications to generate local oscillator (LO) signals, perform frequency and phase modulation, or generate clocks for data converters, etc. A phase-locked loop (PLL) is one of the most commonly used techniques to implement frequency synthesis, especially in communication systems.

A general block diagram of the PLL is shown in Fig. 1.4. It consists of a phase detector (PD), a loop filter (LF), a controlled oscillator, and a frequency divider. Based on the input frequency of the reference signal (REF), the loop adjusts the frequency and phase of its output signal in a feedback manner. The output of the oscillator is also scaled by the frequency divider: the divided signal (FB) is fed into the PD to compare with REF. The output of PD represents the phase error between REF and FB and is used to modulate the oscillator again after being filtered by LF. Therefore, the frequency of the output signal (f_{out}, which equals the frequency of the oscillator, f_{osc}), is related to the reference frequency (f_{ref}) through the division ratio of the frequency divider, i.e., $f_{\text{out}} = N \times f_{\text{ref}}$.

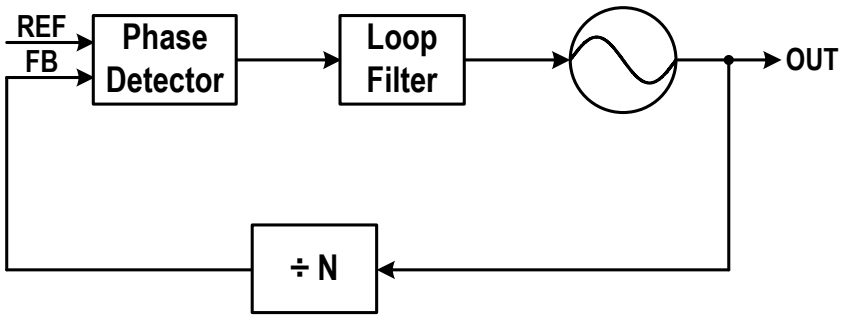


Figure 1.4: General block diagram of a PLL.

When N is constrained to be an integer, the PLL operates as integer-N. Otherwise, it operates in a fractional-N mode. For fractional-N PLLs, f_{out} could vary with a frequency step that is much smaller than f_{ref}, thus offering more flexibility in the loop design, which is greatly beneficial in communication systems.

The open-loop transfer function of the PLL shown in Fig. 1.4 is expressed as

$$H_{\text{ol}}(s) = \frac{\phi_{\text{fb}}}{\phi_{\text{ref}}} = \frac{1}{N} \cdot K_{\text{PD}} H_{\text{LF}}(s) \cdot \frac{2\pi K_{\text{osc}}}{s} \tag{1.1}$$

where ϕ_{ref} and ϕ_{fb} represent the (excess) phase of REF and FB, K_{PD} is the PD gain, $H_{\text{LF}}(s)$ the transfer function of LF, and K_{osc} the frequency gain of the oscillator. Based on (1.1), a closed-loop transfer function from REF ($H_{\text{cl,ref}}$) and from the oscillator output ($H_{\text{cl,osc}}$) to the PLL output could be obtained. The calculation shows that

$$H_{\text{cl,ref}}(s) = \frac{\phi_{\text{out}}}{\phi_{\text{ref}}} = \frac{N H_{\text{ol}}(s)}{1 + H_{\text{ol}}(s)} = \frac{N K_{\text{PD}} H_{\text{LF}}(s) \cdot 2\pi K_{\text{osc}}}{Ns + K_{\text{PD}} H_{\text{LF}}(s) \cdot 2\pi K_{\text{osc}}} \tag{1.2}$$

and

$$H_{\text{cl,osc}}(s) = \frac{\phi_{\text{out}}}{\phi_{\text{osc}}} = \frac{1}{1 + H_{\text{ol}}(s)} = \frac{Ns}{Ns + K_{\text{PD}} H_{\text{LF}}(s) \cdot 2\pi K_{\text{osc}}} \tag{1.3}$$

in which ϕ_{out} is the (excess) phase of OUT, and ϕ_{osc} represents the phase fluctuation at the oscillator output. Note that the phase quantity ϕ_{ref} in (1.2) is still normalized to the reference frequency domain. When normalized to the frequency domain of the oscillator instead (e.g., such a transform is generally needed when modeling sub-sampling PLLs), (1.2) should be divided by N. Eqs. (1.2) and (1.3) prove that any perturbation injected in the reference path experiences low-pass filtering while that injected at the oscillator output is high-pass filtered by the loop. This leads to an optimal PLL bandwidth at which the oscillator and the loop components contribute to the output jitter almost equally [14]. The number of poles in the transfer functions (1.2) and (1.3) also determines the order of the PLL, while the PLL type is related to the number of poles at DC. Since the oscillator will always contribute one DC pole due to the integration of its frequency modulation to obtain the corresponding phase information, the PLL is at least of type I. The loop could be made type II by including

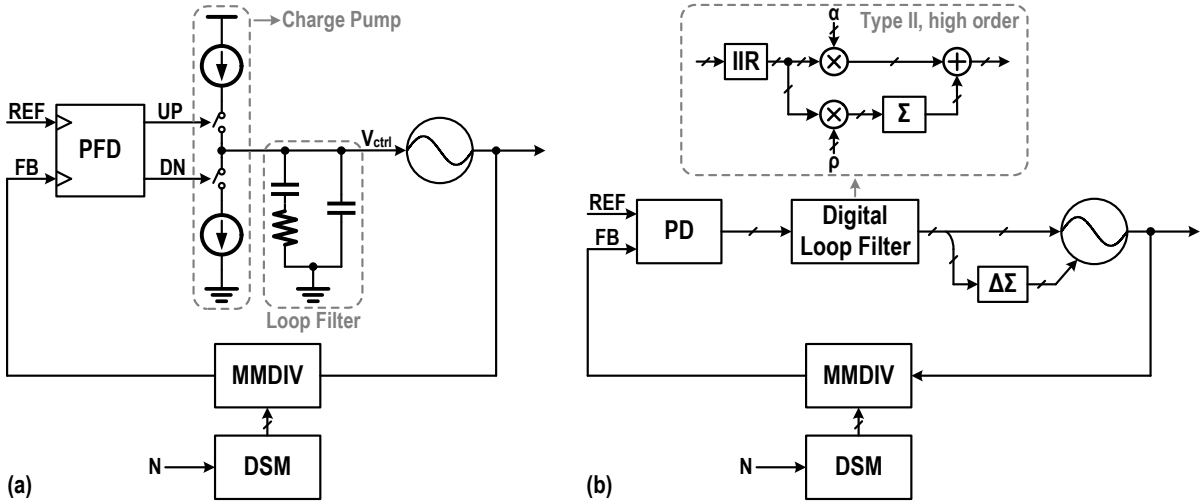


Figure 1.5: Block diagram of (a) an analog CPPLL and (b) a divider based digital PLL.

one integrator in LF. Compared to a type I PLL, in which the static phase error ($\phi_{\mathrm{e,ss}}$) between REF and DIV varies with the output frequency, $\phi_{\mathrm{e,ss}}$ is ideally zero for a type II loop, which is beneficial in some applications [15].

Based on the implementation approach, the PLL structures could be further classified into two categories: analog [16–25] and digital [26–33]. Conventionally, the analog charge-pump PLL (CPPLL) [16–18, 22], shown in Fig. 1.5 (a), was dominating as the design choice in the past. In a CPPLL, the phase error is measured by the phase/frequency detector (PFD), which generates two pulses ('UP' and 'DN') with a width difference similar to the phase error timing. The pulses then control the corresponding current branches in the charge pump (CP) to charge/discharge the capacitors in LF. Hence, the control signal (V_{ctrl}) of the voltage-controlled oscillator (VCO) is increased/decreased, and the VCO frequency is modulated accordingly. To realize fractional-N operation, a multi-modulus divider (MMDIV) controlled by the $\Delta\Sigma$ modulator (DSM) is commonly used in the loop. As the technology keeps scaling down, the design of the CPPLL is becoming increasingly difficult due to analog imperfections such as the reduced supply voltage and the short-channel effects of the transistors. Therefore, digital alternatives are being explored in the sub-micron CMOS [26–34]. In contrast to the CPPLL, the phase error information is converted into the digital domain, as can be observed from Fig. 1.5 (b), and further processed by the digital loop filter (DLF). The loop dynamic could be better controlled with DLF, while the removal of the bulky passive capacitors

and resistors in the analog filter of CPPLL could also help in reducing the silicon area. The DLF output is used to tune a digitally controlled oscillator (DCO), instead of a VCO, and another $\Delta\Sigma$ modulator could be applied to dither the least significant bits (LSBs) of the DCO control word for finer frequency resolution. Such digital intensive implementations also lend the loop naturally to the advanced digital calibration techniques in scaled CMOS technologies. Since the phase information is already available in the digital format, various calibration algorithms could be easily employed to improve the loop performance.

1.3 Thesis Objective

The main objective of this dissertation work is to carry out research on the powering strategy for sensitive analog and RF components, especially the PLLs, and accordingly to develop a new loop architecture for an improved power efficiency and reduced design complexity.

To achieve this goal, the conventional arrangement of powering the SoCs is investigated first. This thesis will mainly focus on the limitation of the LDO efficiency based on the practical requirements of the PLL. Following this, a fractional-N digitally intensive PLL architecture tolerant of supply ripples is then developed as described in the rest of this thesis, ultimately enabling its direct operation under the output of DC-DC converters.

1.4 Thesis Outline

This thesis is composed of two parts. The first part (Chapters 2 and 3) focuses on the analysis of the power management strategy for SoCs, showing the benefits of supplying the PLL directly from the switched-capacitor-based DC-DC converters. Then, the design and implementation of a fractional-N digitally insensitive PLL, capable of maintaining its performance in face of a large supply ripple, ultimately enabling its direct connection to the converter output, is elaborated in the second part (Chapters 4 and 5). The thesis is organized as follows.

In Chapter 2, the issues of powering a PLL from a DC-DC converter with output ripples are analyzed in three aspects. To tackle these issues,

either LDOs should be used to suppress the amplitude of the ripples, or extra techniques need to be invented to alleviate their effects on the performance of PLL.

In Chapter 3, the limitations on the power efficiency of the integrated LDOs powering PLLs are analyzed. It is found that the use of LDOs consumes extra voltage headroom and could largely degrade the power efficiency of the system. Hence, it is desired that the PLL could operate directly from the converter output. A brief discussion of different SoC powering scenarios is also included at the end of this chapter.

In Chapter 4, a feed-forward supply ripple replication and cancellation technique is proposed to suppress the supply pushing of the LC oscillator, which is the most sensitive block to the supply ripples in the PLL. To verify the proposed technique, measurement results of a 40-nm prototype are presented. Moreover, the oscillator is directly powered by a three-stage recursive switched-capacitor DC-DC converter to further verify its effectiveness.

In Chapter 5, a fractional-N digitally intensive PLL that is practically insensitive to supply ripples is designed and implemented in 40-nm CMOS. The phase detector is realized in voltage domain through cascading a supply-insensitive slope generator with the output of a current DAC, while a low-power ripple-pattern estimation and cancellation algorithm is implemented at the output of the SAR ADC to prevent the supply-induced delay variation of loop components from modulating the oscillator's frequency. The technique proposed in Chapter 4 with an improved calibration loop is also employed for the oscillator design here. Extensive experimental results of the prototype under both sinusoidal and sawtooth supply ripples are also presented at the end of the chapter.

Finally, Chapter 6 concludes the dissertation with some suggestions for future improvements.

1.4.1 Original Contributions

The original contributions of this work are summarized from Section 6.2 as follows:

- Quantitative analysis of the PLL's spurious and phase noise degradation due to the ripples and noise on its supply and derivation of the

corresponding limitations on the LDO efficiency (Chapters 2 and 3).
- Quantitative analysis of four different SoC powering scenarios (Chapter 3).
- Introduced a feed-forward supply ripple replication and cancellation technique with an on-chip calibration loop to suppress the supply pushing of the LC oscillator (Chapter 4).
- Design and implementation of a fractional-N digitally intensive PLL that is insensitive to supply ripples (Chapter 5).

Chapter

2

Effects of Supply Ripple on the Spectral Purity of PLL

This chapter investigates the effects of supply ripples that stem from the switching operation of an integrated DC-DC converter on the PLL's spectral purity. Output spurs at the ripple frequency generated by the supply pushing of the oscillator or the output delay variation of loop components are quantified. For a fractional-N operation, the effects of intermodulation between the ripple frequency and the synthesized fractional frequency are also analyzed. Based on the aforementioned discussions, the requirement on the ripple amplitude is also determined. Note that although a digital PLL structure is chosen as an example in a portion of the analysis in this chapter, the result is also valid for analog PLLs.

2.1 Spurs Due to Oscillator Supply Pushing

It is well-known that the level of spurious tones around the carrier that are induced by a sinusoidal supply ripple with a peak-to-peak amplitude of $A_{\mathrm{rip,osc}}$ and a frequency of f_{rip} can be estimated by

$$S_{\mathrm{osc}} = 20 \cdot \log_{10}\left(\frac{K_{\mathrm{push}} \cdot A_{\mathrm{rip,osc}}}{4 f_{\mathrm{rip}}}\right), \tag{2.1}$$

where K_{push} is the supply pushing of the oscillator. Considering that f_{rip}, which is expected to be in the range of several to tens of MHz for switched-capacitor-based DC-DC converters, is much higher than the typical bandwidth (<1 MHz) of a PLL, this spur will appear at the PLL output with little attenuation (see Fig. 2.1). From (2.1), to guarantee a <−50 dBc spur level under a 50 $\mathrm{mV_{pp}}$ ripple, K_{push} should be less than 1.26 MHz/V, which is much lower than that in state-of-the-art RF oscillators [35].

Consequently, $A_{\mathrm{rip,osc}}$ should be suppressed to a sufficiently small value. From (2.1), the maximum ripple amplitude that could be tolerated by the oscillator for a given spur level S_{osc} can be calculated as

$$A_{\mathrm{rip,osc}} < \frac{4 f_{\mathrm{rip}}}{K_{\mathrm{push}}} 10^{S_{\mathrm{osc}}/20}. \tag{2.2}$$

It shows that the tolerable ripple amplitude increases with f_{rip} due to the decrease in the oscillator's frequency-to-phase conversion gain.

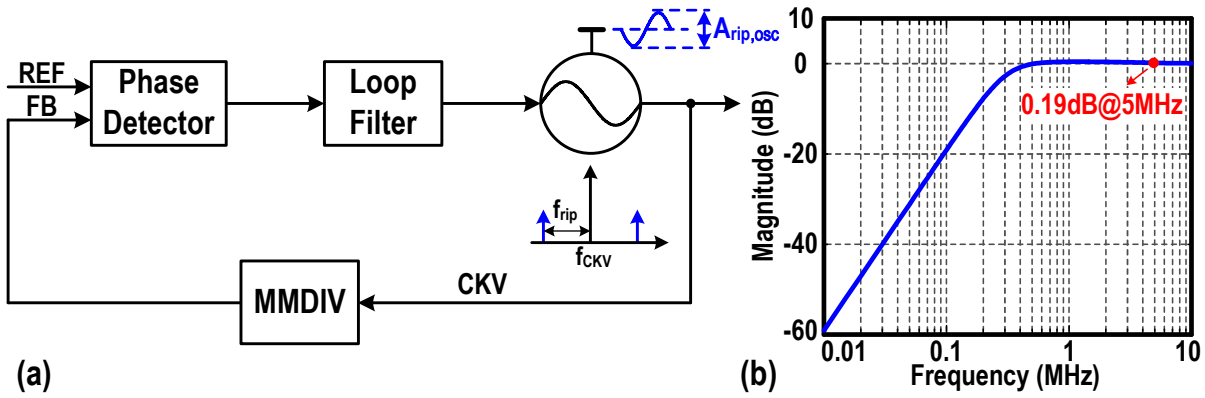


Figure 2.1: (a) Spurs produced by the supply pushing of the oscillator in a PLL. (b) High-pass magnitude response of a type-II PLL with a typical 300 kHz bandwidth and a damping factor of 0.707.

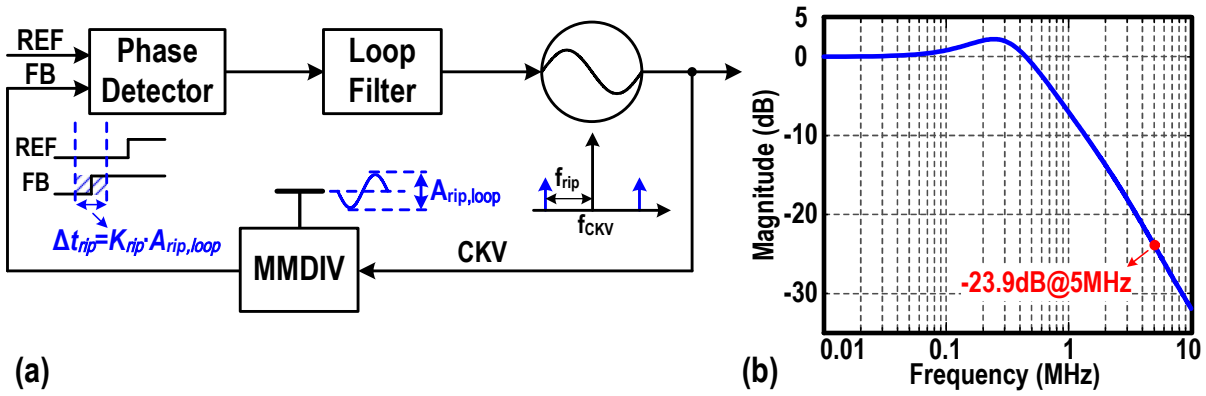


Figure 2.2: (a) Spurs produced by the supply ripple modulating the divider output delay. (b) Low-pass magnitude response of a type-II PLL with a typical 300 kHz bandwidth and a damping factor of 0.707.

2.2 Spurs Due to Delay Perturbations of PLL's Components

Supply ripples also degrade the PLL's spectral purity by modulating the delay of the edge-critical loop components. Figure 2.2 (a) shows an example in which the propagation delay of the multi-modulus divider (MMDIV) is affected by its supply voltage. This delay variation is then sensed by the phase detector (PD) and transferred to the PLL's output, leading to spurs at f_{rip} from the carrier. Since the supply perturbation is relatively small, it is reasonable to assume that the delay variation, Δt_{rip}, is proportional to the ripple amplitude $A_{\mathrm{rip,loop}}$, i.e.,

$$\Delta t_{\mathrm{rip}} = K_{\mathrm{rip}} \cdot A_{\mathrm{rip,loop}}, \tag{2.3}$$

where K_{rip} is the supply sensitivity of the MMDIV delay. Hence, the corresponding peak-to-peak phase deviation presented at the PD input is

$$\Delta\phi_{\mathrm{rip}} = 2\pi \frac{K_{\mathrm{rip}} \cdot A_{\mathrm{rip,loop}}}{T_{\mathrm{CKV}}}, \tag{2.4}$$

in which T_{CKV} is the oscillation period. This will result in an extra phase variation at the PLL output with a peak-to-peak amplitude of

$$\Delta\phi_{\mathrm{rip,out}} = 2\pi \frac{K_{\mathrm{rip}} \cdot A_{\mathrm{rip,loop}}}{T_{\mathrm{CKV}}} \cdot 10^{\mathrm{TF_{loop}}/20}, \tag{2.5}$$

in which $\mathrm{TF}_{\mathrm{loop}}(f_{\mathrm{rip}})$ expresses the amount of low-pass attenuation (in dB) provided by the loop at f_{rip}. Note that $\Delta\phi_{\mathrm{rip}}$ is normalized to f_{osc} directly, thus $\mathrm{TF}_{\mathrm{loop}} \approx 1$ at low frequency offsets, as shown in Fig. 2.2 (b). Instead, if $\Delta\phi_{\mathrm{rip}}$ was normalized to f_{ref}, $\mathrm{TF}_{\mathrm{loop}}$ should be multiplied by the division ratio, resulting in the same expression shown in (2.5). Based on (2.5), the output signal of the PLL, x_{PLL}, is expressed as

$$x_{\mathrm{PLL}} = A_{\mathrm{osc}} \sin\left(\omega_{\mathrm{osc}} t + \frac{\Delta\phi_{\mathrm{rip,out}}}{2} \sin\left(\omega_{\mathrm{rip}} t\right)\right), \tag{2.6}$$

where A_{osc} is the amplitude of CKV. Given that $|\Delta\phi_{\mathrm{rip,out}}|$ is typically much less than $\pi/6$, (2.6) could then be approximated as

$$\begin{aligned} x_{\mathrm{PLL}} \approx & A_{\mathrm{osc}} \sin\left(\omega_{\mathrm{osc}} t\right) + \\ & A_{\mathrm{osc}} \cdot \frac{\Delta\phi_{\mathrm{rip,out}}}{4} \cdot \left(\sin[(\omega_{\mathrm{osc}} + \omega_{\mathrm{rip}})t] - \sin[(\omega_{\mathrm{osc}} - \omega_{\mathrm{rip}})t]\right). \end{aligned} \tag{2.7}$$

Combining (2.7) and (2.5), the spur level induced by the delay variation of MMDIV under supply ripple is calculated as

$$S_{\mathrm{dly}} = 20 \cdot \log_{10}\left(\frac{\phi_{\mathrm{rip,out}}}{4}\right) = 20 \cdot \log_{10}\left(\frac{\pi \cdot K_{\mathrm{rip}} \cdot A_{\mathrm{rip,loop}}}{2T_{\mathrm{CKV}}}\right) + \mathrm{TF}_{\mathrm{loop}}. \tag{2.8}$$

The magnitude response of a type-II digital PLL (DPLL) with a typical 300 kHz bandwidth is shown in Fig. 2.2 (b). Note that a wider bandwidth would result in a lower attenuation by the loop ($\mathrm{TF}_{\mathrm{loop}}$), worsening the spur performance due to the delay variation, while a narrower bandwidth would provide less filtering of the oscillator phase noise (PN), consequently affecting the in-band PN and jitter performance of the loop [14]. For a 5 MHz f_{rip}, the suppression offered by the loop is only −23.9 dB. Hence, with a simulated $K_{\mathrm{rip}} \approx 400$ ps/V, a 50 $\mathrm{mV_{pp}}$ ripple causes a ~ -40 dBc spur at a 5 GHz carrier, necessitating extra techniques to tackle this issue and further reducing the corresponding spur to below the desired level.

When $A_{\mathrm{rip,loop}}$ is reduced to suppress this spur, the limitation on ripple amplitude could be derived from (2.8), and the result is shown below:

$$A_{\mathrm{rip,loop}} < \frac{2 \cdot 10^{(S_{\mathrm{dly}} - \mathrm{TF}_{\mathrm{loop}}(f_{\mathrm{rip}}))/20}}{\pi f_{\mathrm{osc}} K_{\mathrm{rip}}}. \tag{2.9}$$

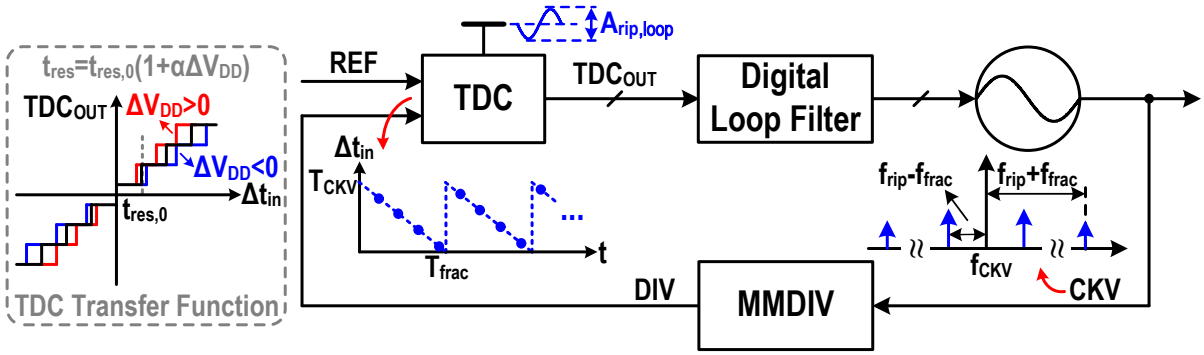


Figure 2.3: Conventional time-domain DPLL employing the TDC to quantify phase error.

From (2.9), it is observed that the tolerable ripple amplitude decreases at higher f_{osc} since a similar Δt_{rip} corresponds then to larger $\Delta\phi_{\text{rip}}$ and $\Delta\phi_{\text{rip,out}}$.

2.3 Spurs Due to Intermodulation Between f_{rip} and f_{frac}

Conventionally, the fractional-N DPLL has been realized in the time domain and quantizes its phase error by means of a time-to-digital converter (TDC) [26, 27, 36–38]. As shown in Fig. 2.3, when synthesizing a fractional channel of a fractional frequency ω_{frac}, the time difference presented at the TDC input shows a sawtooth waveform at ω_{frac}:

$$\Delta t_{\text{in,1st}} = T_{\text{CKV}} \cdot W_{\text{sawtooth}}\left(\omega_{\text{frac}} t\right), \tag{2.10}$$

where $W_{\text{sawtooth}}\left(\omega_{\text{frac}} t\right)$ represents the sawtooth waveform with a fundamental frequency of ω_{frac} and a peak-to-peak amplitude of 1. Hence, the TDC should cover at least one oscillation cycle with fine resolution and good linearity, thereby increasing the design complexity and power consumption. Typically, the implementation of the TDC is based on inverters. Thus, its time resolution, t_{res}, is sensitive to the variation on its supply voltage,

$$t_{\text{res}} = t_{\text{res,0}} \cdot \left(1 + 0.5\alpha A_{\text{rip,loop}} \sin(\omega_{\text{rip}} t)\right), \tag{2.11}$$

where $t_{\text{res,0}}$ represents the nominal time resolution of TDC, and α is the supply sensitivity of TDC resolution in V^{-1}. As a result, the TDC output,

$\mathrm{TDC_{OUT}}$, is modulated by the supply ripple

$$\begin{aligned}\mathrm{TDC_{OUT}} &= \frac{\Delta t_{\mathrm{in,1st}}}{t_{\mathrm{res}}} = \frac{T_{\mathrm{CKV}} \cdot W_{\mathrm{sawtooth}}\left(\omega_{\mathrm{frac}} t\right)}{t_{\mathrm{res,0}} \cdot \left(1 + 0.5\alpha A_{\mathrm{rip,loop}} \sin(\omega_{\mathrm{rip}} t)\right)} \\ &\approx \frac{T_{\mathrm{CKV}} \cdot W_{\mathrm{sawtooth}}\left(\omega_{\mathrm{frac}} t\right)}{t_{\mathrm{res,0}}} \left(1 - 0.5\alpha A_{\mathrm{rip,loop}} \sin(\omega_{\mathrm{rip}} t)\right). \end{aligned} \quad (2.12)$$

The Fourier series of $W_{\mathrm{sawtooth}}\left(\omega_{\mathrm{frac}} t\right)$ is

$$W_{\mathrm{sawtooth}}\left(\omega_{\mathrm{frac}} t\right) = \frac{1}{2} + \sum_{n=1}^{\infty} \frac{1}{n\pi} \cdot \sin(n\omega_{\mathrm{frac}} t). \quad (2.13)$$

From (2.12), it is observed that the first term in (2.13) generates a DC component corresponding to the DC value of the TDC input Δt_{in}. In addition, it also generates a ω_{rip} term, $(\alpha A_{\mathrm{rip,loop}} T_{\mathrm{CKV}})/(4t_{\mathrm{res,0}}) \cdot \sin(\omega_{\mathrm{rip}} t)$, whose effect is similar to that discussed in Section 2.2. Therefore, the first term in (2.13) could be ignored in the following analysis. The second term in (2.13) will generate intermodulation terms in (2.12). We will focus on its fundamental component ($n = 1$) since it has the largest magnitude. By replacing this fundamental component into (2.12), we obtain

$$\begin{aligned}\mathrm{TDC_{OUT}} =& \frac{T_{\mathrm{CKV}} \cdot \sin(\omega_{\mathrm{frac}} t)}{\pi t_{\mathrm{res,0}}} \left(1 - 0.5\alpha A_{\mathrm{rip,loop}} \sin(\omega_{\mathrm{rip}} t)\right) \\ =& \frac{T_{\mathrm{CKV}}}{\pi t_{\mathrm{res,0}}} \sin(\omega_{\mathrm{frac}} t) + \frac{\alpha A_{\mathrm{rip,loop}} T_{\mathrm{CKV}}}{4\pi t_{\mathrm{res,0}}} \cdot \\ & \left(\cos[(\omega_{\mathrm{rip}} + \omega_{\mathrm{frac}})t] - \cos[(\omega_{\mathrm{rip}} - \omega_{\mathrm{frac}})t]\right). \end{aligned} \quad (2.14)$$

Hence, the equivalent TDC input under supply ripple, assuming a constant time resolution of $t_{\mathrm{res,0}}$, could be calculated as

$$\begin{aligned}\Delta t_{\mathrm{in,equ}} =& \frac{T_{\mathrm{CKV}}}{\pi} \sin(\omega_{\mathrm{frac}} t) + \\ & \frac{\alpha A_{\mathrm{rip,loop}} T_{\mathrm{CKV}}}{4\pi} \cdot \left(\cos[(\omega_{\mathrm{rip}} + \omega_{\mathrm{frac}})t] - \cos[(\omega_{\mathrm{rip}} - \omega_{\mathrm{frac}})t]\right). \end{aligned} \quad (2.15)$$

The first term in (2.15) is solely the result of the fractional-N operation, and is typically removed from $\mathrm{TDC_{out}}$ in digital domain afterwards in order not to affect the fractional spur level of the loop. In contrast, the second term in (2.15) contains frequency components at the intermodulation

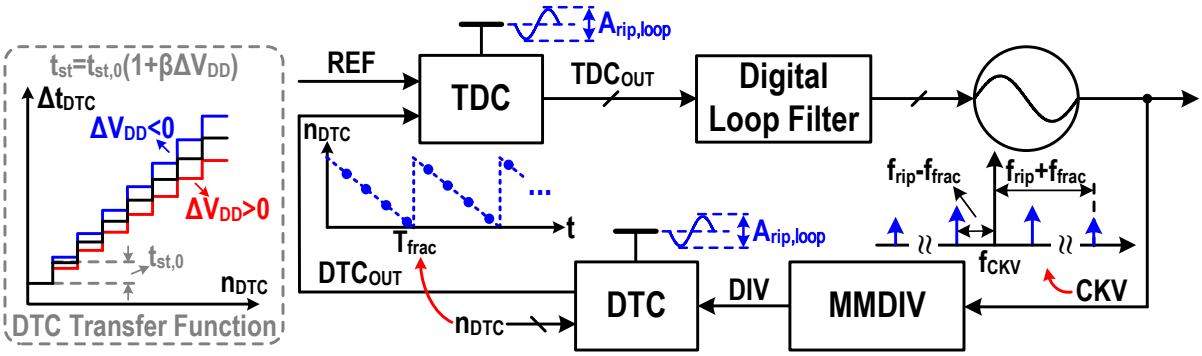


Figure 2.4: Conventional time-domain DPLL employing DTC and TDC.

frequencies, $f_{\text{rip}} \pm f_{\text{frac}}$, which, when located in-band, correspond to a phase fluctuation of

$$\Delta\phi_{\text{TDC,int}} = \frac{\alpha A_{\text{rip,loop}}}{2} \cdot \left(\cos[(\omega_{\text{rip}} + \omega_{\text{frac}})t] - \cos[(\omega_{\text{rip}} - \omega_{\text{frac}})t] \right). \quad (2.16)$$

Thus, the resulting PLL output, x_{PLL}, could be expressed as

$$\begin{aligned} x_{\text{PLL}} &= A_{\text{osc}} \sin(\omega_{\text{osc}} t + \Delta\phi_{\text{TDC,int}}) \\ &= A_{\text{osc}} \sin\left(\omega_{\text{osc}} t + \frac{\alpha A_{\text{rip,loop}}}{2} \cdot \left(\cos[(\omega_{\text{rip}} + \omega_{\text{frac}})t] - \cos[(\omega_{\text{rip}} - \omega_{\text{frac}})t] \right)\right). \end{aligned} \quad (2.17)$$

Given that $\alpha A_{\text{rip,loop}}/2$ is much less than $\pi/6$, (2.17) could then be approximated as

$$\begin{aligned} x_{\text{PLL}} \approx & A_{\text{osc}} \sin(\omega_{\text{osc}} t) \\ & + A_{\text{osc}} \cdot \frac{\alpha A_{\text{rip,loop}}}{4} \cdot \left(\cos[(\omega_{\text{osc}} + \omega_{\text{int},+})t] + \cos[(\omega_{\text{osc}} - \omega_{\text{int},+})t] \right) \\ & - A_{\text{osc}} \cdot \frac{\alpha A_{\text{rip,loop}}}{4} \cdot \left(\cos[(\omega_{\text{osc}} + \omega_{\text{int},-})t] + \cos[(\omega_{\text{osc}} - \omega_{\text{int},-})t] \right) \end{aligned} \quad (2.18)$$

in which $\omega_{\text{int},+} = \omega_{\text{rip}} + \omega_{\text{frac}}$ and $\omega_{\text{int},-} = \omega_{\text{rip}} - \omega_{\text{frac}}$. Equation (2.18) shows that the intermodulation components in $\Delta t_{\text{in,equ}}$ would generate spurs at $f_{\text{rip}} \pm f_{\text{frac}}$ with a level of $20\log_{10}(\alpha \cdot A_{\text{rip,loop}}/4)$ when they fall *in-band*.

In order to limit the TDC input range, a digital-to-time converter (DTC) is typically inserted before it [28, 29, 33, 39, 40], as shown in Fig. 2.4. The delay generated by the DTC compensates for the sawtooth phase error corresponding to the synthesized fractional channel (ω_{frac}). Hence, the

DTC input codeword may be estimated by

$$n_{\mathrm{DTC}} = \frac{T_{\mathrm{CKV}} \cdot W_{\mathrm{sawtooth}}\left(\omega_{\mathrm{frac}} t\right)}{t_{\mathrm{st},0}} \tag{2.19}$$

where $t_{\mathrm{st},0}$ is the nominal DTC time step. By virtue of the fine-resolution DTC, the TDC should ideally see a constant input. Thus, the power consumption, linearity, and supply sensitivity of the TDC can be significantly relaxed. However, the DTC performance becomes crucial as it needs to cover a large dynamic range with sufficiently fine resolution. Since the DTC delay is typically set by changing the load of an inverter [28, 41], its time step is also sensitive to supply and can be modeled by

$$t_{\mathrm{st}} = t_{\mathrm{st},0} \cdot \left(1 + 0.5\beta A_{\mathrm{rip,loop}} \sin(\omega_{\mathrm{rip}} t)\right) \tag{2.20}$$

where β is the supply sensitivity of DTC delay in V^{-1}. Consequently, the DTC output delay is modulated by the supply ripple as

$$\begin{aligned} \Delta t_{\mathrm{DTC}} &= n_{\mathrm{DTC}} \cdot t_{\mathrm{st}} \\ &= T_{\mathrm{CKV}} \cdot W_{\mathrm{sawtooth}}\left(\omega_{\mathrm{frac}} t\right) \left(1 + 0.5\beta A_{\mathrm{rip,loop}} \sin(\omega_{\mathrm{rip}} t)\right). \end{aligned} \tag{2.21}$$

Note, the Fourier series of $W_{\mathrm{sawtooth}}\left(\omega_{\mathrm{frac}} t\right)$ is already given in (2.13). Similar to the case of the PLL that only employs the TDC, the first term in (2.13) now mainly corresponds to a delay offset here, which cancels with the DC value of the delay between REF and DIV in the locking state, and can be ignored in the following analysis. The intermodulation terms are generated by the second term of (2.13), and we will also focus on its fundamental component ($n = 1$) due to its largest magnitude. By replacing this fundamental component into (2.21), we would obtain

$$\begin{aligned} \Delta t_{\mathrm{DTC}} =& T_{\mathrm{CKV}} \cdot \frac{1}{\pi} \sin(\omega_{\mathrm{frac}} t) \cdot \left(1 + 0.5\beta A_{\mathrm{rip,loop}} \sin(\omega_{\mathrm{rip}} t)\right) \\ =& \frac{T_{\mathrm{CKV}}}{\pi} \sin(\omega_{\mathrm{frac}} t) + \frac{\beta A_{\mathrm{rip,loop}} T_{\mathrm{CKV}}}{4\pi} \cdot \\ & \left(\cos[(\omega_{\mathrm{rip}} - \omega_{\mathrm{frac}})t] - \cos[(\omega_{\mathrm{rip}} + \omega_{\mathrm{frac}})t]\right) \end{aligned} \tag{2.22}$$

The first term in (2.22) compensates for the deterministic delay variation between REF and DIV due to the fractional-N operation, while its second

term contains intermodulation, potentially generating in-band spurs at the PLL output. Following a similar analysis used for the TDC based loop above, the phase fluctuation corresponding to the intermodulation terms in (2.22) is

$$\Delta\phi_{\text{DTC,int}} = \frac{\beta A_{\text{rip,loop}}}{2} \cdot (\cos[(\omega_{\text{rip}} - \omega_{\text{frac}})t] - \cos[(\omega_{\text{rip}} + \omega_{\text{frac}})t]). \quad (2.23)$$

Hence, the output signal of the PLL could be expressed as

$$\begin{aligned} x_{\text{PLL}} =& A_{\text{osc}} \sin(\omega_{\text{osc}} t + \Delta\phi_{\text{DTC,int}}) \\ =& A_{\text{osc}} \sin\left(\omega_{\text{osc}} t + \frac{\beta A_{\text{rip,loop}}}{2} \cdot (\cos[(\omega_{\text{rip}} - \omega_{\text{frac}})t] - \cos[(\omega_{\text{rip}} + \omega_{\text{frac}})t])\right). \end{aligned} \quad (2.24)$$

Since $\beta A_{\text{rip}}/2$ is much less than $\pi/6$, (2.24) could then be approximated as

$$\begin{aligned} x_{\text{PLL}} \approx& A_{\text{osc}} \sin(\omega_{\text{osc}} t) \\ &+ A_{\text{osc}} \cdot \frac{\beta A_{\text{rip,loop}}}{4} \cdot (\cos[(\omega_{\text{osc}} + \omega_{\text{int},-})t] + \cos[(\omega_{\text{osc}} - \omega_{\text{int},-})t]) \\ &- A_{\text{osc}} \cdot \frac{\beta A_{\text{rip,loop}}}{4} \cdot (\cos[(\omega_{\text{osc}} + \omega_{\text{int},+})t] + \cos[(\omega_{\text{osc}} - \omega_{\text{int},+})t]). \end{aligned} \quad (2.25)$$

From (2.25), it can be concluded that the intermodulation terms in Δt_{DTC} would also generate spurs at $f_{\text{rip}} \pm f_{\text{frac}}$ at the PLL output, and when they fall *in-band*, the spur level should be $20\log_{10}(\beta \cdot A_{\text{rip,loop}}/4)$.

Based on circuit-level simulations in the employed 40-nm CMOS technology node, α and β are around $1.2 \sim 2.05\,\text{V}^{-1}$, corresponding to a spur level of $-31.8 \sim -36.5\,\text{dBc}$ under a $50\,\text{mV}_{\text{pp}}$ ripple. Considering that f_{frac} is likely subject to frequent changes, a calibration of the intermodulation terms could be unfeasible. Thus, in order to achieve the desired spur level S_{int}, $A_{\text{rip,loop}}$ should satisfy the following requirement

$$A_{\text{rip,loop}} < \frac{4 \cdot 10^{S_{\text{int}}/20}}{K_{\text{PD,rip}}} \quad (2.26)$$

where $K_{\text{PD,rip}}$ represents the supply sensitivity of the PD and equals to α and β for the DPLL structure shown in Fig. 2.3 and Fig. 2.4, respectively.

2.3.1 Effect of Higher-Order Modulation

The analysis above assumes that a first-order $\Delta\Sigma$ modulation is used in the loop. Nevertheless, the conclusion of reducing the PD supply sensitivity and the requirement on $A_{\text{rip,loop}}$ could also be extended to a higher-order modulation. For a higher-order modulation, the sawtooth pattern at the PD input would be randomized, reducing the spur level due to the intermodulation. However, its quantization noise around f_{rip} will be down-converted by the DTC/TDC supply sensitivity, thus degrading the in-band PN. Therefore, it is still necessary to improve the supply sensitivity of PD and/or reduce the amplitude of the supply ripple.

Consider the loop in Fig. 2.4 as an example. Assuming the integer divider is driven by an n^{th} order $\Delta\Sigma$ modulator, then (2.21) is rewritten as

$$\begin{aligned}\Delta t_{\text{DTC}} &= T_{\text{CKV}} \cdot W_{\text{DSM}}(t)\left(1 + 0.5\beta A_{\text{rip,loop}} \sin(\omega_{\text{rip}} t)\right) \\ &= T_{\text{CKV}} \cdot W_{\text{DSM}}(t) + \frac{\beta A_{\text{rip,loop}}}{2} \cdot T_{\text{CKV}} \cdot W_{\text{DSM}}(t) \sin(\omega_{\text{rip}} t) \end{aligned} \quad (2.27)$$

in which $W_{\text{DSM}}(t)$ represents the waveform of the accumulated quantization error of the $\Delta\Sigma$ modulator, which falls back to $W_{\text{sawtooth}}(\omega_{\text{frac}} t)$ for a first-order modulation. The first term in (2.27) is desired as it compensates for the deterministic time error between REF and DIV due to the modulation. In contrast, the second term proves that under the supply ripple, the accumulated quantization noise of the $\Delta\Sigma$ modulator would be scaled by the supply sensitivity of the DTC time step and down-converted by f_{rip}. Since the transfer function from DTC_{OUT} to the DPLL output is low-pass shaped, this noise down-conversion may raise the in-band phase noise of the loop.

Converting (2.27) into the phase domain, we obtain

$$\begin{aligned}\Delta\phi_{\text{DTC}} &= 2\pi \cdot \frac{\Delta t_{\text{DTC}}}{T_{\text{CKV}}} \\ &= W_{\phi,\text{DSM}}(t) + \frac{\beta A_{\text{rip,loop}}}{2} \cdot W_{\phi,\text{DSM}}(t) \sin(\omega_{\text{rip}} t). \end{aligned} \quad (2.28)$$

In (2.28), $W_{\phi,\text{DSM}}(t) = 2\pi \cdot W_{\text{DSM}}(t)$ is the phase error between REF and DIV induced by the modulation, and its power spectrum density (PSD)

could be expressed as

$$S_{\phi,\text{DSM}}(\Delta f) = \frac{(2\pi)^2}{12} \cdot \frac{1}{f_{\text{ref}}} \cdot \left(2\sin\left(\frac{\pi\Delta f}{f_{\text{ref}}}\right)\right)^{2(n-1)}. \tag{2.29}$$

Note that due to the accumulation of the quantization error in the loop, the order of $S_{\phi,\text{DSM}}(\Delta f)$ is 1 less than that of the $\Delta\Sigma$ modulator. The second term in (2.28) is the product of $W_{\phi,\text{DSM}}(t)$ and a sinewave at f_{rip}. Hence, its PSD could be obtained through convolving $S_{\phi,\text{DSM}}(\Delta f)$ with the PSD of the sinewave. Therefore, the PSD of $\Delta\phi_{\text{DTC}}$ could be calculated as

$$\begin{aligned} S_{\Delta\phi_{\text{DTC}}}(\Delta f) =& S_{\phi,\text{DSM}}(\Delta f) + \frac{(\beta A_{\text{rip,loop}})^2}{16} \cdot \\ & \left(S_{\phi,\text{DSM}}(\Delta f - f_{\text{rip}}) + S_{\phi,\text{DSM}}(\Delta f + f_{\text{rip}})\right). \end{aligned} \tag{2.30}$$

As mentioned previously, the second term in (2.30) is the PSD of the down-converted accumulated quantization noise of the $\Delta\Sigma$ modulator. Its magnitude is proportional to the square of both β and the ripple amplitude, which is easily expected from the analysis above.

To preserve the inherent phase noise performance under supply variation, the supply sensitivity of DTC time step, β, should be limited. Given the phase noise $\mathcal{L}(\Delta f)$ of the PLL, we have

$$\frac{(\beta A_{\text{rip,loop}})^2}{16}\left(S_{\phi,\text{DSM}}(\Delta f - f_{\text{rip}}) + S_{\phi,\text{DSM}}(\Delta f + f_{\text{rip}})\right) \ll 10^{\mathcal{L}(\Delta f)/10}. \tag{2.31}$$

When in-band phase noise is considered, we have $\Delta f \ll f_{\text{rip}}$. Thus (2.31) becomes

$$\frac{(\beta A_{\text{rip,loop}})^2}{8} \cdot \frac{(2\pi)^2}{12} \cdot \frac{1}{f_{\text{ref}}} \cdot \left(2\sin\left(\frac{\pi f_{\text{rip}}}{f_{\text{ref}}}\right)\right)^{2(n-1)} \ll 10^{\mathcal{L}(\Delta f)/10}. \tag{2.32}$$

Therefore, the requirement on β is

$$\beta \ll \frac{2\sqrt{6 f_{\text{ref}}}}{\pi A_{\text{rip,loop}}} \cdot \frac{10^{\mathcal{L}(\Delta f)/20}}{\left(2\sin\left(\pi f_{\text{rip}}/f_{\text{ref}}\right)\right)^{(n-1)}} \tag{2.33}$$

The result in (2.33) shows that the maximum β allowed is reduced for a higher f_{rip} and would reach the minimum value when $f_{\text{rip}} = 0.5 f_{\text{ref}}$. This

is in accordance with the analysis above, since the quantization noise from the $\Delta\Sigma$ modulator is high pass shaped and reaches its maximum value at $0.5f_{\text{ref}}$. For $A_{\text{rip,loop}} = 50\,\text{mV}$, $f_{\text{ref}} = 50\,\text{MHz}$ and $f_{\text{rip}} = f_{\text{ref}}/3$, calculations show that $\beta \ll 1.27$ is required for an in-band PN of -100 dBc/Hz when the second-order $\Delta\Sigma$ modulator is employed. If we want to limit the PN degradation due to the intermodulation effect to 1 dB (0.5 dB), the down-converted noise should be at least $\sim 6\,\text{dBc}$ ($\sim 10\,\text{dBc}$) lower than the in-band PN. Based on (2.33), we can then calculate that $\beta < 0.638\,(0.402)$, which is still much lower than the simulated value mentioned above.

Similar to the analysis in previous sections, $A_{\text{rip,loop}}$ could be reduced to relax the requirement on β. From (2.32), the requirement of the ripple amplitude for a certain β value is derived as

$$A_{\text{rip,loop}} \ll \frac{2\sqrt{6f_{\text{ref}}}}{\pi\beta} \cdot \frac{10^{\mathcal{L}(\Delta f)/20}}{\left(2\sin\left(\pi f_{\text{rip}}/f_{\text{ref}}\right)\right)^{(n-1)}}. \tag{2.34}$$

To limit the PN degradation within 0.5 dB, (2.34) would become

$$A_{\text{rip,loop}} < \sqrt{\frac{12f_{\text{ref}}}{5}} \cdot \frac{1}{\pi\beta} \cdot \frac{10^{\mathcal{L}(\Delta f)/20}}{\left(2\sin\left(\pi f_{\text{rip}}/f_{\text{ref}}\right)\right)^{(n-1)}}. \tag{2.35}$$

The analysis of the loop in Fig. 2.3 would be similar to the aforementioned discussions. At the same time, by replacing the supply sensitivity of DTC delay (β) with the supply sensitivity of TDC resolution (α), Equations (2.31) to (2.35) remain valid.

2.4 Conclusion

This chapter analyzes the effects of the output ripple of a DC-DC converter on the spectral purity of the PLL. The quantitative analysis reveals that the generation of spurs at the ripple frequency due to the oscillator supply pushing or the supply induced delay variations of loop components in the PLL output demands either a lower ripple amplitude or suppressed supply sensitivities of the oscillation frequency and components' delay to meet the corresponding performance requirement. It also shows that the supply sensitivity of the phase detector (PD) would lead to

intermodulation between the fractional frequency and the ripple frequency, possibly degrading the spur performance or in-band phase noise depending on the order of $\Delta\Sigma$ modulation used in the loop. Similarly, this places corresponding limitations on the ripple amplitude or the PD sensitivity in order to meet the relevant requirement.

Chapter

3

Analysis of LDO Efficiency

A brief analysis of a low dropout (LDO) linear regulator is presented in this chapter[1]. Based on the position of the dominant pole, LDOs are divided into two types of typologies with very different power supply rejection performance. For the LDO typology with the dominant pole located at the output of the error amplifier, the limitation on its power efficiency is derived based on the practical requirements of the oscillator and the PLL. Based on this, different powering scenarios of a system-on-chip are further identified and briefly discussed.

[1]Part of the material in this chapter has been published in the IEEE Transactions on Circuits and Systems I (TCAS-I) [42].

3.1 Introduction

As already shown in Chapter 1, integrated circuits and systems powered by batteries or energy harvesters generally need buck and/or boost switching DC-DC converters, which transform the output levels of energy sources to the system's nominal supply voltage with sufficiently high efficiency [43]. However, as discussed in Chapter 2, if the DC-DC converter directly supplies sensitive analog or RF components, such as oscillators and phase-locked loops (PLLs), its output ripples can severely degrade their performance. Consequently, a low dropout (LDO) linear regulator is typically inserted after the switching converter to suppress the ripples and stabilize the supply voltage (see Fig. 1.3). In order to provide adequate ripple suppression with low output noise, an LDO may require additional off-chip components and/or relatively high voltage and current overhead, thus degrading the system power efficiency. Moreover, to isolate the sensitive oscillator from the clocked phase detection circuitry, PLLs usually require two separate LDOs [44], further worsening the system complexity and cost (see Fig. 3.1).

In this chapter, a brief analysis of the LDO performance is presented. Based on the practical requirements of oscillators and PLLs, the limitation on power efficiency of LDOs is derived, indicating the benefits of designing PLLs that could operate directly under the outputs of the DC-DC converters.

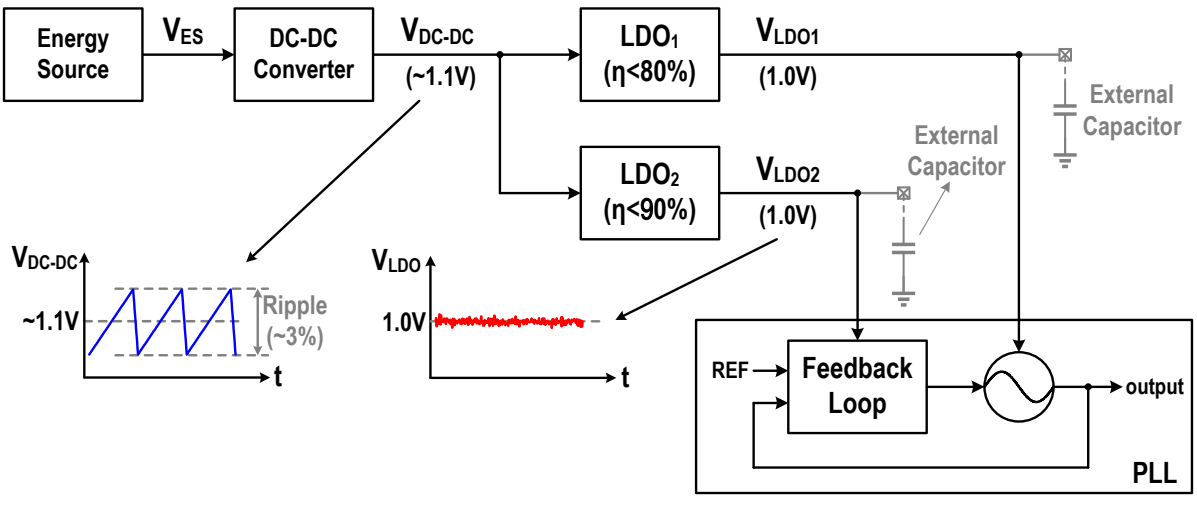


Figure 3.1: Conventional arrangement to power up a PLL system through the cascade of a DC-DC converter with LDOs.

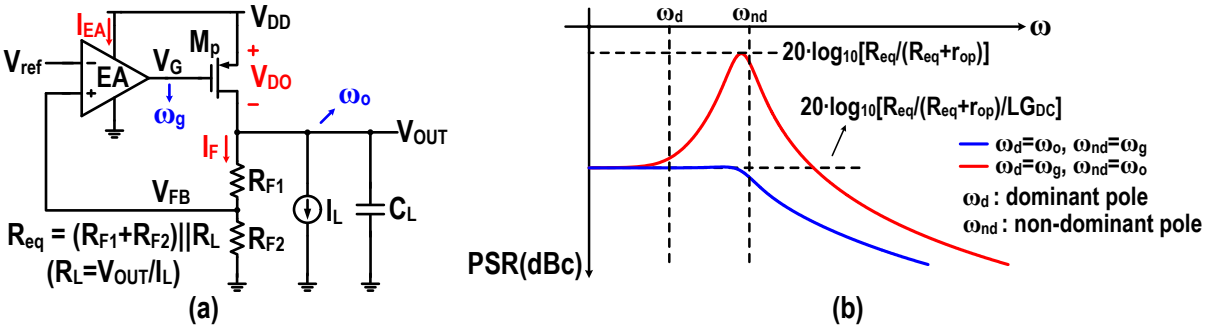


Figure 3.2: (a) Block diagram and (b) PSR response of typical LDO topologies when V_{G} is tightly coupled to V_{DD}.

3.2 LDO Topologies

The LDO shown in Fig. 3.2 (a) consists of a pass transistor ($\mathrm{M_p}$), an error amplifier (EA), a feedback network (R_{F1} and R_{F2}), and an accurate voltage reference (V_{ref}). To suppress the ripple on V_{DD} at the LDO output, V_{OUT}, the LDO operates in a feedback manner. R_{F1} and R_{F2} shift V_{OUT} to a proper level

$$V_{\mathrm{FB}} = \frac{R_{\mathrm{F2}}}{R_{\mathrm{F1}} + R_{\mathrm{F2}}} \cdot V_{\mathrm{OUT}} = \beta_{\mathrm{F}} \cdot V_{\mathrm{OUT}}, \tag{3.1}$$

where $\beta_{\mathrm{F}} = R_{\mathrm{F2}}/(R_{\mathrm{F1}} + R_{\mathrm{F2}})$ is the feedback factor of the network. V_{FB} is then compared with V_{ref} through the EA. The output of EA modulates the gate terminal of $\mathrm{M_p}$, V_{G}, such that V_{OUT} is kept constant. In steady state, the DC level of V_{OUT} could be estimated as

$$V_{\mathrm{OUT}} \approx \left(1 + \frac{R_{\mathrm{F1}}}{R_{\mathrm{F2}}}\right) V_{\mathrm{ref}} = \frac{V_{\mathrm{ref}}}{\beta_F} \tag{3.2}$$

where the DC gain of EA, $A_{\mathrm{EA},0}$, is assumed to be sufficiently high.

The power supply rejection (PSR) of the LDO, defined as the ratio between the voltage fluctuation amplitude at V_{OUT} and V_{DD}, could be calculated as

$$\mathrm{PSR} = \frac{\Delta V_{\mathrm{OUT}}}{\Delta V_{\mathrm{DD}}} = \frac{1 + g_{\mathrm{mp}} r_{\mathrm{op}}}{1 + g_{\mathrm{mp}} r_{\mathrm{op}} \beta_{\mathrm{F}} A_{\mathrm{EA}}(s) + r_{\mathrm{op}} \left(\frac{1}{R_{\mathrm{F1}}+R_{\mathrm{F2}}} + \frac{1}{R_{\mathrm{L}}} + sC_{\mathrm{L}}\right)} \tag{3.3}$$

where $A_{\mathrm{EA}}(s)$ represents the gain of EA, and g_{mp} and r_{op} are the transconductance and output resistance of $\mathrm{M_p}$, respectively. For a simple EA with

the dominant main pole at its output (ω_g), $A_{\mathrm{EA}}(s)$ could be expressed as

$$A_{\mathrm{EA}}(s) = \frac{A_{\mathrm{EA},0}}{1 + s/\omega_g}. \tag{3.4}$$

Then, (3.3) could be rewritten as

$$\mathrm{PSR} = \frac{(g_{\mathrm{mp}} + 1/r_{\mathrm{op}})\,(r_{\mathrm{op}} \parallel R_{\mathrm{eq}}) \cdot (1 + s/\omega_g)}{(1 + s/\omega_g)\,(1 + s/\omega_o) + \beta_{\mathrm{F}} \cdot g_{\mathrm{mp}}\,(r_{\mathrm{op}} \parallel R_{\mathrm{eq}}) \cdot A_{\mathrm{EA},0}} \tag{3.5}$$

where $R_{\mathrm{eq}} = (R_{\mathrm{F1}} + R_{\mathrm{F2}}) \parallel R_{\mathrm{L}}$, and $\omega_o = ((r_{\mathrm{op}} \parallel R_{\mathrm{eq}})\, C_{\mathrm{L}})^{-1}$ is the pole frequency at the output node. Since the gain of the output $\mathrm{M_p}$ stage is

$$A_{\mathrm{O}}(s) = \frac{A_{\mathrm{O},0}}{1 + s/\omega_o} = \frac{g_{\mathrm{mp}}\,(r_{\mathrm{op}} \parallel R_{\mathrm{eq}})}{1 + s/\omega_o}, \tag{3.6}$$

the PSR could be simplified as

$$\mathrm{PSR} = \frac{A_{\mathrm{O}}\,(s) + R_{\mathrm{eq}}/(r_{\mathrm{op}} + R_{\mathrm{eq}}) \cdot 1/(1 + s/\omega_o)}{1 + \beta_{\mathrm{F}} A_{\mathrm{O}}\,(s)\, A_{\mathrm{EA}}\,(s)} \tag{3.7}$$

$$= \frac{(g_{\mathrm{mp}} + 1/r_{\mathrm{op}})\,(r_{\mathrm{op}} \parallel R_{\mathrm{eq}}) \cdot (1 + s/\omega_g)}{(1 + s/\omega_g)\,(1 + s/\omega_o) + \beta_{\mathrm{F}} \cdot A_{\mathrm{O},0} \cdot A_{\mathrm{EA},0}}. \tag{3.8}$$

Note that the expression in (3.7) is in accordance with the feedback theory, and the second term in its numerator is caused by r_{op}, which directly links the system input (V_{DD}) and output (V_{OUT}).

In order to provide a better insight into the PSR behavior of the LDO, it is sometimes assumed that the V_{DD} variation is directly passed on to V_{G} across all frequencies (through a coupling capacitor between V_{G} and V_{DD} for example) [45–47]. Under this assumption, the PSR expression becomes

$$\mathrm{PSR} = \frac{R_{\mathrm{eq}}/(r_{\mathrm{op}} + R_{\mathrm{eq}}) \cdot (1 + s/\omega_g)}{(1 + s/\omega_g)\,(1 + s/\omega_o) + \beta_{\mathrm{F}} \cdot A_{\mathrm{O},0} \cdot A_{\mathrm{EA},0}}. \tag{3.9}$$

Compared to (3.5) and (3.8), (3.9) reveals that the PSR is worsened when V_{G} is not perfectly coupled to V_{DD} since g_{mp} would inject an extra ripple-induced current into the load impedance.

The analysis above shows that the LDO is a two-pole system with the poles located at the LDO output (ω_o) and the output of the EA (ω_g),

respectively. Depending on whether ω_o or ω_g is the dominant pole of the system, LDOs could be divided into two main topological types with very different PSR performance [45–48]. For the ω_o-dominant topology, a high PSR at high frequencies is easily obtained since the output capacitor, C_{L}, provides a low-impedance path to ground for supply ripples with frequencies higher than the closed-loop bandwidth (ω_{REG}) of the regulator (blue curve in Fig. 3.2 (b)). For frequencies below ω_{REG}, PSR remains flat since the -20 dB/decade reduction in the loop gain above ω_o is compensated by the open-loop PSR improvement due to the same filtering effect of C_{L}. Although superior PSR performance over the entire frequency range could be achieved by this LDO topology, the value of C_{L} could be increased in the μF range to guarantee the loop stability [49], leading to integration difficulties. The ω_g-dominant topology, also referred to as a 'capacitor-less' LDO in the literature, avoids the use of large C_{L}, but the PSR starts to degrade after ω_g due to the roll-off in the loop gain (red curve in Fig. 3.2 (b)) [47, 48, 50, 51]. From (3.9), the PSR of this topology would peak to its worst value of about $R_{\mathrm{eq}}/(r_{\mathrm{op}} + R_{\mathrm{eq}})$ at around ω_{REG}. If V_{G} is not coupled to V_{DD}, the level of this peak would further increase to about $g_{\mathrm{mp}}\,(r_{\mathrm{op}} \parallel R_{\mathrm{eq}}) + R_{\mathrm{eq}}/(r_{\mathrm{op}} + R_{\mathrm{eq}})$, as can be estimated from (3.8). When the frequency is increased beyond ω_o, C_{L} suppresses the supply ripple and the PSR improves by 20 dB/decade. Favoring a full-system integration, the capacitor-less LDO topology is chosen as the main focus of the following analysis in this chapter.

3.3 Performance of LDO

The performance of the LDO could be described by a set of metrics, including the PSR, the output noise, the dropout voltage, line and load regulation, line and load transient response, etc. [52]. Since the power efficiency of the system is of interest here, this chapter will mainly focus on the PSR and the output noise requirements when powering a PLL, as they have a direct impact on the LDO efficiency.

3.3.1 PSR Requirement

When supplied by a switched-capacitor DC-DC converter, the amplitude of the sawtooth-shaped ripple on V_{DD} is related to both the output current and the flying capacitor (C_{fly}) of the converter. Assume that the output current of the converter is dominated by the load current (I_{L}) of the LDO, then the peak-to-peak ripple amplitude could be expressed as

$$A_{\mathrm{rip,saw}} = \frac{I_{\mathrm{L}}}{C_{\mathrm{fly}} f_{\mathrm{SW}}} \tag{3.10}$$

where f_{SW} is the switching frequency of the converter and typically equals to the ripple frequency, f_{rip}, at V_{DD}. From (3.10), the peak-to-peak amplitude of the fundamental component of the saw-tooth ripple is calculated as

$$A_{\mathrm{rip}} = \frac{2A_{\mathrm{rip,saw}}}{\pi} = \frac{2I_{\mathrm{L}}}{\pi C_{\mathrm{fly}} f_{\mathrm{SW}}}. \tag{3.11}$$

For oscillators, the maximum ripple amplitude on V_{OUT} that could be tolerated for a desired spur level due to supply pushing is given in (2.2), which is rewritten here for convenience

$$A_{\mathrm{rip,osc}} < \frac{4f_{\mathrm{rip}}}{K_{\mathrm{push}}} 10^{S_{\mathrm{osc}}/20}. \tag{3.12}$$

Combining (3.11) and (3.12), the required PSR of the LDO powering the oscillator should be

$$\mathrm{PSR}_{\mathrm{osc}} = \frac{A_{\mathrm{rip,osc}}}{A_{\mathrm{rip}}} < \frac{2\pi C_{\mathrm{fly}} f_{\mathrm{rip}}^2 10^{S_{\mathrm{osc}}/20}}{I_{\mathrm{osc}} K_{\mathrm{push}}} \tag{3.13}$$

where I_{osc} is the current consumption of the oscillator. Note that there is a quadratic relation between $\mathrm{PSR}_{\mathrm{osc}}$ and f_{rip} since both the output ripple amplitude of the converter and the filtering capability of the oscillator tank improve simultaneously by increasing f_{rip}. However, it comes at the price of a higher dynamic power consumption driving the converter switches, potentially degrading the system efficiency.

For other loop components, as discussed in Section 2.2, the variation of their output delay induced by the supply ripple also leads to spurs at f_{rip}.

Therefore, the tolerable ripple amplitude is expressed as

$$A_{\text{rip,loop}} < \frac{2 \cdot 10^{(S_{\text{dly}} - \text{TF}_{\text{loop}}(f_{\text{rip}}))/20}}{\pi f_{\text{osc}} K_{\text{rip}}}. \tag{3.14}$$

Comparing (3.14) with (3.11), the PSR of the LDO powering the loop components is calculated to be

$$\text{PSR}_{\text{loop}} = \frac{A_{\text{rip,loop}}}{A_{\text{rip}}} < \frac{C_{\text{fly}} f_{\text{rip}} 10^{(S_{\text{dly}} - \text{TF}_{\text{loop}}(f_{\text{rip}}))/20}}{I_{\text{loop}} f_{\text{osc}} K_{\text{rip}}}. \tag{3.15}$$

where I_{loop} is the current consumption of loop components. As expected, PSR_{loop} is inversely proportional to f_{osc} since a similar delay variation corresponds to a higher phase deviation when f_{osc} increased.

When a fractional-N PLL is considered, the intermodulation between f_{frac} and f_{rip} due to the supply sensitivity of PD is discussed in detail in Section 2.3. For a first-order $\Delta\Sigma$ modulation, Equation (2.26) shows that $A_{\text{rip,loop}}$ should be constrained to

$$A_{\text{rip,loop}} < \frac{4 \cdot 10^{S_{\text{int}}/20}}{K_{\text{PD,rip}}}, \tag{3.16}$$

leading to a PSR of

$$\text{PSR}_{\text{loop}} = \frac{A_{\text{rip,loop}}}{A_{\text{rip}}} < \frac{2\pi C_{\text{fly}} f_{\text{rip}} 10^{S_{\text{int}}/20}}{K_{\text{PD,rip}} I_{\text{loop}}}. \tag{3.17}$$

For a higher-order modulation, Equation (2.34), which is also repeated below, sets the limitation on $A_{\text{rip,loop}}$ in order not to affect the inherent PN of the PLL

$$A_{\text{rip,loop}} \ll \frac{2\sqrt{6 f_{\text{ref}}}}{\pi K_{\text{PD,rip}}} \cdot \frac{10^{\mathcal{L}(\Delta f)/20}}{\left(2 \sin\left(\pi f_{\text{rip}} / f_{\text{ref}}\right)\right)^{(n-1)}}. \tag{3.18}$$

Thus, the required PSR of the LDO becomes

$$\text{PSR}_{\text{loop}} = \frac{A_{\text{rip,loop}}}{A_{\text{rip}}} \ll \frac{\sqrt{6 f_{\text{ref}}}}{K_{\text{PD,rip}} I_{\text{loop}}} \cdot \frac{C_{\text{fly}} f_{\text{rip}} \cdot 10^{\mathcal{L}(\Delta f)/20}}{\left(2 \sin\left(\pi f_{\text{rip}} / f_{\text{ref}}\right)\right)^{(n-1)}} \tag{3.19}$$

If the PN degradation should be within 0.5 dB, then (3.19) would become

$$\mathrm{PSR}_{\mathrm{loop}} = \frac{A_{\mathrm{rip,loop}}}{A_{\mathrm{rip}}} < \sqrt{\frac{3f_{\mathrm{ref}}}{5}} \cdot \frac{C_{\mathrm{fly}} f_{\mathrm{rip}}}{K_{\mathrm{PD,rip}} I_{\mathrm{loop}}} \cdot \frac{10^{\mathcal{L}(\Delta f)/20}}{\left(2\sin\left(\pi f_{\mathrm{rip}}/f_{\mathrm{ref}}\right)\right)^{(n-1)}} \quad (3.20)$$

In practical designs, the minimum value calculated through (3.15) and (3.17) or (3.20) should be chosen as the PSR requirement of the LDO powering the loop components.

3.3.2 Noise Requirement

Besides the PSR requirements, the output noise is also an important performance metric of an LDO. Since this noise is applied on the supply of the PLL circuitry, it may degrade the output PN performance of the loop.

When the oscillator is considered, similar to the case of supply ripples, the noise on the supply would also modulate f_{osc}. Therefore, the PN induced by the noise on the oscillator supply can be estimated by

$$\mathcal{L}_{\mathrm{osc,sup}}(\Delta f) = 10\log_{10}\left(\frac{K_{\mathrm{push}}^2 \overline{v_{\mathrm{n,supo}}^2(\Delta f)}}{\Delta f^2}\right) \quad (3.21)$$

where $\overline{v_{\mathrm{n,supo}}^2(\Delta f)}$ is the PSD of the oscillator supply noise. To preserve the inherent PN of oscillator $[\mathcal{L}_{\mathrm{osc}}(\Delta f)]$, especially at higher frequency offset where the PN of the PLL is dominanted by the oscillator PN, it is required that $\mathcal{L}_{\mathrm{osc,sup}}(\Delta f) \ll \mathcal{L}_{\mathrm{osc}}(\Delta f)$, leading to the following requirement

$$\overline{v_{\mathrm{n,supo}}^2(\Delta f)} \ll \frac{10^{-\mathrm{FoM_{osc}}/10}}{10^3 P_{\mathrm{osc}}} \left(\frac{f_{\mathrm{osc}}}{K_{\mathrm{push}}}\right)^2 \quad (3.22)$$

in which $\mathrm{FoM_{osc}}$ and P_{osc} are the Figure-of-Merit and power consumption of the oscillator respectively. To keep the noise degradation within ∼0.5 dB, i.e. $\mathcal{L}_{\mathrm{osc,sup}}(\Delta f) < \mathcal{L}_{\mathrm{osc}}(\Delta f)$ - 10 dB, then the oscillator supply noise should be

$$\overline{v_{\mathrm{n,supo}}^2(\Delta f)} < \frac{1}{10} \cdot \frac{10^{-\mathrm{FoM_{osc}}/10}}{10^3 P_{\mathrm{osc}}} \left(\frac{f_{\mathrm{osc}}}{K_{\mathrm{push}}}\right)^2 \quad (3.23)$$

The expression in (3.22) and (3.23) seems to indicates that a larger supply noise can be tolerated by the oscillator at a higher f_{osc}. However, for the

LC oscillator which is typically used due to its better PN performance, the total tank capacitance (C_{tot}) is composed of a variable capacitor used to tune f_{osc} and a voltage-dependent parasitic capacitance of the oscillator core transistors (C_{par}). Hence, the effective value of C_{par} is modulated by the supply voltage. As f_{osc} increases, the variable capacitance is reduced, and C_{par} becomes a bigger portion of C_{tot}, thereby increasing K_{push}. Consequently, $f_{\text{osc}}/K_{\text{push}}$ remain almost constant over the f_{osc} range. Meanwhile, the variation of the equivalent value of C_{par} ($C_{\text{par,equ}}$) comes from the fact that the time interval during which the transistors stay in various operating regions is altered when the oscillation amplitude varies due to the supply ripple. When f_{rip} increases, such variations show shorter patterns. However, the ratio of variation in each operating region to the period of the supply ripple remains relatively constant, leading to a similar variation of $C_{\text{par,equ}}$. Therefore, K_{push} is weakly related to f_{rip}. Based on the discussion above, it could be concluded that (3.22) and (3.23) has provided a general requirement on the oscillator supply noise independent of f_{osc} and f_{rip}.

For other loop components, the output delay would also be varied by the noise on their supply voltage, leading to extra phase deviation at the PD input. To guarantee that the PN of the PLL is not degraded, it is required that

$$K_{\text{rip}}^2 \overline{v_{\text{n,supc}}^2(\Delta f)} \cdot (2\pi f_{\text{osc}})^2 \ll 10^{\mathcal{L}_{\text{loop}}(\Delta f)/10} \tag{3.24}$$

where $\overline{v_{\text{n,supc}}^2(\Delta f)}$ is the PSD of the supply noise of loop components, and $\mathcal{L}_{\text{loop}}(\Delta f)$ represents the inherent PN contributed by loop components. Therefore, the required output noise of the corresponding LDO could be calculated as

$$\overline{v_{\text{n,supc}}^2(\Delta f)} \ll \frac{10^{\mathcal{L}_{\text{loop}}(\Delta f)/10}}{(2\pi K_{\text{rip}} f_{\text{osc}})^2}. \tag{3.25}$$

Superficially, Equation (3.25) seems to indicate that a lower noise level could be tolerated at a higher f_{osc}. However, such a conclusion fails to take into consideration the dependence of $\mathcal{L}_{\text{loop}}(\Delta f)$ on f_{osc}. Adopting the Figure-of-Merit of the loop components [14]

$$\text{FoM}_{\text{loop}} = |\mathcal{L}_{\text{loop}}(\Delta f)| + 20\log_{10}\left(\frac{f_{\text{osc}}}{1\,\text{Hz}}\right) - 10\log_{10}\left(\frac{P_{\text{loop}}}{1\,\text{mW}}\right), \tag{3.26}$$

in which P_{loop} is the power consumption of loop components, Equation (3.25) could be rewritten as

$$\overline{v_{\text{n,supc}}^2(\Delta f)} \ll \frac{10^{-\text{FoM}_{\text{loop}}/10}}{10^3 P_{\text{loop}}} \left(\frac{1}{2\pi K_{\text{rip}}}\right)^2. \tag{3.27}$$

When the noise degradation should be limited to ∼0.5 dB, i.e. the noise induced by $\overline{v_{\text{n,supc}}^2(\Delta f)}$ is more than 10 dB lower than $\mathcal{L}_{\text{loop}}(\Delta f)$, (3.27) becomes

$$\overline{v_{\text{n,supc}}^2(\Delta f)} < \frac{1}{10} \cdot \frac{10^{-\text{FoM}_{\text{loop}}/10}}{10^3 P_{\text{loop}}} \left(\frac{1}{2\pi K_{\text{rip}}}\right)^2. \tag{3.28}$$

Since K_{rip} is not related to f_{rip}, (3.27) and (3.28) has also set the general requirement on the supply noise of the loop component independent of f_{osc} and f_{rip}.

3.3.3 Power Efficiency

The power efficiency of the LDO can be expressed as

$$\eta = \frac{V_{\text{OUT}}}{V_{\text{DD}}} \cdot \frac{I_{\text{L}}}{I_{\text{L}} + I_{\text{Q}}} = \frac{V_{\text{DD}} - V_{\text{SD}}}{V_{\text{DD}}} \cdot \frac{I_{\text{L}}}{I_{\text{L}} + I_{\text{F}} + I_{\text{EA}}} \tag{3.29}$$

where V_{SD} is the voltage drop across the source and drain terminal of transistor M_{p}, and I_{Q} is the quiescent current of the LDO which mainly consists of the current flowing through the feedback resistors (I_{F}) and the EA (I_{EA}). The minimum value of V_{SD} without degrading the LDO performance is named the dropout voltage, V_{DO}. Hence, the maximum achievable power efficiency of the LDO is

$$\eta_{max} = \frac{V_{\text{DD}} - V_{\text{DO}}}{V_{\text{DD}}} \cdot \frac{I_{\text{L}}}{I_{\text{L}} + I_{\text{F}} + I_{\text{EA}}} \approx \left(1 - \frac{V_{\text{DO}}}{V_{\text{DD}}}\right)\left(1 - \frac{I_{\text{F}}}{I_{\text{L}}} - \frac{I_{\text{EA}}}{I_{\text{L}}}\right) \tag{3.30}$$

in which I_{F} and I_{EA} is assumed to be much smaller than I_{L}.

Several LDOs with $\eta > 95\%$ are reported in literature [9, 53, 54]. However, they do not meet the requirements discussed previously. Therefore, the goal of the following section is to quantify the efficiency degradation of the LDO while satisfying the aforementioned requirements.

3.4 Limitation on Power Efficiency

To calculate the limitation on the power efficiency of the LDO, Section 3.3.3 reveals that its dropout voltage V_{DO} and quiescent current I_{Q} need to be quantified. As will be shown later, I_{Q} is mainly determined by the output noise of the LDO, while V_{DO} is related to its PSR performance.

3.4.1 Limitation Due to I_{F}

The thermal noise generated by the resistors in the feedback network, with a two-sided PSD of $2kT\left(R_{\mathrm{F1}} \parallel R_{\mathrm{F2}}\right)$, directly appears at the input of the EA. When transferred to V_{OUT}, its PSD is scaled by $1/\beta_{\mathrm{F}}^2$ at low frequencies, resulting in

$$\overline{v_{\mathrm{n,OUT,R}}^2} = \frac{2kT\left(R_{\mathrm{F1}} \parallel R_{\mathrm{F2}}\right)}{\beta_{\mathrm{F}}^2} = \left(\frac{R_{\mathrm{F1}}}{R_{\mathrm{F2}}}\right) 2kT\left(R_{\mathrm{F1}} + R_{\mathrm{F2}}\right). \tag{3.31}$$

This value begin to roll-off only when the frequency is increased above ω_{REG}. Therefore, in order not to affect the noise performance of the circuit being driven, it is required that the extra output noise induced by $\overline{v_{\mathrm{n,OUT,R}}^2}$ should be much less than the inherent noise of the circuit.

By using (3.23) and (3.31), we have

$$\left(\frac{R_{\mathrm{F1}}}{R_{\mathrm{F2}}}\right) 2kT\left(R_{\mathrm{F1}} + R_{\mathrm{F2}}\right) < \frac{1}{10} \cdot \frac{10^{-\mathrm{FoM_{osc}}/10}}{10^3 P_{\mathrm{osc}}} \left(\frac{f_{\mathrm{osc}}}{K_{\mathrm{push}}}\right)^2. \tag{3.32}$$

Given that $P_{\mathrm{osc}} = V_{\mathrm{OUT}} \cdot I_{\mathrm{osc}}$ and $I_{\mathrm{F}} = V_{\mathrm{OUT}}/(R_{\mathrm{F1}} + R_{\mathrm{F2}})$, (3.32) can be rewritten as

$$\left(\frac{I_{\mathrm{F}}}{I_{\mathrm{osc}}}\right) > 10 \cdot \frac{2kT\left(1/\beta_{\mathrm{F}} - 1\right) V_{\mathrm{OUT}}^2}{10^{-(\mathrm{FoM_{osc}}+30)/10}} \left(\frac{K_{\mathrm{push}}}{f_{\mathrm{osc}}}\right)^2 \tag{3.33}$$

Similarly, through combining (3.28) and (3.31), it could be derived that

$$\left(\frac{I_{\mathrm{F}}}{I_{\mathrm{loop}}}\right) > 10 \cdot \frac{2kT\left(1/\beta_{\mathrm{F}} - 1\right) V_{\mathrm{OUT}}^2}{10^{-(\mathrm{FoM_{loop}}+30)/10}} \left(2\pi K_{\mathrm{rip}}\right)^2 \tag{3.34}$$

Based on (3.33) and (3.34), it is worth to point out that the efficiency degradation due to I_{F} does not change with the load current for a constant

V_{OUT}. Indeed, when the I_{L} increases, the noise power tolerated by the oscillator or loop components decreases with the same ratio, requiring a proportional increase of I_{F}. Thus the ratio $I_{\mathrm{F}}/I_{\mathrm{L}}$ remains constant.

When considering $\mathrm{FoM_{osc}} = 190\,\mathrm{dB}$ and $K_{\mathrm{push}} = 50\,\mathrm{MHz/V}$ for a 5 GHz state-of-the-art LC oscillator, then (3.33) suggests $I_{\mathrm{F}}/I_{\mathrm{osc}} > \sim 8\%$ under 1 V V_{OUT}. Note that $\beta_{\mathrm{F}} \approx 0.5$ is used in the calculation here which sets the input common-mode voltage of the EA to a reasonable value, i.e. around the middle of the supply range. A higher $\mathrm{FoM_{osc}}$ would degrade the power efficiency even further. For $\mathrm{FoM_{osc}} = 196\,\mathrm{dB}$, $I_{\mathrm{F}}/I_{\mathrm{osc}} > \sim 14\%$ even with $\beta_{\mathrm{F}} \approx 0.7$. For other loop components, $I_{\mathrm{F}}/I_{\mathrm{loop}} < 1\%$ even for $\mathrm{FoM_{loop}} \approx 300\,\mathrm{dB}$ and $K_{\mathrm{rip}} \approx 400\,\mathrm{ps/V}$. This confirms the general belief that the oscillator is the most sensitive block to supply noise in the PLL.

3.4.2 Limitation Due to I_{EA}

The transfer function from the input-referred noise of the EA to V_{OUT} is similar to that of the feedback resistors. For simplicity, the EA is assumed to be a differential amplifier loaded by an active current mirror. Therefore, the two-sided PSD of its input-referred noise, $\overline{v_{\mathrm{n,IN,EA}}^2}$, is expressed as [55]

$$\overline{v_{\mathrm{n,IN,EA}}^2} = 2\frac{2kT\gamma}{g_{\mathrm{m,in}}} + 2\left(\frac{g_{\mathrm{m,cm}}}{g_{\mathrm{m,in}}}\right)^2 \frac{2kT\gamma}{g_{\mathrm{m,cm}}} = \frac{4kT\gamma}{g_{\mathrm{m,in}}} + \frac{4kT\gamma g_{\mathrm{m,cm}}}{g_{\mathrm{m,in}}^2}. \tag{3.35}$$

where $g_{\mathrm{m,in}}$ and $g_{\mathrm{m,cm}}$ are the transconductance of the transistors in the input differential pair and current mirror respectively. Assuming that $g_{\mathrm{m,in}} = g_{\mathrm{m,cm}}$, then $\overline{v_{\mathrm{n,IN,EA}}^2} = 8kT\gamma/g_{\mathrm{m,in}}$, and the total noise appeared on V_{OUT} due to $\overline{v_{\mathrm{n,IN,EA}}^2}$ could be calculated as

$$\overline{v_{\mathrm{n,OUT,EA}}^2} = \frac{\overline{v_{\mathrm{n,IN,EA}}^2}}{\beta_{\mathrm{F}}^2} = \frac{8kT\gamma}{g_{\mathrm{m,in}}}\left(1 + \frac{R_{\mathrm{F1}}}{R_{\mathrm{F2}}}\right)^2. \tag{3.36}$$

Similar to $\overline{v_{\mathrm{n,OUT,R}}^2}$, the extra noise induced by $\overline{v_{\mathrm{n,OUT,EA}}^2}$ should be much lower than the inherent circuit noise. Combining (3.36) with (3.23) or (3.28), the efficiency degradation due to I_{EA} could be calculated as

$$\left(\frac{I_{\mathrm{EA}}}{I_{\mathrm{osc}}}\right) > 10 \cdot \frac{16kT\gamma V_{\mathrm{OUT}}}{10^{-(\mathrm{FoM_{osc}}+30)/10}\left(g_{\mathrm{m,in}}/I_{\mathrm{D,EA}}\right)\beta_{\mathrm{F}}^2}\left(\frac{K_{\mathrm{push}}}{f_{\mathrm{osc}}}\right)^2 \tag{3.37}$$

and

$$\left(\frac{I_{\mathrm{EA}}}{I_{\mathrm{loop}}}\right) > 10 \cdot \frac{16kT\gamma V_{\mathrm{OUT}}}{10^{-(\mathrm{FoM}_{\mathrm{loop}}+30)/10}\left(g_{\mathrm{m,in}}/I_{\mathrm{D,EA}}\right)\beta_{\mathrm{F}}^{2}}\left(2\pi K_{\mathrm{rip}}\right)^{2} \tag{3.38}$$

where $I_{\mathrm{D,EA}} = I_{\mathrm{EA}}/2$ is the drain current of the input transistors in EA. γ is the excess noise coefficient of MOS transistors, and equals to 2/3 in strong inversion for long channel devices. The expression in (3.37) and (3.38) also suggest that the efficiency degradation due to I_{EA} is constant with respect of the load current.

For a 5 GHz LC oscillator with $\mathrm{FoM}_{\mathrm{osc}} = 190\,\mathrm{dB}$ and $K_{\mathrm{push}} = 50\,\mathrm{MHz/V}$ when $V_{\mathrm{OUT}} = 1\,\mathrm{V}$, the efficiency degradation calculated with (3.37) is $I_{\mathrm{EA}}/I_{\mathrm{osc}} > \sim 15\%$ assuming $g_{\mathrm{m,in}}/I_{\mathrm{D,EA}} = 12$ and $\beta_{\mathrm{F}} = 0.5$. When $\mathrm{FoM}_{\mathrm{osc}}$ is rised to 196 dB, $I_{\mathrm{EA}}/I_{\mathrm{osc}}$ also increases to $> \sim 30\%$ even with $\beta_{\mathrm{F}} = 0.7$. For other loop components, $I_{\mathrm{EA}}/I_{\mathrm{loop}} < 1\%$ for $\mathrm{FoM}_{\mathrm{loop}} \approx 300\,\mathrm{dB}$ and $K_{\mathrm{rip}} \approx 400\,\mathrm{ps/V}$, which is similar to the $I_{\mathrm{F}}/I_{\mathrm{loop}}$ result.

3.4.3 Limitation Due to V_{DO}

When the output of EA is tightly coupled to V_{DD}, (3.9) reveals the existence of a PSR hump with a level of $R_{\mathrm{eq}}/(r_{\mathrm{op}} + R_{\mathrm{eq}})$ around ω_{REG} for the ω_g dominant topology (see Fig. 3.2 (b)). To limit the PSR around this hump to a reasonable value, i.e. 0.5 for the analysis here, $r_{\mathrm{op}} = R_{\mathrm{eq}} \approx R_{\mathrm{L}}$ is required. For 1 mA I_{L} under 1 V V_{OUT}, $r_{\mathrm{op}} \approx R_{\mathrm{L}} = 1\,\mathrm{k\Omega}$. The length of $\mathrm{M_p}$, L_{p}, could be determined by r_{op}. Given that $r_{\mathrm{op}} = 1/(\lambda I_{\mathrm{L}})$ and $\lambda = V_{\mathrm{E}}^{-1}L_{\mathrm{p}}^{-1}$, L_{p} is calculated as

$$L_{\mathrm{p}} = \frac{r_{\mathrm{op}}I_{\mathrm{L}}}{V_{\mathrm{E}}} \approx \frac{V_{\mathrm{OUT}}}{V_{\mathrm{E}}}, \tag{3.39}$$

where the typical value of V_{E} is $10\,\mathrm{V}/\mu\mathrm{m}$. For $V_{\mathrm{OUT}} = 1\,\mathrm{V}$, L_{P} is calculated to be $0.1\mu\mathrm{m}$. Note that L_{p} is only related to V_{OUT} since the variation of I_{L} leads to similar simultaneous changes in r_{op} and R_{L}.

The loop gain of the LDO, $LG(s)$, is expressed as

$$LG(s) = \beta_{\mathrm{F}}A_{\mathrm{O}}(s)\,A_{\mathrm{EA}}(s) = \frac{\beta_{\mathrm{F}}A_{\mathrm{O,0}}A_{\mathrm{EA,0}}}{(1+s/\omega_o)(1+s/\omega_g)}. \tag{3.40}$$

Thus, its phase margin (PM) could be calculated as

$$\mathrm{PM} = 180^\circ - \tan^{-1}\left(\frac{\omega_{REG}}{\omega_g}\right) - \tan^{-1}\left(\frac{\omega_{REG}}{\omega_o}\right). \tag{3.41}$$

Assuming that the non-dominant pole, ω_o, is sufficiently higher than ω_{REG}, then $\omega_{REG} \approx \beta_\mathrm{F} A_{\mathrm{O},0} A_{\mathrm{EA},0} \cdot \omega_g = LG_\mathrm{DC} \cdot \omega_g$, where $LG_\mathrm{DC} = LG(s)|_{s=0}$ is the loop gain of LDO at DC. Hence, the PM expression in (3.41) could be rewritten as

$$\mathrm{PM} = 180^\circ - \tan^{-1}(LG_\mathrm{DC}) - \tan^{-1}\left(LG_\mathrm{DC} \cdot \frac{\omega_g}{\omega_o}\right). \tag{3.42}$$

From (3.42), the relation between ω_o and ω_g could be derived as

$$\omega_o = \frac{LG_\mathrm{DC}}{\tan\left(180^\circ - \mathrm{PM} - \tan^{-1}(LG_\mathrm{DC})\right)} \cdot \omega_g. \tag{3.43}$$

Note that the PSR at DC, $\mathrm{PSR_{DC}} \approx R_\mathrm{eq}/(r_\mathrm{op} + R_\mathrm{eq}) \cdot {LG_\mathrm{DC}}^{-1} = (2\,LG_\mathrm{DC})^{-1}$. Thus, $LG_\mathrm{DC} = {\mathrm{PSR_{DC}}}^{-1}/2$, and (3.43) could be expressed with $\mathrm{PSR_{DC}}$ as

$$\omega_o = \frac{{\mathrm{PSR_{DC}}}^{-1}/2}{\tan\left(180^\circ - \mathrm{PM} - \tan^{-1}({\mathrm{PSR_{DC}}}^{-1}/2)\right)} \cdot \omega_g. \tag{3.44}$$

For the ω_g-dominant topology considered here, $\mathrm{PSR_{DC}}$ is chosen to be 3 dB higher than the desired PSR of the LDO at f_rip, while the dominant pole, ω_g, is placed at f_rip. This arrangement guarantees that PSR at f_rip just equals to the desired value [$20\log_{10}\left(|1 + j \cdot 1|^{-1}\right) \approx$ -3 dB]. Note that ω_g could be placed at even lower frequencies. However, $\mathrm{PSR_{DC}}$ needs to be increased correspondingly to guarantee the desired PSR at f_rip, which makes the frequency of ω_o relatively constant. When the system is critically damped ($\zeta \approx 0.707$ and $\mathrm{PM} \approx 64^\circ$) with a $\mathrm{PSR_{DC}}$ of -43 dB, (3.44) shows that $\omega_o \approx 140\,\omega_g$. With some margin, we choose $\omega_o = 150\,\omega_g$. Considering a 10 MHz switching frequency, ω_o should be placed at 1.5 GHz, resulting in a total output capacitance [C_L in Fig. 3.2 (a)] of $\sim$210 fF.

To reduce the overdrive voltage of $\mathrm{M_p}$ and improve the LDO's efficiency, the width of $\mathrm{M_p}$, W_p, should be maximized, as will be shown shortly. Therefore, it is desired that the parasitic capacitance of $\mathrm{M_p}$ absorbs all available C_L. Also, any extra decoupling capacitance on V_OUT would push

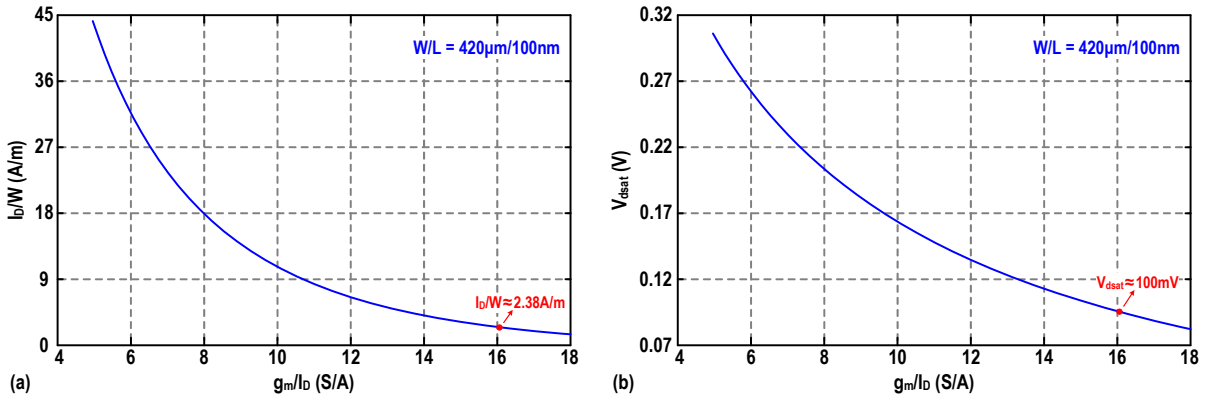


Figure 3.3: (a) Current density and (b) overdrive voltage of the pass transistor for different $g_\mathrm{m}/I_\mathrm{D}$ values.

ω_o closer to ω_g, potentially affecting the stability of the LDO. The parasitic capacitance of $\mathrm{M_p}$ is dominated by its drain-to-bulk (C_DB) and drain-to-gate (C_DG) capacitance. Thus,

$$C_\mathrm{L} = C_\mathrm{DB} + C_\mathrm{DG} = C_\mathrm{ov}W_\mathrm{p} + 0.5C_\mathrm{jbd}W_\mathrm{p}E + C_\mathrm{jbdsw}W_\mathrm{p} \approx 500\,\mathrm{pF/m} \cdot W_\mathrm{p} \tag{3.45}$$

in which $C_\mathrm{ov} \approx 50\,\mathrm{pF/m}$ is the overlapped capacitance per unit width, $\mathrm{E} = 140\,\mathrm{nm}$ is the length of the drain area, and $C_\mathrm{jbd} \approx 1.4\,\mathrm{mF/m^2}$ and $C_\mathrm{jbdsw} \approx 300\,\mathrm{pF/m}$ are the bulk-to-drain junction capacitance per unit area (at the bottom plate) and per unit width (for sidewalls), respectively. Note that C_ov, C_jbd and C_jbdsw are all technology-dependent parameters, and the values used here are from the 40-nm CMOS technology adopted in following designs. Hence, the maximum width of $\mathrm{M_p}$ is calculated to be $W_\mathrm{p} = 420\,\mu\mathrm{m}$.

Fig. 3.3 (a) shows the current density for different $g_\mathrm{m}/I_\mathrm{D}$ values for the pass transistor $\mathrm{M_p}$. With $I_\mathrm{L} = 1\,\mathrm{mA}$ and $W_\mathrm{p} = 420\,\mu\mathrm{m}$, a $g_\mathrm{m}/I_\mathrm{D} \approx 16\,\mathrm{S/A}$ could be achieved. Consequently, $\mathrm{M_p}$ can operate in the weak-inversion region with an overdrive voltage of only 100 mV, as can be gathered from Fig. 3.3 (b). Therefore, V_DO would further degrade the power efficiency of the LDO by a factor of 0.91 under 1 V V_OUT. In actual designs, absorbing C_L totally by $\mathrm{M_p}$ is impractical, since the contribution from other factors, i.e. the routing parasitic and the equivalent load capacitance seen at the supply of circuits, could not be avoided. This would lead to a smaller W_p. Hence, as shown in Fig. 3.3, $g_\mathrm{m}/I_\mathrm{D}$ of $\mathrm{M_p}$ should decrease due to a larger current density, which in turn requires a higher V_DO, further worsening

the system efficiency. It is also observed from Fig. 3.3 that the efficiency degradation due to V_{DO} is relatively constant for practical values. When $g_{\mathrm{m}}/I_{\mathrm{D}}$ varies from 14 ($I_{\mathrm{D}}/W_{\mathrm{p}} \approx 4.1$) to 18 S/A ($I_{\mathrm{D}}/W_{\mathrm{p}} \approx 1.5$), V_{DO} only decreases from $\sim$110 mV to $\sim$80 mV, corresponding to a power efficiency of around $0.9 \sim 0.925\%$ for $V_{\mathrm{OUT}} = 1\,\mathrm{V}$.

When I_{L} increases, R_{L} decreases proportionally under a constant V_{OUT}. Hence, to keep ω_o at the same frequency, C_{L} should be increased by the same ratio. This, in turn, leads to an increase in the width of $\mathrm{M_p}$, which makes the current density of the pass transistor relatively constant, resulting in a similar overdrive voltage. Consequently, the power efficiency degradation due to V_{DO} is not a function of I_{L}.

Summarizing all the aforementioned analysis in this section, it could be concluded that the use of LDOs can lead to severe degradation of the system efficiency. For the LDO powering the oscillator, which is the most supply-sensitive block in the PLL, I_{F}, I_{EA} and V_{DO} could degrade the LDO efficiency by factors of 0.92×, 0.85× and 0.91×, respectively, leading to a total power efficiency of $\sim$ 70%. When $\mathrm{FoM_{osc}}$ increases, the efficiency degradation of this LDO could be even worse. For the LDO powering the loop components, the efficiency degradation is mainly contributed by V_{DO}, and the total power efficiency is limited to around 90%.

3.5 System Level Power Management Strategy

Given the limitation on the power efficiency of LDOs, it could be beneficial to remove them from the power management unit (PMU) of the system, especially in a portable device. In this section, some further discussion on this issue will be provided. To simplify the discussion, all system modules are assumed to be located in the same voltage domain, while the different voltage domains in a real system are generally powered through different sets of voltage regulators [6, 7].

As a starting point of this discussion, it is worth to point out that a DC-DC converter is always needed in the PMU design. As shown in Fig. 3.1, the voltage level available from the energy source, V_{ES}, may be much higher than the nominal supply voltage of the system. Then, if the LDOs are directly connected to V_{ES} without using a switching converter

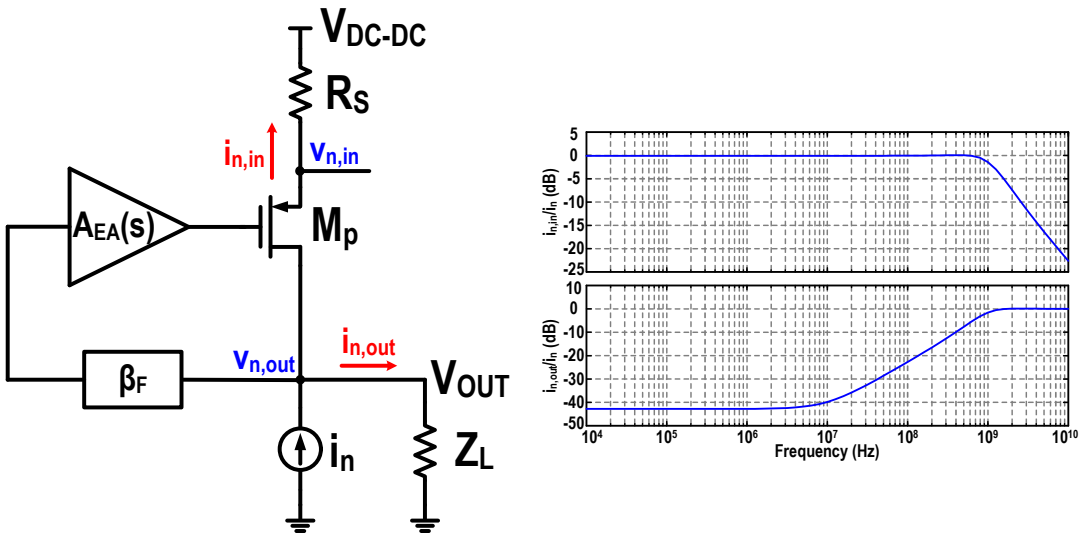


Figure 3.4: Reverse isolation of the LDO.

and generate the nominal supply of the system, their large voltage drop would cause severe degradation of the system power efficiency. For example, $V_{\mathrm{ES}} \approx 3.3\,\mathrm{V}$ for batteries while the nominal supply voltage of the 40-nm CMOS technology could be as low as 1.0 V. Thus, the 2.3 V voltage drop of the LDOs already limits the system efficiency to $< 45\%$. Therefore, a DC-DC converter is needed in the PMU to first convert V_{ES} to the desired voltage level with high efficiency.

3.5.1 Reverse Isolation of LDO and DC-DC Converter

In a complex system-on-chip (SoC), noise may be coupled to the output of the LDO due to the activities of other aggressor modules. Its side effects on both the input and output of the LDO are investigated here.

Figure 3.4 shows the equivalent model of the LDO with a noise current, i_{n}, injected at its output. R_{s} represents the output resistance of its energy source, i.e. a DC-DC converter in this case, while Z_{L} represents the load impedance driven by the LDO. Thus, the transfer function from i_{n} to the LDO input ($i_{\mathrm{n,in}}$) could be calculated as

$$\frac{i_{\mathrm{n,in}}}{i_{\mathrm{n}}} = \frac{\beta_{\mathrm{F}} g_{\mathrm{mp}} \left(r_{\mathrm{op}} \parallel Z_{\mathrm{L}}\right) A_{\mathrm{EA}}\left(s\right) + Z_{\mathrm{L}}/\left(r_{\mathrm{op}} + Z_{\mathrm{L}}\right)}{1 + R_{\mathrm{s}}\left(1 + g_{\mathrm{mp}} r_{\mathrm{op}}\right)/\left(r_{\mathrm{op}} + Z_{\mathrm{L}}\right) + \beta_{\mathrm{F}} g_{\mathrm{mp}} \left(r_{\mathrm{op}} \parallel Z_{\mathrm{L}}\right) A_{\mathrm{EA}}\left(s\right)}. \quad (3.46)$$

Replacing Z_{L} with the parallel combination of R_{eq} and C_{L}, (3.46) would

then become

$$\frac{i_{\mathrm{n,in}}}{i_{\mathrm{n}}} = \frac{\beta_{\mathrm{F}} A_{\mathrm{O}}(s) A_{\mathrm{EA}}(s) + R_{\mathrm{eq}}/(r_{\mathrm{op}} + R_{\mathrm{eq}}) \cdot 1/(1 + s/\omega_o)}{1 + R_{\mathrm{s}} \cdot \frac{1+g_{\mathrm{mp}} r_{\mathrm{op}}}{r_{\mathrm{op}}+R_{\mathrm{eq}}} \cdot \frac{1+s/\omega_L}{1+s/\omega_o} + \beta_{\mathrm{F}} A_{\mathrm{O}}(s) A_{\mathrm{EA}}(s)} \tag{3.47}$$

$$\approx \frac{LG(s) + R_{\mathrm{eq}}/(r_{\mathrm{op}} + R_{\mathrm{eq}}) \cdot 1/(1 + s/\omega_o)}{1 + g_{\mathrm{mp}} R_{\mathrm{s}} \cdot \frac{r_{\mathrm{op}}}{r_{\mathrm{op}}+R_{\mathrm{eq}}} \cdot \frac{1+s/\omega_L}{1+s/\omega_o} + LG(s)} \tag{3.48}$$

where $\omega_L = (R_{\mathrm{eq}} C_{\mathrm{L}})^{-1}$. Note that the loop gain $LG(s) = \beta_{\mathrm{F}} A_{\mathrm{O}}(s) A_{\mathrm{EA}}(s)$ is much larger than 1 for frequencies below the dominant pole, while $g_{\mathrm{mp}} R_{\mathrm{s}} \cdot r_{\mathrm{op}}/(r_{\mathrm{op}} + R_{\mathrm{eq}}) \ll 1$ since g_{mp} is in the 10 mS range. Hence, at low frequencies, (3.48) could be approximated as $i_{\mathrm{n,in}}/i_{\mathrm{n}} \approx 1$, indicating that the injected current noise directly appears at the LDO input, which is then converted into voltage noise ($v_{\mathrm{n,in}}$) through R_{s}. Consequently, it is critical to minimize R_{s} to avoid the propagation of the injected noise to other blocks powered by the same converter. When the frequency is increased above the dominant pole, $LG(s)$ starts to drop, and $i_{\mathrm{n,in}}$ begins to be notably filtered around ω_{REG}.

On the other hand, the current noise flowing into Z_{L} ($i_{\mathrm{n,out}}$) due to i_{n} could be expressed as

$$\frac{i_{\mathrm{n,out}}}{i_{\mathrm{n}}} = \frac{1 + [R_{\mathrm{s}}(1 + g_{\mathrm{mp}} r_{\mathrm{op}}) - Z_{\mathrm{L}}]/(r_{\mathrm{op}} + Z_{\mathrm{L}})}{1 + R_{\mathrm{s}}(1 + g_{\mathrm{mp}} r_{\mathrm{op}})/(r_{\mathrm{op}} + Z_{\mathrm{L}}) + \beta_{\mathrm{F}} g_{\mathrm{mp}} (r_{\mathrm{op}} \| Z_{\mathrm{L}}) A_{\mathrm{EA}}(s)}. \tag{3.49}$$

For $Z_{\mathrm{L}} = R_{\mathrm{eq}} \| C_{\mathrm{L}}$, (3.49) becomes

$$\frac{i_{\mathrm{n,out}}}{i_{\mathrm{n}}} = \frac{1 + R_{\mathrm{s}} \cdot \frac{1+g_{\mathrm{mp}} r_{\mathrm{op}}}{r_{\mathrm{op}}+R_{\mathrm{eq}}} \cdot \frac{1+s/\omega_L}{1+s/\omega_o} - \frac{R_{\mathrm{eq}}}{r_{\mathrm{op}}+R_{\mathrm{eq}}} \cdot \frac{1}{1+s/\omega_o}}{1 + R_{\mathrm{s}} \cdot \frac{1+g_{\mathrm{mp}} r_{\mathrm{op}}}{r_{\mathrm{op}}+R_{\mathrm{eq}}} \cdot \frac{1+s/\omega_L}{1+s/\omega_o} + \beta_{\mathrm{F}} A_{\mathrm{O}}(s) A_{\mathrm{EA}}(s)} \tag{3.50}$$

$$\approx \frac{1 + g_{\mathrm{mp}} R_{\mathrm{s}} \cdot \frac{r_{\mathrm{op}}}{r_{\mathrm{op}}+R_{\mathrm{eq}}} \cdot \frac{1+s/\omega_L}{1+s/\omega_o} - \frac{R_{\mathrm{eq}}}{r_{\mathrm{op}}+R_{\mathrm{eq}}} \cdot \frac{1}{1+s/\omega_o}}{1 + g_{\mathrm{mp}} R_{\mathrm{s}} \cdot \frac{r_{\mathrm{op}}}{r_{\mathrm{op}}+R_{\mathrm{eq}}} \cdot \frac{1+s/\omega_L}{1+s/\omega_o} + LG(s)}. \tag{3.51}$$

Similarly, at frequencies lower than the dominant pole, (3.51) could be simplified to

$$\frac{i_{\mathrm{n,out}}}{i_{\mathrm{n}}} \approx \frac{1 - R_{\mathrm{eq}}/(r_{\mathrm{op}} + R_{\mathrm{eq}})}{LG_{\mathrm{DC}}} = \frac{r_{\mathrm{op}}/(r_{\mathrm{op}} + R_{\mathrm{eq}})}{LG_{\mathrm{DC}}}. \tag{3.52}$$

Equation (3.52) reveals that the LDO attenuates any noise injected at

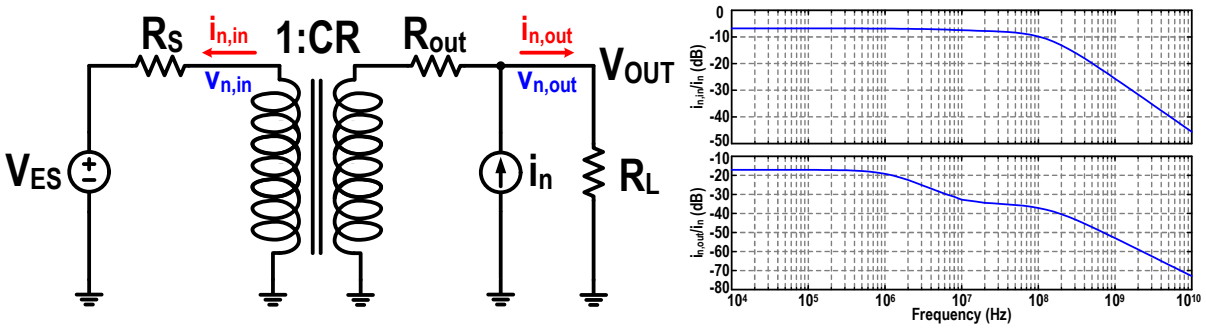


Figure 3.5: Reverse isolation of the switched-capacitor DC-DC converter.

its output by the loop gain. For frequencies higher than the dominant pole, $i_{\mathrm{n,out}}/i_{\mathrm{n}}$ increases due to the reduction of the loop gain and begins to saturate at around ω_{REG}. However, when the output voltage noise ($v_{\mathrm{n,out}}$) is considered, its amplitude rolls off at $\sim 20\,\mathrm{dB/decade}$ after the non-dominant pole since C_{L} provides a low impedance path to ground for $v_{\mathrm{n,out}}$.

Similar analysis has also been done for a switched-capacitor DC-DC converter. Figure 3.5 shows the equivalent model of the converter, in which conversion ratio (CR) is the ratio between the output and input voltage of the converter. R_{s} is the equivalent output resistance of the energy source V_{ES}, while R_{out} represents the output resistance of the converter. When i_{n} is injected at its output, the current noise that reaches the input ($i_{\mathrm{n,in}}$) is calculated as

$$\frac{i_{\mathrm{n,in}}}{i_{\mathrm{n}}} = \frac{R_{\mathrm{L}} \cdot \mathrm{CR}}{R_{\mathrm{L}} + R_{\mathrm{out}} + R_{\mathrm{s}} \cdot \mathrm{CR}^2}. \tag{3.53}$$

Typically, $R_{\mathrm{L}} \gg \left(R_{\mathrm{out}} + R_{\mathrm{s}} \cdot \mathrm{CR}^2\right)$, (3.53) can then be simplified to $i_{\mathrm{n,in}}/i_{\mathrm{n}} \approx \mathrm{CR}$ at low frequencies. For the buck converter considered here, its output voltage is lower than the input, resulting in $\mathrm{CR} < 1$. Hence, in contrast to the LDO structure, the injected current noise at the converter output is *firstly* attenuated by CR when referred to the input, and then be converted into voltage noise $v_{\mathrm{n,in}}$ through R_{s}. As a result, for a similar small R_{s}, the (buck) converter provides a slightly better isolation when compared to the LDO. When the frequency is increased, $i_{\mathrm{n,in}}$ would be further filtered, which is also shown in Fig. 3.5.

The current noise flowing into the load of the converter ($i_{\mathrm{n,out}}$) due to

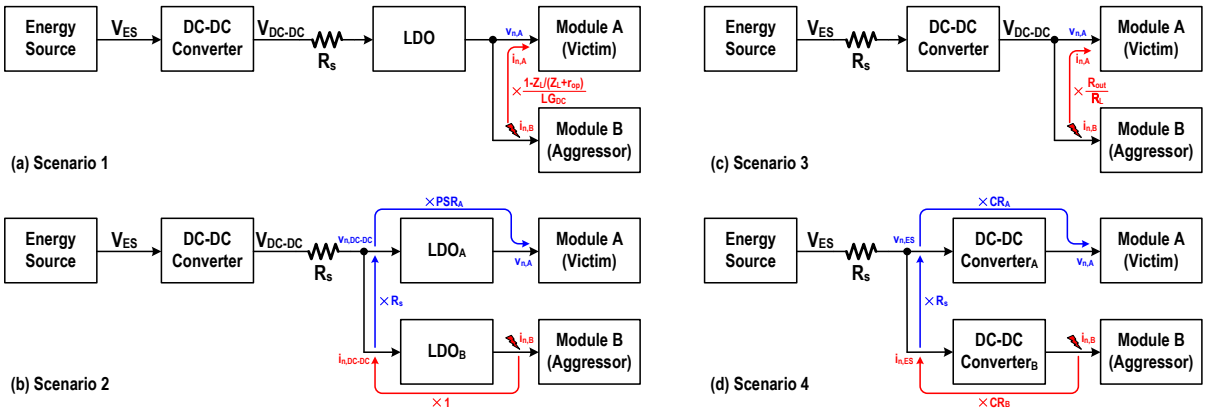


Figure 3.6: Four different scenarios of the PMU arrangement for a complex RF SoC.

i_n is also calculated as

$$\frac{i_\mathrm{n,out}}{i_\mathrm{n}} = 1 - \frac{i_\mathrm{n,in}}{\mathrm{CR}\cdot i_\mathrm{n}} = \frac{R_\mathrm{out} + R_\mathrm{s}\cdot \mathrm{CR}^2}{R_\mathrm{L} + R_\mathrm{out} + R_\mathrm{s}\cdot \mathrm{CR}^2}. \tag{3.54}$$

Eq. (3.54) could be simplified to $i_\mathrm{n,out}/i_\mathrm{n} \approx R_\mathrm{out}/{R_\mathrm{L}}^2$, indicating that the output current noise is also reduced by the converter at low frequencies. However, compared to that of the LDO where the output current noise is reduced by the loop gain, the attenuation could be smaller. When the frequency is increased, the current noise flowing into the load resistance is also filtered (see Fig. 3.5).

3.5.2 Power Management Strategy for SoC

With the insight gained from the analysis above, the arrangement of the PMU for a complex RF SoC is considered here. Depending on whether the LDOs are used and how the LDOs or converters are shared between blocks, four different scenarios are identified (see Fig. 3.6). As shown in Fig. 3.6 (a) and (b), the conventional approach of cascading LDOs with the DC-DC converter is adopted in the first two scenarios, while the converter outputs directly power the system in the last two scenarios (see Fig. 3.6 (c) and (d)).

For the first two scenarios, the main difference lies in whether the LDO is shared between different blocks. Here, the SoC is assumed to consist

[2]Note that the higher value (i.e., ~ -17dB) at very low frequency shown in Fig. 3.5 is incurred by the interleaving technique. As mentioned in Section 4.6, interleaving is typically adopted in the switched-capacitor DC-DC converter design to reduce the switching losses.

only two modules (module A and B) for simplicity with the performance of module A being affected by the disturbance injected by module B in the following analysis. In scenario 1, both modules are supplied by the same LDO (see Fig. 3.6 (a)). Thus, when module B injects a current noise ($i_{\mathrm{n,B}}$) to the LDO output, the amount of noise that reaches the supply of module A ($i_{\mathrm{n,A}}$) is governed by (3.49)$\sim$(3.52). After being multiplied by the corresponding load impedance Z_{L}, the voltage noise at the supply of module A ($v_{\mathrm{n,A}}$) could be obtained. As discussed previously, $i_{\mathrm{n,A}}$ is suppressed by LG_{DC} of the LDO at low frequencies ($v_{\mathrm{n,A}} \approx r_{\mathrm{op}} R_{\mathrm{eq}}/(r_{\mathrm{op}} + R_{\mathrm{eq}})\,/LG_{\mathrm{DC}}$), guaranteeing the isolation between the two modules. However, when the frequency increases beyond the dominant pole (ω_g in Fig. 3.2 (a)) of the LDO, $i_{\mathrm{n,A}}$ and, correspondingly, $v_{\mathrm{n,A}}$ in this scenario deteriorate due to the roll-off of the loop gain, and it is not until around the non-dominant pole (ω_o in Fig. 3.2 (a)) of the LDO that $v_{\mathrm{n,A}}$ starts to be filtered again due to the reduction in load impedance. Hence, the isolation between module A and B is not satisfying at higher frequencies in this scenario. To overcome this problem, as shown in Fig. 3.6 (b), two different LDOs, $\mathrm{LDO_A}$ and $\mathrm{LDO_B}$, are used to power module A and B, respectively. To simplify the discussion, it is assumed that the pole locations of both LDOs are the same. The LDOs are connected to a DC-DC converter with an equivalent output resistance of R_{s}. In this scenario, the current noise injected at the output of $\mathrm{LDO_B}$, $i_{\mathrm{n,B}}$, by module B directly appears at its input ($i_{\mathrm{n,DC-DC}}$) at low frequencies, which is further converted into the voltage noise, $v_{\mathrm{n,DC-DC}}$, through R_{s}. $v_{\mathrm{n,DC-DC}}$ is then transferred to the output of $\mathrm{LDO_A}$ after being attenuated by its PSR, $\mathrm{PSR_A}$, generating the supply noise of module A ($v_{\mathrm{n,A}}$). Therefore, $v_{\mathrm{n,A}} = R_{\mathrm{s}} \cdot \mathrm{PSR_A} \cdot i_{\mathrm{n,B}} \approx R_{\mathrm{s}} R_{\mathrm{eq}}/(r_{\mathrm{op}} + R_{\mathrm{eq}})\,/LG_{\mathrm{DC}}$ at frequencies lower than the dominant pole of the LDOs, avoiding the possible performance degradation of module A. When the frequency is increased above the dominant pole, $\mathrm{PSR_A}$ will start to degrade. However, a small R_{s} (i.e., $R_{\mathrm{s}} \ll r_{\mathrm{op}}$) would absorb most of the noise and still guarantees good isolation between the two modules. When the frequency is further increased beyond $\sim\omega_{REG}$, $i_{\mathrm{n,DC-DC}}$ will be suppressed while $\mathrm{PSR_A}$ will also start rolling off again after the non-dominant pole. Both phenomena help to improve the isolation between the two modules at high frequencies.

As already mentioned, it is desired to design the PMU without LDOs

for better system efficiency. In this case, similar to when the LDOs are used, two scenarios are also possible depending on whether the DC-DC converter is shared between different modules (see Fig. 3.6 (c) and (d)). As shown in Fig. 3.6 (c), both module A and B are powered by the same converter in scenario 3. Thus, as can be gathered from (3.54), the current noise injected by module B ($i_{\mathrm{n,B}}$) is attenuated by $R_{\mathrm{out}}/R_{\mathrm{L}}$ before reaching the supply of module A at low frequencies, generating $v_{\mathrm{n,A}} = R_{\mathrm{out}} \cdot i_{\mathrm{n,B}}$. In order to provide a better isolation between the two modules, scenario 3 is further modified to that shown in Fig. 3.6 (d), where modules A and B are powered by two separate DC-DC converters, $\mathrm{Converter_A}$ and $\mathrm{Converter_B}$, respectively. Therefore, based on previous discussions, the current noise injected by module B ($i_{\mathrm{n,B}}$) is attenuated by the CR of $\mathrm{Converter_B}$, $\mathrm{CR_B}$, at low frequencies when referred to its input ($i_{\mathrm{n,ES}}$). $i_{\mathrm{n,ES}}$ is then converted into the voltage noise, $v_{\mathrm{n,ES}}$, through the equivalent resistance seen at the output of the energy source (R_{s} in Fig. 3.6 (d)). Finally, $v_{\mathrm{n,ES}}$ is scaled by the CR of $\mathrm{Converter_A}$, $\mathrm{CR_A}$, to generate the noise on the supply of module A, leading to $v_{\mathrm{n,A}} = R_{\mathrm{s}} \cdot \mathrm{CR_A} \cdot \mathrm{CR_B} \cdot i_{\mathrm{n,B}}$. Assuming that the supply voltage of the two modules in the same SoC is similar, then $\mathrm{CR_A} = \mathrm{CR_B} = \mathrm{CR}$, and the supply noise of module A could be simplified as $v_{\mathrm{n,A}} = R_{\mathrm{s}} \cdot \mathrm{CR}^2 \cdot i_{\mathrm{n,B}}$. Since R_{s} is generally very small, $v_{\mathrm{n,A}}$ is largely suppressed compared to the previous scenario. At higher frequencies, $v_{\mathrm{n,A}}$ would be further filtered by the two converters (please refer to Fig. 3.5), leading to improved isolation between module A and B.

Now, let us compare the arrangement in Fig. 3.6 (d) to that in Fig. 3.6 (b). Although in both cases the small R_{s} helps to suppress the noise seen by module A, scenario 2 could have a higher degree of isolation at low frequencies due to the term $\mathrm{PSR_A}$. Consequently, besides suppressing the effect of the supply ripples (please refer to Chapter 2), module A (and B), if sensitive to the coupled noise, should also be designed using techniques that reduce the effect of the supply noise, providing an equivalent 'PSR'. Assuming similar 'PSR' and R_{s} values for both scenarios, the arrangement in scenario 4 could offer a slightly better isolation performance than that in scenario 2 due to the CR^2 factor[3]. Without the equivalent 'PSR',

[3] $\mathrm{Converter_{A,B}}$ are considered to be buck converters with $\mathrm{CR} < 1$ here. For an energy harvester, its output level, which is typically lower than the nominal supply of the SoC, would fluctuate due to the environment in which it operates. Hence, the output of the energy harvester is typically stored in some

the corresponding module itself should have sufficient tolerance to the possible coupled noise. It is also obvious that for both scenarios, the small equivalent resistance R_s at the output of the converter/energy source could play a critical role of absorbing most of the noise interference injected by the aggressor module and guaranteeing good isolation between different modules at higher frequencies. Therefore, it could be concluded that by carefully dividing the system into different modules with proper design techniques, and directly powering each module with a dedicated DC-DC converter, the efficiency degradation due to LDOs could be avoided while the good isolation between different modules is still guaranteed. Such a powering scheme is also beneficial in terms of the supply noise from the PMU components. The relatively large flying capacitor (C_{fly}) used by the switched-capacitor DC-DC converter guarantees its low output noise, which is generally much smaller than that of the LDO [42]. However, as already mentioned above, all modules in the system now need to adopt circuit or system level techniques to suppress the effects of the ripples and/or noise on the supply. The rest of this thesis will focus on the design of frequency synthesizers, and techniques that enable the direct operation of a fractional-N DPLL from a switched-capacitor DC-DC converter are proposed and verified.

To end the discussion in this section, it is also worth to point out that the total power efficiency and silicon cost of the converters in Fig. 3.6 (d) are similar to those in Fig. 3.6 (c). For a switched-capacitor DC-DC converter, the silicon area it occupies is typically dominated by its C_{fly}. The total capacitance of C_{fly} needed in scenario 4 is identical to that in scenario 3, although it shows that more DC-DC converters should be used in scenario 4. As shown in (3.10) and (3.11), the amplitude of the ripple at the converter output is proportional to the current drawn by its load. Hence, in scenario 3, the total amount of flying capacitance needed is calculated as $C_{\text{fly,S3}} = I_{\text{L,tot}}/(2A_{\text{rip,saw}}f_{\text{SW}})$, where $I_{\text{L,tot}}$ is the total current drawn by the system. On the other hand, the system is divided into m modules in scenario 4, each providing a current of $I_{\text{L,i}}$. Therefore, the converter powering the ith module, $\text{Converter}_{\text{i}}$, requires a flying capacitance of $C_{\text{fly,i,S4}} = I_{\text{L,i}}/(2A_{\text{rip,saw}}f_{\text{SW}})$,

energy storage elements (i.e., supercapacitors or batteries) first, which is also responsible for providing higher V_{ES}. Then, buck converters ($\text{Converter}_{\text{A,B}}$) could follow to further convert V_{ES} to the desired supply voltage.

resulting in a total amount of $C_{\text{fly,S4}} = \sum_{i=1}^{m} C_{\text{fly,i,S4}} = \left(\sum_{i=1}^{m} I_{\text{L,i}}\right) / (2A_{\text{rip,saw}} f_{\text{SW}})$. Since $I_{\text{L,tot}} = \sum_{i=1}^{m} I_{\text{L,i}}$, we have $C_{\text{fly,S3}} = C_{\text{fly,S4}}$. Hence, when powering the same system with similar requirement on ripple amplitude, the total flying capacitance needed in Fig. 3.6 (d) equals that in Fig. 3.6 (c), occupying similar area on chip. As to the power efficiency, it is already calculated in [42] and [56] (see also Section 4.6) that the power loss of the switched-capacitor based converter in scenario 3 could be expressed as

$$P_{\text{LOSS,S3}} = nC_{\text{g}}V_{\text{sw}}^2 f_{\text{SW}} + R_{\text{S}} I_{\text{L,tot}}^2 \tag{3.55}$$

where n is the number of switches operating at f_{SW} with a clock voltage swing of V_{sw}, C_{g} is the equivalent gate capacitance of each switch and R_{S} is the equivalent output resistance of the converter. Since the ith converter ($\text{Converter}_{\text{i}}$) in scenario 4 only needs to provide a portion of the total load current, i.e., $I_{\text{L,i}} = a_i I_{\text{L,tot}}$, the width of all its switches would be scaled down by a_i [42]. Thus, the power loss of $\text{Converter}_{\text{i}}$ in scenario 4 becomes

$$\begin{aligned} P_{\text{LOSS,i,S4}} &= nC_{\text{g,i}}V_{\text{sw}}^2 f_{\text{SW}} + R_{\text{S,i}} I_{\text{L,i}}^2 = n\left(a_i C_{\text{g}}\right) V_{\text{sw}}^2 f_{\text{SW}} + \frac{R_{\text{S}}}{a_i}\left(a_i I_{\text{L,tot}}\right)^2 \\ &= a_i P_{\text{LOSS,S3}}. \end{aligned}$$

Therefore, the total power loss of converters in scenario 4 is $P_{\text{LOSS,S4}} = \sum_{i=1}^{m} P_{\text{LOSS,i,S4}} = \left(\sum_{i=1}^{m} a_i\right) P_{\text{LOSS,S3}}$. Obviously, $\sum_{i=1}^{m} a_i = 1$, leading to the expected result of $P_{\text{LOSS,S3}} = P_{\text{LOSS,S4}}$, which proves the claim that the total power efficiency, $P_{\text{OUT}}/(P_{\text{OUT}} + P_{\text{LOSS}})$, of converters in scenario 4 is not affected compared to that in scenario 3. Note that the conclusions above are obtained assuming that all converters in scenario 4 are optimized for the most stringent $A_{\text{rip,saw}}$ requirement imposed by each block, which should also be met by the converter in scenario 3. Furthermore, scenario 4 also provides the flexibility to optimize a specific converter based on the ripple requirement of the block it powers.

3.6 Conclusion

This chapter focuses on the analysis of power efficiency of the LDOs powering the PLL. To achieve full-system integration, the LDO topology with its dominant pole located at the error amplifier output is selected, and the results show a $\sim$0.9$\times$ efficiency degradation due to the dropout voltage required by the PSR performance. For the LDO powering the oscillator, the increased quiescent current needed to suppress the supply noise could further degrade the system efficiency by $\sim$0.7–0.8$\times$. A brief discussion of four different SoC powering scenarios are also provided at the end of the chapter.

Chapter

4

Supply Pushing Reduction Technique for LC Oscillators

This chapter proposes a method to suppress supply pushing of an LC oscillator such that it may directly operate from a switched-mode DC-DC converter generating fairly large ripples[1]. A ripple replication block generates an amplified ripple replica at the gate terminal of the tail current source to stabilize the oscillator's tail current and thus its oscillating amplitude. The parasitic capacitance of the active devices and correspondingly the oscillation frequency are stabilized in turn. A calibration loop is also integrated on-chip to automatically set the optimum replication gain that minimizes the variation of the oscillation amplitude. A 4.9–5.6 GHz oscillator is realized in 40-nm CMOS and occupies 0.23 mm^2 while consuming 0.8–1.3 mW across the tuning range (TR). The supply pushing is improved to <1 MHz/V resulting in a low <−49 dBc spur due to 0.5–12 MHz sinusoidal supply ripples as large as 50 mV_{pp}. The effectiveness of the proposed technique is also experimentally verified in face of saw-tooth, multi-tone and modulated supply ripples. To further verify the proposed

[1]Material of this chapter has been published in the IEEE Journal of Solid-State Circuits [57].

technique under realistic scenarios, a 3-stage recursive switched-capacitor DC-DC converter with two conversion ratio options per stage is proposed to power the LC oscillator directly. Both are fabricated in 40-nm CMOS. The measured phase noise of the oscillator is not degraded, while $<-65\,\mathrm{dBc}$ spur is achieved under the $30\,\mathrm{mV_{pp}}$ ripple of the converter.

4.1 Introduction

As discussed in Chapter 3, it is beneficial to power the integrated electronic devices directly by the switched-capacitor DC-DC converters and avoid the efficiency degradation of the LDOs. However, as shown in Section 2.1, the output ripples of the converter would generate spurs around the oscillation frequency when an LC-tank oscillator is connected directly without using an LDO.

In order to suppress these spurs, the supply sensitivity of the oscillator needs to be reduced. Several techniques have already been proposed in literature to reduce supply pushing of the oscillator [58–61]. In [58], the oscillator is deliberately biased at the point of lowest sensitivity. The sharp slope of frequency vs. current curve around this optimum point makes this approach only practical for tiny ripples (i.e. 1 mV in [58]). In [59, 60], two constant-g_m bias circuits with different current sensitivities to supply are employed in a ring oscillator (RO) to generate a more stabilized current under supply variations. Furthermore in [60], a calibration loop was added to obtain a more accurate current sensitivity ratio between the two constant-g_m stages. However, the spur level improvement is limited to $\sim$10 dBc for low ripple frequencies ($f_{\text{rip}} < 1$ MHz) and gets even worse when f_{rip} increases [60]. Moreover, even when applied to an LC oscillator, the mismatches in the current mirroring ratios limit the spur level to no better than -35 dBc under a 50 mV_{pp} ripple.

There are also some frequency compensation techniques based on a PLL [62–67]. In [62], the PLL loop needs to be periodically opened for calibration. In [63], a test signal that is slow enough compared to the PLL bandwidth is applied on the supply of a ring oscillator, but this could lead to a long calibration time of more than hundreds of microseconds. Moreover, unlike in a ring oscillator [62, 63], it is difficult to modulate the supply of an LC oscillator. For [64] and [65], f_{rip} should be limited to less than 1 MHz for the techniques to be effective. This limitation is mainly a result of the finite bandwidth of the sub-sampling phase detector in the loop [64] or measuring the frequency deviation with a counter [65]. In [66], the supply induced frequency variation is compensated by adding a replica generation block to the reference path. However, the additional block is

bulky and power-hungry, while the PLL bandwidth may also restrict the maximum ripple frequency that can be handled. A noise suppression loop was implemented in [67]. It detects the ripple-induced frequency variation by comparing the inverter delay in an RO with a voltage-controlled delay cell, and corrects it through a feedback control. However, for LC oscillators that do not provide multiple phases, the delay cell should cover the full oscillation period, thus increasing its power and area consumption.

This chapter proposes a feed-forward supply ripple replication and cancellation technique wholly contained within an LC oscillator in order to make it *practically* insensitive to supply ripples of switching DC-DC converters. The proposed technique manipulates the gate voltage of customarily used tail current transistor and does not require any extra voltage headroom. The chapter is organized as follows. Section 4.2 discusses operating principles of the proposed technique, while detailed circuit design is given in Section 4.3. Measurement results are disclosed in Section 4.4.

4.2 Feed-forward Ripple Replication and Cancellation

As argued above, the supply pushing of LC-tank oscillators, even those at state-of-the-art, needs to be substantially reduced to allow them to operate *directly* from DC-DC converters, which naturally contain high level of ripples. In this section, the operating principle of the proposed supply pushing reduction technique based on the ripple replication and cancellation will be elaborated.

4.2.1 Mechanism of Supply Pushing

The variation of oscillating frequency f_{osc} with the supply voltage, V_{DD}, is mainly caused by the variation of parasitic capacitances seen by the resonant tank [68]. The cross-coupled transistors provide a negative transconductance to sustain the oscillation and will experience cut-off, saturation and triode operating regions during each oscillation cycle. When V_{DD} varies, the tail current, I_0, and the corresponding oscillation amplitude, V_{osc}, will also vary. Thus it will change the time interval during which

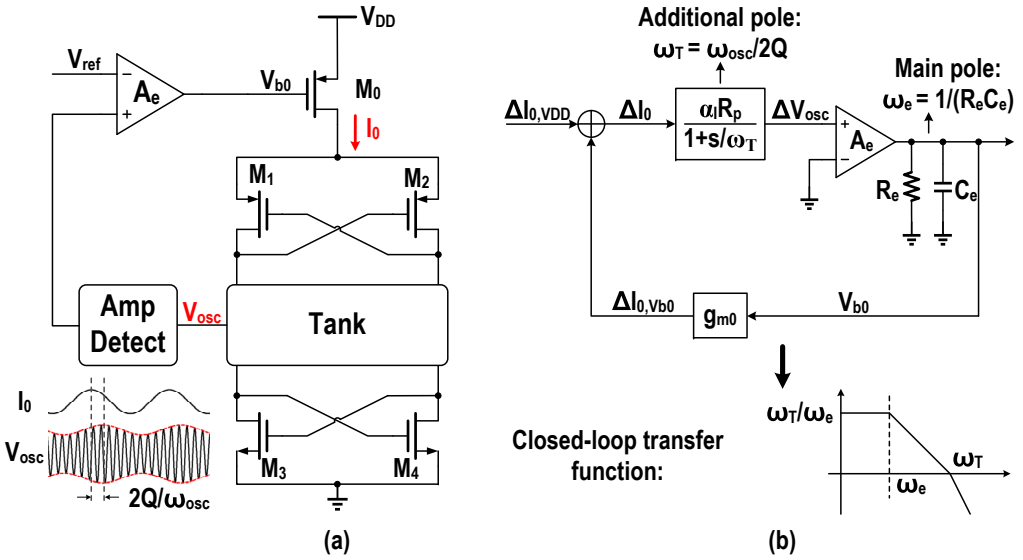


Figure 4.1: (a) Schematic and (b) block diagram of an LC oscillator with amplitude tracking loop.

the transistors stay in each operating region. Since the gate capacitance of MOS transistors shows nonlinear dependence on the voltages at their terminals (i.e. $V_{\rm gs}$ and $V_{\rm ds}$), the change in their operating states would vary the equivalent parasitic capacitance, $C_{\rm par,equ}$ [69]. Thus, the oscillating frequency will be pushed. If a periodical ripple is on $V_{\rm DD}$, I_0 and $V_{\rm osc}$ will also show periodical variations. Therefore, the change of $C_{\rm par,equ}$ will also be periodical and could manifest itself as large spurs in the output spectrum of the oscillator. To be able to obtain a clean output spectrum when $V_{\rm DD}$ contains ripples, I_0 and $V_{\rm osc}$ should be stabilized under $V_{\rm DD}$ variations.

4.2.2 Amplitude Tracking Loop

Conventional solutions to stabilize the oscillating amplitude of an LC oscillator resort to employing an amplitude tracking loop across PVT variations [70] and to bias the oscillator at the optimum operational point [best figure-of-merit (FoM)] [71]. It is instructive to examine this loop for stabilizing I_0 and $V_{\rm osc}$ under supply ripples.

Fig. 4.1 (a) shows the schematic of an LC oscillator with amplitude tracking loop. The tail current source transistor, M_0 is PMOS, which is fairly robust to (local) ground induced perturbations. Replacing M_0 with an NMOS transistor will not help much as its $V_{\rm gs}$ will be now very sensitive to local ground perturbations and its I_0 sensitivity to $V_{\rm DD}$ will

still be felt through the M_0's channel length modulation. The loop first detects the oscillation amplitude, and then compares it with the reference value V_{ref}. The comparison outcome will adjust I_0 by varying the gate bias voltage V_{b0} of M_0. This feedback loop will keep on working to fix V_{osc} at the level corresponding to V_{ref}. When I_0, and correspondingly V_{osc}, are modulated by the supply ripple, V_{b0} will be modulated in reaction through the amplitude tracking loop. As a result, the variation of I_0 and V_{osc} will be reduced by an amount equal to the loop gain of the amplitude tracking loop, thus reducing the variation of oscillating frequency.

Unfortunately, this method is limited by the pole from the resonance tank. When the supply varies, I_0 will follow almost immediately. However, due to a 'memory' of the tank, there is a time delay, $2Q/\omega_{osc}$, between the variation of the current flowing through the tank and the subsequent effect on the oscillation amplitude across the tank, as shown in Fig. 4.1 (a) [70]. Such a time delay creates an additional low-frequency pole located at $\omega_{osc}/(2Q)$ and will limit the bandwidth of the amplitude tracking loop [see Fig. 4.1 (b)] [72]. This bandwidth limitation could limit the spur level that can be reached with this method. To alleviate this limitation, the pole at the output of the amplifier must be pushed to a very high frequency, since the pole related to the tank is almost fixed. However, this may lead to a significant increase in the current consumption of the loop.

4.2.3 Proposed Technique

In this section, a feed-forward supply pushing reduction technique for LC oscillators that entirely avoids the use of the amplitude tracking loop around the oscillator core is proposed. Fig. 4.2 (a) illustrates its principle. To stabilize I_0, and thus V_{osc}, in face of V_{DD} variations, a replica of the supply ripple is applied to the gate of PMOS current source M_0 to stabilize its V_{gs}. As a result, the variation of I_0 and V_{osc} would be largely suppressed. If M_0 is an ideal device, whose drain current is solely controlled by its V_{gs} according to the square law, then an exact copy of the supply ripple waveform is required at its gate terminal V_{b0} to keep I_0 and V_{osc} constant. As shown in Fig. 4.2 (b), the variations of I_0 and V_{osc} do get largely suppressed when the waveform applied at V_{b0} is the same as that of the supply ripple (gain, $G = 1$). Hence, the frequency variations due to the supply voltage are

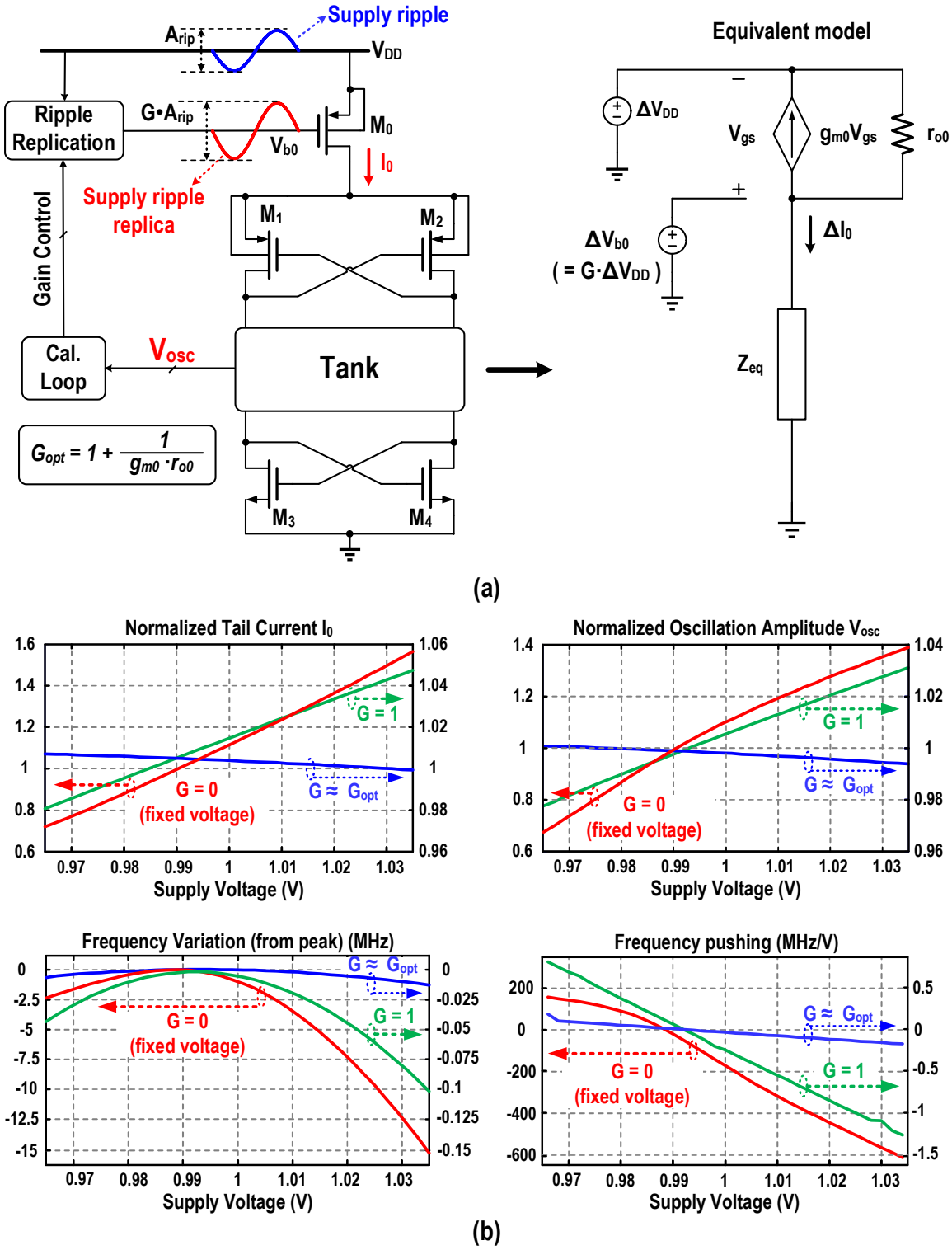


Figure 4.2: (a) Conceptual block diagram of the proposed supply pushing reduction technique with the equivalent model to estimate the optimum gain (G_{opt}) of the ripple replication block, and (b) simulation results of an LC oscillator with the proposed technique.

largely reduced, resulting in a much lower supply pushing of the oscillator. However, for nanoscale CMOS technologies, the channel-length modulation

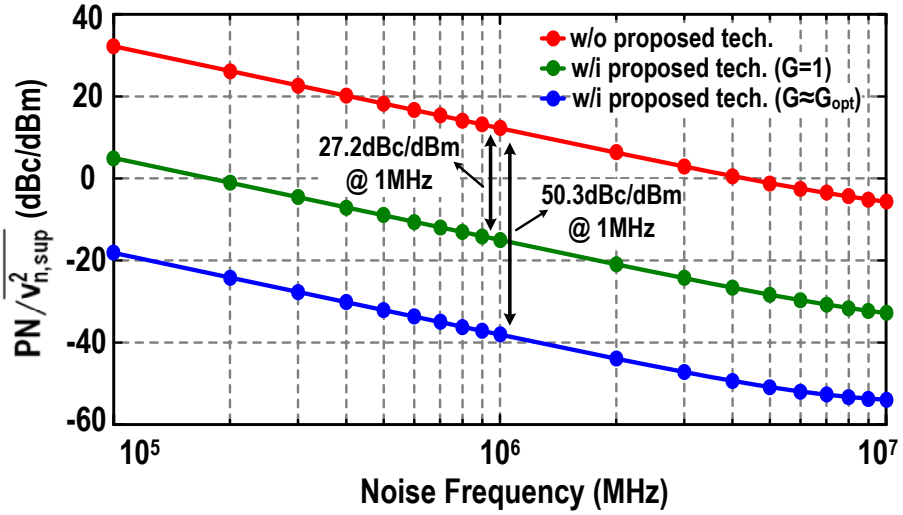


Figure 4.3: Simulated transfer function of the supply noise to phase noise of the oscillator with/without the proposed supply pushing reduction technique.

effect is not negligible. This means that the drain current of M_0 also depends on its V_{ds}. Thus the waveform at V_{b0} should be an *amplified* replica of the supply ripple to compensate for the residue current variation due to the variation of V_{ds} of M_0. Fig. 4.2 (a) also shows the equivalent model to estimate the optimum gain (G_{opt}). Based on this model, the supply variation, ΔV_{DD}, induced tail current variation, $\Delta I_{0,V_{DD}}$, could be calculated as

$$\Delta I_{0,V_{DD}} \approx \frac{1 + g_{m0} \cdot r_{o0}}{r_{o0} + Z_{eq}} \Delta V_{DD} \tag{4.1}$$

while the tail current variation induced by $\Delta V_{b0} = G \cdot \Delta V_{DD}$ is

$$\Delta I_{0,V_{b0}} \approx -\frac{g_{m0} \cdot r_{o0}}{r_{o0} + Z_{eq}} \Delta V_{b0} \tag{4.2}$$

where Z_{eq} is the large-signal equivalent impedance of the cross-coupled transistors M_{1-4} and the tank that is seen by M_0, while g_{m0} and r_{o0} are the effective transconductance and output resistance of M_0, respectively. To compensate for the tail current variation due to V_{ds}, the magnitudes of (4.1) and (4.2) should be equal. Hence, G_{opt} is calculated as

$$G_{opt} \approx 1 + \frac{1}{g_{m0} \cdot r_{o0}}. \tag{4.3}$$

Since $g_{m0} \cdot r_{o0}$ is relatively large (e.g. >10), G_{opt} is slightly higher than 1. Fig. 4.2 (b) also shows that I_0 and V_{osc} are further stabilized (i.e. ~10×

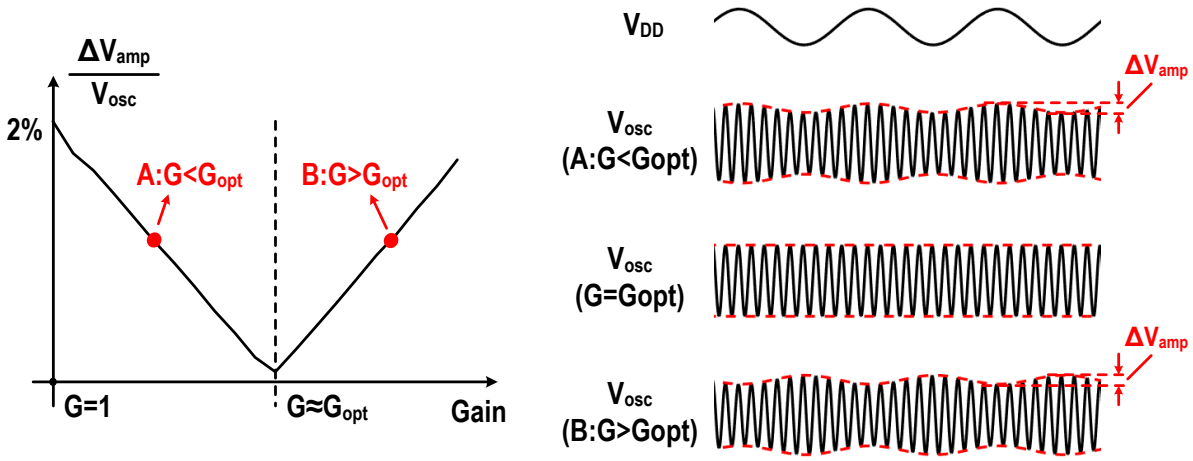


Figure 4.4: Operating principle of the calibration loop based on oscillation amplitude variation (ΔV_{amp}).

smaller variations compared to $G = 1$ case) under supply variations when $G \approx G_{\text{opt}}$, thus the supply pushing of the oscillator becomes much lower. It also translates into a significant reduction in the thermal noise of supply to phase noise (PN) conversion as can be gathered from Fig. 4.3.

The similar feed-forward principle was applied to LDOs in order to improve their PSR at several megahertzs of ripple frequencies [47, 49, 73]. However, they lack a reliable calibration for the optimum gain, which will be proposed later. Also, they still tend to use large off-chip capacitors [49] or extra on-chip capacitance occupying large silicon area [47]. When the LDO is integrated with a current-biased oscillator, the pass transistor should be placed above the tail current source M_0, thus consuming extra voltage headroom. Merging the pass transistor with M_0 would reclaim this headroom, but the oscillator becomes voltage-biased, whose current is poorly controlled over PVT variations. Also, higher supply sensitivity of a voltage-biased oscillator would place higher demands on the PSR performance of the LDO, resulting in large power and area overhead [74].

The amplified supply ripple replica at V_{b0} is generated by the proposed ripple replication block (RRB). As can be gathered from (4.3), the optimum gain is prone to PVT variations. Therefore, a calibration loop is also integrated on-die, as indicated in Fig. 4.2 (a). The calibration scheme is based on measuring the variation of the oscillation amplitude, ΔV_{amp}, in response to the V_{DD} perturbations. Fig. 4.4 shows the operating principle. When $G < G_{\text{opt}}$ (case A), $\Delta I_{0,V_{\text{bo}}}$ is smaller than $\Delta I_{0,V_{\text{DD}}}$, so ΔV_{amp} is in

phase with ΔV_{DD} and decreases in magnitude as G gets closer to G_{opt}. However, when $G > G_{\mathrm{opt}}$ (case B), $\Delta I_{0,V_{\mathrm{b0}}}$ becomes larger than $\Delta I_{0,V_{\mathrm{DD}}}$. Then, ΔV_{amp} is out of phase with ΔV_{DD}, and its magnitude increases again with the increase of G. At the optimum point, $G = G_{\mathrm{opt}}$, and ideally a constant oscillation amplitude is maintained under supply variations. Thus, the calibration loop measures ΔV_{amp} under different gain settings to calculate the optimum operating point for the oscillator circuit.

4.3 Circuit Implementation

This section discusses the detailed circuit realization of a 5 GHz LC oscillator with the proposed feed-forward supply pushing reduction technique and the on-chip calibration loop.

4.3.1 Ripple Replication Block

Fig. 4.5 shows the schematic of the implemented LC oscillator with the RRB. Here, the complementary cross-coupled oscillator structure is chosen due to its lower power consumption compared to its NMOS- and PMOS-only counterparts at the same V_{DD} and equivalent parallel resistance of the tank [75].

The RRB is proposed to bias the gate terminal of tail current source of the LC oscillator. To generate the required replica with the desired gain larger than 1, the ripple replication block is logically divided into two parts. The first part (dashed grey box in Fig. 4.5) contains a diode-connected PMOS transistor, $\mathrm{M_{b0}}$, in series with two cascode NMOS transistors, $\mathrm{M_{b1,2}}$. Due to the high output impedance of the cascode, $\mathrm{M_{b0}}$ just 'replicates' the supply ripple to V_{b0} with a fixed gain of 1. Thus, the first term on the right hand side of (4.3) is covered by this part. To boost the gain above 1, the fractional part (dashed blue box in Fig. 4.5) is introduced to inject some extra current proportional to V_{DD} into the cascode node, V_{inj}. To digitally control the fractional gain, current sources $\mathrm{M_{pk}}$ $(k = 0, 1, \ldots, n)$ are individually turned on/off by switch transistors $\mathrm{M_{sk}}$ $(k = 0, 1, \ldots, n)$ according to the digital code S_{t} generated by the calibration loop. The fractional part thus provides an adjustable transconductance between V_{DD} and V_{inj}. The ultimate gain G provided by the ripple replication block is

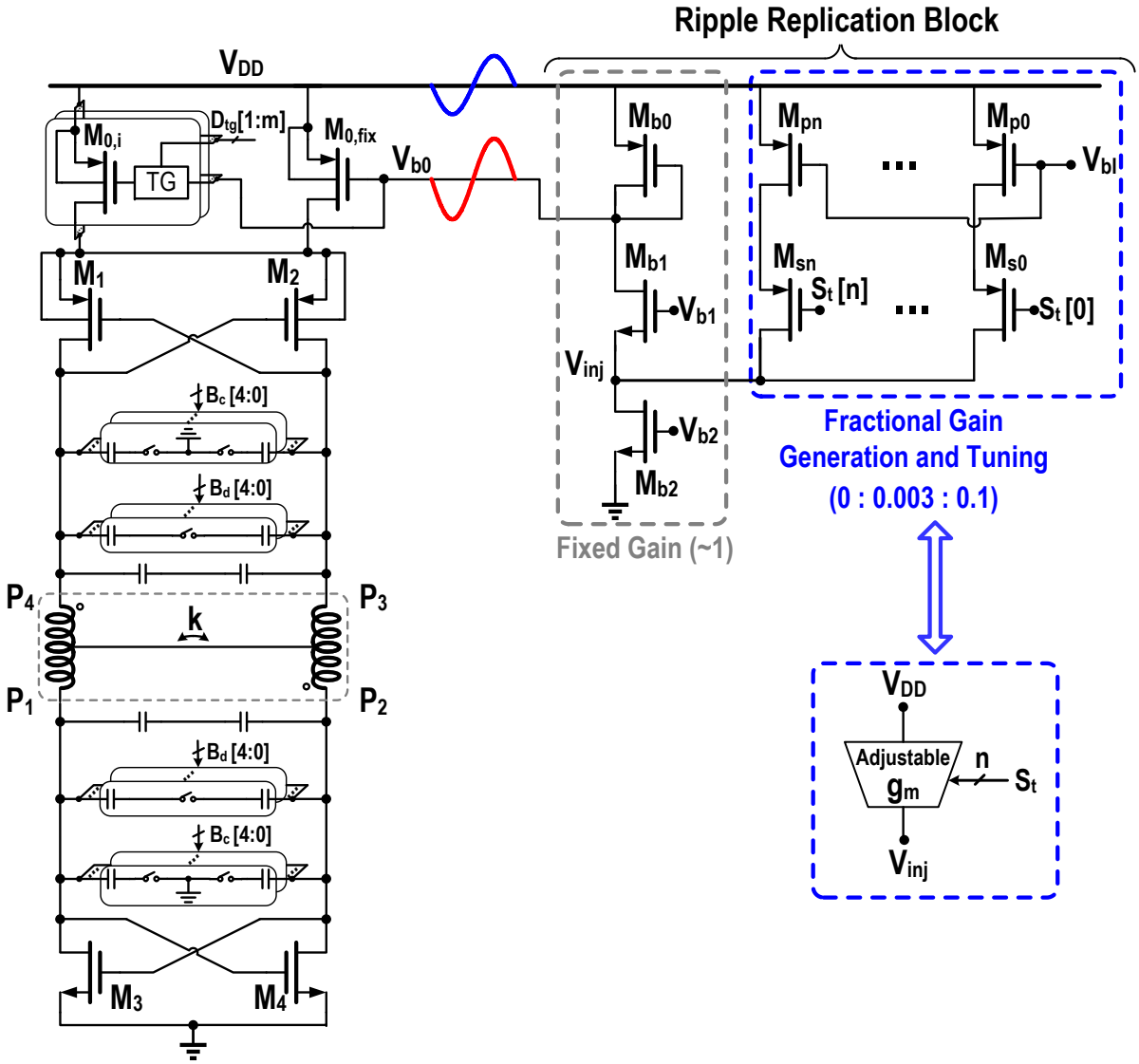


Figure 4.5: Schematic of the implemented LC oscillator with the RRB.

calculated as

$$G = a + b \cdot \frac{g_{m,f}}{g_{m,b0}} \tag{4.4}$$

where $g_{m,f}$ and $g_{m,b0}$ are the total equivalent transconductance of the fractional part and the transconductance of $\mathrm{M_{b0}}$, respectively. The coefficients a and b in (4.4) are determined by

$$\begin{cases} a = \dfrac{(1+g_{m,b0}\cdot r_{o,b0})(r_{o,b1}+r_{o,b2}+g_{m,b1}\cdot r_{o,b1}\cdot r_{o,b2})}{(1+g_{m,b0}\cdot r_{o,b0})(r_{o,b1}+r_{o,b2}+g_{m,b1}\cdot r_{o,b1}\cdot r_{o,b2})+r_{o,b0}} \\ b = \dfrac{g_{m,b0}\cdot r_{o,b0}(1+g_{m,b1}\cdot r_{o,b1})r_{o,b2}}{(1+g_{m,b0}\cdot r_{o,b0})(r_{o,b1}+r_{o,b2}+g_{m,b1}\cdot r_{o,b1}\cdot r_{o,b2})+r_{o,b0}} \end{cases} \tag{4.5}$$

where $g_{m,bi}$ and $r_{o,bi}$ are the transcoductance and output resistance of $\mathrm{M_{bi}}$,

respectively. Given that $g_{m,bi} \cdot r_{o,bi} \gg 1$, the gain G could be approximated as

$$G \approx 1 + \frac{g_{m,f}}{g_{m,b0}} \tag{4.6}$$

Since G_{opt} is only slightly larger than 1, the required $g_{m,f}$ should be much smaller than $g_{m,b0}$. Therefore, the total current injected into V_{inj} is much smaller than the current consumed by M_{b0}, and would not lead to a large variation of the operating point of the LC oscillator. In practice, the gain provided by the integer part is slightly lower than 1 due to the finite output impedance of the cascode transistors [as can be gathered from (4.4) and (4.5)]. Furthermore, for designs with lower V_{DD}, the cascode transistor M_{b1} could be removed which would further reduce the gain of the integer part. However, any reasonable (i.e., ∼5%) integer gain degradation can be easily covered by the fractional part.

4.3.1.1 Bandwidth and Power Consumption Trade-off

The required bandwidth of the ripple replication block is determined by the maximum spur level allowed at the highest ripple frequency.

Assuming a phase shift of θ between the supply ripple at oscillator's V_{DD}, which is $0.5 \cdot A_{\text{rip}} \cos(2\pi f_{\text{rip}} t)$, and the generated replica at V_{b0} at the optimum gain, the tail transistor M_0 would experience an effective supply variation of

$$V_{\text{rip,eff}} = -A_{\text{rip}} \cdot \sin\left(\frac{\theta}{2}\right) \cdot \sin\left(2\pi f_{\text{rip}} t - \frac{\theta}{2}\right), \tag{4.7}$$

where A_{rip} is the peak-to-peak amplitude of the supply ripple. Therefore, the spur level in the output spectrum of the oscillator could be calculated as

$$S_{\text{spur-carrier}} = 20 \cdot \log_{10}\left(\frac{K_{\text{push}} \cdot A_{\text{rip}} \cdot \sin\left(\frac{\theta}{2}\right)}{2 f_{\text{rip}}}\right). \tag{4.8}$$

To guarantee $<\!-50\,\text{dBc}$ spur level at $f_{\text{rip}} = 20\,\text{MHz}$, which is the highest ripple frequency considered in this implementation, the maximum tolerable θ is calculated to be ∼3° under $50\,\text{mV}_{\text{pp}}$ ripple and $K_{\text{push}} \approx 100\,\text{MHz/V}$.

In the frequency range of interest, the ripple replication block may be approximated as a single-pole system, with the pole located at $\omega_p = g_{m,b0}/C_{\text{L}}$, where C_{L} is the capacitive load at V_{b0}. Thus, to obtain ∼3° phase

shift at 20 MHz, $\omega_p \approx 400$ MHz is required. Considering ∼800 fF load, the calculated $g_{m,b0}$ should be about 2.0 mS. With $g_m/I_{ds} \approx 12$, the current consumption of the integer part is calculated to be ∼170 μA. Together with the ∼12 μA consumed by the fractional part at the maximum G of ∼1.1, the total current consumption of the ripple replication block is around 180 μA. The PMOS transistors in the fractional part are sized to achieve tuning resolution of ∼0.003 as a trade-off between the resolution and calibration time. Therefore, a 5-bit thermometer code is implemented to cover the aforementioned maximum G.

Due to the distributed layout design, there could be a delay between the routed V_{DD} at the oscillator's M_0 source and at the ripple replication block. That delay can increase the ripple phase shift θ of the ripple replication block. In this design, since the proposed ripple replication block is simple and compact, it is easily placed next to M_0. Hence, this effect is negligible, especially at ripple frequencies < 20 MHz.

4.3.1.2 Sizing and Biasing of Tail Transistor

The tail current transistor M_0 is designed here with a channel length of 120 nm, contributing to the capacitive load C_L mentioned above. The optimal gain G_{opt} is simulated to be in the middle of the 1–1.1 range provided by the ripple replication block, leaving enough margin on both sides. By using M_0 with a shorter channel length, C_L could be reduced, leading to a lower power consumption. However, the required G_{opt} would increase due to a smaller output resistance of M_0, which could adversely affect the tuning resolution and/or calibration time.

Under the 1 V nominal supply voltage, V_{ds} of M_0 is chosen to be around 250 mV. A smaller V_{ds} may allow the oscillator to operate under lower supply voltage, thus reducing its power consumption. However, a larger M_0 would be needed to provide similar tail current, which also generates more noise, degrading the PN and FoM performance of the oscillator [76]. Moreover, with a lower V_{ds}, the output resistance of M_0 also becomes smaller, leading to an increase in G_{opt}. Combined with the increased parasitic capacitance due to the larger device size, the bandwidth of the ripple replication block would be reduced under similar power consumption, thus increasing the phase shift θ of the replica at V_{b0}. As discussed above, this would increase

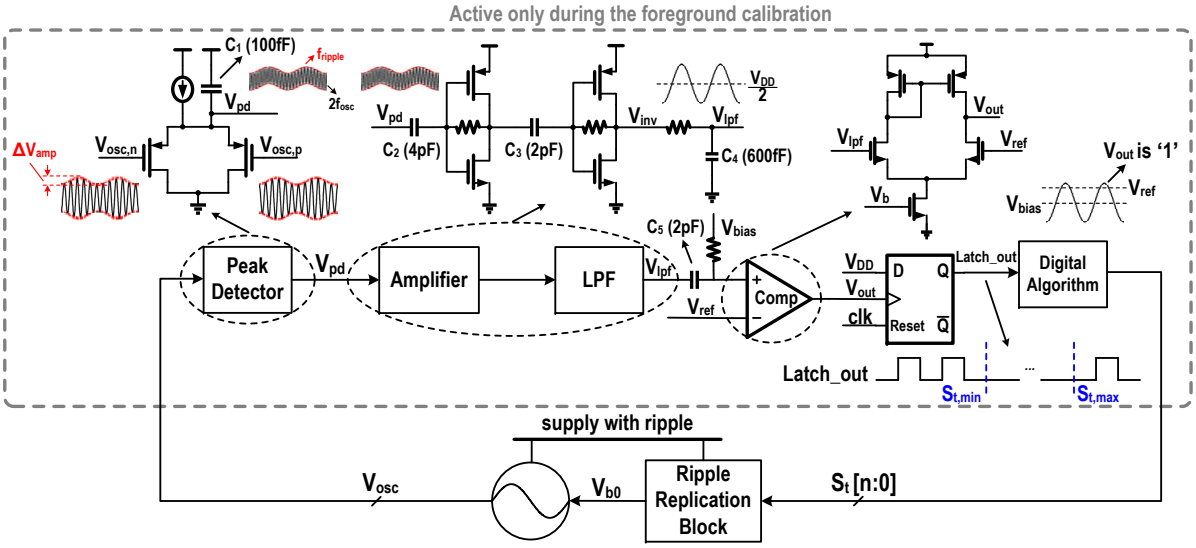


Figure 4.6: Block diagram of the calibration loop.

the output spur level of the oscillator. Hence, it is not beneficial to reduce V_{ds} further.

In the actual design, M_0 is implemented as a parallel combination of a fixed part, $\mathrm{M}_{0,\mathrm{fix}}$, with a bank of unit transistors, $\mathrm{M}_{0,\mathrm{i}}$, as shown in Fig. 4.5. Each $\mathrm{M}_{0,\mathrm{i}}$ could be switched in separately to tune the oscillation swing by enabling the corresponding transmission gate (TG) before its gate terminal with the control code $D_{\mathrm{tg,i}}$. When TG is disabled by $D_{\mathrm{tg,i}}$, the gate terminal of $\mathrm{M}_{0,\mathrm{i}}$ is also pulled up to V_{DD}. The tail current resolution is $\sim$30 μA to ensure the oscillator operates within 1 dB of its optimum PN across the tuning range (TR). To cover the required current range under PVT variations, 27 such unit transistors are implemented.

4.3.2 Calibration Loop

Fig. 4.6 shows the block diagram of the integrated calibration loop. As discussed in Section 4.2.3, the perturbation of the oscillation amplitude, ΔV_{amp}, is used in the loop as a stimulus to calibrate G_{opt}. Hence, the outputs of the oscillator are first connected to a peak detector. Ideally, the output of the peak detector, V_{pd}, contains two frequency components: the desired one at f_{rip}, and the additional one at the second harmonic of the oscillation frequency, f_{osc}. V_{pd} is then amplified through self-biased inverters. To amplify the small input level at V_{pd} (e.g., 1 mV) to a large enough amplitude (e.g., 250 mV) at the output, a large gain (e.g., 48 dB)

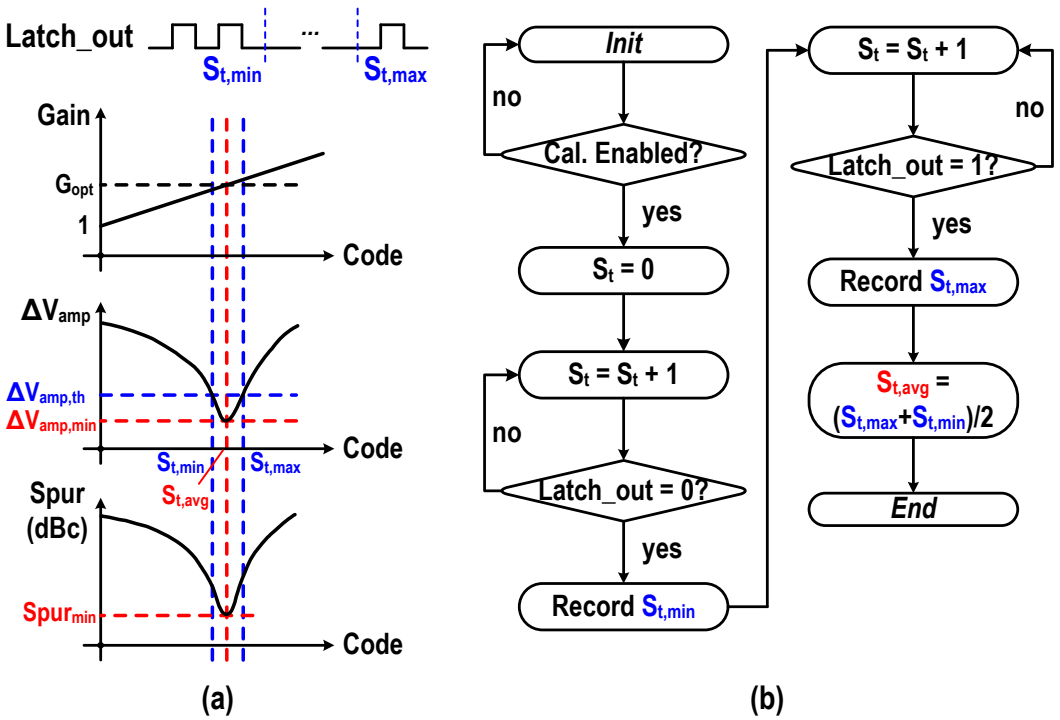


Figure 4.7: (a) Operating principle and (b) flow chart of the calibration loop with the proposed algorithm.

is needed. Hence, two inverter stages with bandwidth of ∼20 MHz are implemented to provide the required gain [see Fig. 4.8 (a)]. The output of the inverter chain, V_{inv}, is filtered by a simple RC low-pass filter (LPF). The cut-off frequency of the LPF is set to pass through the desired frequency component at f_{rip}, while the second harmonic at $2 \times f_{\mathrm{osc}}$ is filtered out. If there is any mismatch in the input differential pair of the peak detector, V_{pd} would contain a third frequency component at f_{osc}. Since f_{osc} (several gigahertzs) is much higher than f_{rip} (tens of megahertzs), this component is easily filtered out by the inverter chain and the LPF. Hence, the mismatch in the peak detector will not affect the calibration results. The output of the LPF, V_{lpf}, is then compared with a reference value, V_{ref}, through a comparator. V_{ref} is roughly set to a voltage higher than the product of the desired ΔV_{amp} and the DC gain of the peak detector cascade with the inverter stages. The output of the comparator is connected to the clock terminal of a D flip-flop (DFF). When V_{ref} is crossed, the comparator's output becomes high, triggering the output of the DFF to flip to '1'. The digital algorithm in the loop monitors the latch output, Latch_out, and calculates the optimum control code S_{t} for the ripple replication block.

The digital block attempts to find the minimum point of ΔV_{amp} versus

the control code [$\Delta V_{\mathrm{amp,min}}$ in Fig. 4.7 (a)]. However, to precisely detect $\Delta V_{\mathrm{amp,min}}$, a set of comparators and DFFs would be needed. The simulated amplitude variation at the output of the LPF is ∼300 mV. Thus, 20 comparators, followed by a DFF each, are required to realize a voltage resolution of 15 mV. Some offset calibration techniques may also be needed to reduce the input referred offset of comparators to a level much lower than the voltage resolution. The digital algorithm then counts the number of '1' in the output of the DFFs to determine ΔV_{amp}. Such a method could increase the design complexity greatly. To avoid this, a calibration algorithm is proposed whereby only one comparator without any offset calibration could be used in the loop. Fig. 4.7 (a) shows the operating principle of the proposed technique. The reference voltage, V_{ref}, at the comparator input is roughly set to a value corresponding to an oscillation amplitude variation of $\Delta V_{\mathrm{amp,th}}$, which is higher than $\Delta V_{\mathrm{amp,min}}$. The calibration process starts from a small value of S_{t}, where $G < G_{\mathrm{opt}}$ and $\Delta V_{\mathrm{amp}} > \Delta V_{\mathrm{amp,th}}$. Thus, the initial value of Latch_out is '1'. The algorithm keeps increasing S_{t}, which decreases ΔV_{amp} as G approaches G_{opt}. When ΔV_{amp} becomes lower than $\Delta V_{\mathrm{amp,th}}$, Latch_out changes from '1' to '0'. The algorithm records this code as $S_{\mathrm{t,min}}$, and then increases S_{t} again. When S_{t} is large enough, ΔV_{amp} would be higher than $\Delta V_{\mathrm{amp,th}}$ again, and Latch_out switches back to 1. The algorithm records this code as $S_{\mathrm{t,max}}$, and the optimum code, $S_{\mathrm{t,avg}}$, is calculated as the average of these two recorded codes. Fig. 4.7 (b) reveals the operational flow chart of this calibration process.

Fig. 4.8 (a) shows the simulated transfer function from the output of the peak detector to the input of the comparator. The lower cutoff frequency of this band-pass response is due to the AC-coupling used to accommodate the DC levels of different stages in the loop. It sets the lowest f_{rip} that the loop can handle. In this work, this frequency is designed to be ∼2 MHz. Considering the current trend in increasing the switching frequency of the DC-DC converters to several or even tens of megahertz [77–80], this value appears reasonable. A lower cutoff frequency could be adopted to detect lower ripple frequencies, but at the expense of increased loop settling time. When S_{t} changes in each calibration step, the current injected by the fractional part varies, leading to slight variations in the tail current and the oscillation amplitude of the oscillator. Hence, due to the band-pass

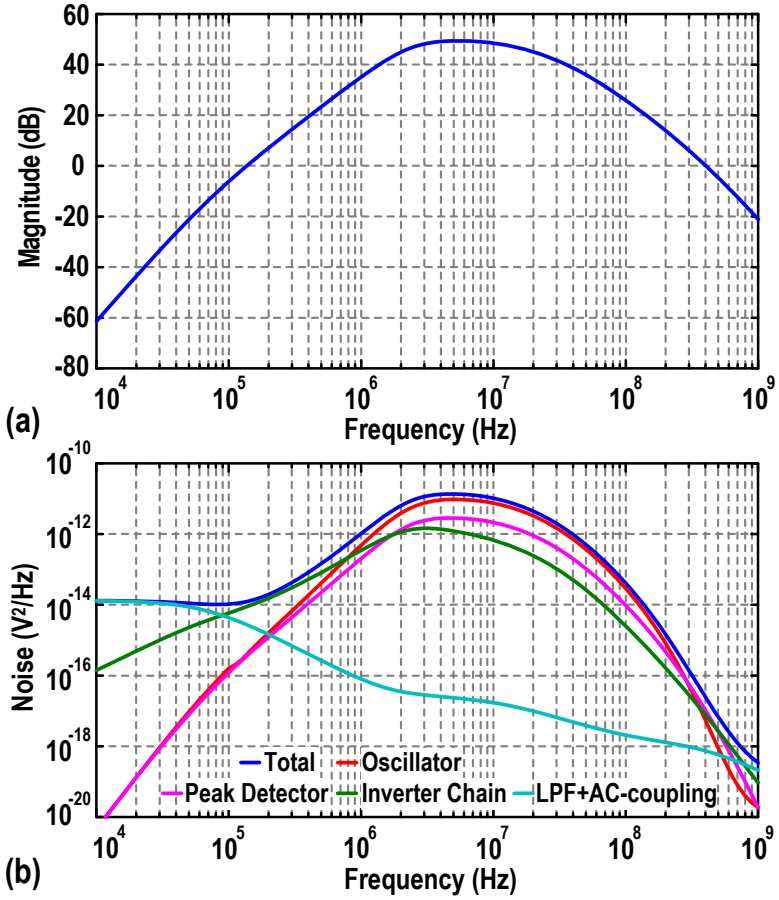


Figure 4.8: (a) Simulated transfer function from V_{pd} to comparator input, and (b) simulated power spectrum density of noise at comparator input with the contribution from different noise sources.

characteristic of the loop, it needs certain time for settling before correctly functioning. With 2 MHz corner frequency, the settling time is 0.5 μs per step.

Fig. 4.8 (b) shows the simulated power spectrum density (PSD) of noise at the comparator's input. The major part of it is contributed by the oscillator itself. The differential output of the oscillator is less affected by the variation of the common-mode voltage, but the output level of the peak detector would be modulated. Thus, the calibration loop is more sensitive to the common-mode noise from the oscillator, e.g. noise of the tail current source. After being shaped by the transfer function of the inverter chain and LPF, the common-mode noise is finally passed to the comparator's input. From Fig. 4.8 (b), the integrated noise is around 14 mV, corresponding to $\sim$0.095 mV equivalent input noise at the input of the peak detector. To achieve <-50 dBc spur level, ΔV_{amp} is simulated to be

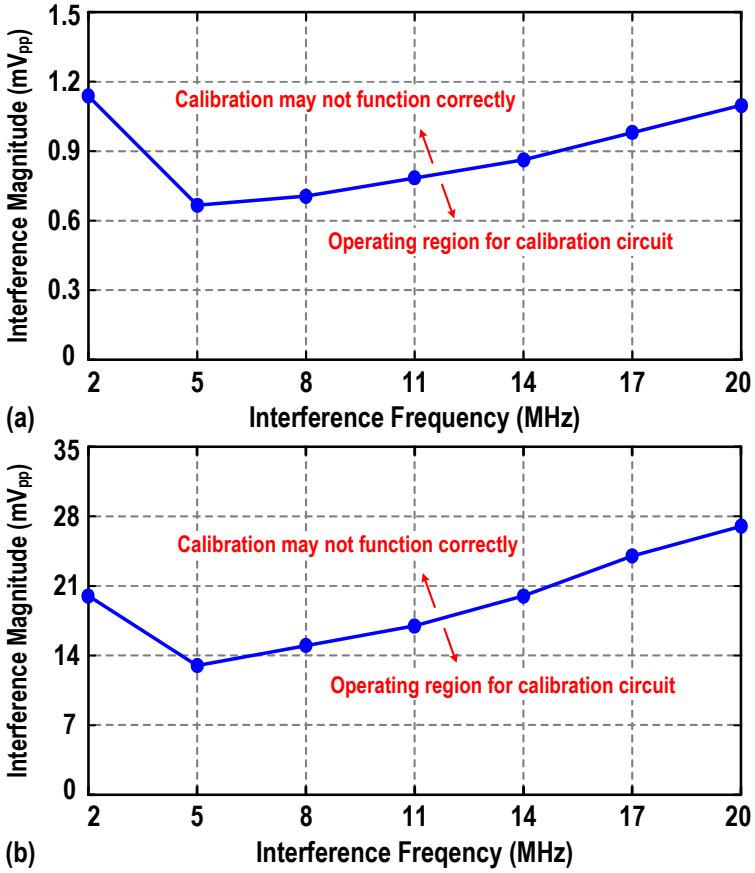


Figure 4.9: Simulated magnitude limit of the interference for effective calibration when the interference is coupled into (a) the DC output of the RRB and (b) the ground.

$\sim$1.8 mV (0.64 $\mathrm{mV_{rms}}$), leading to a SNR of 16.5 dB, which is sufficient for an effective calibration.

The proposed calibration algorithm and RRB are still effective even if the ripple of the DC-DC converter is simultaneously coupled through the supply and other parasitic paths, e.g. into the DC output of the RRB or ground. Since the coupling through both paths would also vary the tail current, and correspondingly the oscillation amplitude, their effect would be detected and minimized by the calibration algorithm through adjusting G_{opt}. Besides the supply ripples, interference from other sources with different frequencies may also modulate the oscillation amplitude. However, with proper design techniques, e.g. shielding and placing guard rings, which are common in oscillator design, the effect of these interference should be non-dominant, and the calibrated code is still around the optimum one.

Figure 4.9 shows the simulation results when the interference is coupled into the DC output of the RRB or the ground while the oscillator supply experiences a 50 $\mathrm{mV_{pp}}$ 8 MHz ripple. When the interference magnitude falls

in the region below the lines in Fig. 4.9, the calibration loop is still able to locate the optimal S_t for suppressing the spur induced by the supply ripples. When the interference magnitude increases above the lines, the calibrated S_t may begin to shift from the optimal one due to the amplitude variation induced by the interference being added onto that induced by the supply ripples. For small code shift, <-50 dBc spur level could still be achieved. When the interference increases further, the code shift would become lager, increasing spur level, and the calibration loop may also fail to converge under a large enough interference. However, considering the active area of the oscillator and the small footprint of RRB placed next to M_0, it seems not realistic to have some interference with magnitude much larger than the $0.6\sim1.2\,mV_{pp}/13\sim28\,mV_{pp}$ limit in Fig. 4.9 when proper design techniques have been adopted.

It should be pointed out that the main purpose of the calibration loop in this prototype is to verify the ripple replication circuitry and the principle of the calibration algorithm. Hence, a quiet supply is used for the calibration loop. If the ripple also exists on the supply of the loop, its effect could be suppressed with RC filtering since the power consumption of the peak detector and the amplifier, which are the supply-sensitive blocks in the loop, is much smaller compared to that of the oscillator. When used in the whole system, e.g., PLL, the calibration loop may also be powered by the regulators used for other supply-sensitive blocks, e.g., TDC and DTC. Since the loop only operates for a short time ($\sim40\,\mu$s in worst case) at system start-up or whenever needed at the beginning of IoT packets, it would not affect the system efficiency and the performance of other blocks during the normal operation. If the entire system was to be powered by the SC converter directly, a >40 dB power supply rejection ratio would be required for the calibration loop. In the next chapter, a modified calibration loop with >60 dB power supply rejection ratio in the frequency range of interest (2–20 MHz) is proposed and integrated in the PLL, making the whole system supply insensitive.

4.3.3 Oscillator Implementation

The designed oscillator uses a transformer-based resonant tank. Since the RRB is connected to the gate of tail current source M_0, its output

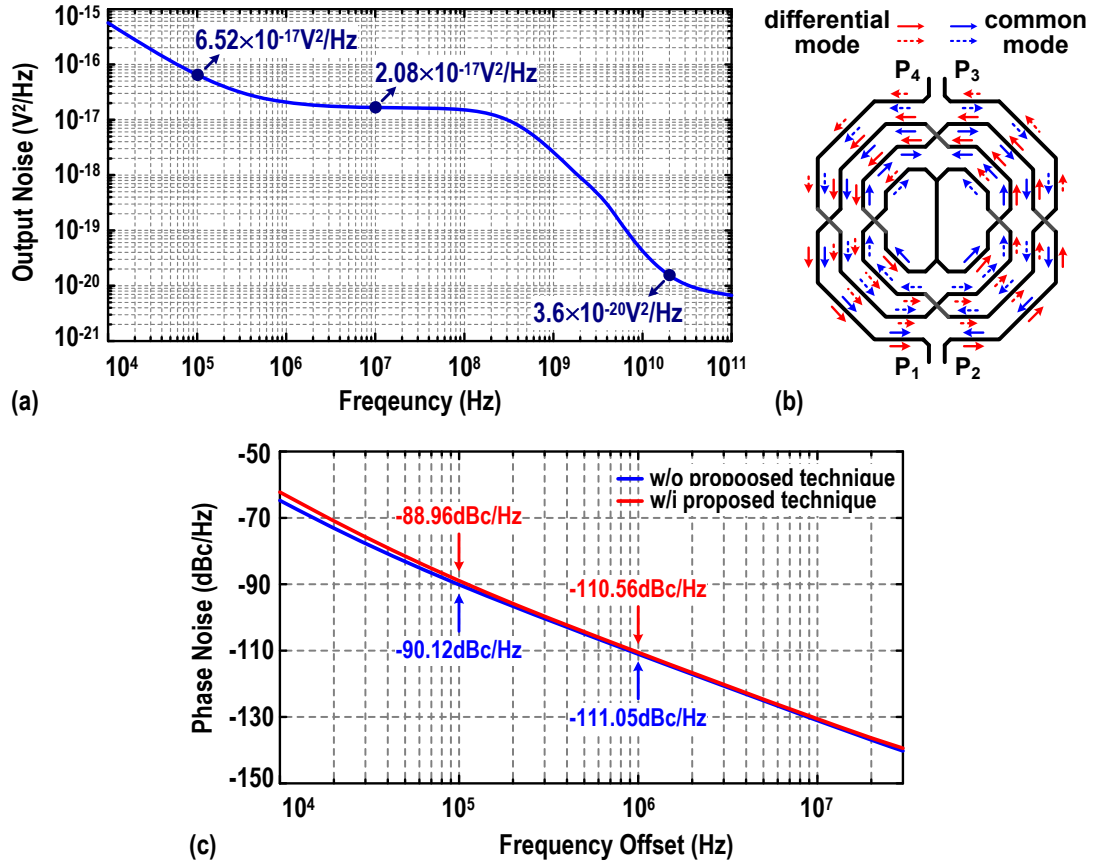


Figure 4.10: (a) Output noise of the RRB, (b) schematic of the symmetrical transformer, and (c) simulated oscillator phase noise w/i and w/o the RRB.

noise [see Fig. 4.10 (a)] will modulate the oscillator's tail current, thus converting into PN. Similar to the tail current noise, only the noise around DC and even harmonics of f_{osc} would cause PN degradation [81–83]. The thermal noise around the even harmonics of f_{osc} is filtered out due to the bandwidth of the RRB, as shown in Fig. 4.10 (a), and would not limit the PN performance. For the noise around DC, its up-conversion into PN is related to the DC component, c_0, of the ISF function of the tail current source [84, 85]. To achieve small c_0, the implicit common-mode resonance technique [35, 86] is employed. Single-ended capacitor banks connected to a symmetrical transformer, as shown in Fig. 4.10 (b), are used to tune the common-mode resonance frequency to around $2 \times f_{\text{osc}}$. Hence, the second harmonic component of the oscillation waveform is aligned with the fundamental one, and would not affect the symmetry of the waveform. Therefore, c_0 is kept small and the up-conversion of the low-frequency noise is largely suppressed [84, 87]. Simulation results in Fig. 4.10 (c) show that the PN degradation is only 1.16 dBc at 100kHz frequency offset. Note

that the reported spot noise (as expressed in nV/$\sqrt{\text{Hz}}$ unit) of the LDOs in [50, 51] at 100 kHz is more than 30 times the value shown in Fig. 4.10 (a). Hence, even with the common-mode resonance technique, the oscillator's PN would be greatly degraded when powered by these LDOs.

Both the NMOS and PMOS cross-coupled transistors M_{1-4} provide the negative transconductance in the complementary structure. The body terminals of the PMOS cross-coupled pair, $M_{1,2}$, are deliberately connected to their source terminals to avoid the body effect. Otherwise, their threshold voltage, V_{th}, would be modulated under supply variations thus varying the oscillation amplitude V_{osc}, consequently pushing f_{osc}. Simulation results show that this body effect could limit the supply pushing to no better than 9.5 MHz/V. Note that the above mentioned NMOS alternative to the tail transistor M_0 would not be effective unless a costly triple-well technology is used.

4.4 Measurement Results

The LC oscillator with the proposed feed-forward ripple replication and cancellation technique is implemented in TSMC 40-nm 1P8M CMOS process without ultra-thick metal layers. The proposed calibration loop is also integrated on-die. Fig. 4.11 (a) shows the chip micrograph. The total active area is 0.23 mm^2, in which the oscillator core occupies about 0.215 mm^2. The additional area occupied by the RRB with its biasing circuit and the calibration loop is just 0.012 mm^2, including 8.7pF capacitance of the calibration loop. To enhance the tank's Q-factor, the symmetrical transformer is designed by stacking the top two metal layers with the aluminum capping layer. The spacing between each turn of the transformer is optimized for a magnetic coupling factor of 0.31. The simulated differential inductance of the transformer is 1.7 nH. Q-factor of the whole tank is estimated to be $\sim$7. The capacitor banks are split into a 5-bit differential bank and a 5-bit common-mode bank to tune the common-mode resonance frequency.

The measured power consumption of the oscillator is around 0.81 mW at the maximum oscillation frequency, while the RRB consumes about 0.2 mW, as shown in Fig. 4.11 (b). Note that the RRB also serves to bias M_0 properly. Therefore, compared to oscillator designs biased through current

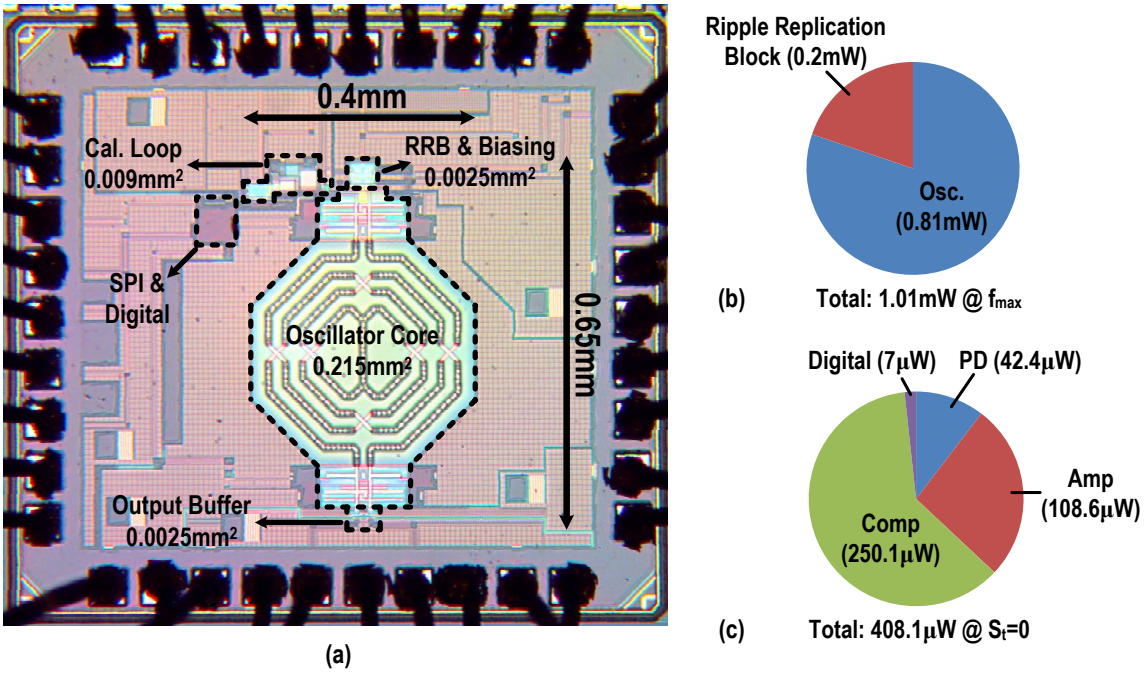


Figure 4.11: (a) Chip micrograph of LC oscillator with reduced supply pushing, (b) measured power breakdown of the oscillator at maximum oscillation frequency during normal operation, and (c) simulated power breakdown of the calibration loop when $S_t = 0$.

mirrors, the extra power consumption is only induced by the fractional part of RRB, which is only around 20 μW in this design. During calibration, the power consumed by the calibration loop when $S_t = 0$, which is the worst case, is around 0.41 mW, and the simulated power breakdown of the loop is also shown in Fig. 4.11 (c). With a longest calibration time at cold start of $\sim$40 μs and a BLE packet length of $\sim$400 μs, the average power consumption of the loop ($P_{\text{cal,avg}}$) when the calibration is done at the beginning of *each* packet would be $< 41\,\mu$W. In practice, the calibration time should be much less than 40 μs since the calibration process is terminated once the optimal code is calculated. Meanwhile, the power consumption of the calibration loop also reduces as S_t approaches the optimal value. When S_t is at the optimal code, the power consumed by the calibration loop is reduced to about 0.26 mW. This is mainly contributed by the decrease of the comparator power consumption from $\sim$0.25 mW at $S_t = 0$ to $\sim$0.09 mW around the optimal S_t, since the tail current source of the comparator is pushed into triode region by the its low input voltage. Using an average value of 0.335 mW and a typical calibration time of 25 μs from simulation, $P_{\text{cal,avg}}$ is reduced to only 21 μW.

The measured tuning range (TR) is 4.9–5.7 GHz (15%). Fig. 4.12 shows

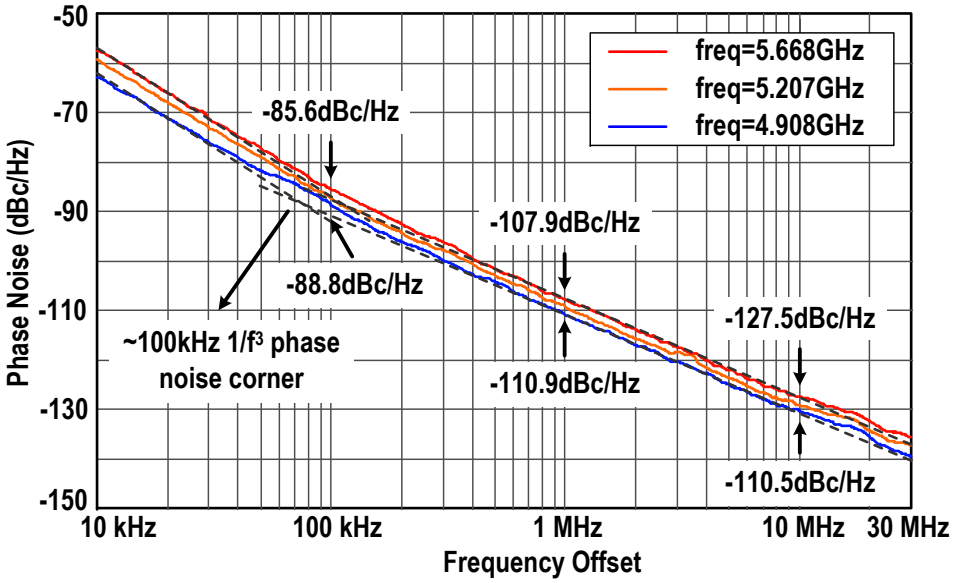


Figure 4.12: Measured phase noise of the oscillator across the TR.

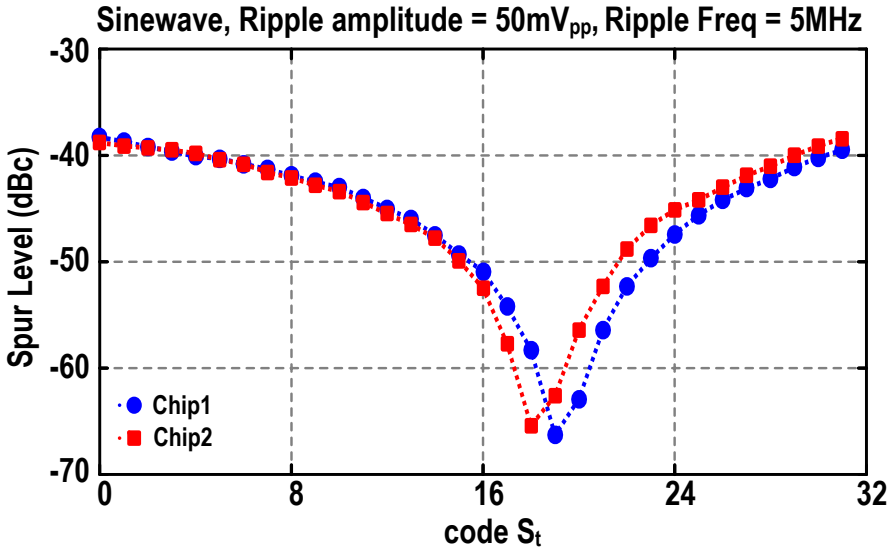


Figure 4.13: Measured spur level over the control code S_t.

the measured PN performance across the TR. PN varies from -108 to $-111\,\mathrm{dBc/Hz}$ @1 MHz offset, with a flicker noise corner of around 100 kHz. To verify the concept of the proposed technique, the control code S_t of the RRB is manually swept while a $50\,\mathrm{mV_{pp}}$ 5MHz sinusoidal ripple is applied on the oscillator supply. As shown in Fig. 4.13, there exists an optimum code at which the spur level is lower than $-60\,\mathrm{dBc}$, corresponding to a $>27\,\mathrm{dB}$ improvement over the $S_t = 0$ case. Note that $G \approx 1$ when $S_t = 0$, and the oscillator already benefits from the significantly reduced supply pushing.

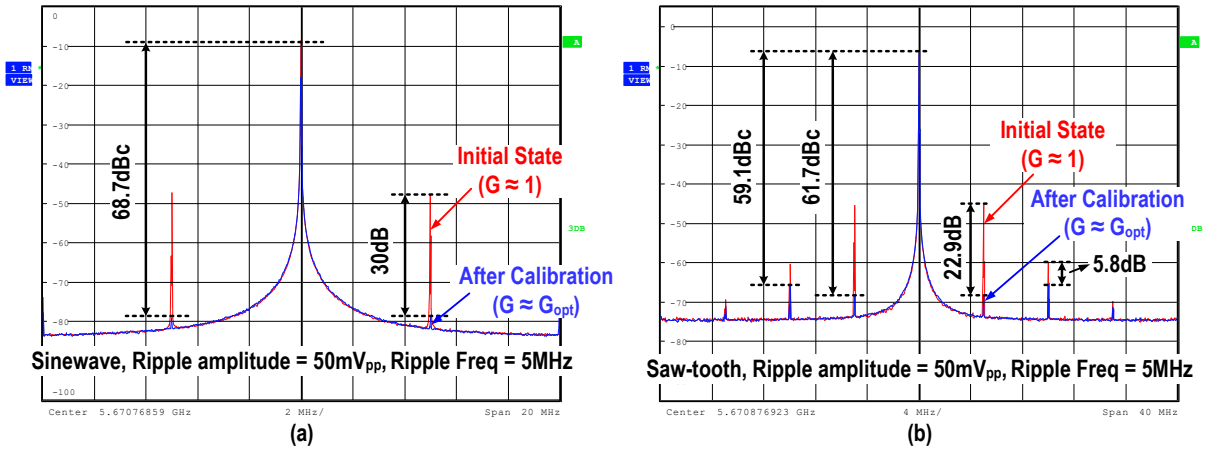


Figure 4.14: Measured oscillator spectra before and after automatic calibration under $50\,\mathrm{mV_{pp}}$ 5 MHz (a) sinusoidal and (b) saw-tooth ripple.

Effectiveness of the automatic calibration loop is verified in Fig. 4.14 (a), which compares the spectra before and after the calibration. With the supply contamination by a $50\,\mathrm{mV_{pp}}$ 5 MHz sinusoidal ripple, the spur level is reduced by 30 dB and reaches −68.7 dBc after the calibration. Fig. 4.15 (a) shows the measured spur level over the frequency of the supply ripple. The proposed technique achieves $\leq$−49 dBc optimum spur levels under $\leq 50\,\mathrm{mV_{pp}}$, 0.5–20 MHz sinusoidal ripples, while the calibrated spur levels closely follow the optimum ones in most cases. In Fig. 4.15 (c), the spur level is measured across the tuning range of the oscillator. The worst-case spur under a $50\,\mathrm{mV_{pp}}$ 5 MHz sinusoidal ripple is $\leq$−59 dBc. Fig. 4.15 (b) and Fig. 4.15 (d) display the oscillator's supply pushing based on the measured spur levels. When the ripple frequency is lower than 12 MHz, the calculated supply pushing is lower than 1 MHz/V for both the optimum and calibrated cases.

Similar measurements are also performed for saw-tooth ripples. The spectra before and after the calibration are compared in Fig. 4.14 (b). Under a $50\,\mathrm{mV_{pp}}$ 5 MHz saw-tooth ripple, the spur at the fundamental offset is reduced by 22.9 dB and reaches −61.7 dBc after the calibration. For spurs at higher harmonics, the suppression is also observed, but with lower magnitudes (5.8 dB suppression for the second harmonic reaching −59.1 dBc after the calibration). Fig. 4.15 (e) reports the spur levels over the ripple frequency. The worst-case spur of −47 dBc is found under $\leq 50\,\mathrm{mV_{pp}}$, 0.5–20 MHz saw-tooth ripples, while the calibration results follow the optima. In Fig. 4.15 (f), the spurs are lower than −58 dBc within

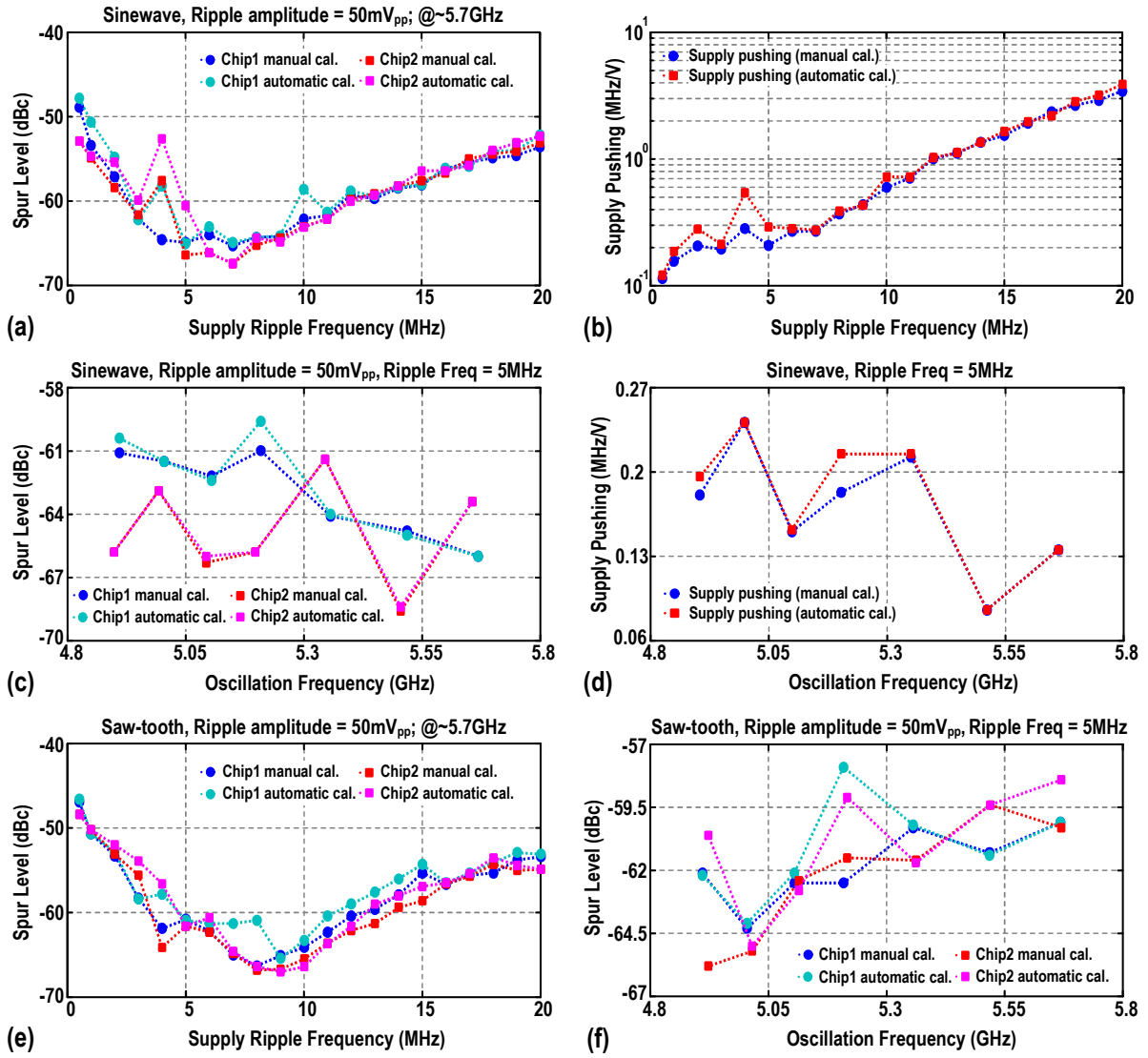


Figure 4.15: (a) Measured spur levels over the sinusoidal ripple frequency and (b) the corresponding supply pushing for both the manual and automatic calibrations; (c) Measured spur levels over the oscillation frequency under the sinusoidal ripple and (d) the corresponding supply pushing for both the manual and automatic calibrations; (e) Measured spur levels over the frequency of the saw-tooth ripple and (f) over the oscillation frequency under the saw-tooth ripple.

the entire tuning range under a 50 $\mathrm{mV_{pp}}$ 5 MHz saw-tooth ripple.

Fig. 4.16 (a) shows the measured oscillator spectrum under a 50 $\mathrm{mV_{pp}}$ 2.5 MHz supply ripple. A spur can also be observed at an offset frequency of 5 MHz (i.e., 2×2.5 MHz). This second ripple harmonic spur mainly comes from the nonlinearity of the fractional part of the ripple replication block. To achieve fine tuning resolution, small transistors with low overdrive voltage are used in the fractional part. Hence, these transistors operate in moderate or weak inversion region, where the nonlinearity is relatively

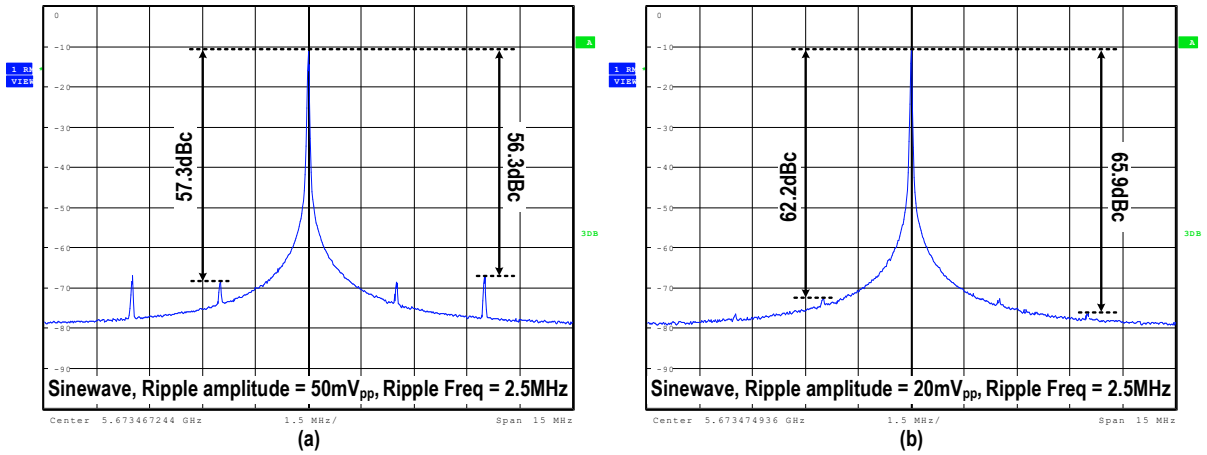


Figure 4.16: Measured oscillator spectra under (a) 50 $\mathrm{mV_{pp}}$ and (b) 20 $\mathrm{mV_{pp}}$ 2.5 MHz sinusoidal ripple.

large. The simulated second harmonic intercept point of these transistors is $V_{\mathrm{IP2}} = 2 \cdot (V_{\mathrm{GS}} - V_{\mathrm{TH}}) \approx 100\,mV$. Consequently, with 50 $\mathrm{mV_{pp}}$ ripple on supply, which is already comparable to the overdrive voltage of the transistors, relatively large second ripple harmonic spur is generated. To improve the performance at the second ripple harmonic, transistors with smaller aspect ratio (W/L) and increased overdrive voltage should be used. Simulations show that the spur at $2 \times f_{\mathrm{rip}}$ is improved by 4.8 dBc when the overdrive voltage of these transistors is increased to 100 mV, while the current penalty is only 3.2 μA at G_{opt}. Also, the spur at the second ripple harmonic falls drastically with a lower ripple amplitude. As shown in Fig. 4.16 (b), the measured spur level at the second harmonic is reduced to -65.9 dBc under a 20 $\mathrm{mV_{pp}}$ ripple, which is a target of our SC converter design, and should bear little practical consequences.

Fig. 4.17 (a) compares the measured oscillator spectra before and after the automatic calibration when the supply is subjected to a two-tone ripple which consists of 8- and 12 MHz components of equal amplitude. The envelope of the ripple is kept at 50 $\mathrm{mV_{pp}}$. The automatic calibration is still effective under this scenario, and the plot shows that the spur at 8/12 MHz offset are reduced by 22.3/20.8 dB and reach $-65.3/-62.4$ dBc respectively after the calibration. The non-linearity effect not only induces small spurs (≤ -64.9 dBc) at the second harmonics of these two tones, but also generates additional spurs at the sum (20 MHz) and difference (4 MHz) frequencies of these two tones with a level of -61.3 dBc and -58.2 dBc respectively, which are still far below the -50 dBc limitation of the IoT

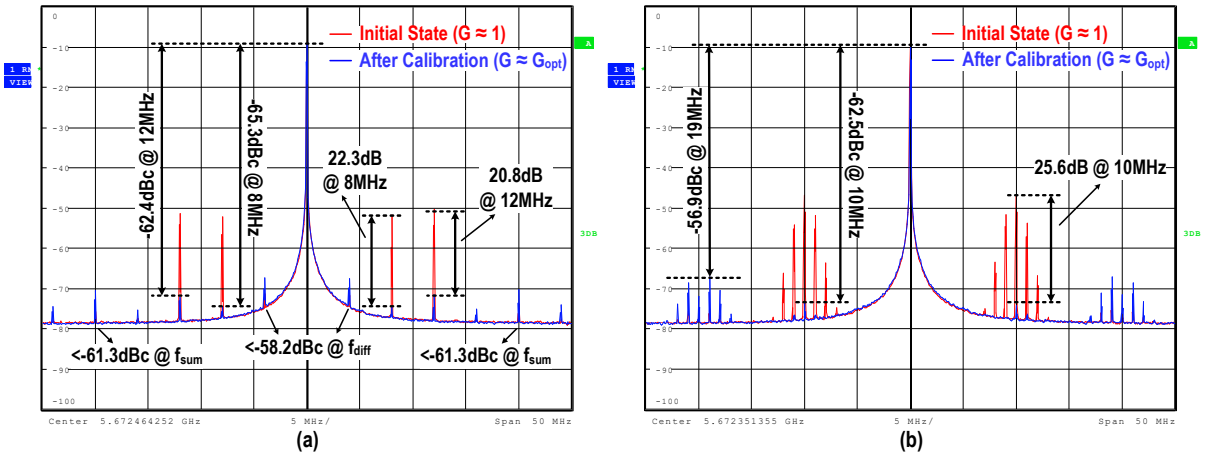


Figure 4.17: Measured oscillator spectra before and after automatic calibration under (a) two-tone and (b) frequency modulated ripple.

applications. Fig. 4.17 (b) compares the measured spectra before and after the automatic calibration when a 50 $\mathrm{mV_{pp}}$ 10 MHz frequency modulated (FM) ripple is applied to the supply. The modulation rate and maximum frequency deviation are both 1 MHz to clearly show the effect of modulation. The plot shows that the spurs around 10 MHz are reduced to ≤ -62.5 dBc after the calibration, corresponding to a 25.6 dB reduction at 10 MHz, while the spurs induced by nonlinearity around 20 MHz are ≤ -56.9 dBc.

Fig. 4.18 shows the measured spur levels under a 50 $\mathrm{mV_{pp}}$ 5 MHz sinusoidal ripple at different DC supply voltages and temperatures. For the variation of the DC supply voltage, the optimal code varies by $\sim\pm 3$ under ± 100 mV variation, and the spur level remains <-50 dBc without any re-calibrations. Due to a relatively low power consumption of the IoT system, the on-chip temperature variation is very slow [88]. As shown in Fig. 4.18 (b), the optimal code only changes by $\sim\pm 1$ under $\pm 10^{\circ}$C variation. Hence, the effect of DC supply variation and temperature drift are slow enough to be compensated by intermittent re-calibrations. Moreover, when a re-calibration is performed once every several or tens of data packets, the starting code S_{t} could be placed near the optimal code of the last calibration. As a result, $P_{\mathrm{cal,avg}}$ is further reduced to a negligible level.

Table 4.1 summarizes the performance of the proposed technique and compares it to prior works. When compared to a state-of-the-art LC oscillator in [35], the proposed technique demonstrates $>10\times$ improvement of the supply pushing. In comparison with other supply pushing reduction techniques [58, 60, 66, 67], the proposed technique shows the lowest supply

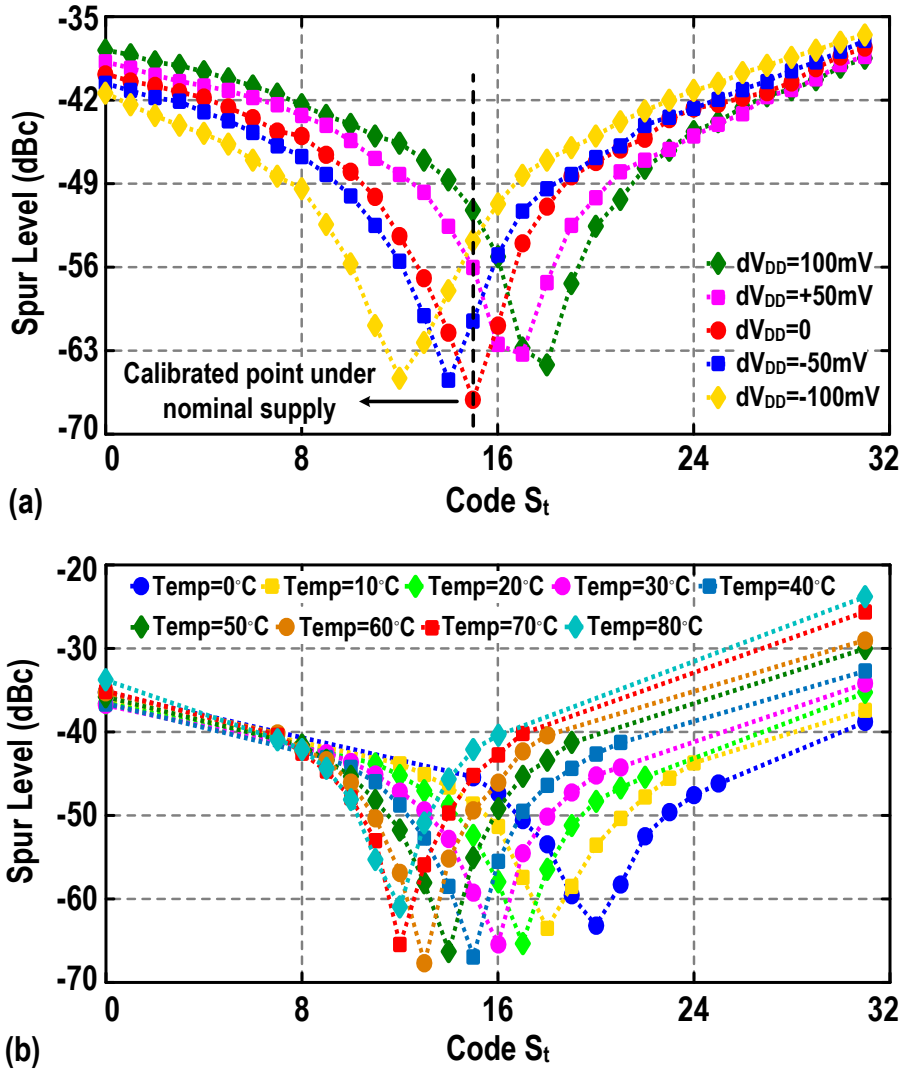


Figure 4.18: Measured spur levels over the control code S_t under different (a) DC supply voltages and (b) temperatures.

pushing, comparable or larger spur reduction, while the additional power is small. The proposed technique is also compared with state-of-the-art LDO designs in Table 4.2. Though [49] achieves higher PSR with a lower power consumption, a large off-chip capacitor is used which is against the IoT miniaturization. Also, it lacks a reliable calibration which could lead to ∼20 dB PSR variation under process and temperature changes. In [47], a correlation-based calibration scheme is implemented, but non-ideal effects, such as an offset of the mixer lead to incorrect calibration results. Moreover, compared with other state-of-the-art LDOs with on-chip capacitors [47, 48, 50, 51], our work demonstrates one of the highest PSR at 10 MHz with less or comparable (extra) power.

Table 4.1: Performance Summary and Comparison with State-of-the-Art

			This work	JSSC2017 [35]	ESSCIRC2016 [66]	ISSCC2014 [58]	ISSCC2016 [60]	VLSI2017 [67]
Description			Feed-forward compensation	$2\times f_{osc}$ implicit resonance	FCW compensation	Bias at lowest K_{push} point	Two constant-Gm biasing	Noise suppression loop
Osc. Type			LC	LC	LC	Ring	Ring	Ring
Tech. (nm)			40 (w/o UTM)	28 (w/i UTM)	65	40	40	65
V_{DD} (V)			1.0	0.9	1.0	1.1	1.1	1.0
Frequency Range (GHz)			4.9-5.7 (15%)	2.85-3.75 (27.2%)	3.2-4.8 (40%)	2.418 (NA)	3.2 (NA)	3.2 (NA)
PN (dBc/Hz) @1MHz			-107.9 to -110.9	-127.5 to -131	-108* @ 3.57GHz	NA	NA	-88*
Ripple Amplitude			$50mV_{pp}$	NA	NA	$1mV_{pp}$	$50mV_{pp}$	$20mV_{pp}$
Sinewave	Spur (dBc)	@1MHz	<-54	NA	NA	-45	-25	-57
		@5MHz	<-58	NA	NA	-49	NA	-48
	K_{push} (MHz/V)	@1MHz	<0.16#	6-30	NA	22.5#	45***	0.63#***
		@5MHz	<0.5#	6-30	NA	70.9#	NA	4#
	Improv. (dB)	@1MHz	18-24**	NA	NA	28	10	30
		@5MHz	24-30**	NA	NA	19	NA	30
Saw-tooth	Spur (dBc)	@1MHz	<-50	NA	-50	NA	NA	NA
		@5MHz	<-58	NA	-51	NA	NA	NA
	Improv. (dB)	@1MHz	11.3**	NA	15	NA	NA	NA
		@5MHz	22-27**	NA	12	NA	NA	NA
Osc. Power Cons. (mW)			0.8-1.3	6.6	18.9†	6.4†	2.95†	2.73†
Power Cons. K_{push} Reduction Tech. (mW)			0.2	NA	2.4	NA	NA	0.45
Area of K_{push} Reduction Tech. (mm^2)			0.012	NA	0.35‡	NA	NA	0.004
Total Area (mm^2)			0.23	0.15	0.63†	0.013‡	0.0216‡	0.047†

*Estimated from out-of-band phase noise of PLL **Compared with the case S_I=0 (Gain=1) where the supply pushing of the oscillator is already suppressed
#Calculated value from the spur level † Power/area of the ADPLL ‡ Estimate from the chip micrograph
***Ripple frequency lower than the PLL bandwidth, supply pushing is calculated assuming 20dBc/decade suppression from the loop

Table 4.2: Comparison with LDO Designs

		This work	JSSC'10 [49]	CICC'11 [47]	JSSC'14 [50]	VLSI'17 [51]	JSSC'18 [48]
Tech. (nm)		40	130	180	180	40	65
V_{in} (LDO)/ V_{DD} (osc.) (V)		1.0	>1.15	1.8	1.8	1.1	1.2
V_{out} (LDO) (V)		NA	1	1.5	1.6	1	1
$V_{drop\text{-}out}$ (LDO)/ V_{ds} of M_0 (osc.) (V)		0.25	>0.15	0.3	0.2	0.1	0.2
PSR (dB)	**@1MHz**	<-55.9	-80	-50	-65	-60	-52
	@10MHz	<-42.5	-60	-22	-42	-35	-37
Total Capacitance		8.6pF (on-chip)	4μF (off-chip)	125pF (on-chip)	128pF (on-chip)	104pF (on-chip)	260pF (on-chip)
Additional Current Consumption (mA)		0.2 +0.021#	0.05	0.3	0.08	0.275	0.1535
Additional Power Consumption (mW)		0.2 +0.021#	0.0575	0.54	0.144	0.3025	0.1842
Noise (LDO/RRB) @100kHz (nV/$\sqrt{Hz}$)		8**	NA	NA	270	274	NA
Total Area (mm^2)		0.012	0.049	0.041	0.14*	0.008*	0.087

*100pF on-chip load capacitance not included **Value obtained from post-layout simulation
#0.2mA(mW) from RRB always exists during normal operation; 0.021mA(mW) is the average power consumption of the calibration loop, when conservatively assuming a calibration is done for every BLE packet (~400μs)

4.5 Conclusion

This chapter presented a method to significantly reduce supply pushing in current-mode LC oscillators while consuming no extra voltage headroom. The proposed RRB generates an amplified supply ripple replica at the gate

terminal of the oscillator's tail current source, in order to stabilize the tail current and oscillation amplitude under supply variations. The oscillation frequency is stabilized in turn, leading to $< 1\,\text{MHz/V}$ supply pushing for supply ripples up to 12 MHz. To suppress the phase noise degradation due to the extra circuitry, implicit common-mode resonance is used in the resonant tank. A calibration loop with a simple and effective algorithm is also integrated on-chip, which effectively finds the optimum gain for the ripple replication block. The operation of the loop is based on detecting and minimizing the variation of the oscillation amplitude. Hence it is also effective when the ripple is simultaneously coupled through the supply and other parasitic paths.

4.6 Appendix: System Design of a DC-DC Converter Directly Powering the Oscillator

In this appendix section, the design and measurement of the DC-DC converter directly powering up the LC oscillator without degrading its spectral purity will be demonstrated[2]. Fig. 4.19 shows the block diagram of the proposed system.

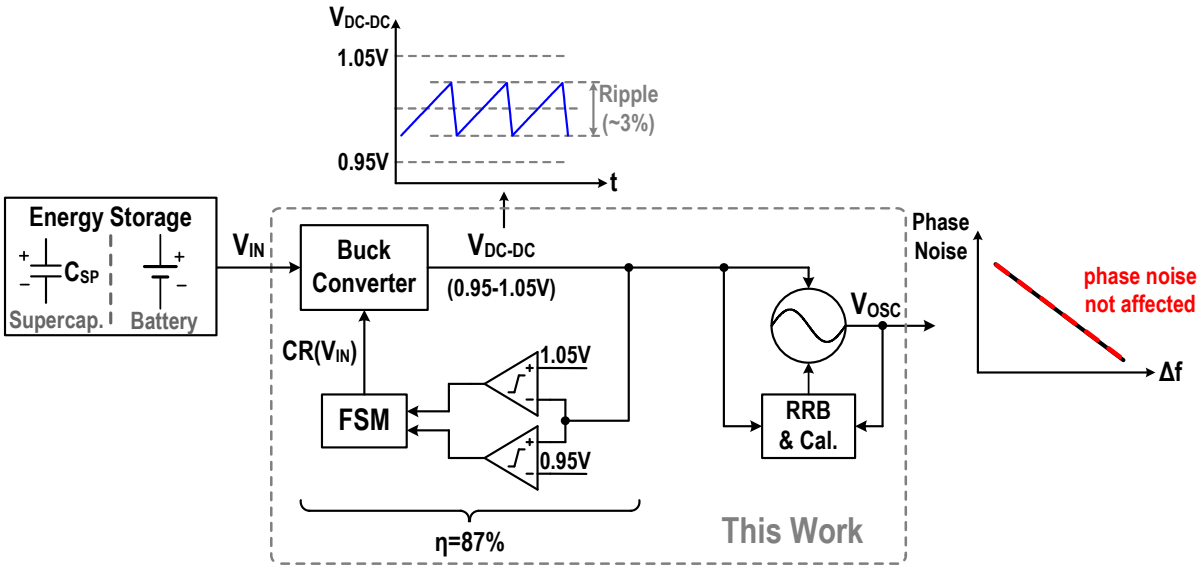
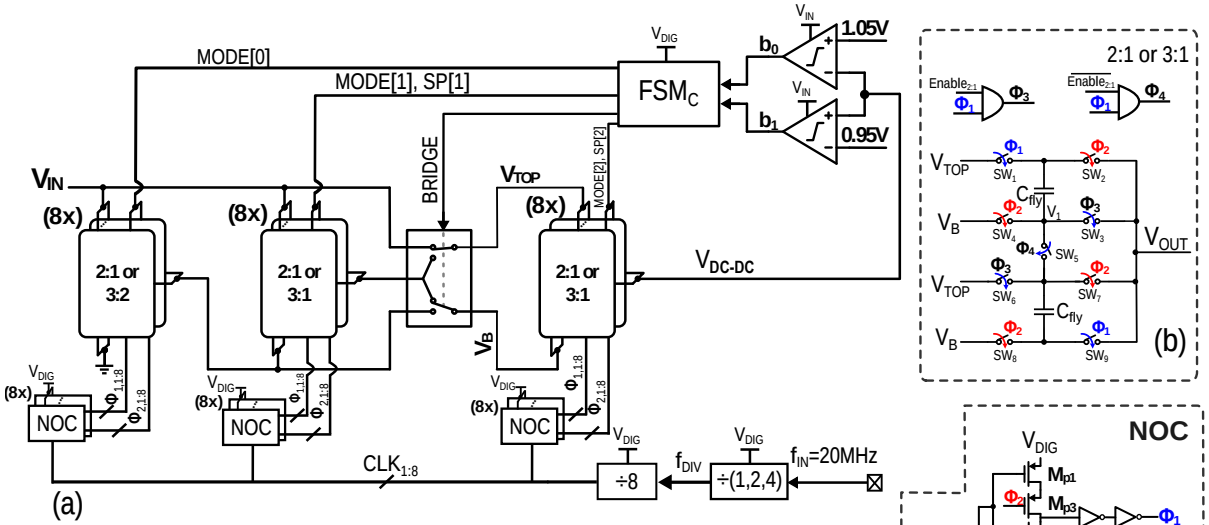


Figure 4.19: Block diagram of the proposed system.

[2]Material of this section has been published in the IEEE Transactions on Circuits and Systems I (TCAS-I) [56]. The converter is designed by Alessandro Urso, a PhD student at TU Delft. The author is responsible for the oscillator design and measurements.



	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
f_{sw}	f_{IN} /4	f_{IN}	f_{IN}	f_{IN}/2	f_{IN}/2	f_{IN}	f_{IN}	f_{IN}/4	f_{IN}	f_{IN}/2	f_{IN}/2	f_{IN}/2
CR	1/2	5/9	7/12	5/8	2/3	19/27	13/18	3/4	7/9	5/6	7/8	11/12
MODE	000	011	010	000	011	111	101	000	111	010	000	100
SP-BRIDGE	11-0	00-1	00-1	00-1	01-0	00-1	00-1	01-0	01-0	00-0	00-0	00-0
K_{SSL}	1/4	36/81	69/144	29/64	1/3	308/729	131/324	5/16	26/81	1/3	21/64	47/144
K_{FSL}	2	268/81	34/9	29/8	22/9	2156/729	463/162	5/2	182/81	47/18	21/8	187/72

Figure 4.20: (a) Detailed block diagram of the three-stage recursive switched capacitor (RSC) DC-DC converter with a table showing the control signals for all the converter states; (b) detailed representation of a 2:1 or 3:1 stage and (c) the non-overlapping clock (NOC) generator.

4.6.1 DC-DC Converter

The recursive switched-capacitor (RSC) [89] topology is adopted in the designed DC-DC converter. In order to avoid cascading many RSC stages as in [89], a 3-stage RSC topology with two conversion ratio (CR) options per stage is proposed. As shown in Fig. 4.20, each stage in the proposed topology could operate in two CR modes (2:1, 3:2 or 3:1), while only one set of bridge switches is placed between the last two stages, allowing the connection of the output of the second stage to either the top or bottom voltage of the third stage. Assisted by the equivalent model of the SC converter [see Fig. 4.21 (a)], the required CR range is determined by

$$\begin{cases} \mathrm{CR}_{\min} = \dfrac{V_{\mathrm{DC-DC,min}} + R_{\mathrm{S}} I_{\mathrm{L,min}}}{V_{\mathrm{IN,max}}} \\ \mathrm{CR}_{\max} = \dfrac{V_{\mathrm{DC-DC,max}} + R_{\mathrm{S}} I_{\mathrm{L,max}}}{V_{\mathrm{IN,min}}} \end{cases} \tag{4.9}$$

where $V_{\mathrm{IN,max(min)}}$ and $I_{\mathrm{L,max(min)}}$ are the maximum (minimum) input voltage and load current considered in the converter design. $V_{\mathrm{DC-DC,max(min)}}$ repre-

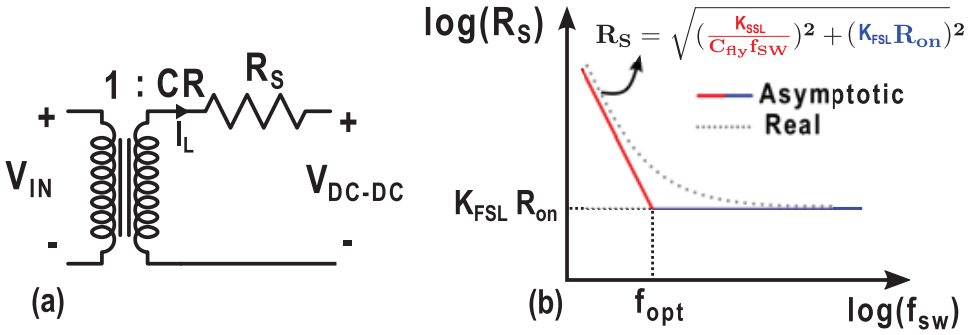


Figure 4.21: (a) Equivalent model of an SC DC-DC converter; and (b) its equivalent output resistance versus switching frequency.

sents the maximum (minimum) voltage allowed at the converter output, and equals 1.05 V (0.95 V) for a ±5% accuracy around the 1 V nominal output level. Given that $R_S = 50\,\Omega$, $1.3\,\text{V} < V_{IN} < 2.2\,\text{V}$ and $0.5\,\text{mA} < I_L < 2\,\text{mA}$, (4.9) shows that CR varies from 0.5 to 0.9. Therefore, the first stage in the proposed topology does not need the 3:1 configuration and its output is always connected to the bottom voltage of the second stage, allowing for a higher CR. The resolution of the CR should be fine enough to guarantee that the difference between the converter output corresponding to two consecutive CRs is less than V_{DC-DC} accuracy. Hence, assuming a constant R_S, the required CR resolution can be estimated by

$$\text{CR}_{\text{res}} = (\text{CR}_{i+1} - \text{CR}_i) < \frac{0.1\text{V}_{\text{OUT}}}{\text{V}_{\text{IN,max}}} = 0.0455. \tag{4.10}$$

In the proposed design, 12 CRs are implemented to realize this resolution.

The equivalent output impedance of the converter, R_S, can be modeled by the well-known equation below [90]

$$R_S = \sqrt{R_{SSL}^2 + R_{FSL}^2} = \sqrt{\left(\frac{K_{SSL}}{C_{fly} f_{SW}}\right)^2 + \left(K_{FSL} R_{on}\right)^2} \tag{4.11}$$

where R_{SSL} and R_{FSL} are the resistances in the slow and fast switching limit (SSL, and FSL), respectively. K_{SSL} and K_{FSL} are topology-dependent coefficients valid respectively in the SSL and FSL regions [90]. Fig. 4.21 (b) shows a sketch of (4.11) versus the switching frequency (f_{SW}). In the SSL region, the charge-sharing mechanism dominates the losses, whereas, in the FSL region, the finite on-resistance of the switches (R_{on}) is the main source of inefficiency. Taking both the conduction losses and switching

losses into consideration, the converter loss could be modeled as

$$P_{\mathrm{LOSS}} = nC_{\mathrm{g}}V_{\mathrm{sw}}^2 f_{\mathrm{SW}} + R_{\mathrm{S}}I_{\mathrm{L}}^2 \tag{4.12}$$

where n is the number of switches operating at f_{SW} with a clock voltage swing of V_{sw}, and C_{g} is the equivalent gate capacitance of each switch. Therefore, to maximize the power efficiency, it is required that the converter operates at the boundary between the fast and slow switching limits. In the proposed RSC converter, the stages are rearranged in a series/parallel configuration to guarantee $V_{\mathrm{DC-DC}} = 1\,V \pm 5\%$ for $V_{\mathrm{IN}} \in \{1.3-2.2\}\,V$, resulting in a varying R_{SSL} and R_{FSL}. Therefore, with a fixed f_{SW}, R_{S} of the proposed converter greatly varies with the particular configuration used, dramatically affecting the converter efficiency. The large R_{S} variation can also violate the resolution requirement imposed by (4.10). In the worst case, even the monotonicity of $V_{\mathrm{DC-DC}}$ as a function of CR could be violated due to this variation. To overcome this problem, f_{SW} in the configuration with a higher R_{S} can be modulated by a factor of 2× or 4× in order to bring f_{SW} close to the optimal value again, resulting in a fairly constant R_{S} which maximizes the power efficiency of the converter and guarantees the resolution and monotonicity conditions being always met. In the proposed design, an external clock with f_{IN} =20 MHz provids the highest possible f_{SW}, while a flip-flop-based frequency divider implemented internally performs the frequency division (of 1, 2 or 4) to generate f_{DIV} with the desired f_{SW} (see Fig. 4.20). Each stage of the converter is further divided into eight smaller interleaved units. This allows to avoid the need for an output capacitor and to reduce the switching losses of the converter [91]. The corresponding eight interleaved clock phases ($\mathrm{CLK}_{1:8}$) are generated by further dividing f_{DIV} [92]. A non-overlapping clock (NOC) circuit is embedded in each unit to generate the two non-overlapped phases (Φ_1 and Φ_2) from $\mathrm{CLK}_{1:8}$.

During the operation, $V_{\mathrm{DC-DC}}$ is compared with two reference levels, 0.95 V and 1.05 V, at a rate of 1 MHz. Two bits ($\mathrm{b}_{0,1}$) are generated to indicate whether $V_{\mathrm{DC-DC}}$ is within the range, higher or lower. The converter's FSM ($\mathrm{FSM}_{\mathrm{C}}$) then decides to keep the same state or move to the next higher/lower one. Each state has a unique set of control signals (MODE, SP, BRIDGE), which determines f_{SW}, the series or parallel

connection of stages, and the CR of each stage. The table in Fig. 4.20 (b) reports all the converter's states and their control signals.

4.6.2 LC Oscillator with RRB

The structure of the implemented LC oscillator is similar to that shown in Fig. 4.5. The calibration loop (see Fig. 4.6) is also integrated on-chip to set the optimal control code for RRB automatically. Note that the calibration is only performed in one of the converter states and used during the entire operation.

As discussed in Section 4.3.1.1, due to the finite bandwidth of RRB, a phase shift between the supply ripple and its replica at high ripple frequencies would result in residue variations of I_0, degrading the spur levels. Hence, the capacitive load at V_{b0} and the RRB current are optimized based on the highest f_{SW} of the converter (20 MHz). At lower f_{SW}, the oscillator inherently suffers from a lower spur suppression due to a higher tank impedance, requiring tighter I_0 variations. Thus, the RRB gain resolution is designed for the lowest f_{SW} (5 MHz) to guarantee a low enough spur over the f_{SW} range. The RRB is effective as long as M_0 stays in the saturation region. Thanks to the CR adjustment of the converter, the DC level of the oscillator supply only varies by ± 50 mV, which is low enough to keep M_0 safely in saturation. Since the RRB is fully integrated into the oscillator biasing network, only the noise of its extra variable g_m stage degrades the oscillator PN by a negligible amount (i.e., $\sim$0.06 dB). Moreover, the extra current consumed by the RRB, mainly contributed by the variable g_m stage also, is only 20 μA, which leads to a current efficiency degradation of 98%.[3]

4.6.3 Experimental Results

The proposed DC-DC converter and the oscillator are fabricated in the same standard 40-nm CMOS process. The symmetrical transformer in the LC oscillator is designed with the ultra thick top metal layer for better Q.

[3]The oscillator is considered to be biased with a current mirror here for the comparison with other system designs (see Table 4.3). In practice, the tail current source of the oscillator may be tuned through an amplitude tracking loop to guarantee the optimum operation point across PVT variations. In this case, more stringent PSR and noise requirements may be placed on LDOs, further worsening their power efficiency (please refer to Chapter 3).

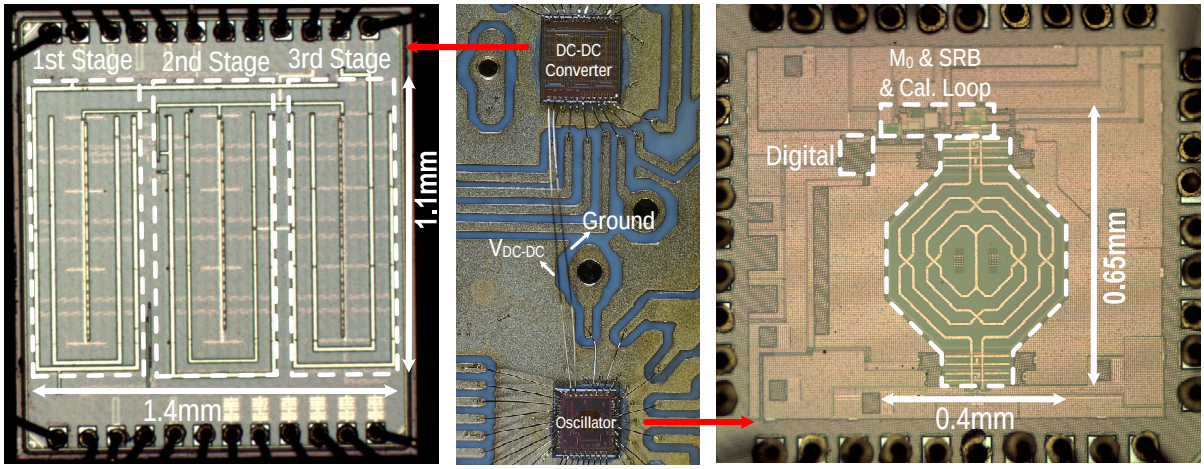


Figure 4.22: Die micrographs of the DC-DC converter (left), the oscillator (right), and photo highlighting their direct connection (middle).

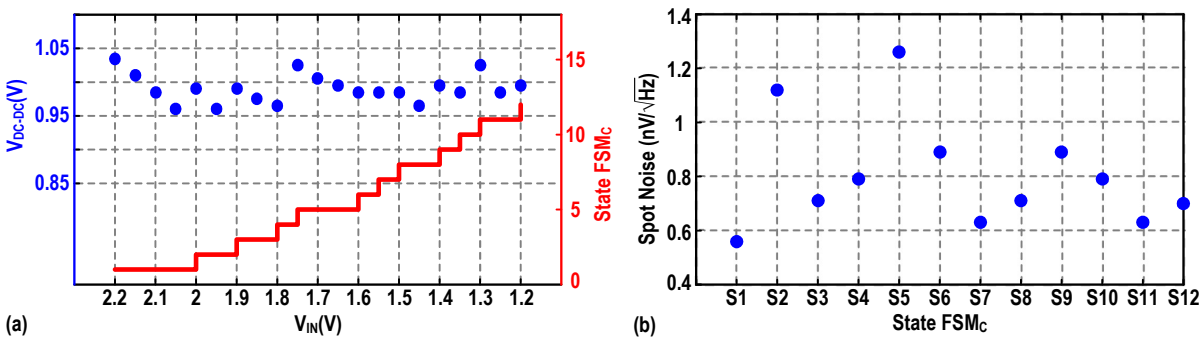


Figure 4.23: (a) Measured output voltage of the DC-DC converter versus V_{IN} for $I_{\mathrm{L}} = 1\,\mathrm{mA}$; and (b) measured spot noise of the converter across different $\mathrm{FSM_C}$ state.

Their chip micrographs, as well as a photo highlighting the direct connection of the converter's output to the oscillator supply rail, are shown in Fig. 4.22. They occupy an active area of $1.54\,\mathrm{mm}^2$ and $0.23\,\mathrm{mm}^2$, respectively. The total on-chip capacitance of the DC-DC converter $C_{\mathrm{fly}} = 2.7\,\mathrm{nF}$ is equally divided among the three stages.

Fig. 4.23 (a) shows the line regulation of the converter for $I_{\mathrm{L}} = 1\,\mathrm{mA}$ along with the state of the $\mathrm{FSM_C}$. The CR and f_{SW} change accordingly to keep $V_{\mathrm{DC-DC}}$ within the desired range. The output noise of the converter is also measured, and the result is shown in Fig. 4.23 (b) over different converter states. In this measurement, V_{IN} is tuned so that $V_{\mathrm{DC-DC}}$ is $\sim$1V when the converter is operating in the corresponding state. The noise is always $< 1.3\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ which is well below the supply noise requirement of the oscillator.

Fig. 4.24 (a) shows the phase noise of the oscillator when powered from

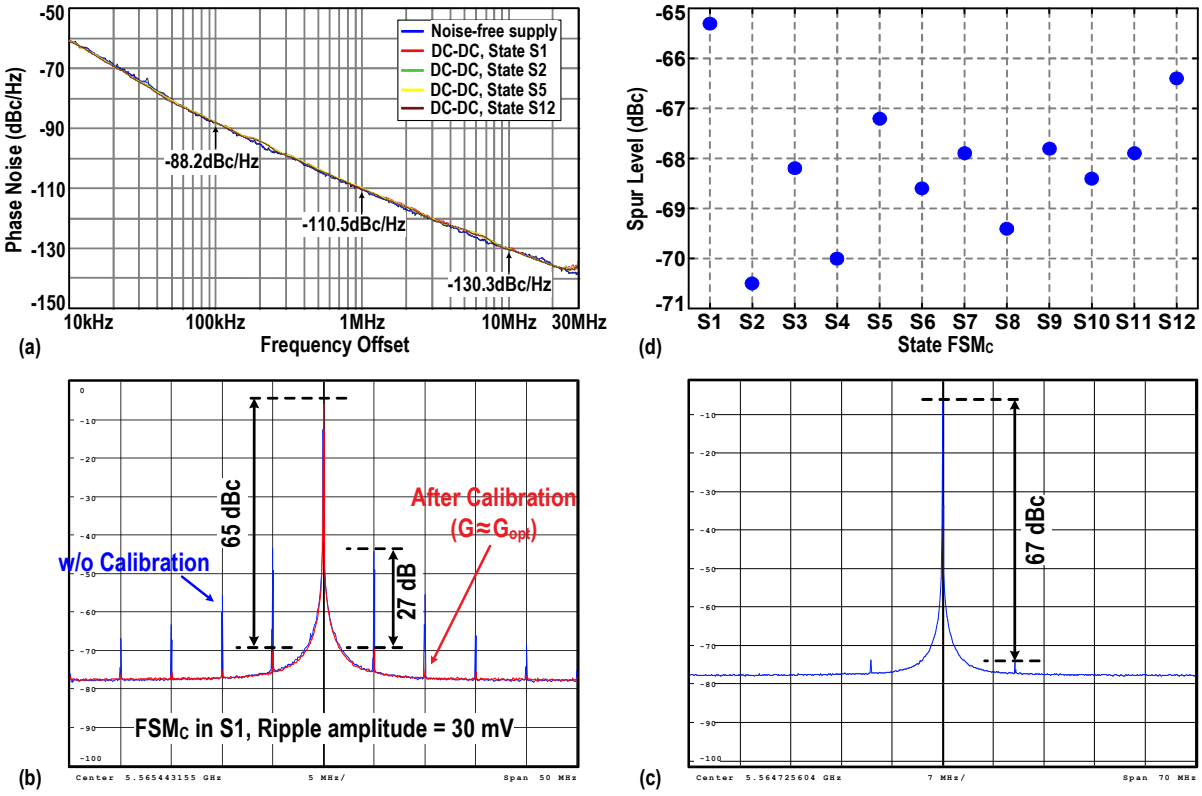


Figure 4.24: (a) Measured oscillator PN performance at f=5.5 GHz and (b) its spectrum before and after calibration of the RRB with FSM_C in State S1 and (c) State S5; (d) spur level across different converter states when the oscillator is calibrated only at State S1.

a 'noise-free' supply and from the DC-DC converter in different FSM_C states for the oscillation frequency of 5.5 GHz. The inherent PN of the oscillator is not degraded, proving that the supply does not limit the oscillator performance. Fig. 4.24 (b) shows the spectrum of the oscillator before and after calibration when powered from the DC-DC converter with a ripple amplitude of $\sim$30 mV_{pp}. The spur level is reduced by 30 dB and reaches -65 dBc after the calibration, which is 15 dB lower than the IoT requirements (i.e., <-50 dBc). A similar measurement is also performed while the oscillator is powered by the DC-DC converter in state S5, and the spectrum is depicted in Fig. 4.24 (c). Fig. 4.24 (d) shows the spurious level of the oscillator across all the states of the FSM_C when the RRB of the oscillator is only calibrated in State S1. The spur level always stays below -65 dBc.

Table 4.3 summarizes the performance of the whole system and compares it with prior art. This work is more suitable for a full system integration by avoiding external components and demonstrates the highest system peak

Table 4.3: Comparison with Systems Powering Up LC Oscillators

		This work	JSSC'15 [43]	TPE'16 [93]	TCAS-I'08 [94]	ESSCIRC'14 [74]
System Architecture		DC-DC + OSC	DC-DC + LDO + OSC**	DC-DC + LDO***	LDO + OSC	LDO + OSC
Tech. (nm)		40	55	65	250	65
V_{IN} (V)		1.3-2.2	1.6-3.3#	2.4-2.6	X	X
$V_{IN,LDO}$ (V)		X	1.4	1.05	2.0-2.5	0.6
$V_{OUT,LDO}$ (V)		1.0	1.2	1.0	1.5-2	0.4
$V_{LDO,drop}$ (mV)		0	200	50	500	200
η_{DC-DC} (%)		87	92	80.3	X	X
η_{LDO} (%)		X	<85.7	<94.9	<79	<60
η_{RRB} (%)		98	X	X	X	X
η_{Total} (%)		85	<79	<76.2	<79	<60
#ext. comp.		0	2	0	1	0
Osc. supply noise ($nV/\sqrt{Hz}$)		1.26(S5) @10MHz	NA	14.1# @20MHz	32 @100kHz	2.0†† @10MHz
C_{LDO} (F)		X	NA	41p	50n	390p
$I_{Quiescent}$ (μA)		20	NA	10 (V_{IN})	120	500 (1.2V)
PSR (dB)	**@5MHz**	27.0*	>20	15	35	31†
	@10MHz	29.6*	>20	15	NA	26†

*PSR of the fractional part of RRB **Oscillator is part of the whole transceiver ***Can be used to power up an oscillator
#Estimated from the measurement result †Simulated value ††Calculated from phase noise with K_{push}=250MHz/V
X=not needed in the system

power efficiency thanks to the removal of the LDO voltage headroom. The equivalent PSR of our approach in the table only accounts for the extra improvement contributed by the fractional part of the RRB. Compared to the systems with LDOs, our fully passive SC converter exhibits >10× lower supply noise and our RRB shows comparable or higher power supply rejection improvement, preserving the oscillator's spectral purity for IoT applications.

Chapter

5

Supply Insensitive Fractional-N Digitally Intensive PLL

In this chapter, we present a 4.5–5.1 GHz fractional-N digitally intensive PLL (DPLL) capable of maintaining its performance in face of a large supply ripple, thus enabling a direct connection to a switched-mode DC-DC converter[1]. Based on the method proposed in Chapter 4, supply pushing of its LC oscillator is suppressed by properly replicating the supply ripple onto the gate of its tail current transistor, while the optimum replication gain is determined by a modified on-chip calibration loop tolerant of supply variations. A proposed configuration of cascading a supply-insensitive slope generator with an output of a current DAC linearly converts the phase error timing into a corresponding voltage, which is then quantized by a SAR ADC to generate a digital phase error. We also introduce a low-power ripple pattern estimation and cancellation algorithm to remove the phase error component due to the supply-induced delay variations of loop components. Implemented in 40-nm CMOS, the DPLL prototype achieves the performance of 428 fs rms jitter, <-55 dBc fractional spur, and

[1]Material of this chapter has been published in the IEEE Journal of Solid-State Circuits [95].

$<-54\,\mathrm{dBc}$ maximum spur, while consuming $3.25\,\mathrm{mW}$ and being subjugated to a sinusoidal or sawtooth supply ripple of $50\,\mathrm{mV_{pp}}$ at $50\,\mathrm{MHz}$ reference divided by 3, 6 or 12.

5.1 Introduction

Since the LDO used to suppress the output ripples of the DC-DC converter degrades the system power efficiency and/or require additional off-chip components, it deems beneficial for the PLL to be powered directly from the converter, thus entirely avoiding the use of LDOs. As already discussed in Chapter 2, the implementation of such a PLL faces three main challenges: the supply pushing of the oscillator, the output delay variation of loop components and the intermodulation between f_{rip} and f_{frac}.

To suppress the supply pushing of the LC oscillator, Chapter 4 proposed a feed-forward ripple replication and cancellation technique. Although the corresponding spur level could be reduced to below $\sim -50\,\mathrm{dBc}$ under the $50\,\mathrm{mV_{pp}}$ 0.5–20 MHz supply ripple with minimal power penalty, its on-chip calibration loop is still sensitive to supply variations. Therefore, similar as in [67], a clean supply is still required to power the calibration loop.

For the output delay and transfer function variations of PLL loop components under supply ripple, Section 2.2 shows that the suppression provided by the loop may be insufficient for a reasonable f_{rip}. Thus, additional techniques still appear to be needed to reduce the corresponding spurs. Moreover, in the scarcely available literature on PLLs with reduced supply sensitivity, mainly the integer-N operation is considered [44, 96], while the intermodulation problem between f_{rip} and f_{frac} of fractional-N operation, which is generally used in real applications, is seldom discussed.[2]

As already mentioned at the beginning of Chapter 2, the analysis in that chapter is valid for both analog and digital PLL implementations. Compared to the case of DTC/TDC in a digital PLL, a charge pump in the conventional analog PLL may offer a lower sensitivity to supply. However, the charge pump could become overly sensitive by a mismatch between its 'up' and 'down' current branches [46]. Meanwhile, the divider, phase/frequency detector (PFD), and buffers used as an interface between different blocks are still affected by the supply ripple, thus necessitating calibrations to remove their effects. Since the phase error information in the analog [22–25] or hybrid [99, 100] PLLs is processed in the voltage domain, the implementation of the calibration loops would be more complex than

[2]Note that the intermodulation effect analyzed in [97, 98] is between the reference frequency and the oscillation frequency, generating fractional spurs, which is not similar to the effect mentioned here.

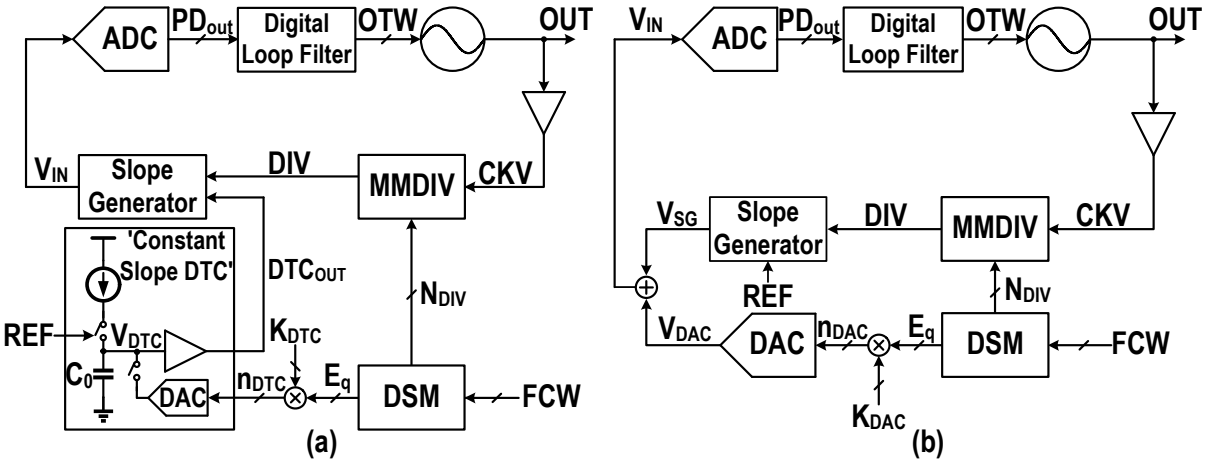


Figure 5.1: ADC-based fractional-N DPLL structure using (a) a constant-slope DTC or (b) a DAC.

in their digital counterparts and further deteriorated by the non-idealities of analog circuits in sub-micron technologies. In contrast, a highly digitally intensive PLL (DPLL) features the natural ability to exploit various digital calibration techniques to tackle the aforementioned issues with relative ease. Consequently, a DPLL is favored when architecting for the direct powering by the switch-mode DC-DC converter. In this chapter, we propose a digital-to-analog converter (DAC)-assisted fractional-N DPLL architecture to enable direct operation under a large $50\,\mathrm{mV_{pp}}$ supply ripple. The reduced supply sensitivity of the proposed voltage-domain PD suppresses the intermodulated terms, while the effect of the supply induced delay variation is cancelled through digital calibration. The supply pushing of the LC oscillator is also reduced through the feedforward cancellation technique with an improved calibration loop.

The chapter is organized as follows. Section 5.2 derives the proposed loop structure. Detailed circuit implementations of different DPLL blocks are discussed in Section 5.3, while measurement results are provided in Section 5.4.

5.2 Proposed DPLL Architecture

In contrast to the conventional time-domain realizations, implementation of the phase detection in the voltage domain [see Fig. 5.1 (a) as an example] has been gaining popularity in recent years [41, 101–106]. Assisted by a steep slope of the sampled waveform, the analog-to-digital

converter (ADC)-based PD could achieve a fine resolution at low power consumption [41,101–103]. Due to its power efficiency and simple structure, a successive-approximation register (SAR)-ADC is beneficially employed in the DPLL design. By operating in the voltage domain with only one comparator and a capacitive DAC (CDAC), it also provides better immunity to supply variations. However, for fractional-N applications, a DTC is still used to accommodate the limited linear range of the slope generator (SG) and to reduce the dynamic range of the ADC [41, 102]. In order to further exploit the operation in the voltage domain with improved supply immunity, a *constant-slope* DTC should be considered here [107–109]. As shown in Fig. 5.1 (a), the constant-slope DTC charges a load capacitor, C_0, with a constant current at the corresponding edge of the input signal, and flips the following buffer when the charged voltage level reaches its threshold. The variable output delay is achieved by presetting the starting voltage on C_0 to different values using a DAC. Given that this DAC can be implemented with good supply immunity, the DPLL structure of Fig. 5.1 (a) would be able to better tolerate supply ripples.

To detect the phase error, the DPLL structure in Fig. 5.1 (a) traverses between the time and voltage domains several times. First, the constant-slope DTC converts the desired delay into the starting voltage on C_0. Second, the following buffers convert it back to the time domain. Third, the slope generator converts the time difference between the DTC output, $\mathrm{DTC_{out}}$, and the feedback signal, DIV, into the ADC input voltage, V_{IN}. In fact, this process could be simplified, as shown in Fig. 5.1 (b). In this structure, the time difference between the reference signal, REF, and the feedback signal, DIV, is directly converted into a corresponding voltage, V_{SG}, through the slope generator, while a DAC is used to generate a compensation voltage, V_{DAC}, based on the MMDIV quantization error. By summing V_{SG} and V_{DAC}, the resulting V_{IN} will be only proportional to the PN component and vary little when the PLL is locked. The structure in Fig. 5.1 (b) now operates entirely in the voltage domain, reducing its supply sensitivity. Essentially, it converts the time to voltage only once, simplifying the system structure and circuit implementation. A similar voltage-domain PD is also used in [110] to achieve an improved power-jitter trade-off. However, to operate under the supply ripple, the loop in [110]

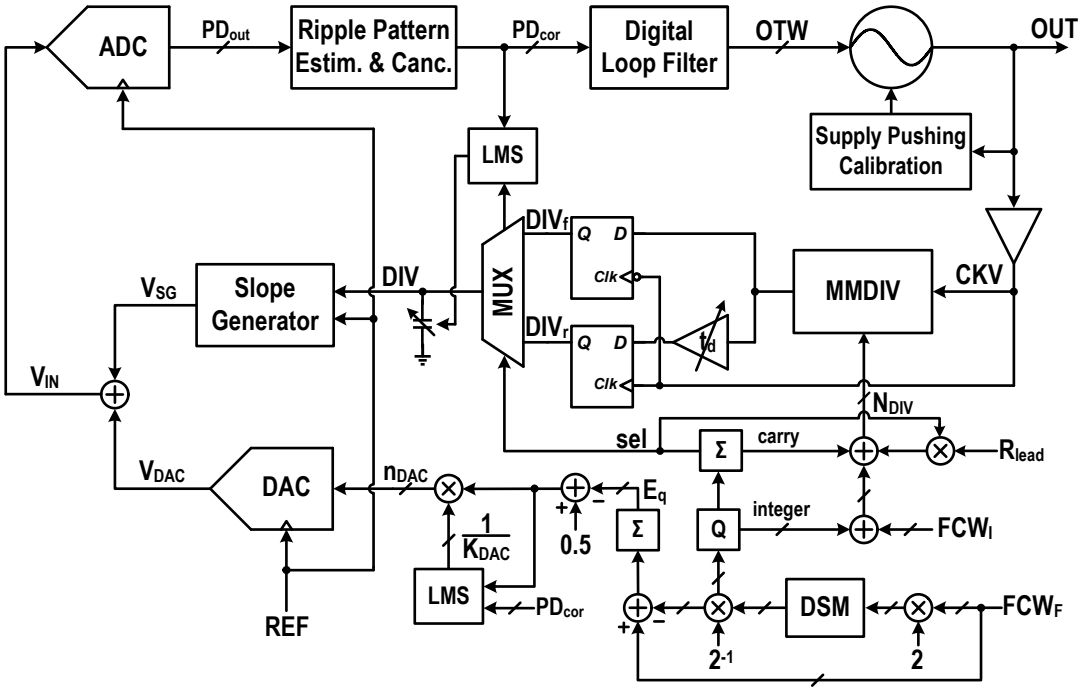


Figure 5.2: Block diagram of the proposed fractional-N DPLL.

and Fig. 5.1 (b) still needs to be further modified.

The complete loop structure is shown in Fig. 5.2. The ripple pattern estimation and cancellation block is inserted after the ADC to remove the phase error pattern at f_{rip} induced by the delay variations of loop components due to the supply ripple. To further suppress the spur due to the intermodulation effect, a second-order $\Delta\Sigma$ modulator is employed, while the MMDIV output is resampled by both edges of the oscillation signal, CKV, to limit the input range of the slope generator for better linearity and noise performance. The mismatch between the two resampling paths is compensated by varying the capacitive load of the multiplexer (MUX) through an LMS algorithm. Finally, to suppress the supply pushing of the LC oscillator, the feed-forward cancellation technique proposed in Chapter 4 is adopted, while its calibration loop has been modified to be able to tolerate the supply ripples.

5.3 Circuit Implementation

In this section, the detailed circuit implementation of key blocks in the proposed fractional-N DPLL is discussed.

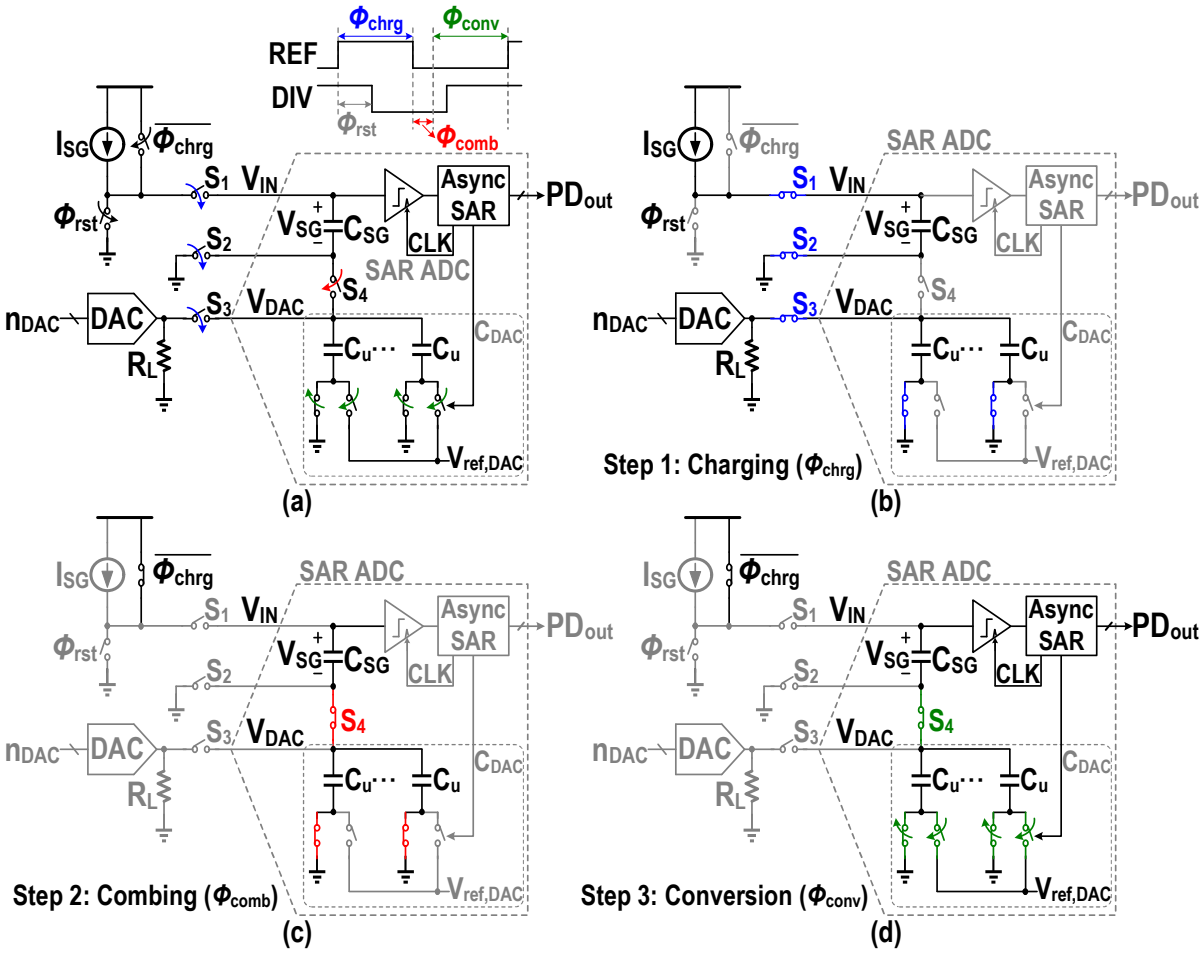


Figure 5.3: (a) Simplified block diagram, and (b)–(d) operational principle of PD.

5.3.1 Phase Detector

5.3.1.1 Operating Principle

A simplified block diagram of the phase detection circuitry is shown in Fig. 5.3 (a). It chiefly consists of a slope generator (SG), a current steering DAC, a combiner switch (S_4), and an SAR ADC converting the phase error to a digital bitstream. The desired phase error is digitized through three steps: charging (ϕ_{chrg}), combining (ϕ_{comb}), and conversion (ϕ_{conv}), as shown in Fig. 5.3 (b)–(d). During the first step ϕ_{chrg}, the current source in the slope generator, I_{SG}, charges the load capacitor, C_{SG}, between the falling edges of REF and DIV [111, 112], converting its input time difference into a corresponding voltage,

$$V_{\text{SG}} = (t_{\text{os}} + E_{\text{q}} \times T_{\text{CKV}} + t_{\text{n}}) \times (I_{\text{SG}}/C_{\text{SG}}), \tag{5.1}$$

where $E_q \times T_{CKV}$ is the deterministic time error due to the fractional operation, t_n is the time difference due to the random noise and supply-induced delay variations in the loop, and t_{os} is the time offset between the falling edges of REF and DIV in the absence of any deterministic and random noise. During the same phase, to compensate for the deterministic part in V_{SG}, the DAC output voltage, V_{DAC}, is also impressed on C_{DAC}, while the bottom plate of its unit capacitors (C_u) is connected to the ground. Note that the same unit capacitors will be used as the charge-scaling DAC by the ADC in the conversion phase. The DAC control code, n_{DAC}, is determined by the accumulated quantization error of the $\Delta\Sigma$ modulator driving the divider (E_q in Fig. 5.2)

$$n_{DAC} = (E_{q,max} - E_q)/\widehat{K}_{DAC}, \tag{5.2}$$

where $E_{q,max}$ is the maximum value of E_q (with a second-order $\Delta\Sigma$ modulator and the resampling technique in Section 5.3.2, $E_{q,max} = 0.5$). $\widehat{K}_{DAC}$ is the estimation of DAC gain, $K_{DAC} = (V_{res} \cdot C_{SG})/(T_{CKV} \cdot I_{SG})$, where V_{res} is the DAC voltage resolution. When it is accurately estimated, the sampled V_{DAC} can be calculated by

$$\begin{aligned} V_{DAC} &= V_{DAC,os} + n_{DAC} \times V_{res} \\ &= V_{DAC,os} + (E_{q,max} - E_q) \times T_{CKV} \times (I_{SG}/C_{SG}) \end{aligned} \tag{5.3}$$

where $V_{DAC,os}$ is an offset voltage independent of n_{DAC}. In the next step ϕ_{comb}, V_{SG} and V_{DAC} are combined by connecting the top plate of C_{DAC} to the bottom plate of C_{SG} through S_4. By summing (5.1) and (5.3), the generated ADC input voltage becomes

$$\begin{aligned} V_{IN} =& t_n \times (I_{SG}/C_{SG}) + \\ & [V_{DAC,os} + (I_{SG}/C_{SG}) \times (t_{os} + E_{q,max} \times T_{CKV})]. \end{aligned} \tag{5.4}$$

The second term in (5.4) is time-invariant related to t_{os}. Due to the feedback operation of the loop, t_{os} will be adjusted automatically such that the corresponding term settles to the ADC's reference level, V_{ref}. Therefore, the ADC only needs to convert the input variations related to t_n. Meanwhile, the charge-recycling switching technique is also employed in the

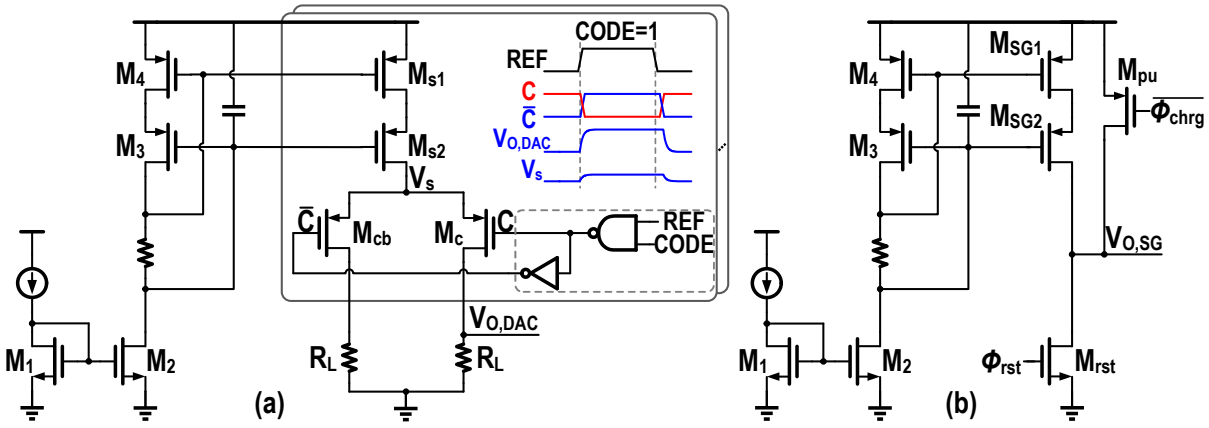


Figure 5.4: Schematic of (a) the current DAC and (b) the slope generator. Note the shift on V_s due to the drain of M_c being at a different potential than that of M_{cb}.

ϕ_{conv} step to improve the ADC power efficiency [113]. Note that the system is designed so that $V_{DAC,os}$ and the C_{SG} charge due to t_{os} equally provide the required input DC offset. Hence, the maximum voltage on the C_{SG} and C_{DAC} capacitors is limited to $\sim V_{ref}/2$, providing enough voltage headroom for the PMOS current sources to operate linearly. In contrast, the DAC and slope generator in [110] sequentially charge the same capacitor to $\sim V_{ref}$. This reduces the voltage headroom of the slope generator's current source, substantially degrading its linearity in a deep sub-micron technology with reduced supply.

5.3.1.2 Circuit Design

Fig. 5.4 (a) shows the DAC schematic, consisting of 290 unary cascode current sources to satisfy the range and linearity requirements. As the DAC is biased through the current mirror, the DAC output variation due to the supply ripple can be estimated by

$$V_{O,DAC} \approx \frac{R_L}{R_L + r_{o,s1} + r_{o,s2} + g_{m,s2} r_{o,s1} r_{o,s2}} \cdot A_{rip} \tag{5.5}$$

where $g_{m,s1(2)}$ and $r_{o,s1(2)}$ are the small-signal transconductance and output resistance of $M_{s1(2)}$, respectively. Eq. (5.5) shows that the high output impedance of the cascode structure is also beneficial in suppressing the supply-induced variation at the DAC output, and consequently, $M_{s1,2}$ are implemented as long channel devices. During the output current transition from one branch to the other, the voltage across the current

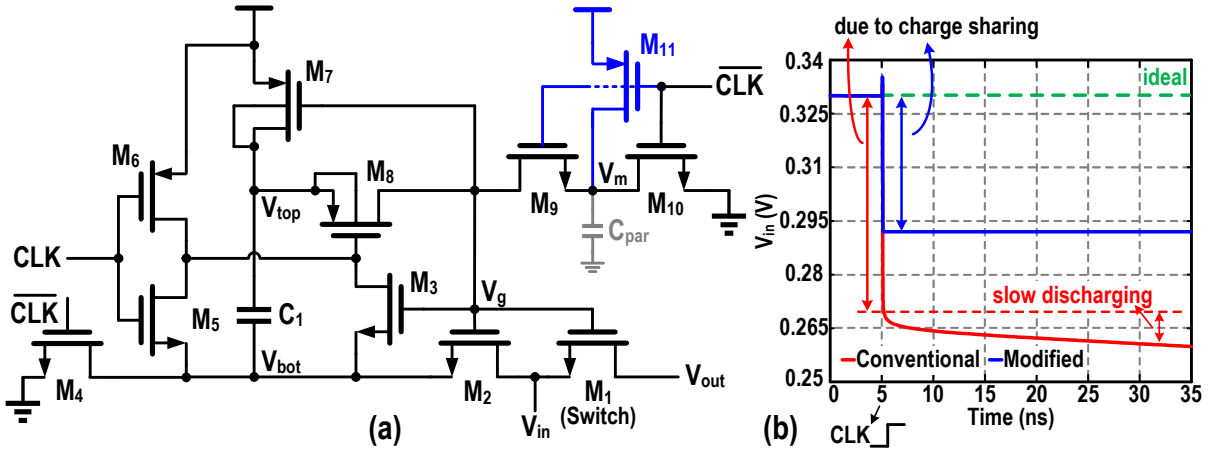


Figure 5.5: (a) Schematic of the bootstrap switch, and (b) simulated performance of S_4 during tracking phase.

source, as observed at V_s, is affected. This dynamic disturbance couples to the bias voltage of the current mirror through the parasitic capacitance of $M_{s1,2}$, degrading the DAC settling speed and linearity. To alleviate this issue, dynamic element matching is employed to relax the matching requirements [114] and to reduce the M_{s1} size and parasitic capacitance. Moreover, to remove the dependence of the output transition on the previous DAC samples, a return-to-zero encoding is adopted here by resetting the DAC output before each conversion. The implementation of the slope generator is shown in Fig. 5.4 (b). Similar to the current DAC, a cascode current source is employed for better linearity and reduced supply sensitivity. After the output voltage, $V_{O,SG}$, has been sampled on C_{SG}, the pull-up transistor, M_{pu}, will pull the output node to the supply in order to suppress any leakage current through switch S_1 during the following steps (see Fig. 5.3).

A bootstrap technique, as shown in Fig. 5.5, is employed to implement the sampler ($S_{1,3}$) and voltage combiner (S_4) switches of Fig. 5.3 for the purpose of minimizing their ON-resistance. In the conventional bootstrap switch [115, 116], due to the reliability considerations of M_{10}, NMOS M_9 with its gate directly connected to supply is added to charge V_m to around $V_{DD} - V_{th}$ during the tracking phase. However, since M_9 is on the verge of turning on, its equivalent resistance is not large enough to suppress the leakage. Unlike in ADC designs, where the input is normally considered a 'voltage source,' the input of S_4 is stored as charge on C_{DAC} [see Figs. 5.3 (c) and (d)]. Therefore, the leakage through M_9 causes the

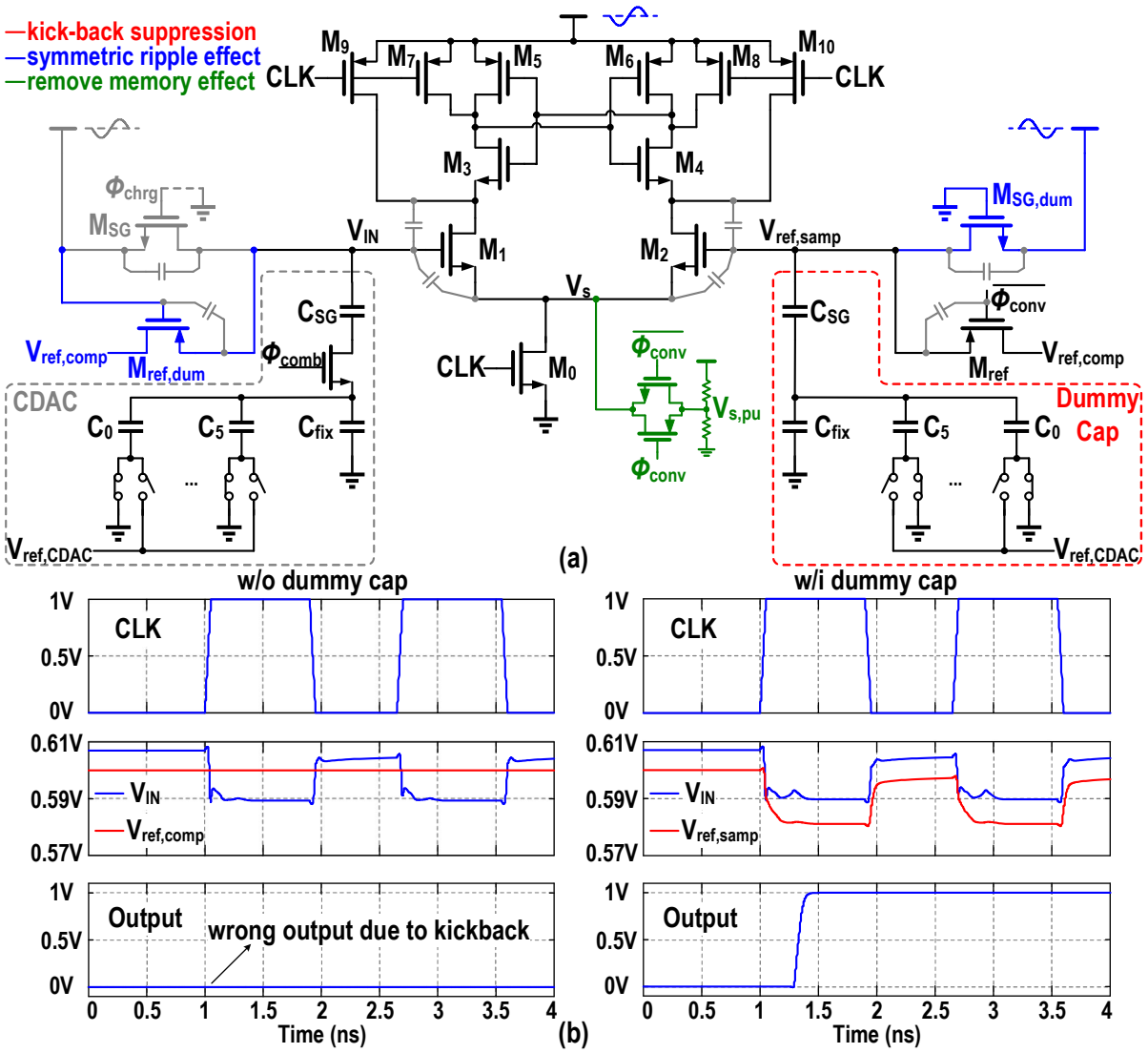


Figure 5.6: (a) Schematic of the comparator in SAR ADC. (b) Simulation results of its kick-back effect.

input level to decrease slowly during the tracking phase, ultimately leading to nonlinearity during the ADC conversion. To overcome this, the M_9 gate is also connected to $\overline{\text{CLK}}$, and M_{11} is added to pull-up V_m to fully turn off M_9 during the tracking phase, providing a large enough OFF-resistance. With the new design, simulations prove that V_{in} remains constant, and the initial drop due to the charge sharing with parasitic capacitance is compensated by the K_{DAC} estimation. Since V_{in} is less than 360 mV in this design, $M_{9,10}$ should not suffer from any reliability issues.

The comparator used in the SAR ADC is shown in Fig. 5.6 (a). During the comparison (i.e., CLK=1), the voltage perturbation at the internal nodes (e.g., V_s jumping to ground and the variation at the source of M_3) is

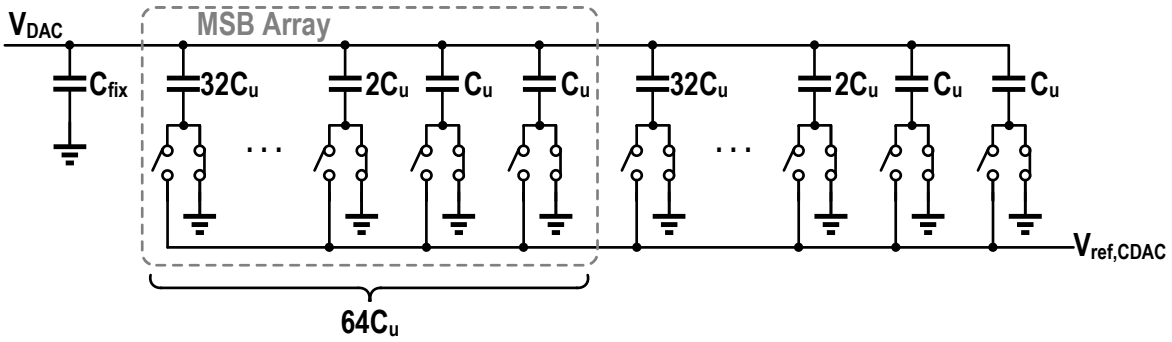


Figure 5.7: Capacitor arrangement of the CDAC in SAR ADC.

coupled to the input, disturbing the input voltage and comparator's decision [see Fig. 5.6 (b) left]. To alleviate this kick-back effect, dummy capacitors [see the red dotted region in Fig. 5.6 (a)] and a sampling switch (M_{ref}) are placed at the other input of the comparator to sample the reference voltage, $V_{ref,samp}$, in every reference cycle. Both V_{IN} and $V_{ref,samp}$ are affected similarly by the kick-back, and consequently, the comparator can decide correctly, as shown in Fig. 5.6(b). Moreover, the supply ripple can also couple to the comparator's inputs through the drain-source/gate-drain parasitic capacitance of M_{SG}/M_{ref}, potentially affecting the comparator's decision. Hence, two dummy switches, $M_{SG,dum}$ and $M_{ref,dum}$ are also inserted [see the components in blue in Fig. 5.6 (a)] such that the supply ripple appears as a CM voltage at the comparator's inputs, thus securing its seamless operation. Finally, the common source node of $M_{1,2}$, V_s, is also pulled up to a fixed voltage during the charging and combining phases to remove the memory of the last conversion at the comparator's internal nodes [see the components in green in Fig. 5.6 (a)].

The arrangement of the 6-bit CDAC in the SAR ADC is also reflected in Fig. 5.6 (a). A fixed capacitor, C_{fix}, is included to adjust the ADC resolution. For the charge-recycling switching, the MSB capacitor in CDAC is further split into a sub-array (see Fig. 5.7) to realize the down-transitions after the first conversion cycle.

Figure 5.8 reports the simulated supply sensitivity (the ratio between the variations of the PD resolution normalized to its nominal value and the supply voltage) of the implemented PD, reading $\beta \approx 0.325\,\mathrm{V}^{-1}$ around the 1 V supply, which is about $3.7\sim 6.3$ times lower than that of the conventional TDC/DTC. To further improve the spur performance, a second-order $\Delta\Sigma$ modulator is employed, as discussed in the following section.

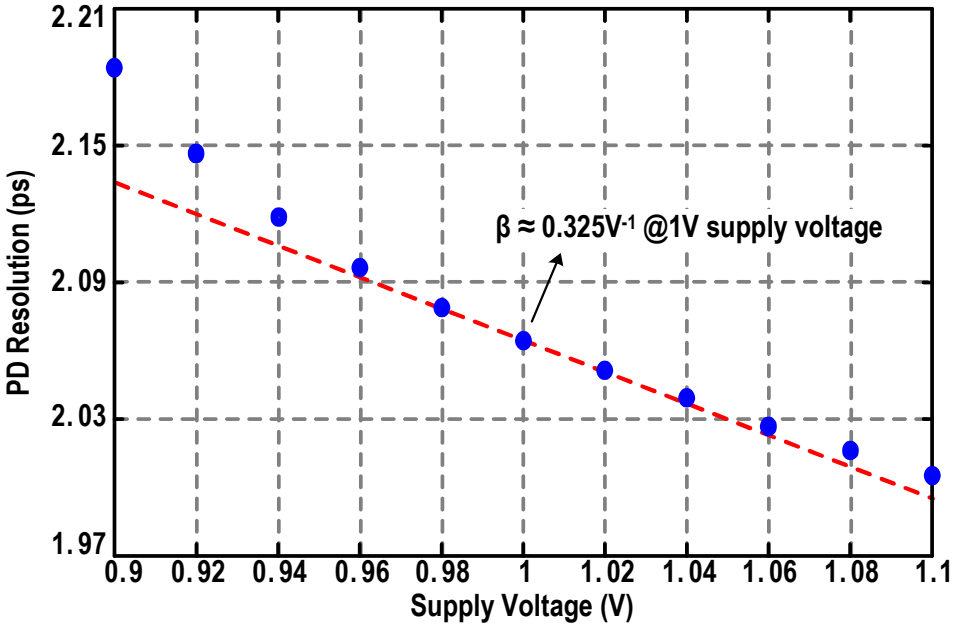


Figure 5.8: Simulated supply sensitivity of the PD.

5.3.2 Divider and Resampler

The oscillator's frequency is divided down by a 6-bit MMDIV, implemented by cascading six stages of divide-by-2/3 cells [117]. A second-order $\Delta\Sigma$ modulator drives the MMDIV to randomize the pattern of division ratio, thereby further suppressing the possible spurs at the intermodulation frequencies and ensuring proper convergence of the K_{DAC} calibration at near-integer channels. However, the maximum time duration in which the slope generator is active increases to $2T_{\mathrm{CKV}}$ in this case. Hence, the dynamic range of V_{SG} is double in comparison with the first-order modulator case, thus compromising the linearity of the cascode current mirror in the slope generator. To reduce the maximum time error related to the high-order $\Delta\Sigma$ modulator, [118] proposed to sequentially resample the divider output by the rising and falling edges of CKV with two flip-flops. Although a fixed timing relationship could be guaranteed in this way, the delay of the flip-flop could easily reach $0.5T_{\mathrm{CKV}}$ at higher oscillation frequencies, leading to a metastability problem. In this design, the divider output is directly resampled in parallel by both the rising and falling edges of CKV (see Fig. 5.9). The following 2-to-1 MUX then selects between the two resampled outputs ($\mathrm{DIV_r}$ & $\mathrm{DIV_f}$), realizing a quantization step of $0.5T_{\mathrm{CKV}}$ and reducing the dynamic range of the slope generator to only one T_{CKV}

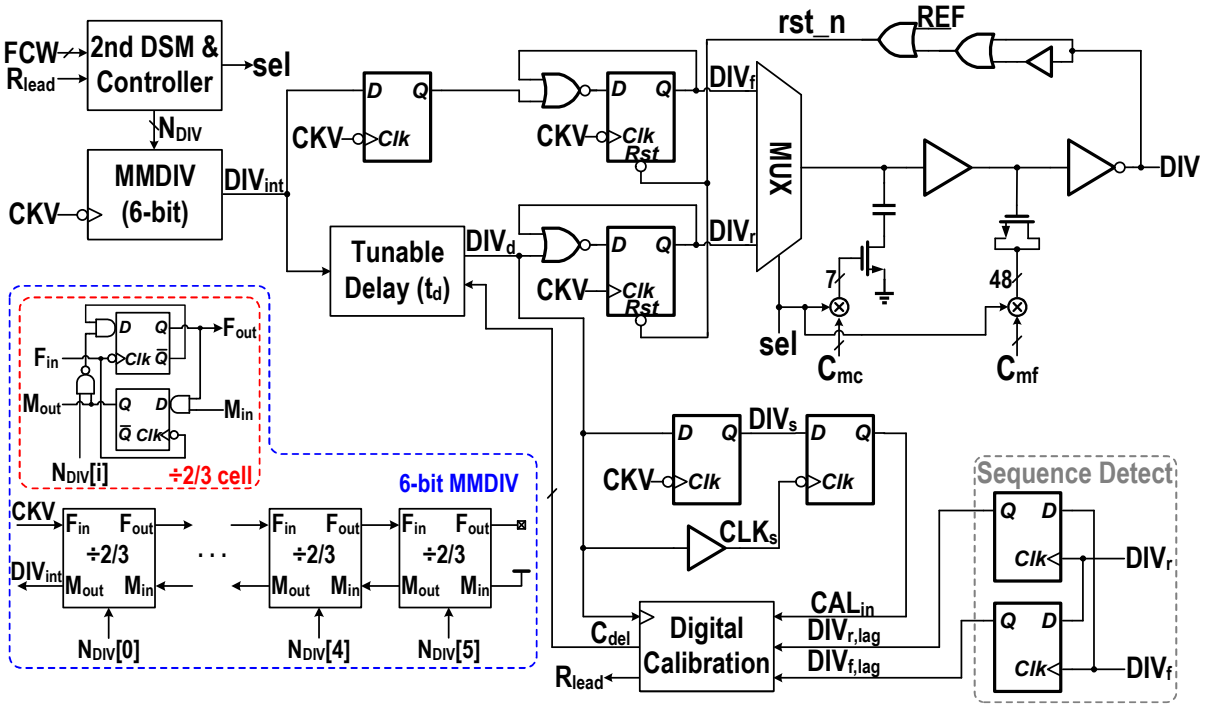


Figure 5.9: Block diagram of the MMDIV and the resample system.

($\pm 0.5T_{\mathrm{CKV}}$). The correct timing relationship is sensed by the sequence detect block and the result ($\mathrm{R_{lead}}$) is provided to correctly control the divider. Besides, a tunable delay (t_{d}) is inserted before the rising-edge triggered resampling flip-flop and calibrated on-chip to avoid metastability. More details will be further elaborated in Section 5.3.3.1.

The input to the $\Delta\Sigma$ modulator represents the fractional frequency ratio between the PLL output and the reference in the unit of the quantization step. Therefore, to correctly control the divider with its quantization step being halved through resampling, the input to the $\Delta\Sigma$ modulator, $\mathrm{FCW_F}$, is doubled first, while the modulator output is divided by two to cancel this effect (see Fig. 5.2) since the divider itself is still an integer one. The integer part of the division result adds with the integer part of the frequency control word, $\mathrm{FCW_I}$, to form the division ratio of MMDIV (N_{div}), while its fractional part is accumulated. By default, $\mathrm{DIV_f}$ leads $\mathrm{DIV_r}$ ($\mathrm{R_{lead}} = 0$). Hence, the 1-bit sum of the accumulation (sel) controls the MUX to pass through $\mathrm{DIV_r}$ when the $0.5T_{\mathrm{CKV}}$ time step is required, and when a carry-out signal is generated, N_{div} is further increased by 1. When $\mathrm{DIV_r}$ leads $\mathrm{DIV_f}$ ($\mathrm{R_{lead}} = 1$), an extra 1 is added to N_{div} when $\mathrm{DIV_r}$ is selected to compensate for the reversed timing relation between $\mathrm{DIV_{f,r}}$.

5.3.3 Digital Calibration

5.3.3.1 Calibration of t_d

Since the MMDIV is triggered by the falling edge of CKV, its output (DIV_{int}) may fall intolerably close to the CKV rising edge. Thus, a tunable delay (t_d) is inserted before the rising-edge triggered resampling flip-flop to avoid metastability. As shown in Fig. 5.9, the tunable delay block aligns its output (DIV_d) with the following falling edge of CKV, so that the maximum setup and hold margin could be guaranteed when sampled by the CKV rising edge. To find the proper value of t_d, its control code is swept, and for each delay setting, the delayed output (DIV_d) is sampled by the falling edge of CKV to obtain the calibration input, CAL_{in}. The optimum control code is reached when CAL_{in} jumps from high to low. A similar principle is used in [119] to delay the rising-edge triggered divider output close to the CKV falling edge so that it would not experience metastability when getting retimed by the CKV rising edge again. However, it faces a dilemma that the proper t_d value needed during the PLL locking should be obtained with the oscillator operating at the desired frequency, which is guaranteed after the loop is locked. The problem is more severe under the supply ripple since both the divider output delay and t_d are affected by the supply perturbations. Thus, due to the incorrect phase relationship between the reference and the supply ripple and the inaccurate T_{CKV}, the t_d values calibrated before the loop settles may also lead to metastability during the normal operation. In this design, DIV_f is guaranteed to be free of metastability through obtaining DIV_{int} from the M_{out} terminal of the first divide-by-2/3 cell (see Fig. 5.9) while placing the corresponding resampling flip-flop in close proximity. Hence, the locking of the loop is guaranteed by operating the $\Delta\Sigma$ modulator in the first-order mode and fixing sel to 0 initially. Then, the proper t_d values are calibrated under the correct phase relationship between the reference and the ripple. After the t_d calibration, the loop switches seamlessly to the second-order $\Delta\Sigma$ operation mode with the resampling process enabled.

The dynamic range of t_d is designed to cover at least one T_{CKV} in the fast process corner. Considering the delay variations under different PVT conditions, the calibration may align DIV_d to the first or second falling

edge after $\mathrm{DIV_{int}}$. Therefore, instead of only sampling $\mathrm{DIV_{int}}$ by the CKV falling edge once [118, 120], two flip-flops in cascade (see Fig. 5.9) perform this sampling twice so that $\mathrm{DIV_f}$ always leads or lags $\mathrm{DIV_r}$ by only $0.5T_{\mathrm{CKV}}$. The uncertainty in the timing relationship is then resolved by the sequence detect block through mutual sampling $\mathrm{DIV_{f,r}}$ by each other, and its output $\mathrm{R_{lead}}$ is used to correctly generate N_{div}.

If the DC supply voltage shifts after the t_{d} calibration, $\mathrm{DIV_d}$ would deviate from its optimum position, and the rising-edge triggered resampling flip-flop may re-enter its metastable state in case $\mathrm{DIV_d}$ becomes too close to the CKV rising edge again. However, only an intermittent re-calibration of the t_{d} value is sufficient considering more than 40 mV of tolerable variation of the DC supply as obtained from simulations. Meanwhile, by varying the t_{d} control code around the calibrated one when sel is 0, the corresponding calibration algorithm could be easily modified to operate in the background and update the t_{d} value when the non-optimum condition is detected.

5.3.3.2 Calibration of Resampler's Mismatch

In the resampling system, any mismatch between the two resampling paths, including the delay mismatch and the deviation from the 50% CKV duty cycle, would lead to spurs at f_{frac}. In [118, 120], this mismatch is compensated by a DTC through an LMS algorithm [121]. However, in the proposed design, compensating the mismatch through the DAC would increase the dynamic range of slope generator and DAC, thus affecting their linearity performance. Meanwhile, the finer DAC resolution ($\sim$0.5 mV for $\sim$0.5 ps equivalent time resolution) required for the accurate compensation also leads to a larger DAC area and power consumption due to more stringent matching requirements and more complex decoding logic. To avoid these issues, the mismatch is compensated directly at the MUX output with a bank of variable capacitors consisting of seven thermometer-coded switched capacitors for coarse-tuning and 48 thermometer-coded MOS capacitors for fine-tuning. The MOS capacitors are sized to achieve $\sim$0.5 ps resolution, thus guaranteeing the <-50 dBc spur level. Since, in practice, the variable capacitors only need to cover a delay range of several picoseconds, its delay step is not expected to largely deviate from the nominal value. Meanwhile, the integral non-linearity requirement of the

capacitor bank is largely relaxed as long as its monotonicity is preserved.

The control codes of the variable capacitors, C_{mc} and C_{mf}, in Fig. 5.9, are generated through the LMS algorithm (see Fig. 5.2). Under a DC-DC converter supply ripple, the mismatch between the two resampling paths periodically changes, and consequently, the compensated C_{mc} and C_{mf} values must be adjusted accordingly. Note that the mismatch variation will be further sampled by the pattern of the MUX selection signal. Thus, in general, the resulting pattern is no longer located at f_{rip}, and could not be tackled by the ripple pattern estimation and cancellation block introduced in the following subsection.

Since, in a practical system, the PLL reference frequency (f_{ref}) is typically provided by a highly stable crystal oscillator, it is reasonable to generate the switching frequency ($f_{\mathrm{sw}} = f_{\mathrm{rip}}$) of the DC-DC converter powering the PLL directly through dividing down f_{ref}. Hence, $f_{\mathrm{rip}} = f_{\mathrm{ref}}/n$ ($n = 1, 2, 3, \dots$), where the integer n represents the division ratio of the corresponding frequency divider. Though the highest f_{sw} is limited to f_{ref} under this arrangement, an even higher f_{sw} would not be preferred due to the complexity of an extra block required to generate f_{sw}. Meanwhile, f_{sw} should also be chosen carefully, balancing the trade-off between the increase in losses of converter switching and clock distribution at the upper f_{sw} end and the sheer complexity of the frequency divider with a large division ratio at the lower end. Bearing these in mind, for $f_{\mathrm{ref}} = 50\,\mathrm{MHz}$ in this design, we selected f_{sw} to be equal to f_{ref} divided by 3, 6 or 12. Therefore, the mismatch pattern repeats itself every n ($n = 3$, 6 or 12 in this design) reference cycles. As a result, n separate LMS loops are used to calibrate C_{mf}, with the ith ($i = 1, \dots, n$) loop calibrating the C_{mf} of the $k \times n + i$ ($k = 1, 2, 3, \dots$) reference cycles. Such an arrangement would guarantee proper compensation even under the pessimistic assumption that the mismatch could vary by a large amount under the $50\,\mathrm{mV_{pp}}$ supply ripple considered here. When the mismatch, and correspondingly, its variation under supply ripple, is largely reduced through carefully balancing the delay between the two resampling paths in the design phase, it is also feasible to implement only one LMS loop calibrating the DC value of C_{mf}. Another LMS loop is also implemented to calibrate an average C_{mc} code for all reference cycles to simplify the calibration process. The detailed operation

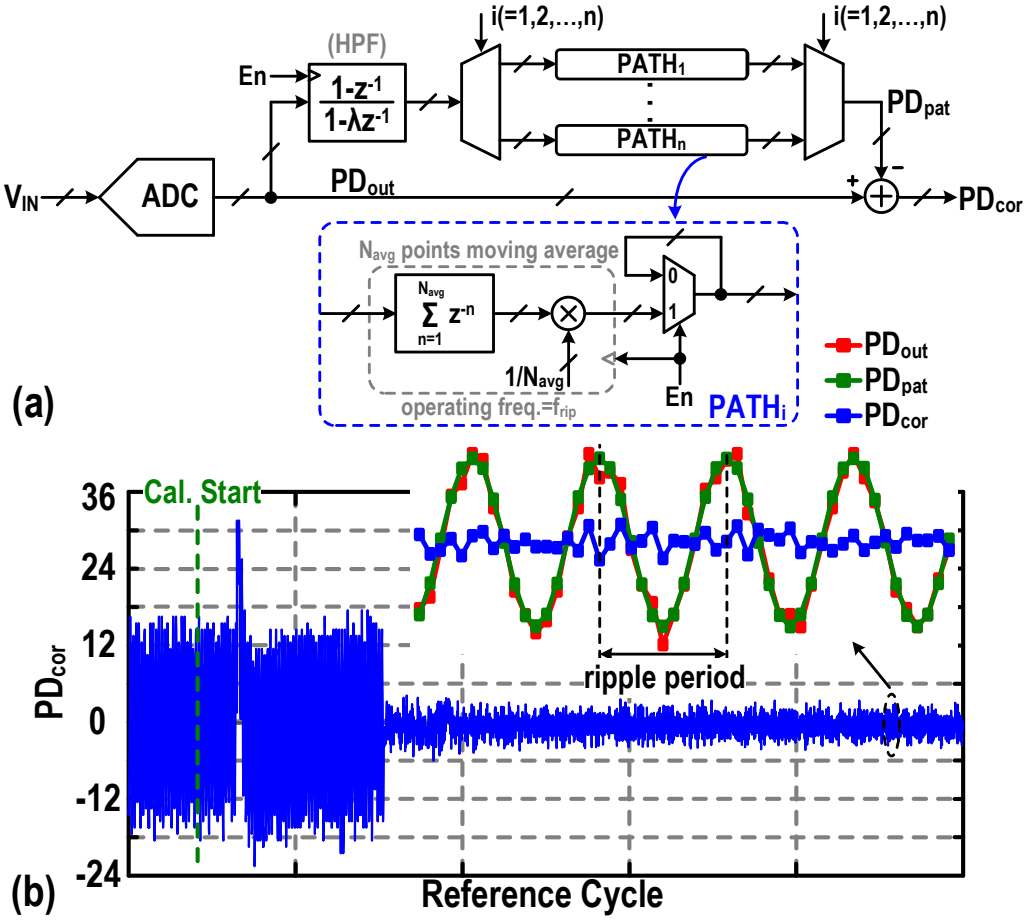


Figure 5.10: (a) Block diagram of the ripple pattern estimation and cancellation; (b) an example of calibration waveform with $f_{\text{rip}} = f_{\text{ref}}/12$.

of the calibration process will be further discussed in Section 5.3.3.4.

5.3.3.3 Ripple Pattern Estimation and Cancellation

As discussed in Chapter 2, the output delay perturbations of MMDIV and resample flip-flops caused by the supply ripple are sensed by the PD, and thus, they appear as spurs at the DPLL output. The subsequent pattern estimation and cancellation block, shown in Fig. 5.10, is used to suppress this effect. Since the SAR ADC output, PD_{out}, shows a periodic digital pattern at f_{rip} due to supply-induced delay variations, the task of this digital block is to extract this pattern and subtract it from PD_{out} before modulating the oscillator. To do so, n $(= f_{\text{ref}}/f_{\text{rip}})$ branches [PATH_{i} in Fig. 5.10 (a)], each storing one different point of PD_{out}, are rotationally enabled.[3] As a general case, PATH_{i} outputs 0 initially, which approaches

[3]For large n (i.e., small $f_{\text{sw}}/f_{\text{rip}}$), the variation of the supply ripple between consecutive reference cycles is small. Hence, the number of the branches may be reduced through reusing the calibrated value of the

the ith value in one period of the f_{rip} pattern at PD_{out} after the calibration is enabled. Hence, by subtracting PD_{pat} from PD_{out}, the effect of the supply-induced delay variations is suppressed. The N_{avg}-point moving-average filter in PATH_{i} is employed to suppress the random noise component in PD_{out} to guarantee accurate estimation of the f_{rip} pattern. To ease the implementation, the value of N_{avg} is limited to integer powers of 2, and simulation shows that $N_{\text{avg}} \geq 16$ is required to suppress the possible PN degradation. In this design, $N_{\text{avg}} = 64$ is used to guarantee that the inherent PN performance of the loop is preserved. A high-pass filter (HPF) is also inserted at the front. The HPF avoids the detected phase error at low-frequency offsets from entering the calibration loop and affecting the generated pattern PD_{pat}. Hence, the PN performance of the DPLL at low-frequency offsets would not be affected by this calibration. The corner frequency of the HPF, controlled by λ, is set to $\sim$125 kHz so that the deviation in the magnitude and phase response of the HPF does not limit the spur level at f_{rip}. A similar algorithm is employed in [122] to suppress the fractional or external DPLL spurs, consuming ~ 2 mW for each calibration loop. In contrast, $f_{\text{ref}}/f_{\text{rip}}$ in this design is a known integer determined during system planning, allowing us to avoid the need for the complex fractional delay filter and the extra calibration loop to optimize the filter coefficient, as in [122], resulting in a much lower power consumption. Meanwhile, after the accurate PD_{pat} is obtained, the extraction process is also turned off by disabling the enable signal (En). After that, only the output of each branch is preserved with all other calculations in the calibration loop disabled, which further reduces the current consumption to $\sim 80\,\mu$A. Compared to the ~ 2 mW consumed by the loop components, the power efficiency is thus only degraded by $\sim 4\%$. The extraction process may also keep operating in the background to track environmental changes if needed, raising the power consumption to $\sim$190 μA. Otherwise, a simple digital threshold detector could be implemented to monitor PD_{cor} and only trigger the extraction process when PD_{cor} exceeds the predefined threshold value, lowering the extra power penalty.

Note that the algorithm cannot suppress the effect of supply noise. Hence, the phase noise induced by the supply noise is determined by the

$k \times n + i$ ($i = 1, 2, 3, \dots$) reference cycles for the nearby reference cycles (i.e., $k \times n + i \pm 1, \dots$).

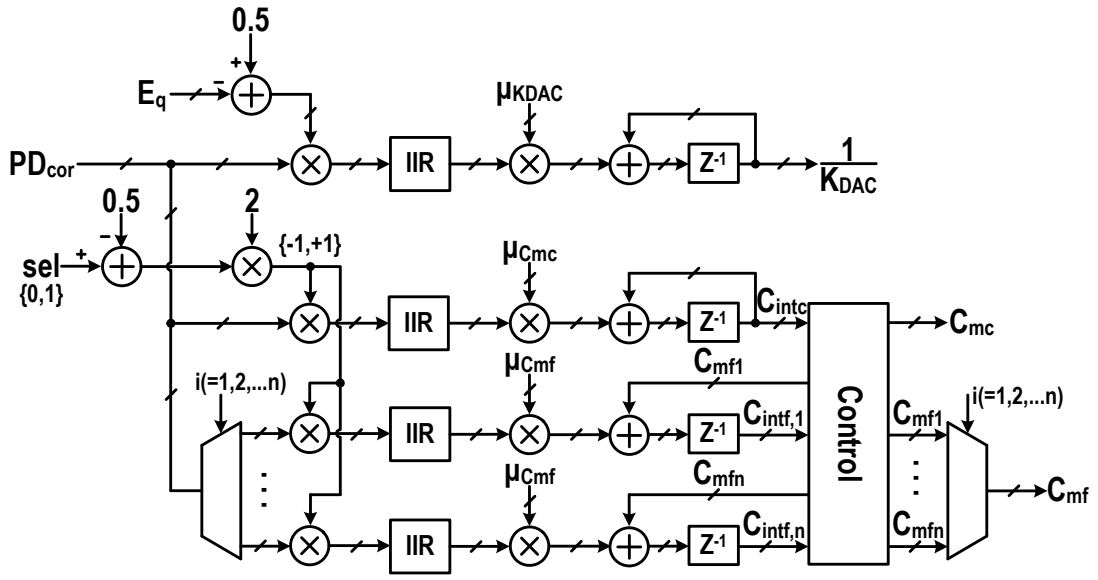


Figure 5.11: Block diagram of the LMS calibration loops for the DAC gain and resampler's mismatch.

intrinsic supply sensitivity of the circuit, which is similar to conventional designs. Meanwhile, in the practical setting, the DC-DC converter typically shows a much lower output noise compared to LDOs [50, 56, 123, 124], thus posing no significant degradation to the loop performance. It is also possible that some noise may be coupled from other functional blocks when used in a larger system. However, the tolerance to this interference from the loop components is relatively high (see Chapter 3), alleviating their effect.

5.3.3.4 Co-operation of Calibration Loops

The detailed block diagram of the LMS loops calibrating K_{DAC} and $C_{\mathrm{mc/f}}$ is shown in Fig. 5.11. The error signal, $\mathrm{PD_{cor}}$, is cross-correlated with $(0.5-E_{\mathrm{q}})$ and also with the selection signal (sel) of the resampler's MUX. A simple first-order IIR filter follows to attenuate non-DC components after the correlation. Note that it is the inverse of K_{DAC}, $1/K_{\mathrm{DAC}}$, that is actually being estimated so that the calculation of n_{DAC} is realized with a multiplier instead of a divider, thus saving power consumption and hardware. The estimation of the coarse C_{mc} and fine C_{mf} control codes is completed in two steps. First, the controller enables the LMS loop to calibrate for an average C_{mc} value over a predefined number of reference cycles. C_{mc} is then fixed and the corresponding LMS loop disabled, while starting the

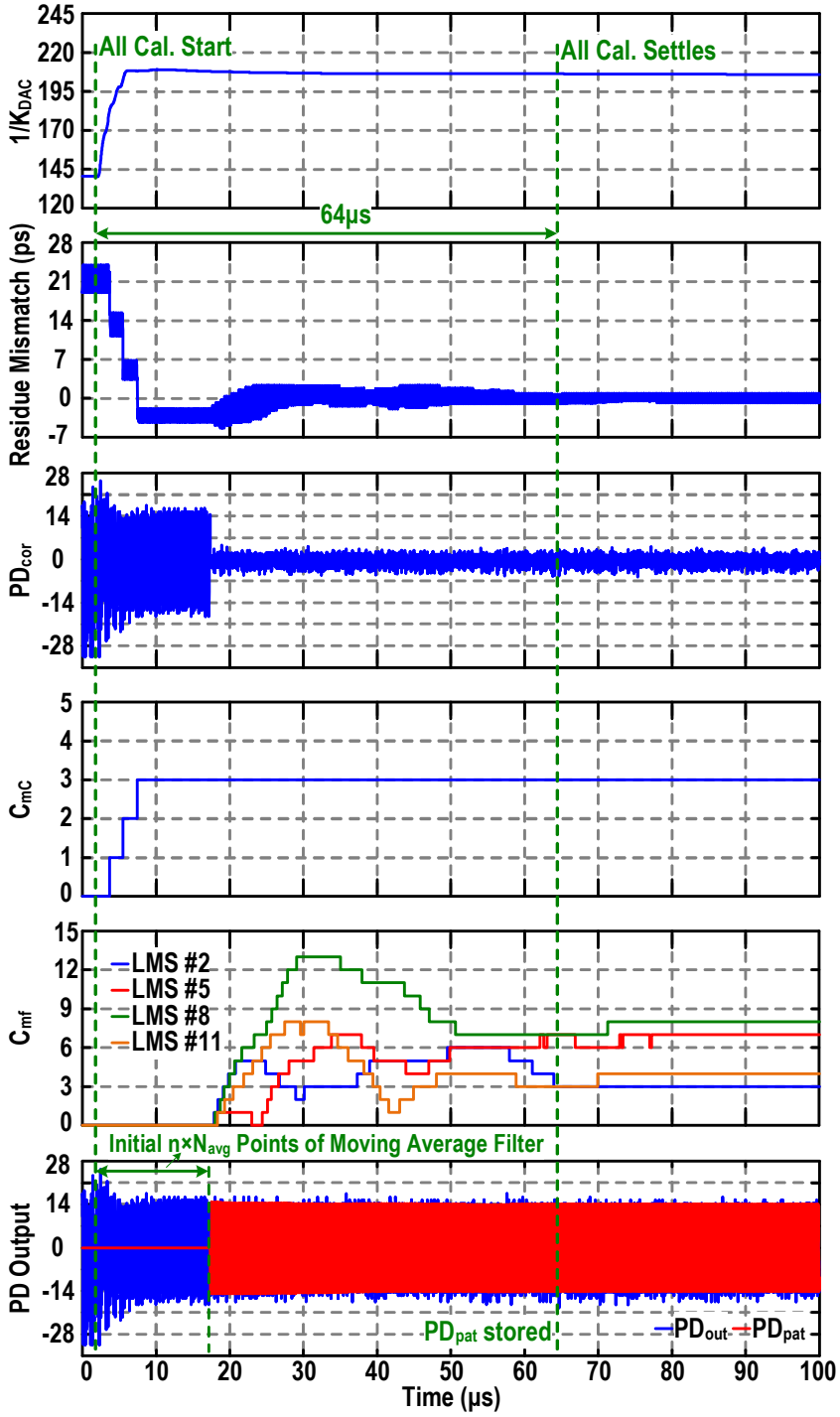


Figure 5.12: Convergence trajectory of the calibration process with $f_{\mathrm{rip}} = f_{\mathrm{ref}}/12$.

calibration of the fine-tuning code C_{mf}. As discussed in Section 5.3.3.2, C_{mf} is estimated cyclically through $n = f_{\mathrm{ref}}/f_{\mathrm{rip}}$ LMS loops (see Fig. 5.11), with the ith $(i = 1, \ldots, n)$ loop correlating the $\mathrm{PD_{cor}}$ and the sel signal of the $k \times n + i$ $(k = 1, 2, 3, \ldots)$ reference cycles. The individual results, $C_{\mathrm{intf,i}}$, are monitored by the controller and directly passed onto C_{mfi} to form the C_{mf} sequence if they remain within the [0, 48] range. When the limits

are exceeded, the controller adds/subtracts 32 to/from $C_{\mathrm{intf,i}}$ to generate the corresponding C_{mfi}, while decreasing/increasing C_{mc} by two for the $k \times n + i$ reference cycles. Therefore, the fine-tuning range is extended with a minimal disturbance introduced during the LMS calibration process.

Fig. 5.12 plots the simulated convergence trajectory of the calibration process with $f_{\mathrm{rip}} = f_{\mathrm{ref}}/12$. The induced mismatch is large to clearly demonstrate the settling behavior. In general, the implemented calibration loops could operate in parallel without a dedicated calibration sequence due to the difference in signal patterns they operate on: The signals that $\mathrm{PD_{cor}}$ is correlated with are related to f_{frac}, with $(0.5 - E_{\mathrm{q}})$ showing the high-pass shaped noise spectrum of the $\Delta\Sigma$ modulator and the sel signal being rich in discrete tones at f_{frac} and its harmonics, while the ripple pattern cancellation algorithm extracts the pattern at f_{rip}. To increase the settling speed, a larger integration step ($\mu_{\mathrm{KDAC,0}}$ and $\mu_{\mathrm{Cmf,0}}$) is employed initially and then gear-shifted to their final values of $\mu_{\mathrm{KDAC,0}}/32$ and $\mu_{\mathrm{Cmf,0}}/32$ in two steps under the control of a reference cycle counter in order not to affect the loop performance during the normal operation. As shown in Fig. 5.12, the settling time of the whole calibration process is $\sim 64\,\mu$s and is dominated by the C_{mf} calibration. For special cases of f_{frac} being close to f_{rip} or its harmonics, the frequency of the sel pattern becomes related to f_{rip}, and the interaction between the $C_{\mathrm{mc/f}}$ calibration and the ripple pattern cancellation could impede the proper loop convergence. However, the problem could be avoided by disabling the $C_{\mathrm{mc/f}}$ calibration in this scenario, while the ripple pattern estimation and cancellation block could cancel the effects of both the supply induced delay perturbation and the resampler's mismatch that is small enough as not to saturate the PD output.

5.3.4 LC Oscillator and Supply Pushing Calibration

The structure of the complementary LC oscillator is shown in Fig. 5.13. It consists of 7-bit 5.2 MHz/LSB binary and 63-bit 125 kHz/LSB unary switched-capacitors for coarse and fine frequency tuning, respectively. An extra switched-capacitor controlled by a first-order $\Delta\Sigma$ modulator is also added to further improve the frequency resolution to $\sim$15 kHz. The first stage of the oscillator's buffer is implemented by an NMOS common-source

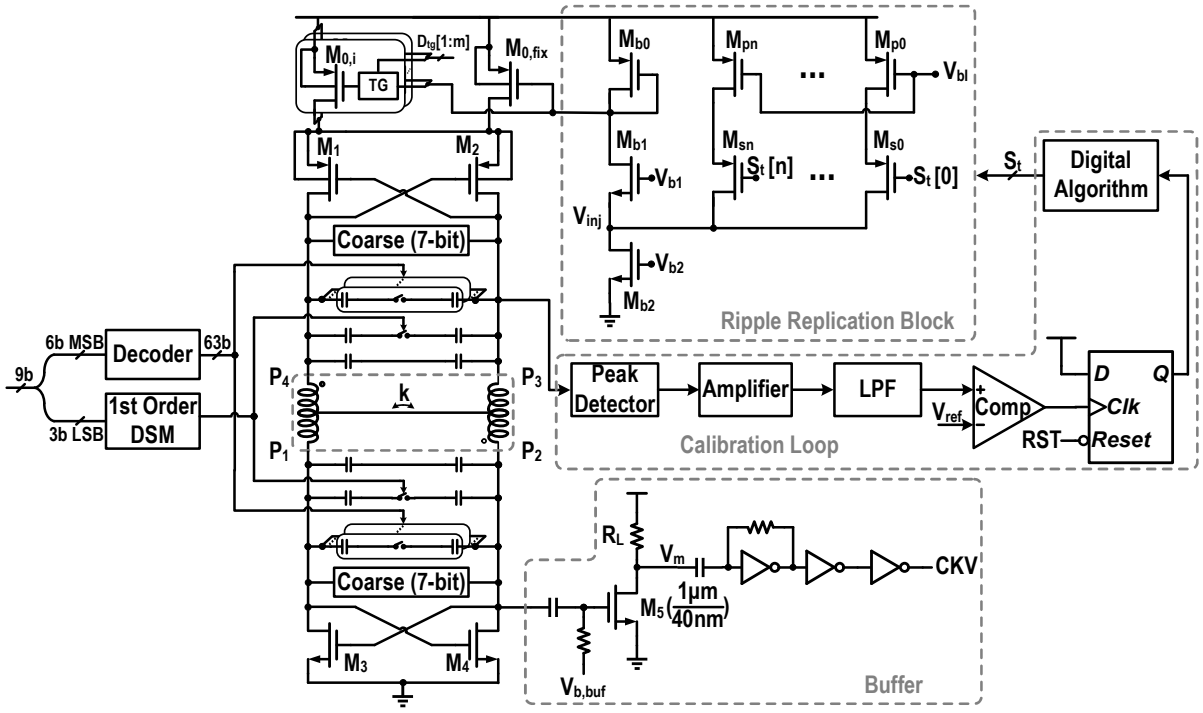


Figure 5.13: Schematic of the LC oscillator with its calibration loop.

amplifier with a load resistor. A tiny NMOS is intentionally used in this stage so that the variation of its input parasitic capacitance due to the supply ripples would not affect the oscillator's performance. Three stages of self-biased inverters then generate a rail-to-rail square wave that drives the MMDIV and the resampling flip-flops.

Similarly to Chapter 4, a ripple replication block (RRB), controlled by the 6-bit $S_t[5:0]$ from the calibration loop, is designed to replicate the supply ripple to the gate of M_0 with a proper gain to stabilize the oscillator tail current and reduce its supply pushing. M_0 is also implemented as a parallel combination of a fixed part, $M_{0,fix}$, with a bank of switchable unit transistors, $M_{0,i}$, to tune the tail current and, correspondingly, the oscillation swing. Thus, compared to the conventional LDO/oscillator integrated solution, the extra voltage headroom consumed by the LDO's pass transistor is saved through performing both supply regulation and current tuning with only one transistor, as already pointed out in Chapter 4.

The principle of the S_t calibration is also similar to that proposed in Chapter 4. The calibration loop first detects and amplifies the variation of the oscillation amplitude. A digital algorithm then determines the optimum code to minimize that amplitude variation, thereby reducing spurious tones.

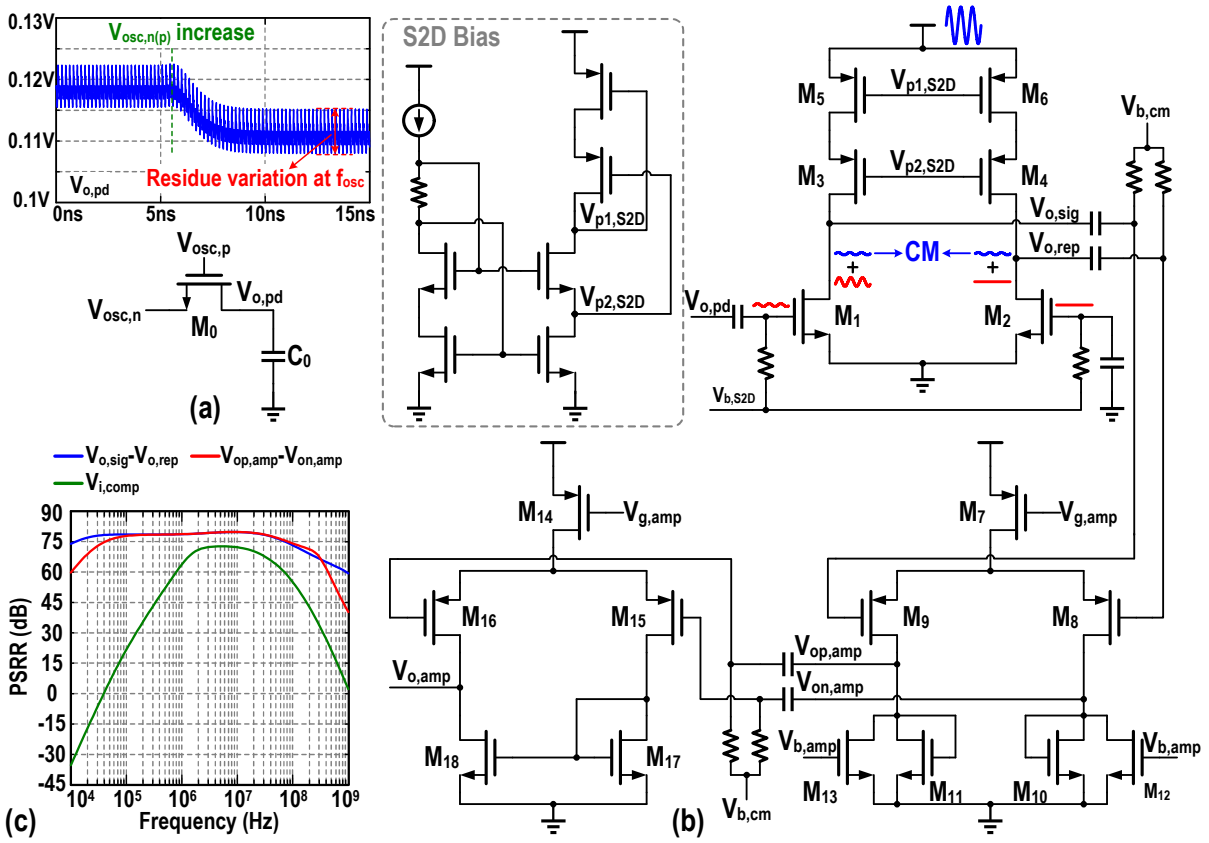


Figure 5.14: Schematic of (a) the peak detector and (b) the amplifier chain in the oscillator calibration loop. (c) Simulated PSRR of the loop.

The reduced supply pushing is also beneficial in significantly suppressing the conversion of thermal noise of supply to phase noise. Foreground calibration is selected due to the relatively relaxed spur requirement of the targeted applications (i.e., <-50 dBc) and the slow supply and temperature drifts of a low-power system whose effect could be compensated with intermittent re-calibrations. However, the calibration loop in Chapter 4 still needs to be powered with a clean supply to operate correctly. In this section, we tackle this issue by modifying the structure of the peak detector and amplification chain.

Fig. 5.14 (a) shows the peak detector, consisting of an NMOS transistor, M_0, and a load capacitor, C_0. The gate and source terminals of M_0 are driven by the oscillator's differential output, $V_{\mathrm{osc,n(p)}}$.[4] Hence, M_0 acts as a switch and approximately turns ON for half of the oscillator cycle when $V_{\mathrm{osc,p}} \geq V_{\mathrm{osc,n}} + V_{\mathrm{th}}$. During this phase, the low-pass filter formed by

[4] A dummy branch with the gate and source terminal of M_0 being swapped is also included to avoid asymmetry between the differential outputs of the oscillator.

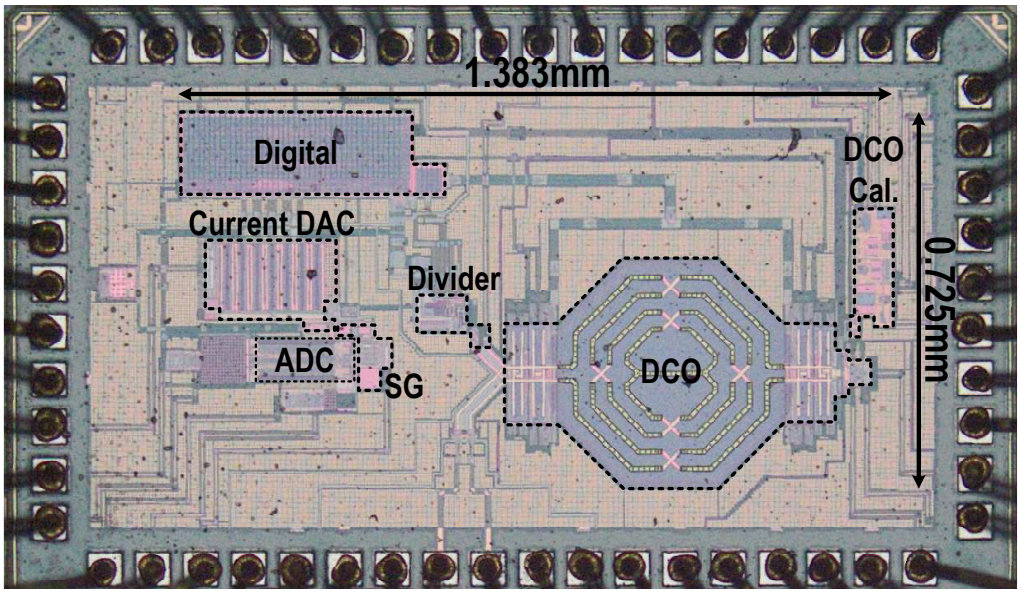


Figure 5.15: Chip micrograph of the DPLL.

M_0 ON-resistance and C_0 filters out the high frequency components and extracts the average value of this half-cycle, leading to a peak detection gain of $\sim 1/\pi$. Since the peak detector is not connected to the supply, its performance is not affected by the supply ripple.

Fig. 5.14 (b) shows the amplifier chain located between the peak detector and comparator. Similarly to the DAC current source, the first amplifier stage is implemented with a cascode PMOS current mirror for higher power supply rejection ratio (PSRR). We now inspect the outputs of the first-stage amplifier. The supply ripple and the peak detector voltage appear as common-mode (CM) and differential-mode (DM) signals, respectively. Therefore, when these signals are sent to the following differential amplifier stages, the desired signal is further amplified, while the supply-induced variations are suppressed by their CM rejection ratio (CMRR). As can be gathered from simulation results in Fig. 5.14 (c), PSRR is higher than 60 dB at the comparator's input over the desired frequency range (i.e., 2–20 MHz), enough for the calibration loop to function correctly under the $50\,\mathrm{mV_{pp}}$ ripple.

5.4 Measurement Results

The proposed fractional-N DPLL is implemented in TSMC 40-nm 1P8M CMOS without the customary ultra-thick metal layers. Fig. 5.15

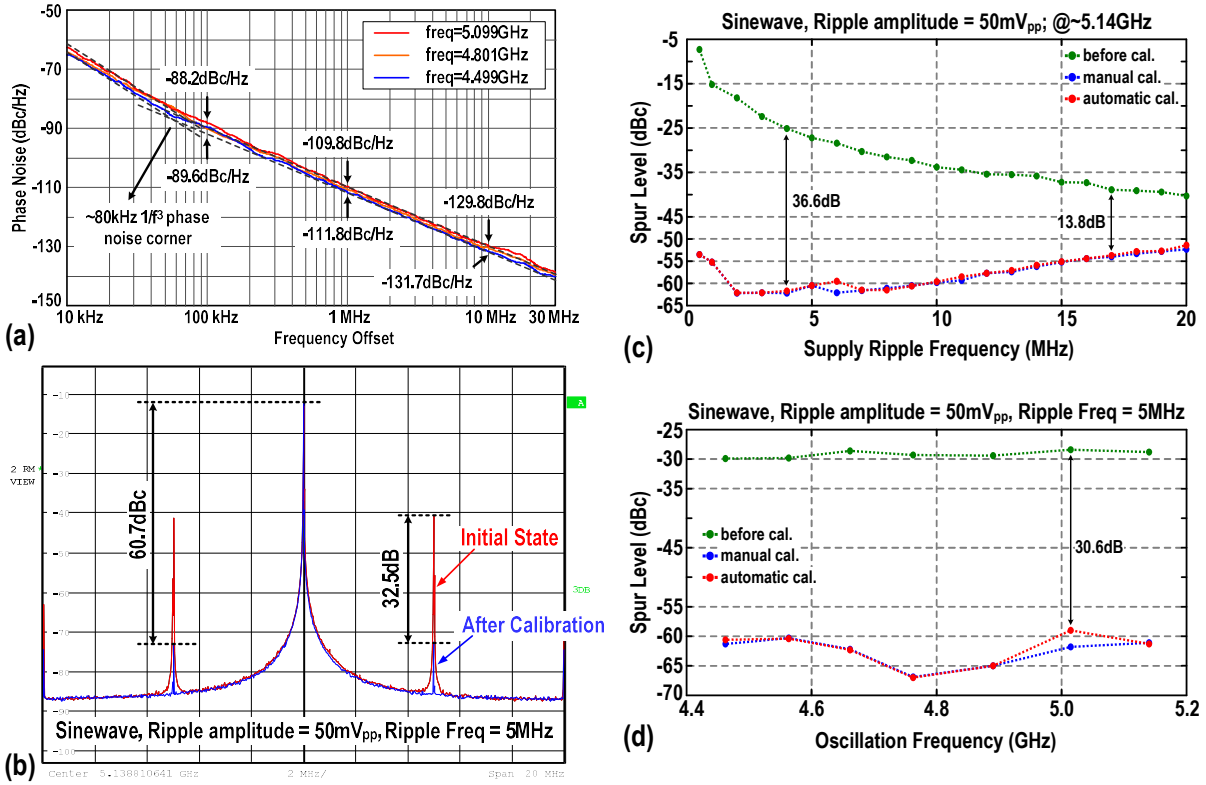


Figure 5.16: Measurements of the free-running DCO: (a) PN across the tuning range; (b) spectrum before and after the automatic calibration in face of 50 $\mathrm{mV_{pp}}$ 5 MHz ripple; (c) spur levels across the ripple frequency, and (d) across the oscillation frequency for both the manual and automatic calibrations.

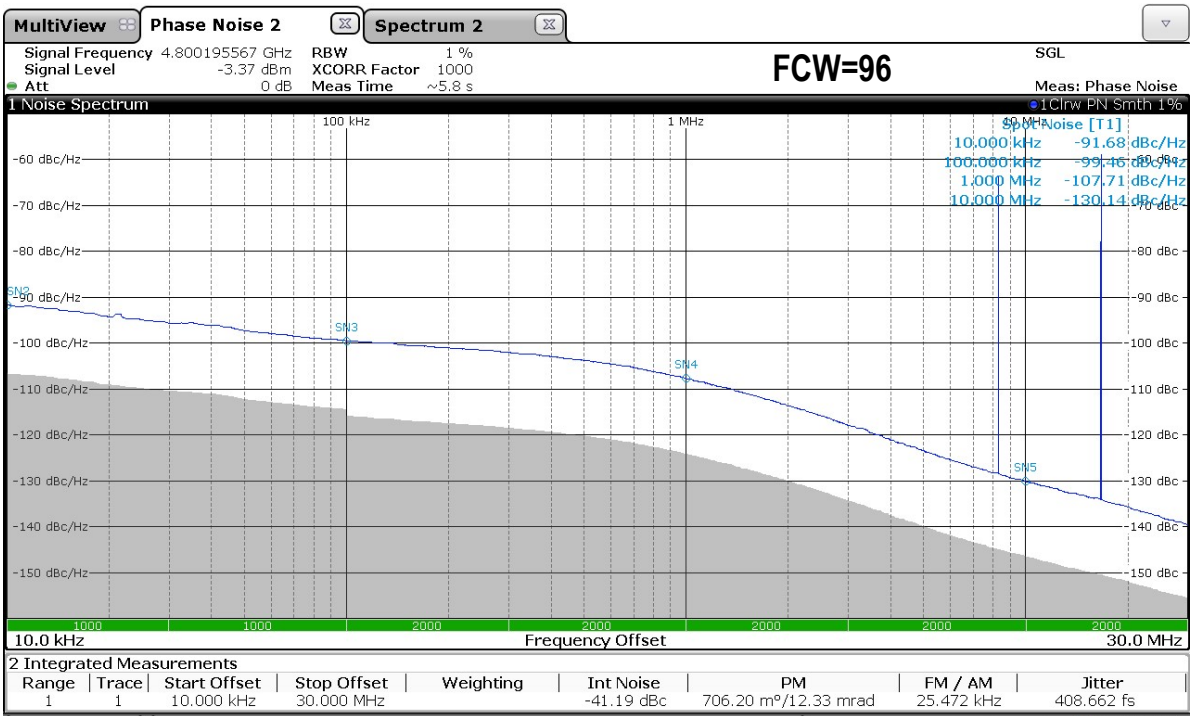
shows the chip micrograph. The DPLL has an active area of 0.39 $\mathrm{mm^2}$, in which the oscillator, the current DAC, and the digital part occupy 0.157 $\mathrm{mm^2}$, 0.14 $\mathrm{mm^2}$, and 0.056 $\mathrm{mm^2}$, respectively. Powered by a 1.0 V supply, the whole loop consumes 3.25 mW (1.02 mW for DCO, 0.92 mW for PD, and 0.63 mW for the digital part).

The DPLL is first set to an open-loop mode to measure the performance of the free-funning DCO. The measured tuning range (TR) is 4.47–5.14 GHz. Fig. 5.16 (a) shows the measured PN performance across the TR. PN varies from −109.8 to −111.8 dBc/Hz @1 MHz offset, with a flicker noise corner around 80 kHz. The effectiveness of the modified calibration loop is verified in Fig. 5.16 (b)–(d). In these measurements, a 50 $\mathrm{mV_{pp}}$ sinewave ripple is applied to the supply of the oscillator core and its calibration loop. Fig. 5.16 (b) compares the oscillator spectrum before and after the calibration. Under the 50 $\mathrm{mV_{pp}}$ 5 MHz supply ripple, the measured spur level is reduced by 32.5 dB and reaches −60.7 dBc after the calibration. Fig. 5.16 (c) shows the measured spur level over the frequency of the supply

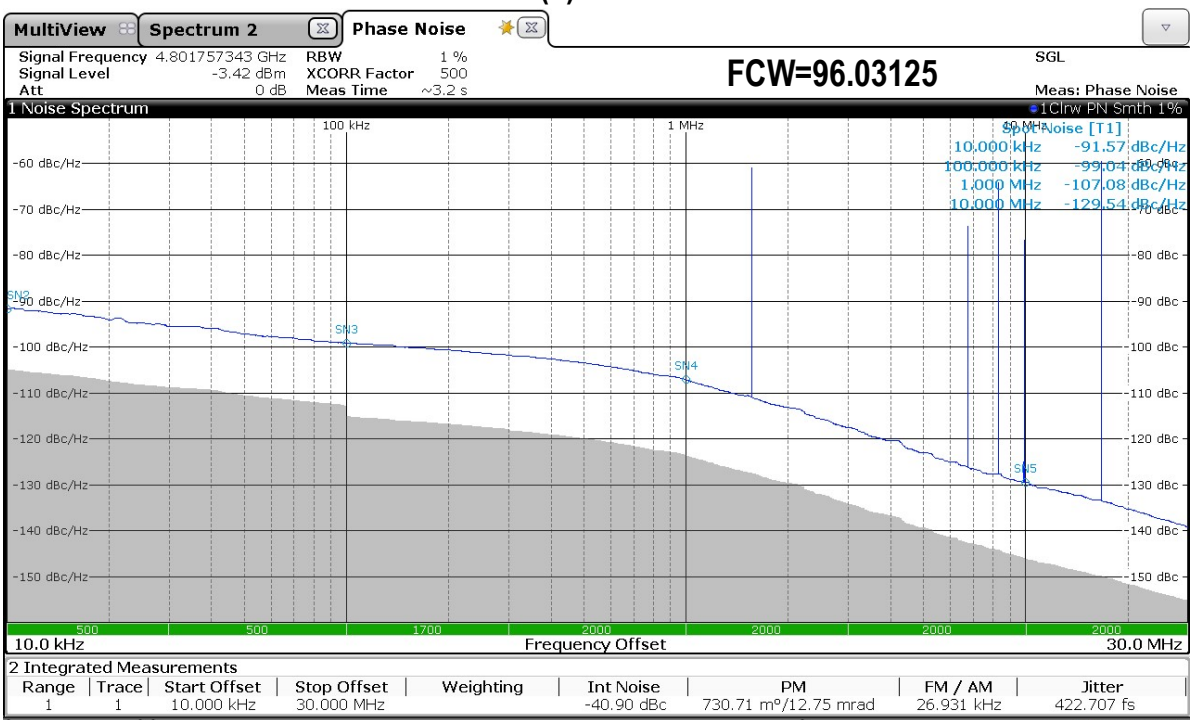
ripple. The oscillator exhibits lower than −51 dBc spur level with the 0.5-to-20 MHz 50 mV_{pp} supply ripples, while the calibration loop is able to successfully find the optimum operating point in most cases. The improvement after the automatic calibration is between 13.8 to 36.6 dB for 4 ∼17 MHz ripples. The rise of the spur level after the calibration at higher f_{rip} is due to the limited bandwidth of RRB, since a phase shift between the supply ripple and its replica would result in a partial cancellation of the oscillator's tail current variation, as discussed in Section 4.3.1.1. In Fig. 5.16 (d), the spur level is measured across the oscillator TR. The worst-case spur level under the 50 mV_{pp} 5 MHz ripple is ≤−59 dBc, while the calibrated value also follows the optimum one successfully on most occasions. The improvement after the calibration is higher than 30 dB across the TR.

The DPLL is measured with a 50 MHz external crystal reference clock and under the 50 mV_{pp} supply ripple. Fig. 5.17 shows the measured PN plot for both the integer-N and fractional-N channels around 4.8 GHz when $f_{rip} = f_{ref}/6$. The rms jitter integrated from 10 kHz to 30 MHz is 423 fs for the fractional-N operation, and 409 fs for the integer-N operation.

The measured DPLL PN is compared with the estimated values in Fig. 5.18. The phase-domain PN estimation is obtained based on the linear s-domain model of the loop, while the time-domain estimation is calculated from the simulation results of the DPLL model in Matlab. The main difference between the measurement result and the estimated PN at low frequency offsets could come from the inaccurate values of the flicker noise of the building blocks. Also, the flicker noise of the comparator, which is difficult to identify from simulation [125], is not considered in the PN estimation, and the simulated input-referred noise of the comparator is assumed to be white. To reduce the parasitic capacitance of the comparator, relatively small transistors are used in the comparator design. Thus, its flicker noise may have a large impact on the low frequency PN of the loop. Fig. 5.18 also plots the phase domain estimation of the noise from major PN contributors in the loop. The noise of the loop components, including the noise from the phase detection circuitry, the noise from the divider and the following resampler, the quantization noise of the ADC, etc, contributes almost half of the integrated jitter, while the other half is dominated by



(a) Int-N



(b) Frac-N

Figure 5.17: Measured DPLL PN at (a) integer-N and (b) fractional-N channels around 4.8 GHz.

the DCO. This results in a DPLL bandwidth setting around the optimal in terms of the jitter performance [14].

The bandwidth of the DPLL is also varied and the measurement results

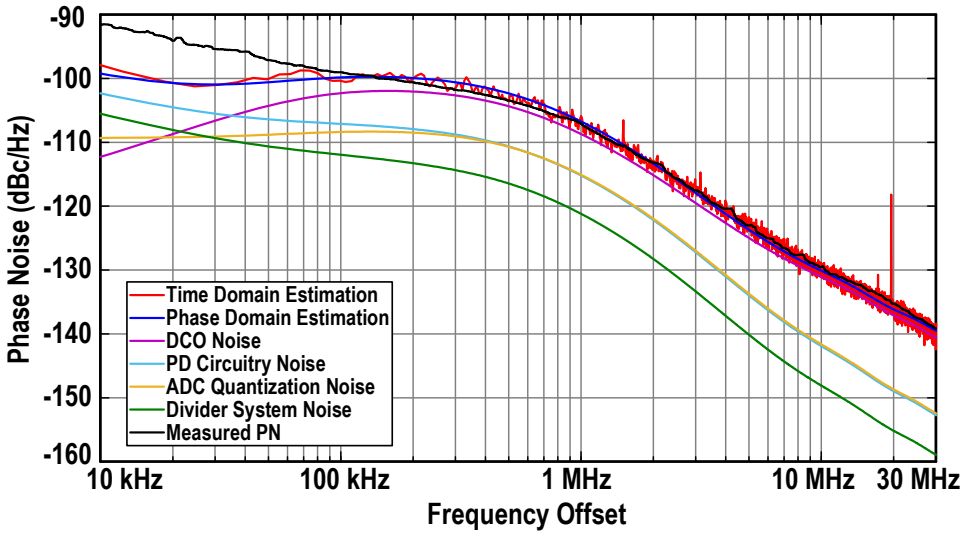


Figure 5.18: Phase and time domain estimation of DPLL PN with a comparison to the measured result at around 4.8015 GHz.

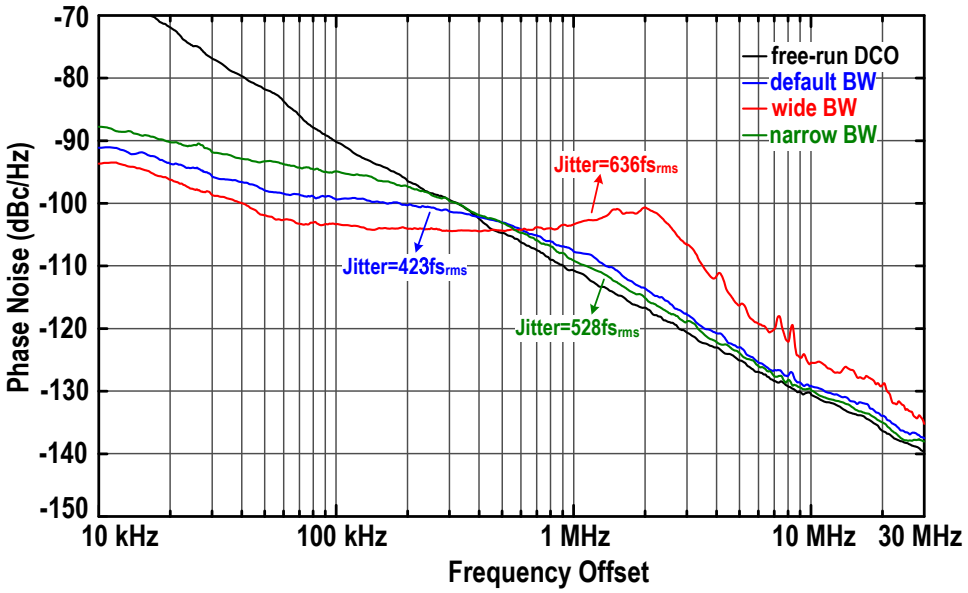


Figure 5.19: Measured DPLL phase noise for different bandwidth settings at around 4.8015 GHz.

are shown in Fig. 5.19. The phase noise of the free running oscillator is also added for comparison. For a wide bandwidth setting of ~ 3 MHz, the in-band PN is reduced to -104 dBc and is dominated by the thermal noise of the phase detection circuitry and the quantization noise of the SAR ADC. In contrast, under a narrow bandwidth setting (~ 0.25 MHz), the DCO noise is not adequately suppressed at low frequency offsets and the in-band phase noise is degraded by about 4 dB. However, the phase noise at higher frequency offsets become closer to that of the free-running oscillator due to the better filtering of the PD noise. At the default bandwidth setting of

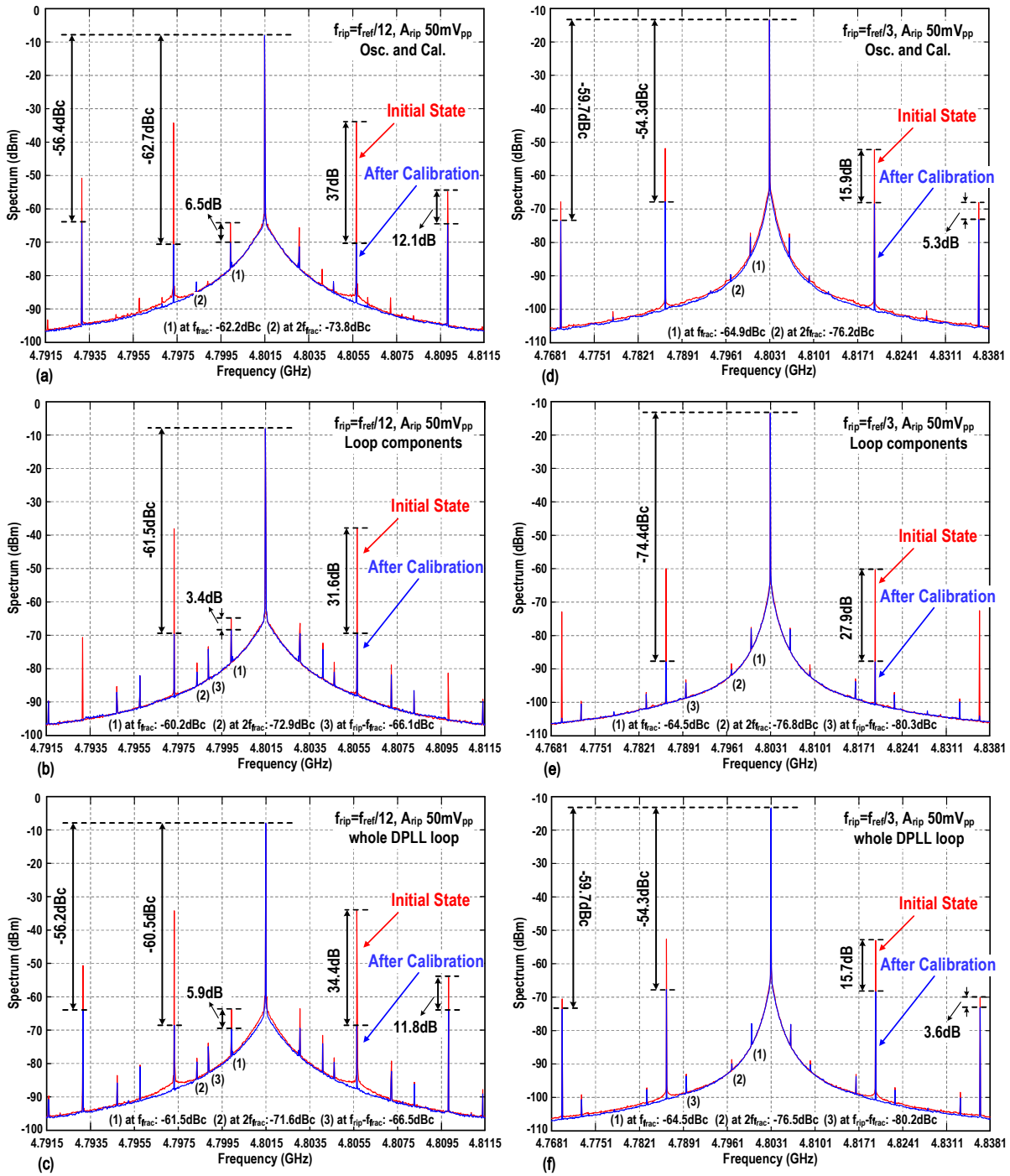


Figure 5.20: Measured DPLL spectra when the 50 $\mathrm{mV_{pp}}$ $f_{\mathrm{ref}}/12$ ($f_{\mathrm{ref}}/3$) supply ripple is applied to (a) (d) the oscillator and its calibration loop, (b) (e) the loop components, and (c) (f) the whole DPLL.

around 500 kHz, an optimum integrated jitter of 423 fs is achieved, which increases to 636 fs and 528 fs for the wide and narrow bandwidth setting, respectively.

The DPLL output spectrum with the default bandwidth setting is measured in three different scenarios. In Fig. 5.20 (a), a 50 $\mathrm{mV_{pp}}$ 4.167 MHz

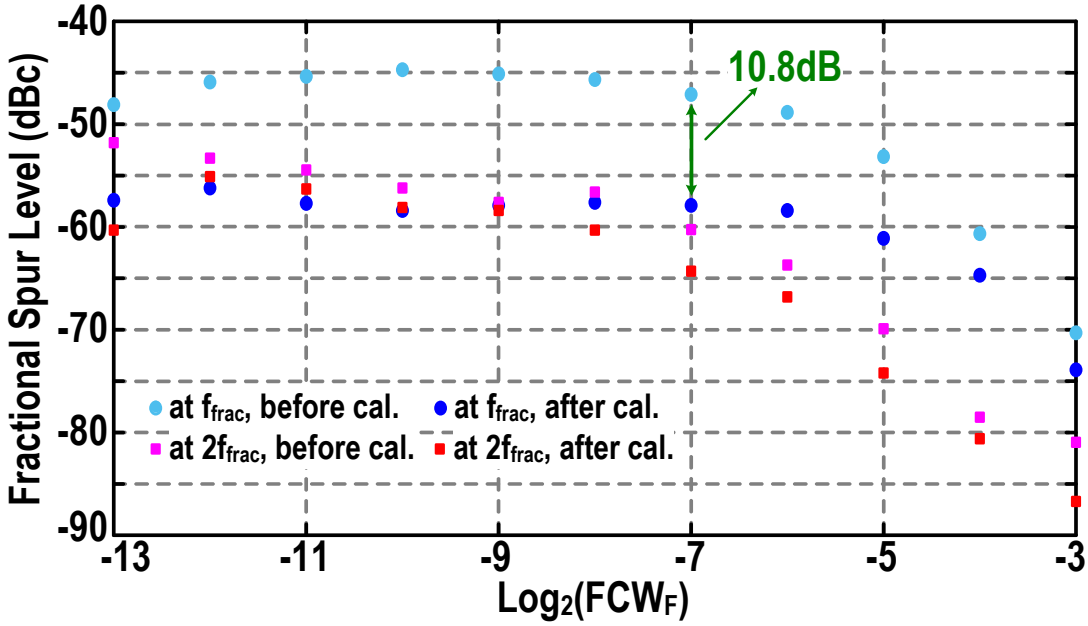


Figure 5.21: Measured fractional spur levels versus fractional FCW ($\mathrm{FCW_F}$).

(i.e., $f_{\mathrm{ref}}/12$) ripple is applied to the oscillator and its calibration loop. The spur at f_{rip} due to the oscillator supply pushing is suppressed by 37 dB and reaches −62.7 dBc after the corresponding calibration is performed. The same ripple is then applied to the DPLL components except for the oscillator. As shown in Fig. 5.20 (b), the spur at f_{rip} due to the delay variations of the loop components is −61.5 dBc, improving 31.6 dB thanks to the ripple pattern estimation and cancellation technique. Finally, the same ripple is applied to the entire DPLL. As shown in Fig. 5.20 (c), when all calibration loops are enabled, the f_{rip} spur is reduced by 34.4 dB and reaches −60.5 dBc. In all three cases, the spur at f_{frac} due to the residue mismatch of the resampling block is <−60 dBc after the mismatch calibration, while the spur at $2 \times f_{\mathrm{frac}}$ originating from the nonlinearity of PD remains <−71.6 dBc. Extra spurs at $f_{\mathrm{rip}} \pm f_{\mathrm{frac}}$ and $2f_{\mathrm{rip}} \pm f_{\mathrm{frac}}$ with levels <−66 dBc could also be observed in Fig. 5.20 (b) and (c). These spurs come from the undesired coupling between the supply of PD and the DCO output, both routed on the top metal layers with only ∼10 μm spacing, and could also be observed when the oscillator is left free-running. In contrast, these spurs disappear when no ripple is applied to the PD supply. To suppress these spurs, the distance between the PD and the oscillator should be increased in future designs.

Similar measurements are performed when the frequency of the 50 $\mathrm{mV_{pp}}$

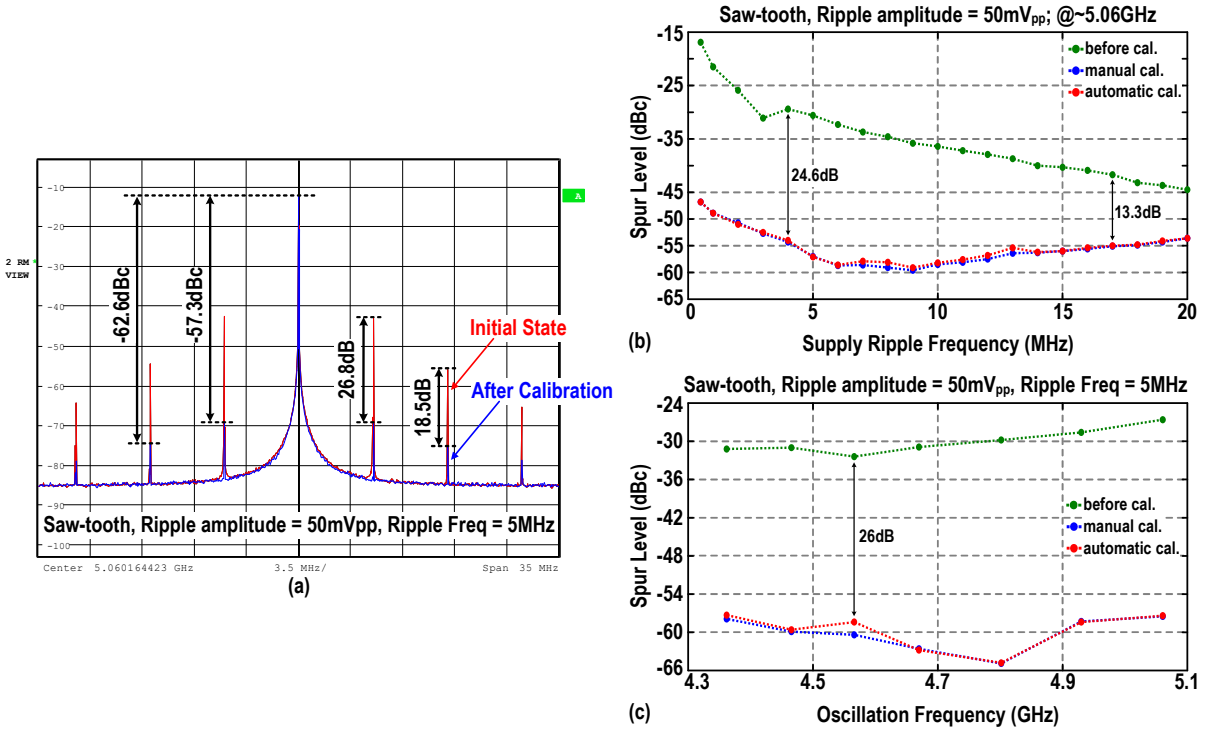


Figure 5.22: Measurements of the free-running DCO under sawtooth ripples: (a) spectrum before and after the automatic calibration in face of a 50 $\mathrm{mV_{pp}}$ 5 MHz ripple; (b) worst-case spur levels across the ripple frequency, and (c) across the oscillation frequency for both the manual and automatic calibrations.

ripple is increased to $f_{\mathrm{ref}}/3$ (i.e., 16.67 MHz). As can be gathered from Fig. 5.20 (d)–(f), the f_{rip} spur is dominated by the oscillator supply pushing since the spur level due to the delay variations of the DPLL components is further suppressed by the low-pass transfer function of the loop. Fig. 5.21 shows the measured spur level at f_{frac} and $2f_{\mathrm{frac}}$ across the fractional frequency, indicating that the mismatch calibration improves the in-band (out-of-band) f_{frac} spur level by about 9 ∼14 dB (3 ∼7 dB). Furthermore, considering both f_{frac} and $2f_{\mathrm{frac}}$ spurs, a worst-case spur level of −55 dBc is achieved after the calibration.

The oscillator and the DPLL are also measured under sawtooth ripples to better mimic the actual scenario of being directly powered by a switched-mode DC-DC converter. Fig. 5.22 shows the measured performance of the free-running DCO when a 50 $\mathrm{mV_{pp}}$ sawtooth ripple is applied to both the oscillator core and the calibration loop. Fig. 5.22 (a) compares the oscillator spectrum before and after the calibration. At a 5 MHz ripple, the spur at the fundamental offset is reduced by 26.8 dB and reaches −57.3 dBc after the calibration. Fig. 5.22 (b) plots the measured spur levels over the

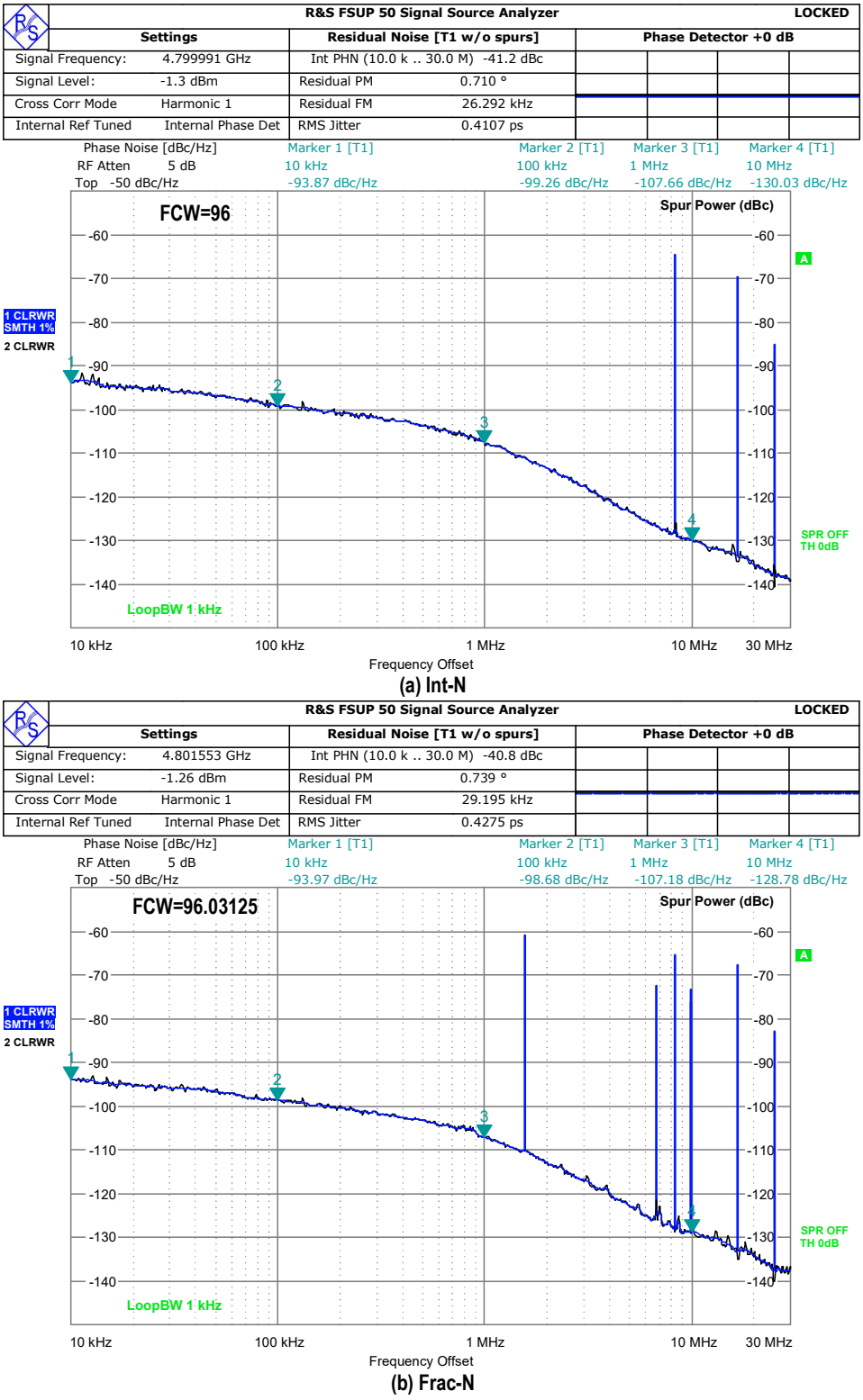


Figure 5.23: Measured DPLL PN at (a) the integer-N and (b) fractional-N channel around 4.8 GHz under the sawtooth ripple.

ripple frequency. In the entire span of 0.5-to-20 MHz, the highest spur is ≤ -46.8 dBc. The observed improvement after the automatic calibration is 13.3 to 24.6 dB for 4 $\sim$17 MHz ripples. The entire oscillator TR was also

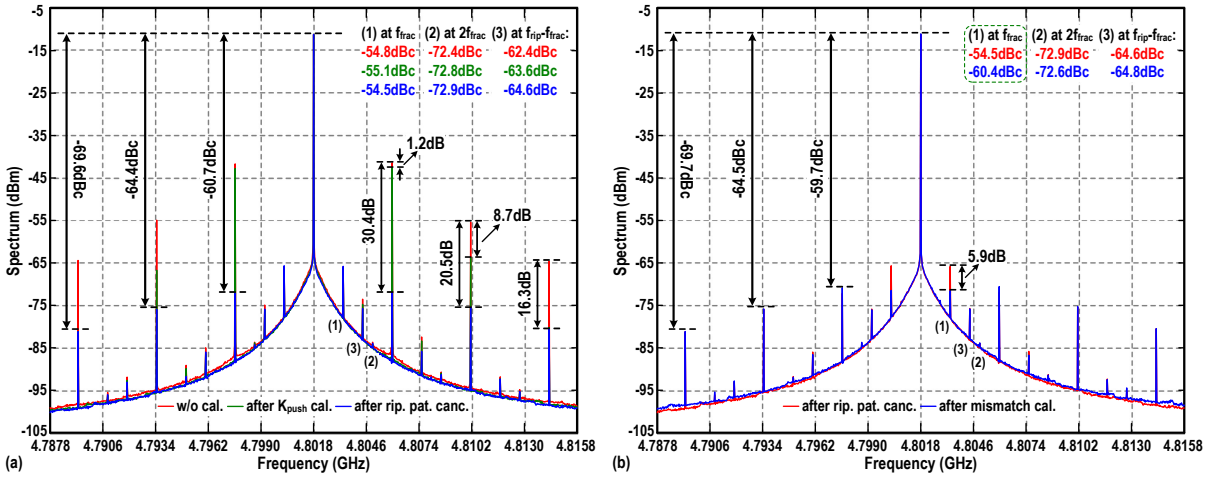


Figure 5.24: Measured DPLL spectrum under a $50\,\mathrm{mV_{pp}}$ $f_{\mathrm{ref}}/12$ sawtooth ripple at the initial state [red curve in (a)], and after enabling the oscillator supply pushing calibration [green curve in (a)], after enabling the ripple pattern estimation and cancellation [blue curve in (a) / red curve in (b)], and after enabling the divider resampler mismatch calibration [blue curve in (b)] sequentially.

scanned and the result is shown in Fig. 5.22 (c). The worst-case spur level is $\leq -57.3\,\mathrm{dBc}$ under a $50\,\mathrm{mV_{pp}}$ 5 MHz sawtooth ripple, while the calibrated value follows the optimum one in most cases. The improvement after the calibration is $> 26\,\mathrm{dB}$ across the TR.

Fig. 5.23 shows the measured PN and spurious performance for both the integer-N and fractional-N operation around 4.8 GHz under the $50\,\mathrm{mV_{pp}}$ sawtooth ripple when $f_{\mathrm{rip}} = f_{\mathrm{ref}}/6$. The integrated jitter is 428 fs for the fractional-N operation, while it is 411 fs for the integer-N operation. As expected, the PN performance of the DPLL under sawtooth ripples remains similar to that measured with sinusoidal ripples.

The measured output spectrum of the DPLL under a $50\,\mathrm{mV_{pp}}$ 4.167 MHz (i.e., $f_{\mathrm{ref}}/12$) sawtooth ripple is shown in Fig. 5.24. Compared to the initial state where no calibration is performed, the spurs at f_{rip} and its harmonics induced by the ripple on the oscillator supply are suppressed after the supply pushing calibration, and the levels of these spurs are now mainly dominated by the variation of the output delay of loop components [see Fig. 5.24 (a)]. When the ripple pattern estimation and cancellation algorithm is enabled, the spectrum in Fig. 5.24 (a) shows that the spur at f_{rip} is suppressed significantly, while the spurs at its harmonics are also lowered. In contrast, the spur level at f_{frac} remains unaffected during these calibrations. To suppress this spur, the mismatch calibration is then enabled, and the

spur level at f_{frac} is reduced from $-54.5\,\text{dBc}$ to $-60.4\,\text{dBc}$ as shown in Fig. 5.24 (b). During the mismatch calibration, the levels of spurs at f_{rip} and its harmonics remain unchanged. The spur level at $2f_{\text{frac}}$ due to the PD nonlinearity also remains at $\sim -72.6\,\text{dBc}$ during these calibrations.

Table 5.1 summarizes the performance of the proposed DPLL and compares it with state-of-the-art designs. We first compare the performance of the prototype under supply ripple to state-of-the-art low-power (<5 mW) fractional-N PLLs under a *clean* supply [25, 108, 111, 112]. The normalized FoM (FoM_R, defined at the bottom of Table 5.1) is $\sim$3 dB worse compared to [108] and [111], while it is $\sim$5 dB worse compared to [112] implemented in SOI technology. This is partly due to the fact that no ultra-thick top metal layer is available in the technology used, limiting the Q-factor of the DCO. Moreover, in order not to offset the advantages of removing the LDOs, no external capacitor is used to filter out the noise of the biasing current in the slope generator and current DAC; this however increases the contribution of PD's circuit noise to the in-band PN by about 40% as per simulations. In contrast, for example, the design in [112] uses several *external* tunable reference voltages to charge/discharge the capacitors in its sampling PD and the following CDAC, which is difficult to integrate on-chip. Next, our prototype is compared to designs with 'dirty' supplies [44, 60, 66, 67, 96]. The f_{rip} spur of the prototype is the lowest under a large $50\,\text{mV}_{\text{pp}}$ supply ripple. Meanwhile, to the best of our knowledge, the proposed design is the first fractional-N PLL that can successfully operate under the supply ripples with acceptable performance.

5.5 Conclusion

This chapter demonstrates a fractional-N DPLL that is insensitive to supply ripples, thereby enabling a direct connection to a DC-DC converter. To tolerate the supply ripple, the feed-forward ripple replication and cancellation technique with an improved calibration loop is adopted to reduce the supply pushing of the LC oscillator. The output of the MMDIV, which is driven by a second-order $\Delta\Sigma$ modulator, is resampled by both edges of the oscillator output to halve the input range of the following slope generator. This facilitates a linear and supply-insensitive conversion from

time to voltage domain by the slope generator. Meanwhile, a current DAC compensates the excursion due to the fractional-N operation in order to limit the dynamic range of the SAR ADC that quantizes the phase error. A ripple pattern estimation and cancellation algorithm is integrated to cancel the phase error induced by the delay variations of the loop component under the supply ripple from the ADC output so that it would not modulate the oscillator. Prototyped in 40-nm CMOS, the DPLL exhibits 428 fs rms jitter and <-55 dBc fractional spur, while the ripple spur is also <-54 dBc.

Table 5.1: Performance Summary and Comparison with Prior Art

		This Work			TCAS-II'12 [96]	TCAS-I'14 [44]	ESSCIRC'16 [66]	VLSI'17 [67]			ISSCC'16 [60]	JSSC'18 [108]	JSSC'21 [112]	TCAS-I'19 [111]	JSSC'21 [25]
Tech. (nm)		40 (w/o UTM)			90	65	65	65			40	65	45 (PDSOI)	130	130
PLL Type		Digital Frac-N			Digital Int-N	Digital Int-N	Digital Int-N	Digital Int-N			Digital Int-N	Digital Frac-N	Analog Frac-N	Analog Frac-N	Analog Frac-N
Osc. Type		LC			Ring	LC	LC	Ring			Ring	LC	LC	LC	LC
Ripple applied to		whole loop			whole loop	GRO PD	Osc.	Osc.			Osc.	-	-	-	-
Cancellation Tech.		SAR ADC based PD Ripple pattern cal. Feedforward K_{push} cal.			Cancel osc. supply noise through oppositve sensitivities	GRO based supply noise monitor	FCW compensation	Noise suppression loop			Two constant-Gm biasing	-	-	-	-
V_{DD} (V)		1.0			0.6	1.0	1.0	1.0			1.1	1.0/0.8	1.0	1.2	1.2
f_{ref} (MHz)		50			50	26	30	50			200	26×2	100	50	50
f_{out} (GHz)		4.47-5.14			0.8	1.4-1.8	3-5	3.2			3.2	2.0-2.8	7.7-9.1	1.9-2.3	1.8-2.3
PN (dBc/Hz)	**In-band**	-99.1 (@100kHz)			NA	-74## (@50kHz)	-103† (@100kHz)	-86.3 (@10kHz)			-105† (@3MHz)	-103.8 (@100kHz)	-120### (@1MHz)	-110.3 (@200kHz)	-109.2 (@200kHz)
	Out-band	-117.5 (@3MHz)			NA	-98## (@1MHz)	-120† (@3MHz)	-108 (@10MHz)			-119† (@100MHz)	-128.0 (@10MHz)	-135### (@10MHz)	-127.9 (@2MHz)	-132† (@10MHz)
PN_{norm}* (dBc/Hz)	**In-band**	-99.1 (@100kHz)			NA	-58.8## (@50kHz)	-100.4† (@100kHz)	-82.8 (@10kHz)			-101.5† (@3MHz)	-97.9 (@100kHz)	-118.3### (@1MHz)	-103.6 (@200kHz)	-102.0 (@200kHz)
	Out-band	-117.5 (@3MHz)			NA	-82.8## (@1MHz)	-117.4† (@3MHz)	-104.5 (@10MHz)			-115.5† (@100MHz)	-122.2 (@10MHz)	-133.3### (@10MHz)	-121.2 (@2MHz)	-124.9† (@10MHz)
Integrated Jitter (ps)		0.428			34.1#	NA	0.52	7.8			3.85	0.53	0.135	0.291	0.414
Frac. Spur (dBc)		<-55			-	-	-	-			-	<-56	<-55####	<-48.6	-57
Frac. $Spur_{norm}$ ** **(dBc)**		<-55			-	-	-	-			-	<-50.1	<-47.9	<-41.9	-49.9
Ripple Amplitude		50mV_{pp}			50mV_{pp}	200mV_{pp}	NA	20mV_{pp}			50mV_{pp}	-	-	-	-
f_{rip} (MHz)		f_{ref}/12	f_{ref}/6	f_{ref}/3	1-100	1.0	0.5-10	0.5	2.5	20	0.1	-	-	-	-
Spur @ f_{rip} (dBc)	**sinewave**	-60.5	-61.6	-54.3	NA	-49##	NA	-63	-45.5	-59.2	-28†	-	-	-	-
	saw-tooth	-59.7	-64.4	-57.6	NA	NA	<-50	NA	NA	NA	NA	-	-	-	-
Power (mW)		3.25			0.66	11.3	21.3	2.73			2.915	0.98	4.5	3.2	2.8
FoM_R* (dB)**		-242.3			-211.1	NA	-234.6	-217.8			-217.6	-245.4	-247.8	-245.7	-243.2
Area (mm^2)		0.39			0.0221	0.65	0.63	0.047			0.0216	0.23	0.1‡	0.45	0.4

*Phase noise normalized to 4.8GHz, $PN_{norm}=PN+20\times\log_{10}(4.8GHz/f_{out})$ **Spur level normalized to 4.8GHz, $Spur_{norm}=Spur+20\times\log_{10}(4.8GHz/f_{out})$ ***$FoM_R=10\times\log_{10}((\sigma_{rms})^2\times Power/1mW\times(f_{ref}/50MHz))$ [126]

#Measured at 280MHz output (f_{ref}=17.5MHz) ##Measured after divide by 2 at 832MHz †Estimated from measurement result ‡Excluding the integrated loop filter

###Estimated from measurement after divide by 2 at ~3.95GHz ####Measured after divide by 4 at ~2.12558GHz

Chapter

6

Conclusion

This dissertation mainly focuses on the analysis and design of a fractional-N digitally intensive PLL that is practically insensitive to supply ripples, enabling its direct operation under the output of a switching DC-DC converter. In this concluding chapter, an overview of the thesis outcome is presented, while the main findings and original contributions are summarized. Based on these, some suggestions and recommendations for future improvements are also provided at the end of this chapter.

6.1 Thesis Outcomes

The use of DC-DC converters followed by low dropout (LDO) linear regulators has long been the 'standard' way of powering the system-on-chip (SoC). The voltage output levels of the energy sources are transformed to the nominal supply voltage of the system with sufficiently high efficiency through the converters. For full system integration and system miniaturization, switched-capacitor DC-DC converters are favored while the switching frequencies would be increased to several or tens of MHz. Nevertheless, as described in Chapter 2, when directly supplying the phase-locked loops (PLLs), the output ripples of converters could severely degrade the PLL's performance by modulating the frequency of the oscillator and the output delay of the loop components. It is also shown that the ripple frequency could intermodulate with the fractional frequency synthesized through the supply sensitivity of phase detectors. Therefore, LDOs are used in cascade with the converters to suppress the ripples in the aforementioned arrangement.

A detailed analysis on the power efficiency of the LDOs powering the PLLs is carried out in Chapter 3. The 'capacitor-less' topology with the dominant pole located at the output of its error amplifier (EA) is selected to avoid the use of large load capacitors, and two separate LDOs are needed for better isolation between the sensitive oscillator and the phase detection blocks. The efficiency of the LDO is mainly limited by both its dropout voltage (V_{DO}) and the quiescent current flowing through the EA (I_{EA}) and the feedback resistors (I_{F}). Calculations show that V_{DO}, established by the power supply rejection performance of the LDO, would consume $\sim$100 mV extra voltage headroom in the 40-nm CMOS technology used here, and degrades the system efficiency by a factor of $\sim$0.9$\times$ at 1 V supply. The level of I_{EA} and I_{F} are mainly determined by the figure-of-merit of the oscillator ($\mathrm{FoM_{osc}}$) and loop components ($\mathrm{FoM_{loop}}$) for the corresponding LDOs, respectively. For the LDO powering the oscillator, the efficiency could further drop by a factor of worse than $\sim$0.7–0.8$\times$ due to the quiescent current. Based on this analysis, it deems beneficial to power the PLL directly with the DC-DC converter. At the end of this chapter, some further discussion on different powering scenarios for SoCs

is also provided.

To enable a direct connection to the converter output, a fractional-N digitally intensive PLL (DPLL) architecture is then developed. In Chapter 4, the supply pushing of the LC oscillator, which is the most supply sensitive block in the PLL, is tackled first. The proposed feed-forward ripple replication and cancellation technique replicates the supply ripple to the gate of the tail current transistor of the oscillator with a proper gain to stabilize the oscillator tail current and reduce its supply pushing. An on-chip calibration loop employing a conventional peak detector and an inverter chain based amplifier is also implemented to find the optimum gain between the replica and the ripple. The prototyped $\sim$5 GHz LC oscillator in 40-nm CMOS achieves a supply pushing of $<$1 MHz/V for supply ripples up to 12 MHz, leading to a $>10\times$ improvement over state-of-the-art oscillator designs at low ripple frequencies. The proposed technique is further verified through powering the oscillator directly with a three-stage recursive switched-capacitor converter. Under the 1.3–2.2 V converter input, a high system peak efficiency of 85% is achieved while the spur level remains below -65 dBc. The inherent phase noise of the oscillator is also preserved due to the low output noise of the converter.

The entire fractional-N DPLL architecture is elaborated and verified in Chapter 5. The feed-forward ripple cancellation technique proposed above is adopted to suppress the oscillator supply pushing, while the design of its calibration loop is further modified to tolerate supply ripples. The intermodulation between the ripple frequency and the fractional frequency is alleviated using the proposed voltage domain phase detector with an improved supply insensitivity. SAR ADC is adopted in the phase detection circuitry to digitize the phase error due to its energy efficiency as well as supply immunity. A low-power ripple pattern estimation and cancellation algorithm is also inserted at the ADC output to extract and remove the pattern at ripple frequency. Consequently, the effect of the supply-induced output delay perturbations of loop components is cancelled in digital domain before modulating the oscillator. Exploiting these techniques, the DPLL prototype, also demonstrated in 40-nm CMOS, exhibits $\sim$428 fs rms jitter and <-55 dBc fractional spur under the 50 $\mathrm{mV_{pp}}$ ripple. Meanwhile, the measured <-54 dBc spur at the ripple frequency is also the lowest

when compared to other PLL designs with techniques to suppress the supply sensitivity of the whole loop or certain building blocks.

6.2 Main Contributions

The main findings and original scientific contributions made during the development of the thesis are summarized as follows:

- The effects of supply ripple on the spectral purity of a PLL are comprehensively analyzed and quantified (Chapter 2).
- The power efficiency of the integrated LDOs powering the oscillator and other loop components of the PLL are derived (Chapter 3).
- Four scenarios of the power management strategy for a real and complex system-on-chip are discussed and compared (Chapter 3).
- A feed-forward supply ripple replication and cancellation technique that suppress the supply pushing of the LC oscillator is proposed and verified (Chapter 4 and 5).
- A phase detection circuitry based on cascading a current-mode slope generator with the output of a current DAC is proposed for improved supply immunity, while a low-power digital algorithm inserted at the SAR ADC's output extracts and removes the pattern due to the supply-induced delay variation of loop components (Chapter 5).
- A fractional-N digitally intensive PLL that is insensitive to supply ripples is designed and implemented in the sub-micron CMOS technology (Chapter 5).

6.3 Suggestions for Future Improvements

This dissertation demonstrates a fractional-N digitally intensive PLL architecture capable of maintaining its performance under supply ripples, facilitating the direct operation of the system under the output of DC-DC converters. The results reveal some aspects for further improvements:

- The analysis in Chapter 3 offers insights into the efficiency limitations of the LDOs powering the PLL. However, it only includes parameters that directly affect the LDO efficiency. Considering a practical LDO

design, it would be beneficial to further analysis the impact of other performance metrics on the LDO efficiency.

- As discussed in Chapter 4, the nonlinearity of the ripple replication block (RRB) could lead to spurs at the second ripple harmonic or the intermodulation frequencies of the tones in the ripple waveform, while its limited bandwidth results in reduced spur level suppression at high ripple frequencies. Therefore, it is worthwhile to research techniques to improve the linearity of RRB and to extend its bandwidth with small power penalty. For example, the feedback technique combined with phase shift compensation methods could be utilized to linearize RRB and achieve higher bandwidth, while the calibration loop could be modified to adjust the feedback ratio which, in turn, modifies the gain of the replica. For a ripple waveform that already contains higher harmonics, i.e., sawtooth ripples, another interesting topic would be to research the possibility of adjusting the amplitude and phase of the harmonic terms generated by the nonlinearity of RRB, so that they could further cancel with the corresponding harmonic components in the ripple waveform, leading to better spur performance.

- AC-coupling is employed in the RRB calibration loop (please refer to Section 4.3.2 and 5.3.4) to accommodate the DC levels of different stages, limiting the lowest ripple frequency that the loop can deal with. To remove this limitation, DC-coupling should be adopted. At the same time, for a reliable operation of the calibration loop, extra techniques/calibrations are required to guarantee the proper biasing conditions of each stage under PVT variations.

- The fractional spur of the DPLL is mainly limited by the linearity of the slope generator, as obtained from simulations. Extra techniques could be explored to further boost the output resistance of the current source in the slope generator for an improved linearity performance. Otherwise, it is also interesting to research on replacing the $\Delta\Sigma$ modulation with other coding methods that can better resist the effect of nonlinearity [33, 127, 128].

Bibliography

[1] W. Zhao and Y. Cao, "New generation of predictive technology model for sub-45 nm early design exploration," *IEEE Transactions on Electron Devices*, vol. 53, no. 11, pp. 2816–2823, Nov 2006.

[2] M. White and Y. Chen, "Scaled CMOS technology reliability users guide," Jet Propulsion Laboratory, Pasadena, CA, USA, Tech. Rep., March 2008. [Online]. Available: https://nepp.nasa.gov/files/16361/08_102_4%20new%20del_White.pdf

[3] S. Bandyopadhyay and A. P. Chandrakasan, "Platform architecture for solar, thermal, and vibration energy combining with MPPT and single inductor," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 9, pp. 2199–2215, Sep. 2012.

[4] M. Babaie, F.-W. Kuo, H.-N. R. Chen, L.-C. Cho, C.-P. Jou, F.-L. Hsueh, M. Shahmohammadi, and R. B. Staszewski, "A fully integrated bluetooth low-energy transmitter in 28 nm CMOS with 36% system efficiency at 3 dBm," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 7, pp. 1547–1565, July 2016.

[5] S. M. Demir, F. Al-Turjman, and A. Muhtaroğlu, "Energy scavenging methods for WBAN applications: A review," *IEEE Sensors Journal*, vol. 18, no. 16, pp. 6477–6488, Aug 2018.

[6] S. J. Yun, J. Lee, Y. C. Im, and Y. S. Kim, "A digital LDO regulator with a self-clocking burst logic for ultralow power applications," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 27, no. 10, pp. 2237–2245, Oct 2019.

[7] M. Huang, Y. Lu, S.-W. Sin, U. Seng-Pan, and R. P. Martins, "A fully integrated digital LDO with coarse–fine-tuning and burst-mode operation," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 63, no. 7, pp. 683–687, July 2016.

[8] V. Kursun and E. G. Friedman, *Multi-voltage CMOS Circuit Design*, 1st ed. Wiley, 2006.

[9] W.-C. Chen, S.-Y. Ping, T.-C. Huang, Y.-H. Lee, K.-H. Chen, and C.-L. Wey, "A switchable digital–analog low-dropout regulator for analog dynamic voltage scaling technique," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 3, pp. 740–750, March 2014.

[10] S. P. Singh, "Simple power-rail sequencing solutions for complex multi-rail systems," Integrated Power Group, Texas Instruments, Tech. Rep., July 2016. [Online]. Available: https://www.ti.com/lit/wp/slyy101/slyy101.pdf?ts=1632771132571&ref_url=https%253A%252F%252Fwww.google.com%252F

[11] L. Tellez and S. M. Nolan, "Analog and power management trends in ASIC and SoC designs," Vidatronic, Bryan, Texas, USA, Tech. Rep., June 2020. [Online]. Available: https://www.vidatronic.com/wp-content/uploads/2020/06/Analog-and-Power-Management-Trends-in-ASIC-and-SoC-Design.pdf

[12] T. V. Breussegem and M. Steyaert, *CMOS Integrated Capacitive DC-DC Converters*, 1st ed. Springer, 2013.

[13] S. R. Sanders, E. Alon, H.-P. Le, M. D. Seeman, M. John, and V. W. Ng, "The road to fully integrated DC–DC conversion via the switched-capacitor approach," *IEEE Transactions on Power Electronics*, vol. 28, no. 9, pp. 4146–4155, Sep. 2013.

[14] X. Gao, E. A. M. Klumperink, P. F. J. Geraedts, and B. Nauta, "Jitter analysis and a benchmarking figure-of-merit for phase-locked loops," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 56, no. 2, pp. 117–121, Feb 2009.

[15] F. M. Gardner, *Phaselock Techniques*, 3rd ed. Wiley, 2005.

[16] C. Vaucher, "An adaptive PLL tuning system architecture combining high spectral purity and fast settling time," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 4, pp. 490–502, April 2000.

[17] S. Pellerano, S. Levantino, C. Samori, and A. Lacaita, "A 13.5-mW 5-GHz frequency synthesizer with dynamic-logic frequency divider," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 2, pp. 378–383, Feb 2004.

[18] T.-H. Lin, C.-L. Ti, and Y.-H. Liu, "Dynamic current-matching charge pump and gated-offset linearization technique for delta-sigma fractional-N PLLs," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 5, pp. 877–885, May 2009.

[19] X. Gao, E. A. M. Klumperink, M. Bohsali, and B. Nauta, "A low noise sub-sampling PLL in which divider noise is eliminated and PD/CP noise is not multiplied by N^2," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3253–3263, Dec 2009.

[20] X. Gao, E. A. M. Klumperink, G. Socci, M. Bohsali, and B. Nauta, "Spur reduction techniques for phase-locked loops exploiting a sub-sampling phase detector," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 9, pp. 1809–1821, Sep. 2010.

[21] X. Gao, E. Klumperink, G. Socci, M. Bohsali, and B. Nauta, "A 2.2GHz sub-sampling PLL with 0.16ps$_{\text{rms}}$ jitter and -125dBc/Hz in-band phase noise at 700μW loop-components power," in *2010 Symposium on VLSI Circuits*, June 2010, pp. 139–140.

[22] D. Turker, A. Bekele, P. Upadhyaya, B. Verbruggen, Y. Cao, S. Ma, C. Erdmann, B. Farley, Y. Frans, and K. Chang, "A 7.4-to-14GHz PLL with 54fs$_{\text{rms}}$ jitter in 16nm FinFET for integrated RF-data-converter SoCs," in *2018 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb 2018, pp. 378–380.

[23] D.-G. Lee and P. P. Mercier, "A sub-mW 2.4-GHz active-mixer-adopted sub-sampling PLL achieving an FoM of -256 dB," *IEEE*

Journal of Solid-State Circuits, vol. 55, no. 6, pp. 1542–1552, June 2020.

[24] Y.-L. Hsueh, L.-C. Cho, C.-H. Shen, Y.-C. Tsai, T.-C. Chueh, T.-Y. Chang, J.-L. Hsu, and J.-H. C. Zhan, "A 0.29mm^2 frequency synthesizer in 40nm CMOS with 0.19ps$_{\text{rms}}$ jitter and <-100dBc reference spur for 802.11ac," in *2014 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb 2014, pp. 472–473.

[25] H. Su, J. Tao, S. D. Balon, and C.-H. Heng, "A 2.3 GHz 2.8 mW sampling $\Delta\Sigma$ PLL achieving -110 dBc/Hz in-band phase noise and 500 MHz FMCW chirp," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 11, pp. 3458–3469, Nov 2021.

[26] L. Vercesi, L. Fanori, F. De Bernardinis, A. Liscidini, and R. Castello, "A dither-less all digital PLL for cellular transmitters," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 8, pp. 1908–1920, Aug 2012.

[27] D. Liao, H. Wang, F. F. Dai, Y. Xu, R. Berenguer, and S. M. Hermoso, "An 802.11a/b/g/n digital fractional-N PLL with automatic TDC linearity calibration for spur cancellation," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 5, pp. 1210–1220, May 2017.

[28] A. Elkholy, T. Anand, W.-S. Choi, A. Elshazly, and P. K. Hanumolu, "A 3.7 mW low-noise wide-bandwidth 4.5 GHz digital fractional-N PLL using time amplifier-based TDC," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 4, pp. 867–881, April 2015.

[29] Y.-H. Liu, J. Van Den Heuvel, T. Kuramochi, B. Busze, P. Mateman, V. K. Chillara, B. Wang, R. B. Staszewski, and K. Philips, "An ultra-low power 1.7-2.7 GHz fractional-N sub-sampling digital frequency synthesizer and modulator for IoT applications in 40 nm CMOS," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 5, pp. 1094–1105, May 2017.

[30] Y. He, Y.-H. Liu, T. Kuramochi, J. van den Heuvel, B. Busze, N. Markulic, C. Bachmann, and K. Philips, "A 673μW 1.8-to-2.5GHz dividerless fractional-N digital PLL with an inherent frequency-capture capability and a phase-dithering spur mitigation for IoT

applications," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb 2017, pp. 420–421.

[31] D. Cherniak, L. Grimaldi, L. Bertulessi, R. Nonis, C. Samori, and S. Levantino, "A 23-GHz low-phase-noise digital bang–bang PLL for fast triangular and sawtooth chirp modulation," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 12, pp. 3565–3575, Dec 2018.

[32] A. Santiccioli, M. Mercandelli, L. Bertulessi, A. Parisi, D. Cherniak, A. L. Lacaita, C. Samori, and S. Levantino, "A 66-fs-rms jitter 12.8-to-15.2-GHz fractional-N bang–bang PLL with digital frequency-error recovery for fast locking," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 12, pp. 3349–3361, Dec 2020.

[33] H. Park, C. Hwang, T. Seong, Y. Lee, and J. Choi, "A 365 $\mathrm{fs_{rms}}$-jitter and -63 dBc-fractional spur 5.3 GHz-ring-DCO-based fractional-N DPLL using a DTC second/third-order nonlinearity cancelation and a probability-density-shaping $\Delta\Sigma$M," in *2021 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 64, Feb 2021, pp. 442–444.

[34] R. B. Staszewski and P. T. Balsara, *All-Digital Frequency Synthesizer in Deep-Submicron CMOS*, 1st ed. Wiley, 2006.

[35] D. Murphy, H. Darabi, and H. Wu, "Implicit common-mode resonance in LC oscillators," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 3, pp. 812–821, March 2017.

[36] P. Lu, A. Liscidini, and P. Andreani, "A 3.6 mW, 90 nm CMOS gated-Vernier time-to-digital converter with an equivalent resolution of 3.2 ps," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 7, pp. 1626–1635, July 2012.

[37] P. Lu, Y. Wu, and P. Andreani, "A 2.2-ps two-dimensional gated-Vernier time-to-digital converter with digital calibration," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 63, no. 11, pp. 1019–1023, Nov 2016.

[38] M. Zanuso, P. Madoglio, S. Levantino, C. Samori, and A. L. Lacaita, "Time-to-digital converter for frequency synthesis based on a digital bang-bang DLL," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 3, pp. 548–555, March 2010.

[39] J. Zhuang and R. B. Staszewski, "A low-power all-digital PLL architecture based on phase prediction," in *2012 19th IEEE International Conference on Electronics, Circuits, and Systems (ICECS 2012)*, Dec 2012, pp. 797–800.

[40] S. Levantino, G. Marzin, and C. Samori, "An adaptive pre-distortion technique to mitigate the DTC nonlinearity in digital PLLs," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 8, pp. 1762–1772, Aug 2014.

[41] W.-S. Chang and T.-C. Lee, "A 5 GHz fractional-N ADC-based digital phase-locked loops with -243.8 dB FOM," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 11, pp. 1845–1853, Nov 2016.

[42] A. Urso, Y. Chen, J. F. Dijkhuis, Y.-H. Liu, M. Babaie, and W. A. Serdijn, "Analysis and design of power supply circuits for RF oscillators," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 12, pp. 4233–4246, Dec 2020.

[43] J. Prummel, M. Papamichail, J. Willms, R. Todi, W. Aartsen, W. Kruiskamp, J. Haanstra, E. Opbroek, S. Rievers, P. Seesink *et al.*, "A 10 mW Bluetooth Low-Energy transceiver with on-chip matching," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 12, pp. 3077–3088, Dec 2015.

[44] Y. Liu, Y. Han, W. Rhee, T.-Y. Oh, and Z. Wang, "A PSRR enhancing method for GRO TDC based clock generation systems," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 3, pp. 680–688, March 2014.

[45] E. Alon, J. Kim, S. Pamarti, K. Chang, and M. Horowitz, "Replica compensated linear regulators for supply-regulated phase-locked

loops," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 2, pp. 413–424, Feb 2006.

[46] A. Arakali, S. Gondi, and P. K. Hanumolu, "Analysis and design techniques for supply-noise mitigation in phase-locked loops," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 11, pp. 2880–2889, Nov 2010.

[47] B. Yang, B. Drost, S. Rao, and P. K. Hanumolu, "A high-PSR LDO using a feedforward supply-noise cancellation technique," in *2011 IEEE Custom Integrated Circuits Conference (CICC)*, Sept 2011, pp. 1–4.

[48] Y. Lim, J. Lee, S. Park, Y. Jo, and J. Choi, "An external capacitorless low-dropout regulator with high PSR at all frequencies from 10 kHz to 1 GHz using an adaptive supply-ripple cancellation technique," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 9, pp. 2675–2685, Sept 2018.

[49] M. El-Nozahi, A. Amer, J. Torres, K. Entesari, and E. Sanchez-Sinencio, "High PSR low drop-out regulator with feed-forward ripple cancellation technique," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 3, pp. 565–577, March 2010.

[50] C. J. Park, M. Onabajo, and J. Silva-Martinez, "External capacitorless low drop-out regulator with 25 dB superior power supply rejection in the 0.4-4 MHz range," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 2, pp. 486–501, Feb 2014.

[51] Y. Lim, J. Lee, Y. Lee, S.-S. Song, H.-T. Kim, O. Lee, and J. Choi, "An external capacitor-less ultralow-dropout regulator using a loop-gain stabilizing technique for high power-supply rejection over a wide range of load current," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, no. 11, pp. 3006–3018, Nov 2017.

[52] P. K. Hanumolu, "Low dropout regulators," in *2015 IEEE Custom Integrated Circuits Conference (CICC)*, 2015, pp. 1–37.

[53] X. Ma, Y. Lu, and Q. Li, "A fully integrated LDO with 50-mV dropout for power efficiency optimization," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 4, pp. 725–729, April 2020.

[54] K. Luria, J. Shor, M. Zelikson, and A. Lyakhov, "Dual-mode low-drop-out regulator/power gate with linear and on–off conduction for microprocessor core on-die supply voltages in 14 nm," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 3, pp. 752–762, March 2016.

[55] T. C. Carusone, D. A. Johns, and K. W. Martin, *Analog Integrated Circuit Design*, 2nd ed. Wiley, 2011.

[56] A. Urso, Y. Chen, R. B. Staszewski, J. F. Dijkhuis, S. Stanzione, Y.-H. Liu, W. A. Serdijn, and M. Babaie, "A switched-capacitor DC-DC converter powering an LC oscillator to achieve 85% system peak power efficiency and -65 dBc spurious tones," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 11, pp. 3764–3777, Nov 2020.

[57] Y. Chen, Y.-H. Liu, Z. Zong, J. Dijkhuis, G. Dolmans, R. B. Staszewski, and M. Babaie, "A supply pushing reduction technique for LC oscillators based on ripple replication and cancellation," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 1, pp. 240–252, Jan 2019.

[58] Y.-C. Huang, C.-F. Liang, H.-S. Huang, and P.-Y. Wang, "A 2.4 GHz ADPLL with digital-regulated supply-noise-insensitive and temperature-self-compensated ring DCO," in *2014 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb 2014, pp. 270–271.

[59] J. Liu, T.-K. Jang, Y. Lee, J. Shin, S. Lee, T. Kim, J. Park, and H. Park, "A 0.012 mm^2 3.1mW bang-bang digital fractional-N PLL with a power-supply-noise cancellation technique and a walking-one-phase-selection fractional frequency divider," in *2014 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb 2014, pp. 268–269.

[60] C.-W. Yeh, C.-E. Hsieh, and S.-I. Liu, "A 3.2 GHz digital phase-locked loop with background supply-noise cancellation," in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, Jan 2016, pp. 332–333.

[61] K.-Y. J. Shen, S. F. S. Farooq, Y. Fan, K. M. Nguyen, Q. Wang, A. Elshazly, and N. Kurd, "A 0.17-to-3.5 mW 0.15-to-5 GHz SoC PLL with 15 dB built-in supply noise rejection and self-bandwidth control in 14 nm CMOS," in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, Jan 2016, pp. 330–331.

[62] T. Wu, K. Mayaram, and U.-K. Moon, "An on-chip calibration technique for reducing supply voltage sensitivity in ring oscillators," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 4, pp. 775–783, April 2007.

[63] A. Elshazly, R. Inti, W. Yin, B. Young, and P. K. Hanumolu, "A 0.4-to-3 GHz digital PLL with PVT insensitive supply noise cancellation using deterministic background calibration," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 12, pp. 2759–2771, Dec 2011.

[64] S. S. Nagam and P. R. Kinget, "A low-jitter ring-oscillator phase-locked loop using feedforward noise cancellation with a sub-sampling phase detector," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 3, pp. 703–714, March 2018.

[65] C.-W. Tien and S.-I. Liu, "A digital phase-locked loop with background supply voltage sensitivity minimization," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 6, pp. 1830–1839, June 2018.

[66] C.-R. Ho and M. S.-W. Chen, "Interference-induced DCO spur mitigation for digital phase locked loop in 65-nm CMOS," in *ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference*, Sept 2016, pp. 213–216.

[67] D. Kim and S. Cho, "A supply noise insensitive PLL with a rail-to-rail swing ring oscillator and a wideband noise suppression loop," in *2017 Symposium on VLSI Circuits*, June 2017, pp. C180–C181.

[68] B. Soltanian and P. Kinget, "AM-FM conversion by the active devices in MOS LC-VCOs and its effect on the optimal amplitude," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, 2006*, June 2006, pp. 4–108.

[69] E. Hegazi and A. A. Abidi, "Varactor characteristics, oscillator tuning curves, and AM-FM conversion," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 6, pp. 1033–1039, June 2003.

[70] A. Zanchi, C. Samori, S. Levantino, and A. L. Lacaita, "A 2-V 2.5-GHz -104-dBc/Hz at 100 kHz fully integrated VCO with wideband low-noise automatic amplitude control loop," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 4, pp. 611–619, Apr 2001.

[71] D. Miyashita, H. Ishikuro, S. Kousai, H. Kobayashi, H. Majima, K. Agawa, and M. Hamada, "A phase noise minimization of CMOS VCOs over wide tuning range and large PVT variations," in *2005 IEEE Custom Integrated Circuits Conference (CICC)*, Sept 2005, pp. 583–586.

[72] J. W. M. Rogers, D. Rahn, and C. Plett, "A study of digital and analog automatic-amplitude control circuitry for voltage-controlled oscillators," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 2, pp. 352–356, Feb 2003.

[73] E. N. Y. Ho and P. K. T. Mok, "Wide-loading-range fully integrated LDR with a power-supply ripple injection filter," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 59, no. 6, pp. 356–360, June 2012.

[74] L. Fanori, T. Mattsson, and P. Andreani, "A Class-D CMOS DCO with an on-chip LDO," in *ESSCIRC 2014 - 40th European Solid State Circuits Conference (ESSCIRC)*, Sept 2014, pp. 335–338.

[75] P. Andreani and A. Fard, "More on the $1/f^2$ phase noise performance of CMOS differential-pair LC-tank oscillators," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2703–2712, Dec 2006.

[76] L. Fanori and P. Andreani, "Highly efficient Class-C CMOS VCOs, including a comparison with Class-B VCOs," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 7, pp. 1730–1740, July 2013.

[77] C. Zheng and D. Ma, "A 10-MHz green-mode automatic reconfigurable switching converter for DVS-enabled VLSI systems," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 6, pp. 1464–1477, June 2011.

[78] O. Trescases, A. Prodić, and W. T. Ng, "Digitally controlled current-mode DC-DC converter IC," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 1, pp. 219–231, Jan 2011.

[79] M. Du, H. Lee, and J. Liu, "A 5-MHz 91% peak-power-efficiency buck regulator with auto-selectable peak- and valley-current control," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 8, pp. 1928–1939, Aug 2011.

[80] D. El-Damak, S. Bandyopadhyay, and A. P. Chandrakasan, "A 93% efficiency reconfigurable switched-capacitor DC-DC converter using on-chip ferroelectric capacitors," in *2013 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb 2013, pp. 374–375.

[81] A. Hajimiri and T. H. Lee, "Design issues in CMOS differential LC oscillators," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 5, pp. 717–724, May 1999.

[82] A. Bevilacqua and P. Andreani, "An analysis of $1/f$ noise to phase noise conversion in CMOS harmonic oscillators," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 5, pp. 938–945, May 2012.

[83] E. Hegazi, J. Rael, and A. A. Abidi, *The Designer's Guide to High-Purity Oscillators*, 1st ed. Springer, 2005.

[84] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Feb 1998.

[85] P. Andreani, X. Wang, L. Vandi, and A. Fard, "A study of phase noise in colpitts and LC-tank CMOS oscillators," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 5, pp. 1107–1118, May 2005.

[86] M. Shahmohammadi, M. Babaie, and R. B. Staszewski, "A $1/f$ noise upconversion reduction technique for voltage-biased RF CMOS oscillators," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 11, pp. 2610–2624, Nov 2016.

[87] D. Murphy, J. J. Rael, and A. A. Abidi, "Phase noise in LC oscillators: A phasor-based analysis of a general result and of loaded Q," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 6, pp. 1187–1203, June 2010.

[88] B. Yousefzadeh and K. A. A. Makinwa, "A BJT-based temperature sensor with a packaging-robust inaccuracy of $\pm 0.3\,^{\circ}\mathrm{C}$ (3σ) from -55 °C to +125 °C after heater-assisted voltage calibration," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb 2017, pp. 162–163.

[89] L. G. Salem and P. P. Mercier, "A recursive switched-capacitor DC-DC converter achieving $2^N - 1$ ratios with high efficiency over a wide output voltage range," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 12, pp. 2773–2787, Dec 2014.

[90] M. D. Seeman, "A design methodology for switched-capacitor DC-DC converters," *UC Berkeley*, 2009. [Online]. Available: https://www2.eecs.berkeley.edu/Pubs/TechRpts/2009/EECS-2009-78.html

[91] H.-P. Le, S. R. Sanders, and E. Alon, "Design techniques for fully integrated switched-capacitor DC-DC converters," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 9, pp. 2120–2131, Sep. 2011.

[92] N. Pourmousavian, F.-W. Kuo, T. Siriburanon, M. Babaie, and R. B. Staszewski, "A 0.5-V 1.6-mW 2.4-GHz fractional-N all-digital PLL for Bluetooth LE with PVT-insensitive TDC using switched-capacitor doubler in 28-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 9, pp. 2572–2583, Sep. 2018.

[93] Y. Lu, W.-H. Ki, and C. Patrick Yue, "An NMOS-LDO regulated switched-capacitor DC–DC converter with fast-response adaptive-phase digital control," *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 1294–1303, Feb 2016.

[94] W. Oh, B. Bakkaloglu, C. Wang, and S. K. Hoon, "A CMOS low noise, chopper stabilized low-dropout regulator with current-mode feedback error amplifier," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 10, pp. 3006–3015, Nov 2008.

[95] Y. Chen, J. Gong, R. B. Staszewski, and M. Babaie, "A fractional-N digitally intensive PLL achieving 428-fs jitter and <-54-dBc spurs under 50-mv_{pp} supply ripple," *IEEE Journal of Solid-State Circuits*, pp. 1–1, 2021.

[96] K.-H. Cheng, J.-C. Liu, and H.-Y. Huang, "A 0.6-V 800-MHz all-digital phase-locked loop with a digital supply regulator," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 59, no. 12, pp. 888–892, Dec 2012.

[97] W. Rhee, K. A. Jenkins, J. Liobe, and H. Ainspan, "Experimental analysis of substrate noise effect on PLL performance," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, no. 7, pp. 638–642, July 2008.

[98] P. V. Brennan, P. M. Radmore, and D. Jiang, "Intermodulation-borne fractional-N frequency synthesiser spurious components," *IEE Proceedings-Circuits, Devices and Systems*, vol. 151, no. 6, pp. 536–542, Dec 2004.

[99] S. Levantino, G. Marzin, C. Samori, and A. L. Lacaita, "A wideband fractional-N PLL with suppressed charge-pump noise and automatic loop filter calibration," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 10, pp. 2419–2429, Oct 2013.

[100] M. Ferriss, B. Sadhu, A. Rylyakov, H. Ainspan, and D. Friedman, "A 12-to-26GHz fractional-N PLL with dual continuous tuning LC-D/VCOs," in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, Jan 2016, pp. 196–198.

[101] Z.-Z. Chen, Y.-H. Wang, J. Shin, Y. Zhao, S. A. Mirhaj, Y.-C. Kuan, H.-N. Chen, C.-P. Jou, M.-H. Tsai, F.-L. Hsueh *et al.*, "Sub-sampling all-digital fractional-N frequency synthesizer with -111 dBc/Hz in-band phase noise and an FOM of -242 dB," in *2015 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb 2015, pp. 268–269.

[102] X. Gao, O. Burg, H. Wang, W. Wu, C.-T. Tu, K. Manetakis, F. Zhang, L. Tee, M. Yayla, S. Xiang *et al.*, "A 2.7-to-4.3 GHz, 0.16ps$_{\text{rms}}$-jitter, -246.8 dB-FOM, digital fractional-N sampling PLL in 28nm CMOS," in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, Jan 2016, pp. 174–175.

[103] Z. Xu, M. Miyahara, K. Okada, and A. Matsuzawa, "A 3.6 GHz low-noise fractional-N digital PLL using SAR-ADC-based TDC," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 10, pp. 2345–2356, Oct 2016.

[104] Y. Hu, X. Chen, T. Siriburanon, J. Du, Z. Gao, V. Govindaraj, A. Zhu, and R. B. Staszewski, "A 21.7-to-26.5GHz charge-sharing locking quadrature PLL with implicit digital frequency-tracking loop achieving 75fs jitter and -250dB FoM," in *2020 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb 2020, pp. 276–278.

[105] J. Kim, Y. Jo, Y. Lim, T. Seong, H. Park, S. Yoo, Y. Lee, S. Choi, and J. Choi, "A 104fs$_{\text{rms}}$-jitter and -61dBc-fractional spur 15GHz fractional-N subsampling PLL using a voltage-domain quantization-error cancelation technique," in *2021 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 64, Feb 2021, pp. 448–450.

[106] J. Du, T. Siriburanon, Y. Hu, V. Govindaraj, and R. B. Staszewski, "A Reference-Waveform Oversampling Technique in a Fractional-N ADPLL," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 11, pp. 3445–3457, 2021.

[107] J. Z. Ru, C. Palattella, P. Geraedts, E. Klumperink, and B. Nauta, "A high-linearity digital-to-time converter technique: Constant-slope

charging," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 6, pp. 1412–1423, June 2015.

[108] H. Liu, D. Tang, Z. Sun, W. Deng, H. C. Ngo, and K. Okada, "A sub-mW fractional-N ADPLL with FOM of -246 dB for IoT applications," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 12, pp. 3540–3552, Dec 2018.

[109] P. Chen, F. Zhang, Z. Zong, S. Hu, T. Siriburanon, and R. B. Staszewski, "A 31-μW, 148-fs step, 9-bit capacitor-DAC-based constant-slope digital-to-time converter in 28-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 11, pp. 3075–3085, Nov 2019.

[110] L. Wu, T. Burger, P. Schönle, and Q. Huang, "A power-efficient fractional-N DPLL with phase error quantized in fully differential-voltage domain," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 4, pp. 1254–1264, April 2021.

[111] J. Tao and C.-H. Heng, "A 2.2-GHz 3.2-mW DTC-free sampling $\Delta\Sigma$ fractional-N PLL with -110-dBc/Hz in-band phase noise and -246-dB FoM and -83-dBc reference spur," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 9, pp. 3317–3329, Sep. 2019.

[112] D. Liao and F. F. Dai, "A fractional-N reference sampling PLL with linear sampler and CDAC based fractional spur cancellation," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 3, pp. 694–704, March 2021.

[113] B. P. Ginsburg and A. P. Chandrakasan, "500-MS/s 5-bit ADC in 65-nm CMOS with split capacitor array DAC," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 4, pp. 739–747, April 2007.

[114] I. Galton, "Why dynamic-element-matching DACs work," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 2, pp. 69–74, Feb 2010.

[115] A. M. Abo and P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 5, pp. 599–606, May 1999.

[116] C.-C. Liu, S.-J. Chang, G.-Y. Huang, and Y.-Z. Lin, "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 4, pp. 731–740, April 2010.

[117] C. Vaucher, I. Ferencic, M. Locher, S. Sedvallson, U. Voegeli, and Z. Wang, "A family of low-power truly modular programmable dividers in standard 0.35-μm CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 7, pp. 1039–1045, July 2000.

[118] D. Tasca, M. Zanuso, G. Marzin, S. Levantino, C. Samori, and A. L. Lacaita, "A 2.9–4.0-GHz fractional-N digital PLL with bang-bang phase detector and 560-fs$_{\text{rms}}$ integrated jitter at 4.5-mW power," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 12, pp. 2745–2758, Dec 2011.

[119] D. Tasca, M. Zanuso, S. Levantino, C. Samori, and A. L. Lacaita, "Low-power divider retiming in a 3–4 GHz fractional-N PLL," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 58, no. 4, pp. 200–204, April 2011.

[120] W. Wu, C.-W. Yao, C. Guo, P.-Y. Chiang, P.-K. Lau, L. Chen, S. W. Son, and T. B. Cho, "A 14nm analog sampling fractional-N PLL with a digital-to-time converter range-reduction technique achieving 80fs integrated jitter and 93fs at near-integer channels," in *2021 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 64, Feb 2021, pp. 444–446.

[121] C. Samori, M. Zanuso, S. Levantino, and A. L. Lacaita, "Multipath adaptive cancellation of divider non-linearity in fractional-N PLLs," in *2011 IEEE International Symposium of Circuits and Systems (ISCAS)*, May 2011, pp. 418–421.

[122] C.-R. Ho and M. S.-W. Chen, "A digital PLL with feedforward multi-tone spur cancellation scheme achieving <-73 dBc fractional spur

and <–110 dBc reference spur in 65 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 12, pp. 3216–3230, Dec 2016.

[123] S. Bu, K. N. Leung, Y. Lu, J. Guo, and Y. Zheng, "A fully integrated low-dropout regulator with differentiator-based active zero compensation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 10, pp. 3578–3591, Oct 2018.

[124] J. Jiang, W. Shu, and J. S. Chang, "A 65-nm CMOS low dropout regulator featuring >60-dB PSRR over 10-MHz frequency range and 100-mA load current range," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 8, pp. 2331–2342, Aug 2018.

[125] B. Razavi, "The StrongARM latch [a circuit for all seasons]," *IEEE Solid-State Circuits Magazine*, vol. 7, no. 2, pp. 12–17, Spring 2015.

[126] J. Zhu, R. K. Nandwana, G. Shu, A. Elkholy, S. J. Kim, and P. K. Hanumolu, "A 0.0021 mm^2 1.82 mW 2.2 GHz PLL using time-based integral control in 65 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 1, pp. 8–20, Jan 2017.

[127] E. Familier and I. Galton, "Second and third-order successive requantizers for spurious tone reduction in low-noise fractional-N PLLs," in *2017 IEEE Custom Integrated Circuits Conference (CICC)*, April 2017, pp. 1–4.

[128] M. P. Kennedy, Y. Donnelly, J. Breslin, S. Tulisi, S. Patil, C. Curtin, S. Brookes, B. Shelly, P. Griffin, and M. Keaveney, "4.48 GHz 0.18μm SiGe BiCMOS exact-frequency fractional-N frequency synthesizer with spurious-tone suppression yielding a -80 dBc in-band fractional spur," in *2019 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb 2019, pp. 272–274.

List of Publications

Journal Papers

- **Y. Chen**, J. Gong, J. Dijkhuis, R. B. Staszewski and M. Babaie, "A fractional-N digitally intensive PLL achieving 428-fs jitter and <-54 dBc spurs under 50-mV_{pp} supply ripple," *IEEE Journal of Solid-State Circuits*, Early Access, 2021. DOI: 10.1109/JSSC.2021.3123386. [IEEE Xplore link (Open Access)]

- **Y. Chen**, Y.-H. Liu, Z. Zong, J. Dijkhuis, D. Dolmans, R. B. Staszewski and M. Babaie, "A supply pushing reduction technique for LC oscillators based on ripple replication and cancellation," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 1, pp. 240–252, Jan. 2019. DOI: 10.1109/JSSC.2018.2871195. [IEEE Xplore link (Open Access)]

- A. Urso*, **Y. Chen***, J. Dijkhuis, Y.-H. Liu, M. Babaie and W. Serdijn, "Analysis and design of power supply circuits for RF oscillators," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 12, pp. 4233–4246, Dec. 2020. DOI: 10.1109/TCSI.2020.3020001. [IEEE Xplore link] (*Equally Credited Authors)

- A. Urso, **Y. Chen**, R. B. Staszewski, J. Dijkhuis, S. Stanzione, Y.-H. Liu, W. Serdijn and M. Babaie, "A switched-capacitor DC-DC converter powering an LC oscillator to achieve 85% system peak power efficiency and -65 dBc spurious tones," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 11, pp. 3764–3777, Nov. 2020. DOI: 10.1109/TCSI.2020.3012106. [IEEE Xplore link (Open Access)]

- P. Chen, X. Huang, **Y. Chen**, L. Wu and R. B. Staszewski, "An on-chip self-characterization of a digital-to-time converter by embedding it in a first-order $\Delta\Sigma$ loop," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 11, pp. 3734–3744, Nov. 2018. DOI: 10.1109/TCSI.2018.2857999. [IEEE Xplore link (Open Access)]

- Y. Wu, M. Shahmohammadi, **Y. Chen**, P. Lu and R. B. Staszewski, "A 3.5–6.8-GHz wide-bandwidth DTC-assited fractional-N all-digital PLL with a MASH $\Delta\Sigma$-TDC for low in-band phase noise," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 7, pp. 1885–1903, Jul. 2017. DOI: 10.1109/JSSC.2017.2682841. [IEEE Xplore link]

Conference Papers

- J. Gong, **Y. Chen**, F. Sebastiano, E. Charbon and M. Babaie, "A 200 dB FoM 4-to-5 GHz cryogenic oscillator with an automatic common-mode resonance calibration for quantum computing applications," in *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2020, pp. 308–310. DOI: 10.1109/ISSCC19947.2020.9062913. [IEEE Xplore link]

- **Y. Chen**, M. Babaie and R. B. Staszewski, "A 350-mV 2.4-GHz quadrature oscillator with nearly instantaneous start-up using series LC tanks," in *IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Nov 2017, pp. 105–108. DOI: 10.1109/ASSCC.2017.8240227. [IEEE Xplore link]

- Y. Wu, M. Shahmohammadi, **Y. Chen**, P. Lu and R. B. Staszewski, "A 3.5–6.8 GHz wide-bandwidth DTC-assited fractional-N all-digital PLL with a MASH $\Delta\Sigma$ TDC for low in-band phase noise," in *ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference*, Sept. 2016, pp. 209–212. DOI: 10.1109/ESSCIRC.2016.7598279. [IEEE Xplore link]

Patent Application

- **Y. Chen** and M. Babaie, "LC oscillator powering arrangement and method of powering an LC oscillator," Publication No. US 10892710 B2, Issued Jan. 2021.

Summary

The scaling of CMOS technology in deep submicron process nodes is accompanied by the integration of more and more functional blocks of a system, whether digital or analog/RF, onto the same chip (i.e., system-on-chip, SoC). These blocks would also place different requirements on their power supplies. To provide various static or dynamically controlled supply voltages needed by the SoC, a dedicated power management unit (PMU) is typically deployed. Following the same trend of system integration, implementing the PMU on-die is also highly desired.

The core of a PMU consists of several sets of voltage regulators that convert the output level of the energy source to the multiple supply voltages required by the integrated system. The DC-DC converters (switching regulators) and the low-dropout (LDO) linear regulators are normally employed in cascade for high power efficiency and for suppressing ripple amplitude demanded by the supply sensitive blocks, respectively. Although much effort has been devoted to the research on the design of fully integrated, or the so-called 'capacitor-less' LDOs, little has been done for the co-analysis and co-design of these LDOs with the load circuitry they power.

Frequency synthesizers have found wide applications in various systems. The phase-locked loop, as one of the most commonly used frequency synthesis techniques, modulates the oscillator in a feedback manner to generate the desired loop output. The first part of this thesis (Chapters 2 and 3) focuses on the power efficiency of the capacitor-less LDO when powering a PLL. Since the PLL, especially its oscillator, is sensitive to the supply perturbations, the LDO should provide a high power supply rejection (PSR) at the ripple frequency, which could be in the range of

several to tens of megahertz for integrated DC-DC converters, with a low output noise. The dropout voltage of the LDO is then determined by the required PSR, consuming extra voltage headroom and degrading the efficiency of the system. The tolerable output noise generally limits the minimum quiescent current consumed by the error amplifier (EA) and the feedback resistors in the LDO. Owning to the stringent requirement of the supply noise imposed by the oscillator in order to preserve its inherent phase noise performance, the efficiency of the corresponding LDO would be further degraded by a large factor due to its quiescent current consumption.

Based on the analysis above, it deems beneficial to power the PLL directly from the output of DC-DC converters. Taking this step further, different scenarios of powering the SoC are also identified and briefly discussed at the end of the first part.

To enable the proposed direct connection, the modules in the PLL should be able to tolerate the output ripples from such converters. In the second part of this thesis (Chapters 4 and 5), a fractional-N digitally intensive PLL (DPLL) architecture capable of maintaining its performance under a large (i.e., $50\,\mathrm{mV_{pp}}$) supply ripple is developed. The digital implementation is selected due to its ability to incorporate various digital calibration techniques with relative ease. The supply pushing of the LC oscillator used in the DPLL is suppressed by the proposed feed-forward ripple replication and cancellation technique, which replicate the supply ripple to the gate of its tail current source with a proper gain, stabilizing the oscillator tail current, and correspondingly, the oscillation swing. The optimal gain is calibrated on-chip through amplifying the oscillation amplitude variation and locating the control setting corresponding to the minimum value. The time error between the reference and the divided output of the oscillator is linearly converted into voltage domain through the current-mode supply-insensitive slope generator, with its input range being halved by resampling the output of the multi-modulus divider (MMDIV), driven by second-order $\Delta\Sigma$ modulation, with both edges of the oscillation signal. The output of a current DAC operating in parallel is also cascaded with the slope generator during phase detection to limit the dynamic range of the SAR ADC used to digitize the phase error. A low-power ripple pattern estimation and cancellation algorithm is also inserted at the ADC output to remove

the effect of the output delay perturbations of loop components under the supply ripple. Employing all these techniques, the proposed DPLL demonstrates, for the first time ever, the acceptable performance while operating under a large $50\,\mathrm{mV_{pp}}$ supply ripple.

List of Figures

List of Tables

Acknowledgements

It has been a long journey to arrive at this final stage of my Ph.D. study at TU Delft. Looking back, the feelings when I first arrived at Delft in Sept. 2014 are still fresh in my memory: excited, curious, but also a bit nervous. Now, after seven years, I'm glad to conclude the adventure with this dissertation. Throughout this seven-year endeavor, I have received support and help from many people, for which I feel both fortunate and grateful.

First of all, I would like to express my deep gratitude and appreciation to my promoter and advisor, Professor Robert Bogdan Staszewski, for all your guidance, support, and encouragement. I contacted you for the first time during my master's research when I encountered some problems in the TDC design. Since no one in the department had any experience with digital PLL design before, I tried to send you an e-mail. A bit to my surprise, you replied on the same day. From then on, I have received quite a lot of help on my master project through communication with you. Later, you kindly offered me the chance to pursue my Ph.D. career in your group at TU Delft. Throughout these years, I have learned a lot from you in many aspects, including your passion and energy towards research. I also greatly appreciate the effort you have spent on improving the quality of my technical papers. It will always be my honor to be part of your research team at TU Delft.

I would also like to express my deep gratitude and appreciation to my co-promoter and daily supervisor, Dr. Masoud Babaie. We got to know each other as officemates when I visited the EWI building for the first time and got my workplace on the 18th floor. After your graduation and being

promoted to Assistant Professor at TU Delft, you joined my supervision team in the second half of 2016. I truly appreciate the enormous effort you have devoted to my research project during the past five years. You helped to shape my research topic, organized technical meetings to discuss the progress, reviewed my design in detail, and revised my papers carefully. Without your steadfast support and guidance, the achievements in my Ph.D. research would not be possible. It is my honor to be one of the first two Ph.D. students you co-promoted at TU Delft.

My appreciation extends to Professor Wouter Serdijn at TU Delft, and Dr. Yao-Hong Liu at IMEC Netherlands. Prof. Serdijn co-led the joint research project with my co-promoter and supervised the converter design part in this project. Dr. Yao-Hong Liu arranged my stay at the Holster Centre to complete the oscillator tape-out. Also, the comments and discussions we have during the User Committee meetings really helped to improve the designs. Meanwhile, I also want to thank both of them for accepting the invitation and being part of my doctoral examine committee.

I also want to give special thanks to other members of my doctoral exam committee: Prof. Andreani, Prof. Levantino, Prof. Nauta, and Prof. Vaucher. Thank you for taking your precious time to review my dissertation and provide valuable suggestions. My gratitude also goes out to other staff members of the Microelectronics Department who have offered a helping hand along the way: Prof. de Vreede, Prof. McCune, Dr. Spirito, and Dr. Alavi.

My Ph.D. work also would not have been completed without the help from our support staff. I am really grateful to Atef Akhnoukh, for all the valuable assistance during the tape-outs and measurements. I also want to thank John Dijkhuis for the technical support while I was completing my oscillator design at the Holster Centre. Special thanks to Wil Straver, Zu-yao Chang, and Ali Kaichouhi for the suggestions on the test board design and wire bonding my chips. Thanks to Antoon Frehe for his support on various IT matters. Last but not least, I would like to thank Marion de Vlieger, our group secretary, for her administrative supports during the past years.

The Ph.D. research is supported by the Chinese Scholarship Council and the Netherlands Organization for Scientific Research. I would like

to express my sincere gratitude for their support. Also, I wish to thank IMEC Netherlands for kindly offering the tape-out opportunities and all the assistance I have received from their staff.

During my Ph.D. study, I was very fortunate to work with many excellent colleagues in and out of TU Delft. Here, I would like to thank Ying Wu first. It is nice to start the Ph.D. research by joining your Huawei project. I really learned a lot from the experience and the nice discussions with you. I also wish to thank Zhirui Zong, Jiang Gong, Zhong Gao, Yiyu Shen, Zhebin Hu, and Linghan Zhang for all the technical and non-technical discussions and the assistance with my designs and measurements. I would also like to thank Zhebin Hu for his help during my job-seeking process. Special thanks to Peng Chen, who helped communicate with their technician on DRC issues during a tape-out through UCD. I would also like to thank Alessandro Usro, who designed the DC-DC converter to power the oscillator directly in our project. My gratitude also extends to my other colleagues and friends of the ELCA, Bioelectronics, and Qutech groups: Mina Shahmohammad, Milad Mehrpoo, Bishnu Patra, Gerasimos Vlachogiannakis, Satoshi Malotaux, Augusto Ximenes, Jingchu He, Amir Reza Ahmadi Mehr, Massoud Tohidian, Iman Madadi, Mohsen Hashemi, Mohsen Mortazavi, Mohammad Ali Montazerolghaem, Gagan Singh, Rui Hou, Yongjia Li, Yao Liu, Rui Guan, Ronaldo Martins da Ponte, Masoud Pashaeifar, Nawaf Almotairi, Mohammad Reza Beikmirza, and many others I may have forgotten to mention here. I also want to thank Zhao Chen and Mingliang Tan for the technical discussion on the SAR ADC design.

The great Chinese community I had met in Delft should never be left out. Many of them have already been mentioned above. Besides the nice working environment, I would also like to thank you all for the hotpot and dinner parties, various exciting activities, as well as the aimless chat and jokes during spare time. Special thanks to Chunsen Shi and Haiyan Lu, for the day trips and other entertainment that helped ease the pressure at work. I also want to express my thanks to other Chinese fellows and friends at TU Delft whom I was fortunate to meet, including Xiang Fu, Jian Fang, Yue Zhao, Yazhou Yang, Lei Xie, Mingxiao Ma, Zhi Hong, Hai Gong, Pengling Wang, Long Xu, and Xin Guo. In addition, I want to give thanks to the roommates I have ever had during these years: Yiyu Shen,

Zhebin Hu, Jiliang Ma, Ruimin Yang, Jing Li, Xianwei Zeng, Heng Wang, Jintao Yu, and Jianyu Chen. Thank you for making my life abroad more fun and convenient.

My experience in PLL design starts during my master's program under the mentorship of Prof. Ruizhi Zhang. I wish to express my deep gratitude towards him for leading me into this interesting field. I am truly grateful for all his guidance and encouragement along the way. I also want to give special thanks to Zhi Li and Yan Song, among my former classmates and friends at Xi'an Jiaotong University, for their help and support during my Ph.D. research.

Finally, my deepest gratitude goes to my beloved family. Great thanks to my dear parents, for your unconditional love, care, and support for me. I love you forever! Also, great thanks to my doting grandparents. I hope to see you soon. (Yeye, I miss you forever, and I believe you are still by my side.) Many thanks to my dear uncles, aunts, and cousins. I have always missed the pleasant gatherings of the whole family during the past years. Now it is time to go back home.

Yue Chen
Feb. 2022
Delft, The Netherlands

About the Author

Yue Chen received the B.Eng. degree in microelectronics and the M.Eng. degree in electronic science and technology from Xi'an Jiaotong University, Xi'an, China, in 2011 and 2014, respectively. He is currently pursuing the Ph.D. degree in electronic engineering at the Microelectronics Department, Delft University of Technology, Delft, The Netherlands.

His current research interests include frequency synthesizer techniques and integrated circuits for wireless communications.