A Si/SiGe based quantum dot with floating gates for scalability

Xue, X.; Corna, A.; Samkharadze, Nodar; Veldhorst, M.; Ishihara, R.; Vandersypen, L.M.K.

Publication date
2018

Document Version
Accepted author manuscript

A Si/SiGe based quantum dot with floating gates for scalability

Y. Xu[1], A. Corna[1], N. Samkharadze[1], M. Veldhorst[1], R. Ishihara[1] and L. M. K. Vandersypen[1]

[1]*QuTech and Kavli Institute of Nanoscience, Delft University of Technology, Lorentzweg 1, 2628CJ Delft, the Netherlands*

For silicon spin qubits based on gate-defined quantum dot, DC lines are required to confine individual electrons in a quantum dot [1]. When considering multiple dot, the voltage applied on the gates typically vary due to the non-uniformity of the substrate, layout design or fabrication process. The standard operating mode is to connect each DC line to a DAC operating at room temperature through the bond wires from the chip to the sample carrier and the refrigerator wiring. However, when scaling towards a fault-tolerant quantum computer, which needs hundreds of thousands of quantum dot, simply adding more wires and electronics would cause problems, due to space constraints in the connection between the sample and the sample board and excessive heat load through the wires. Thus an integration strategy is required to provide specific voltages for each gate efficiently [2].

In this study, we explore a DRAM-based floating gate circuit to bias all the quantum dot gates. A single DAC line can provide different voltages to several DRAM cells sequentially, while the transistor in series with the capacitor is used as a switch to float the gates of the dot from the voltage supply line. In this way the required voltages can be stored locally on the capacitors. All elements are integrated on Si/SiGe based substrate and should be functional at the same cryogenic temperature as the dots. By combining a de-multiplexer to address each DRAM cell, the number of wires needed from the chip to the sample carrier and dilution refrigerator is vastly reduced.

As a proof of concept, we first made a device with a floating plunger gate of a single quantum dot. Most of the device fabrication process follows the normal CMOS fabrication standard. There are some minor differences. Firstly, e-beam lithography is used for all patterns instead of photo lithography since the pitch of a quantum dot is a few tens of nanometers. Secondly, since the process is based on a Si/SiGe hetero-layer substrate, the process temperature is limited to 700°C to prevent strain releasing of the strained-Si layer. Therefore a rapid thermal annealing method is used to activate the implanted phosphorus dopants at 700 °C for 15s and the gate oxide is made by ALD Al_2O_3 at 350 °C.

The device is measured at 20 mK. We observed that the DRAM-like circuit doesn't affect the Coulomb peaks of the quantum dot dramatically. A parallel RC circuit is used to model the discharging behavior of the floating node. The discharging time constant is extracted to be 485 s, which results in a re-charging frequency of approximately 200 Hz if a voltage accuracy of 1 μV is required for the gate voltages.

This work shows that implementing a DRAM-like floating gate structure with qudots has potential for scalability. In the next step, we will measure the performance of a single quantum dot with all gates floating. Furthermore, we will implement a de-multiplexing strategy to address each gate using reduced number of wires as shown in other works [3].

References

[1] T.F. Watson, et al, Nature 555, 633-637 (2018)

[2] L.M.K. Vandersypen, et al, Nature PJ Quantum Information 3,34 (2017)

[3] D.R. Ward, et al, Appl. Phys. Lett. 102, 213107 (2013)