TU Delft

Delft University of Technology

31.2 A 0.9V 28MHz Dual-RC Frequency Reference with 5pJ/Cycle and ±200 ppm Inaccuracy from -40°C to 85°C

Choi, Woojun; Angevare, J.; Park, Injun; Makinwa, Kofi A.A.; Chae, Youngcheol

DOI
10.1109/ISSCC42613.2021.9366021

Publication date
2021

Document Version
Final published version

Published in
2021 IEEE International Solid-State Circuits Conference, ISSCC 2021 - Digest of Technical Papers

Citation (APA)
Choi, W., Angevare, J., Park, I., Makinwa, K. A. A., & Chae, Y. (2021). 31.2 A 0.9V 28MHz Dual-RC Frequency Reference with 5pJ/Cycle and ±200 ppm Inaccuracy from -40°C to 85°C. In *2021 IEEE International Solid-State Circuits Conference, ISSCC 2021 - Digest of Technical Papers* (pp. 434-436). Article 9366021 (Digest of Technical Papers - IEEE International Solid-State Circuits Conference; Vol. 64). IEEE. https://doi.org/10.1109/ISSCC42613.2021.9366021

Important note
To cite this publication, please use the final published version (if applicable).
Please check the document version above.

Copyright
Other than for strictly personal use, it is not permitted to download, forward or distribute the text or part of it, without the consent of the author(s) and/or copyright holder(s), unless the work is under an open content license such as Creative Commons.

Takedown policy
Please contact us and provide details if you believe this document breaches copyrights.
We will remove access to the work immediately and investigate your claim.

This work is downloaded from Delft University of Technology.
For technical reasons the number of authors shown on this cover page is limited to a maximum of 10.

Green Open Access added to TU Delft Institutional Repository

'You share, we take care!' - Taverne project

https://www.openaccess.nl/en/you-share-we-take-care

Otherwise as indicated in the copyright section: the publisher is the copyright holder of this work and the author uses the Dutch legislation to make this work public.

31.2 A 0.9V 28MHz Dual-RC Frequency Reference with 5pJ/Cycle and ±200ppm Inaccuracy from -40°C to 85°C

Woojun Choi[1], Jan A. Angevare[2], Injun Park[1], Kofi A. A. Makinwa[2], Youngcheol Chae[1]

[1]Yonsei University, Seoul, Korea
[2]Delft University of Technology, Delft, The Netherlands

2021 IEEE International Solid- State Circuits Conference (ISSCC) | 978-1-7281-9549-0/20/$31.00 ©2021 IEEE | DOI: 10.1109/ISSCC42613.2021.9366021

Wireless sensor nodes in battery-powered internet-of-things (IoT) applications require a stable on-chip frequency reference with low energy (<10pJ/cycle) and high frequency stability (below ±300ppm). CMOS RC frequency references are promising due to their low-cost integration and high energy efficiency [1-5]. Conventional RC references, however, achieve only moderate accuracy (a few %) due to the large temperature coefficient (TC) of on-chip resistors [3]. First-order TC compensation can be achieved by combining resistors with complementary TCs [1,2]. Although this is energy efficient (<6pJ/cycle), it only partially compensates for the resistors' high-order TCs, limiting the resulting accuracy to about ±500ppm. Better accuracy (±100ppm [4]) can be achieved by using the output of a digital temperature sensor (TS) to perform a polynomial correction of the phase-shift ($\mu_{P,T}$) of an RC filter (Fig. 31.2.1). Alternatively, the phase-shifts (μ_P and μ_N) of two RC filters with complementary TCs can be linearized (T_P and T_N) and combined in the digital domain. Such dual-RC frequency references can also achieve good accuracy (±200ppm [5]). However, both architectures employ an analog phase-domain ΔΣ modulator (Φ-ΔΣM) for each RC filter, which consumes significant energy (25pJ/cycle [4] and 107pJ/cycle [5]) and area (0.3mm² [4] and 1.65mm² [5]).

This paper presents a 0.9V, 28MHz dual-RC frequency reference, which simultaneously achieves ±200ppm accuracy from -40°C to 85°C, <2ppm long-term stability, and 7ps (1σ) period jitter. By using RC polyphase filters (PPFs) and digital Φ-ΔΣM converters, it occupies only 0.06mm², which is 5× less than [4], while achieving similar accuracy. Furthermore, it only consumes 142μW from a 0.9V supply, which corresponds to an energy-efficiency of 5pJ/cycle, more than 5× less than state-of-the-art RC frequency references [4,5].

The proposed dual-RC frequency reference (Fig. 31.2.1, right) consists of a digital frequency-locked loop (FLL), in which the frequency of a digitally controlled oscillator (DCO) is locked to a temperature-independent phase shift derived from two RC PPFs. Phase shifts with complementary TCs are generated by PPFs made from different resistor types (P-poly and Silicided P-poly). These are then digitized by digital Φ-ΔΣMs, which consist of a zero-crossing (ZC) detector [6], a digital counter and simple logic circuits. An XOR gate detects the phase difference between the zero-crossings of the PPF and the reference phases (Φ_0 and Φ_1) selected by the bitstream μ. This is then integrated by a digital counter, which is clocked by a time-counting oscillator F_{CNT} (~280MHz). The bitstream outputs (μ_P and μ_N) of the Φ-ΔΣMs are decimated by sinc filters. The digitized phase-shifts of the PPFs are then linearized by polynomials, resulting in complementary phase shifts (T_P and T_N), which are combined to generate a temperature-independent frequency error e_f. This is driven to zero by the digital loop filter, such that the DCO's output frequency F_{DCO} (=28MHz) is temperature-independent.

Figure 31.2.2 shows the block diagram of the PPF (R_{PPF}=120kΩ and C_{PPF}=8.4pF) and the digital Φ-ΔΣM. They are driven at $F_{DRV}=F_{DCO}/128=218.75$kHz, which is also used to generate the sampling clock F_S and its phase references ($\Phi_{0/1}$ with ±22.5° phase-shifts). The ZC detector is a two-stage continuous-time comparator. Each stage consists of an nMOS differential pair with pMOS loads and a resistive CMFB, whose phase-shift results in an output-frequency error of only 400ppm as the supply voltage varies from 0.85 to 1.05V. The phase difference between the ZC detector output F_{ZCD} and the phase reference F_{DAC} is detected by the XOR gate and integrated by a 13-bit up/down counter. To avoid a simple integer relationship to F_{DRV}, which would lead to limit cycles that limit the resolution of the digital Φ-ΔΣMs, the counter is clocked by a separate free-running oscillator F_{CNT}. The F_{CNT} is generated by a 3-stage current-controlled oscillator (CCO) biased by a supply-insensitive PTAT current source. It can be trimmed (3 bits) to compensate for process variation. A large F_{CNT}/F_{DRV} ratio ensures sufficient time resolution, and the counter's up/down signal is re-clocked by F_{CNT} to avoid meta-stability [7]. Finally, the counter's MSB, i.e. its output polarity, is sampled by F_s, and the resulting bitstream BS controls the phase references in a ΔΣ manner. The digital Φ-ΔΣM achieves a phase resolution of 0.4m° in a bandwidth of 3Hz.

In a digital FLL, the DCO should have enough tuning range to compensate for PVT variations, and enough resolution to facilitate the intended accuracy. Figure 31.2.3 shows the block diagram of the DCO, which consists of an 11-stage CCO controlled by a 4-bit coarse current-steering DAC and a fine ΔΣ DAC. The coarse DAC covers a frequency shift of ±50% in the 28MHz nominal frequency over process corners, while the fine ΔΣ DAC covers a frequency shift of ±12% over voltage and temperature with a resolution of 360Hz. The fine ΔΣ DAC consists of a digital ΔΣM and an RC lowpass filter (LPF). The digital ΔΣM is implemented using a 2nd-order error-feedback structure, and the 2nd-order LPF is designed to achieve the cut-off frequency of 20kHz, effectively removing quantization noise. Its output is converted into a control current by a degenerated pMOS current source, which minimizes current-to-frequency noise. The coarse DAC is similarly implemented, but with a half-V_{DD} bias. To reduce common-mode errors, each CCO delay cell consists of two inverters coupled by transmission gates. The CCO is designed to achieve an open-loop period jitter of 5ps.

The frequency reference was fabricated in 65nm CMOS and occupies 0.06mm² (Fig. 31.2.7). It consumes 158μA from a 0.9V supply. 12 samples in ceramic DIL packages were characterized. For flexibility, the decimation filter, the polynomials, and the digital loop filter were implemented in an external FPGA. To characterize the phase shift of the PPFs over temperature, an external reference frequency of 28MHz was used instead of F_{DCO}. Figure 31.2.4 shows the measured output spectrum of the Φ-ΔΣM with a PPF (Silicided P-poly) driven at the 218.75kHz frequency. By decimating 2^{16} output bits, a temperature resolution of <20mK was achieved for both PPFs. Each PPF is trimmed at two temperatures (-30°C, 40°C) and the remaining systematic error is corrected by a fixed 5th-order polynomial. After the loop is closed, Fig. 31.2.5 (top) shows the error in the resulting DCO output frequency of 12 samples over temperature and supply voltage. This is less than ±200ppm (+190/-130 ppm) from -40°C to 85°C, which corresponds to a TC of 2.56ppm/°C (box method). The measured line sensitivity of the worst-case sample is 580ppm from 0.85 to 1.05V supply voltage, corresponding to a supply sensitivity of 0.29%/V. As shown in Fig. 31.2.5 (bottom), the measured RMS period jitter is 7ps or 196ppm of the period. The Allan Deviation floor is effectively improved by the closed-loop operation, reaching a <2ppm floor beyond 40s measurement time.

Figure 31.2.6 summarizes the performance of the proposed frequency reference and compares it to previous work. Its accuracy (2.56ppm/°C) represents a >3× improvement on [1,2] and is in line with the state-of-the-art [4]. Compared to [4,5], this work is 5× more energy-efficient, and is also much smaller. These results demonstrate that the proposed dual-RC frequency reference can achieve sufficiently high accuracy and low energy consumption to be used in IoT applications.

Acknowledgement:
This paper was supported by the Samsung Research Funding & Incubation Center of Samsung Electronics under Grant SRFC-IT1701-08 and the Samsung Electronics Company, Ltd., Hwaseong, Korea.

References:

[1] A. Khashaba et al., "A 34μW 32MHz RC Oscillator with ±530ppm Inaccuracy from -40°C to 85°C and 80ppm/V Supply Sensitivity Enabled by Pulse-Density Modulated Resistors," *ISSCC*, pp.66-67, Feb. 2020.
[2] M. Ding et al., "A 0.9pJ/cycle 8ppm/°C DFLL-Based Wakeup Timer Enabled by a Time-Domain Trimming and an Embedded Temperature Sensing," *IEEE Symp. VLSI Circuits*, pp. 1-2, June 2020.
[3] J. Lee et al., "A 1.4V 10.5MHz Swing-Boosted Differential Relaxation Oscillator with 162.1dBc/Hz FOM and 9.86ps$_{rms}$ Period Jitter in 0.18μm CMOS," *ISSCC,* pp.106-107, Feb. 2016.
[4] Ç. Gürleyük et al., "A 16MHz CMOS RC Frequency Reference with ±400ppm Inaccuracy from -45°C to 85°C After Digital Linear Temperature Compensation," *ISSCC*, pp.64-65, Feb. 2020.
[5] Ç. Gürleyük et al., "A CMOS Dual-RC Frequency Reference With ±200-ppm Inaccuracy From –45°C to 85°C," *IEEE JSSC*, vol. 53, no. 12, pp. 3386-3395, Dec. 2018.
[6] W. Choi et al., "A Compact Resistor-Based CMOS Temperature Sensor with an Inaccuracy of 0.12°C (3σ) and a Resolution FoM of 0.43 pJ·K² in 65-nm CMOS," *IEEE JSSC*, vol. 53, no. 12, pp. 3356-3367, Dec. 2018.
[7] J. A. Angevare and K. A. A. Makinwa, "A 6800-μm² Resistor-Based Temperature Sensor With ±0.35°C (3σ) Inaccuracy in 180-nm CMOS," *IEEE JSSC*, vol. 54, no. 10, pp. 2649-2657, Oct. 2019.

Authorized licensed use limited to: TU Delft Library. Downloaded on March 22,2022 at 09:43:52 UTC from IEEE Xplore. Restrictions apply.

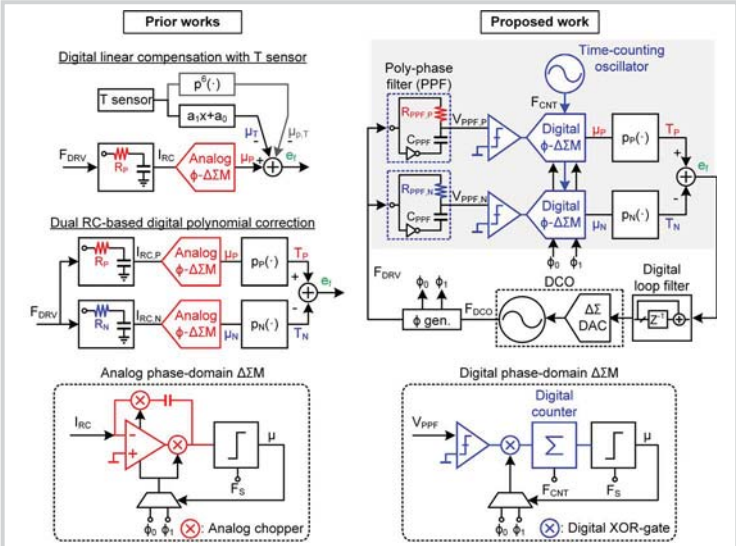

Figure 31.2.1: Comparison of the digital-domain temperature-compensated FLL in prior works with the analog-intensive internal temperature sensor and phase-domain ΔΣ modulator (left), and the proposed dual-RC reference (right).

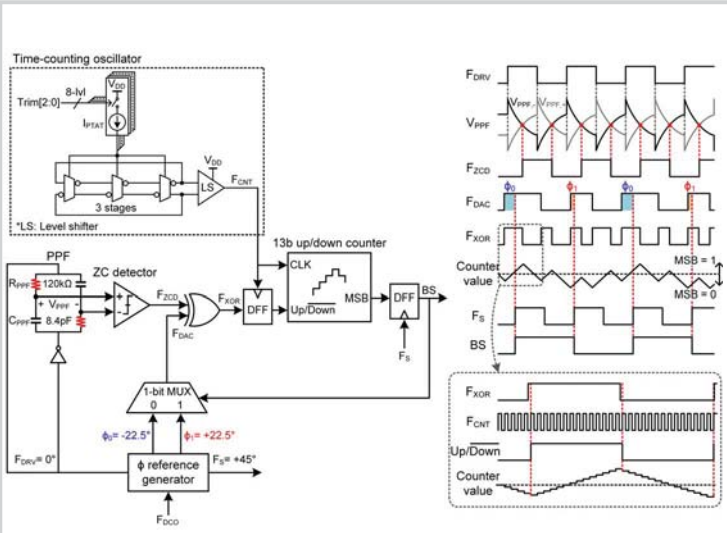

Figure 31.2.2: Block diagram and operating principle of the proposed PPF-based digital Φ-ΔΣM.

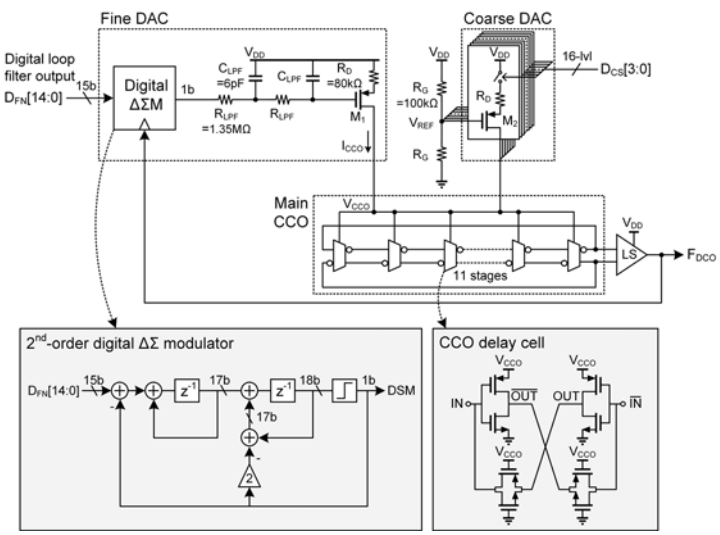

Figure 31.2.3: Circuit implementation of the DCO.

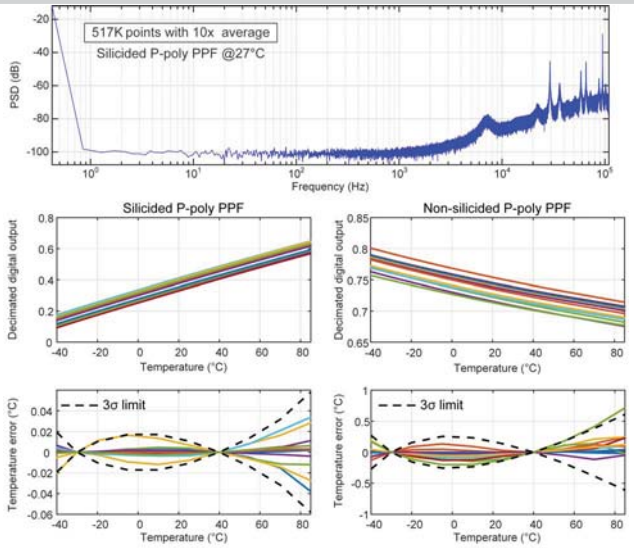

Figure 31.2.4: Measurement results: PSD of the digital Φ-ΔΣM, Decimated digital output versus temperature and Temperature error of Silicided P-poly and P-poly PPF sensors.

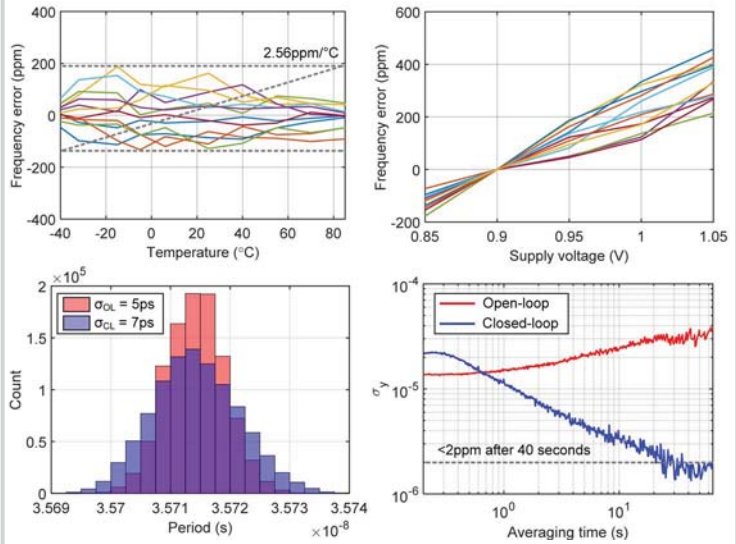

Figure 31.2.5: Measurement results: Frequency error versus temperature, Frequency error versus supply voltage, Period jitter, and Allan Deviation.

Publication	This Work	Gürleyük JSSC18 [5]	Gürleyük ISSCC20 [4]	Cristiano VLSI20	Khashaba ISSCC20 [1]	Ding VLSI20 [2]
Technology	**65nm**	180nm	180nm	180nm	65nm	40nm
Frequency	**28MHz**	7MHz	16MHz	116kHz	32MHz	428kHz
Supply voltage [V]	**0.85-1.05**	1.7-2.0	1.6-2.0	1.8-2.0	1.1-2.3	1-1.4
Area [mm²]	**0.06**	1.65	0.3	1.2	0.18	0.07
Power [μW]	**142**	750	400	0.694	34	0.38
Energy/cycle [pJ/cycle]	**5**	107	25	5.98	1.06	0.9
TC compensation	High-order compensation				1st-order compensation	
Polynomial order	**5**	4	1 / 6†	-††	1	
Temp. range [°C]	**-40 to 85**	-45 to 85	-45 to 85	-15 to 85	-40 to 85	-40 to 80
TC [ppm/°C]	**2.56**	2.5	6.15 / 1.54†	8.7	8.4	8
Line sensitivity [%/V]	**0.29**	0.18	0.12	0.38	0.008†††	0.27
# of samples	**12**	8	20	10	6	1
Period jitter	**7ps (196ppm)**	23.8ps (166ppm)	39ps (624ppm)	-	24ps (768ppm)	-
Allan deviation floor [ppm]	**2**	0.33	0.32	4	2.5	10

† Applying 6th-order polynomial function, †† Piece-wise linear approximation (LUT), ††† Using LDO

Figure 31.2.6: Performance summary and comparison with the state-of-the art works.

Authorized licensed use limited to: TU Delft Library. Downloaded on March 22,2022 at 09:43:52 UTC from IEEE Xplore. Restrictions apply.

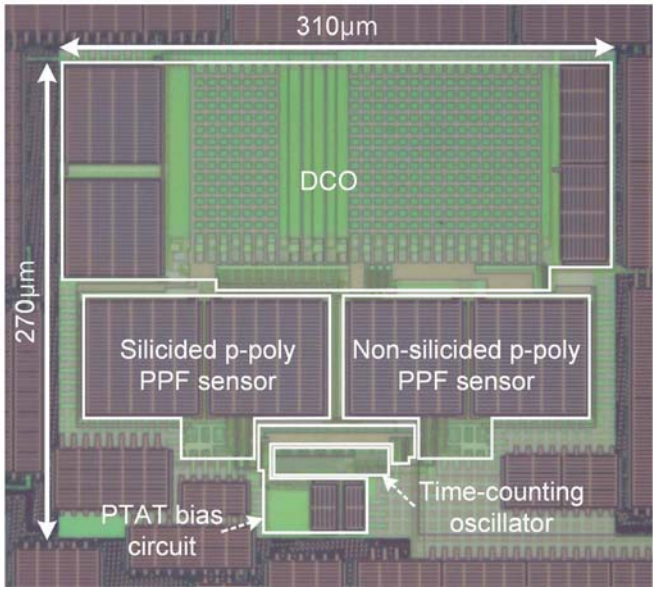

Figure 31.2.7: Die micrograph.

978-1-7281-9549-0/21/$31.00 ©2021 IEEE
Authorized licensed use limited to: TU Delft Library. Downloaded on March 22,2022 at 09:43:52 UTC from IEEE Xplore. Restrictions apply.