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5.6 A 25A Hybrid Magnetic Current Sensor with 64mA Resolution, 1.8MHz Bandwidth, and a Gain Drift Compensation Scheme

Amirhossein Jouyaeian[1], Qinwen Fan[1], Mario Motz[2], Udo Ausserlechner[2], Kofi A. A. Makinwa[1]

[1]Delft University of Technology, Delft, The Netherlands
[2]Infineon Technologies, Villach, Austria

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Magnetic current sensors are used in switched-mode power supplies and motor drivers, where both galvanic isolation and wide bandwidth (BW) are desired. In CMOS, Hall-effect sensors are widely used, but their resistance results in a fundamental trade-off between BW and resolution. Coils have a differentiating characteristic and so can achieve much wider BW and resolution, but cannot sense DC.

By using Hall sensors for low frequencies and coils for high frequencies, wide-band hybrid sensors can be realized [1,2]. In [1], two Hall/coil pairs sense the differential magnetic field around a current rail, thus rejecting CM external fields. The sensor achieves 480mA$_{rms}$ resolution from DC to 3MHz, while dissipating 38.5mW. However, its front-end senses coil voltage, which limits its high-frequency dynamic range (DR), and requires a DC servo loop based on a large (10µF) external capacitor. In [2], the front-end senses the current of a single coil, and thus achieves wider bandwidth (15.3MHz), at the expense of robustness to CM fields. Moreover, its Hall and coil paths are combined off-chip, and it achieves lower resolution (710mA$_{rms}$) and dissipates more power (63.5mW).

This work presents a hybrid current sensor that measures the differential field around a lead-frame-based current rail. By sensing coil current and employing a pole-zero cancellation scheme, its front-end achieves high DR and resolution without external components. Compared to [1], it achieves similar BW (1.8MHz), but with 7.5× better resolution (64mA$_{rms}$), 2× less power dissipation (19.5mW) and 50% less chip area (4.6mm^2).

As shown in Fig. 5.6.1 (top), the current rail consists of a low-resistance (250µΩ) S-shaped lead-frame, which concentrates the magnetic field seen by its two Hall/coil pairs (by about 2× compared to a straight rail) [3]. Each Hall sensor consists of 4 spinning-current Hall plates connected in parallel. The currents in the plates are designed to flow in different directions, resulting in a significant reduction of offset and stress sensitivity [3].

A simplified block diagram of the Hall and coil paths is shown in Fig. 5.6.1 (bottom). Since coil current is proportional to the derivative of lead-frame current (I_{rail}), the coil path consists of a two-stage integrator. The 1st stage is a transimpedance amplifier with a pole at f_{p1}, which ensures that high-frequency components of I_{rail} do not cause its output to clip. To block offset, its output is AC-coupled to the 2nd stage, where it is combined with the output of the Hall path. The 2nd stage implements a pole at f_{p2} and a zero at $f_{z2} = f_{p1}$, thus realizing a coil path with a pole at f_{p2}. By appropriately setting the gain of the Hall path, the overall transfer function is flat, while the Hall sensor's thermal noise is filtered above the crossover frequency $f_c = f_{p2}$, which is chosen to balance the noise contributions of the coil and Hall paths.

A more detailed schematic of the current sensor is shown in Fig. 5.6.2, and the corresponding Bode plots are shown in Fig. 5.6.3. The 1st stage of the coil path (A_1) realizes f_{p1} = 200kHz (R_1C_1). Above this frequency, C_1 (25pF) limits its output swing to ~1.125V when I_{rail} ~25A. The 2nd stage (A_2) realizes f_{z2} = 200kHz (R_3C_3) and f_{p2} = 10kHz (R_4C_3). The coil path thus behaves like an integrator with a 10kHz pole, as shown in Fig. 5.6.3 (left). Although this could be done in a single stage, R_1 would be very large (3MΩ), which, together with the low coil resistance R_{coil} (3.3kΩ), would cause the output of A_1 to clip on its own offset (~2mV). The proposed architecture allows R_1 to be small (32kΩ), resulting in ~20mV offset at the output of A_1. This is then blocked by C_2 (260pF), which together with R_2 (480kΩ) defines a pole at 1.25kHz, and thus has a negligible effect above f_c. The offset of the 2nd stage is amplified by a gain of 2 (R_4=R_{LPF1}+R_{LPF2}), and so it also has a negligible effect (~4mV) on the front-end's output offset. To ensure robustness to spread, the time constants R_1C_1 and R_3C_3 are realized by the same type of components. Also, the large temperature coefficient (TC = 0.36%/K) of R_{coil} is cancelled by realizing $R_{1,3}$ with silicided n-poly resistors (TC = 0.31%/K). R_2 is implemented with a p-poly resistor, whose low TC (-0.02%/K) leads to an overall coil-path TC of 0.03%/K.

To minimize the power consumption of their biasing circuitry, the two spinning Hall sensors are stacked (Fig. 5.6.2). The TC of their sensitivity is compensated by biasing them with a temperature-dependent current (~4mA at room temperature) derived from two trimmable currents with positive (I_{PTC}) and negative (I_{NTC}) TCs, as shown in Fig. 5.6.2. These are implemented by forcing PTAT and CTAT voltages ΔV_{GS} and V_{GS}, generated by a pair of subthreshold biased PMOS transistors, across two resistors.

Figure 5.6.3 (right) shows the transfer function of the various stages of the Hall path. To reduce Hall sensor offset, the spinning-current technique is employed, in which the Hall voltage is up-modulated to twice the spinning frequency ($2f_s$ = 100kHz), while its offset remains at DC [1]. Due to the lead-frame's dimensions, the distance between the two Hall sensors is rather large (~2.4 mm). To maintain signal integrity, their outputs are boosted by local capacitively-coupled amplifiers (CCAs) with a gain of 50 ($A_{3,4}$), before being summed and demodulated by a similar CCA (A_5), which also has a gain of 50. A_2 then combines the outputs of the Hall and coil paths. The CCAs use switched-resistors to realize large DC feedback resistances (>1GΩ), which establish zeros (~500Hz) that block the offsets of the Hall sensors and $A_{3,4}$.The up-modulated offset of A_5 only experiences unity gain, and is filtered by a 50kHz LPF realized by R_{LPF1}, R_{LPF2}, and C_{LPF}. After each spinning-current transition, deadband switches at the virtual ground of A_5 are used to block the resulting thermal settling transients of the Hall sensors, thus reducing their residual offset [4].

$A_{1,2}$ are Miller-compensated amplifiers, with folded-cascode input stages and Class-AB output stages to handle the induced coil currents, and drive external loads (20pF), respectively. To maximize their noise efficiency, $A_{3,4}$ are telescopic current-reuse amplifiers. The equivalent input-referred noise levels of A_1 and $A_{3,4}$ are designed to match the thermal noise of R_{coil} (3.3kΩ) and R_{Hall} (350Ω), respectively.

The current sensor occupies 4.6mm^2 in a 0.18µm CMOS process (Fig. 5.6.7, top). It draws 3.5mA from a 1.8V supply and 4mA (for the Hall sensors) from a 3.3V supply. It is isolated from the lead-frame by a non-conductive die attach (Fig. 5.6.7, bottom). The measured sensitivities of the coil and Hall paths are shown in Fig. 5.6.4, (top left). They both vary by less than 9% from -45°C to 85°C, as shown in Fig. 5.6.4 (top right). The sensor's response to 8A$_{pp}$ sine-wave currents at 500Hz, 10kHz and 500kHz is shown in Fig. 5.6.4 (bottom). After trimming the sensitivity of the Hall sensors (via their bias current), the current sensor's sensitivity (30mV/A) is flat to within 1dB from DC to 1MHz. This is limited by amplifier peaking and the BW of the differential-to-single-ended converter used to drive the spectrum analyzer (Fig. 5.6.5, top left). The sensor's noise spectral density is shown in Fig. 5.6.5 (top right). The total in-band noise (DC to 1.8MHz) corresponds to a resolution of 64mA$_{rms}$, of which the coil and Hall paths contribute 26% and 74%, respectively. As shown in Fig. 5.6.4 (bottom left), the dead-band switches reduce the sensor's offset by about 2×. They also help reduce the input-referred spinning ripple to about 0.26A (74µT with the conversion rate of 283µT/A), which is similar to [1]. The sensor's response to a large current step (0A to 25A) is shown in Fig. 5.6.5, bottom right.

In Fig. 5.6.6, the sensor's performance is summarized and compared with other state-of-the-art CMOS-compatible magnetic current sensors. It achieves the highest resolution (×2.3), the lowest power (×1.8), and the highest dynamic range among hybrid sensors (+13dB), the highest FoM (×22) with off-chip current rail, as well as a wide DC to 1.8MHz BW.

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References:

[1] J. Jiang and K. Makinwa, "Multipath Wide-Bandwidth CMOS Magnetic Sensors," *IEEE JSSC*, vol. 52, no. 1, pp. 198-209, Jan. 2017.
[2] T. Funk et al., "An Integrated and Galvanically Isolated DC-to-15.3 MHz Hybrid Current Sensor," *IEEE APEC*, pp. 1010-1013, 2019.
[3] Mario Motz et al., "A Miniature Digital Current Sensor with Differential Hall Probes Using Enhanced Chopping Techniques and Mechanical Stress Compensation," *IEEE Sensors*, pp. 1-4, Oct. 2012.
[4] J. C. van der Meer et al.,"A Fully Integrated CMOS Hall Sensor with a 3.65 µT 3σ Offset for Compass Applications," *ISSCC*, pp. 246-247, Feb. 2005.
[5] Y. Li, M. Motz and L. Raghavan, "A Fast T&H Overcurrent Detector for a Spinning Hall Current Sensor With Ping-Pong and Chopping Techniques," *IEEE JSSC*, vol. 54, no. 7, pp. 1852-1861, July 2019.
[6] T. Funk and B. Wicht, "A Fully Integrated DC To 75 Mhz Current Sensing Circuit with On-Chip Rogowski Coil," *IEEE CICC*, April 2018.
[7] Allegro MicroSystems, ACS37002 Data Sheet, Accessed on Aug. 10, 2020. Available: https://www.allegromicro.com/en/products/sense/current-sensor-ics/zero-to-fifty-amp-integrated-conductor-sensor-ics/acs37002.

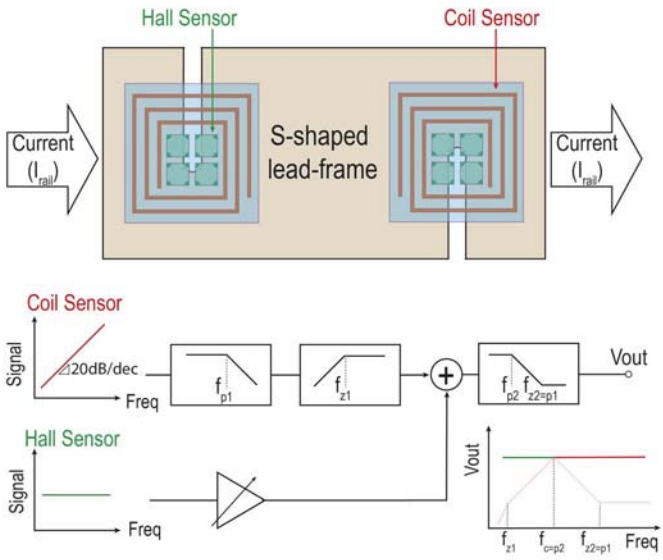

Figure 5.6.1: Simplified system block diagram. The Hall sensor consists of 4 Hall devices (Square N-well + 4 quarter-circle contacts) in quadruple architecture.

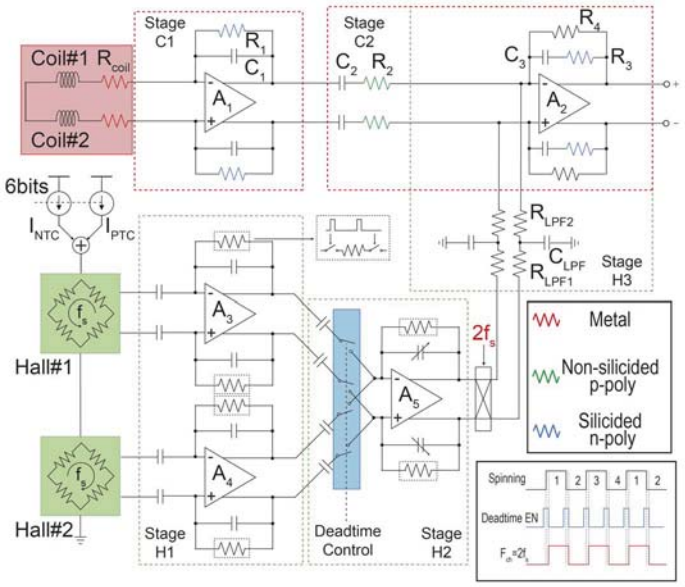

Figure 5.6.2: Full system block diagram.

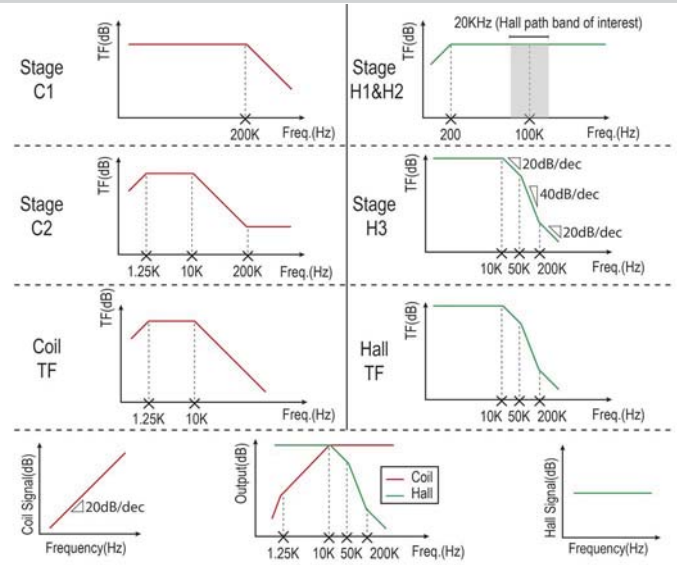

Figure 5.6.3: Transfer functions of different stages in the coil path (left) and Hall path (right).

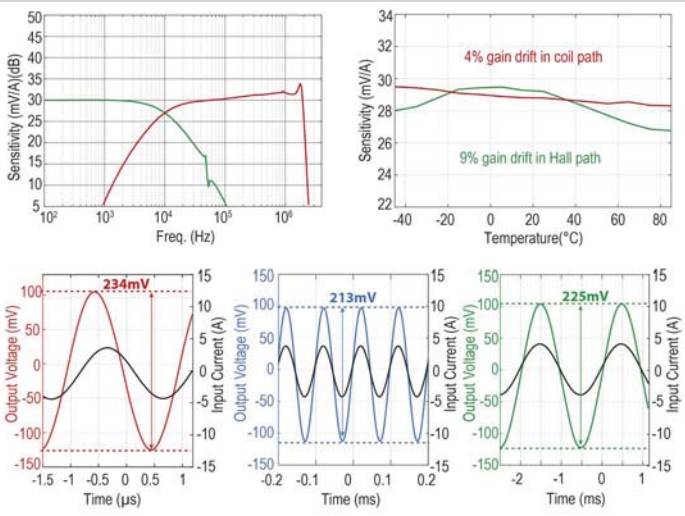

Figure 5.6.4: Measured performance of the Coil (Red) and Hall (Green) paths. Sensitivity vs. frequency (1A p-p) (top left). Sensitivity vs. temperature (1Ap-p @ 100Hz & 100kHz)(top right). Output transient response (after 1024× averaging) (8Ap-p @ 500kHz, 10kHz and 500Hz) (bottom left, middle, right).

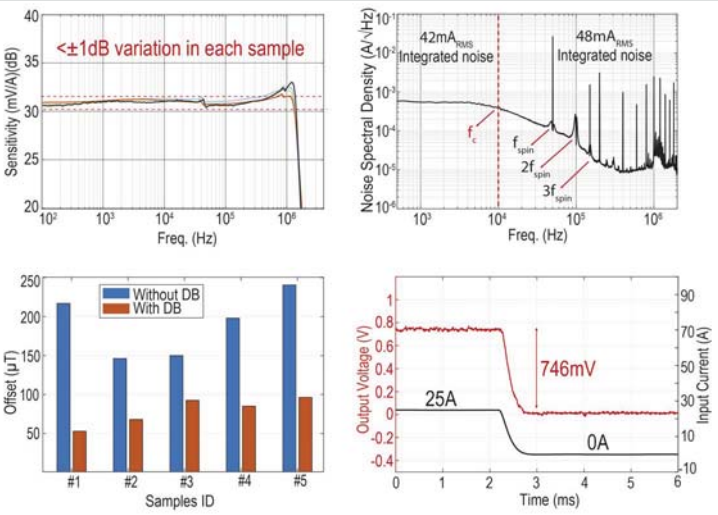

Figure 5.6.5: Measured sensor performance (after 100× averaging): Sensitivity vs. frequency (4 samples, 1A p-p)(top left). Noise spectral density referred to current rail (top right). Offset referred to current rail with dead-band on/off (5 samples) (bottom left), 25A step response (bottom right).

Source	Our work	JSSC'17 [1]	JSSC'19 [5]	CICC'18 [6]	APEC'19 [2]	ACS37002 [7]
Sensor Type	Coil + Hall	Coil + Hall	Hall	Rogowski Coil + Hall	Rogowski Coil + Hall	Hall
Technology (µm)	0.18	0.18	0.35	0.18	0.18	N/A
Supply (V)	1.8/3.3	5	3.3	1.8	1.8	3.3
Area (mm²)	4.6	8.75	N/A	3.17	2.74	N/A
Resolution (mA_{rms})	64	480	480	150	710	160
Input Range (A_{rms})	+/- 25	+/- 3.3 +/- 18[a]	+/- 300	+/- 4.1 +/- 40[a]	+/- 60	+/-66.7
Dynamic Range (dB)	52	17	56	29	39	52
BW (MHz)	1.8	3	1.7	75	15.3	0.4
Power Consumption (mW)	19.5	38.5	13.2	33.7	63.5	39.6
FOM[b]	22.5	0.34	1.02	99[c]	0.48	0.39

[a]extrapolated

[b]$FOM = BW(MHz)/(Resolution(A_{rms})^2 \times Power(mw))$

[c]On-chip current rail

Figure 5.6.6: Performance summary and comparison with state-of-the-art CMOS magnetic current sensors.

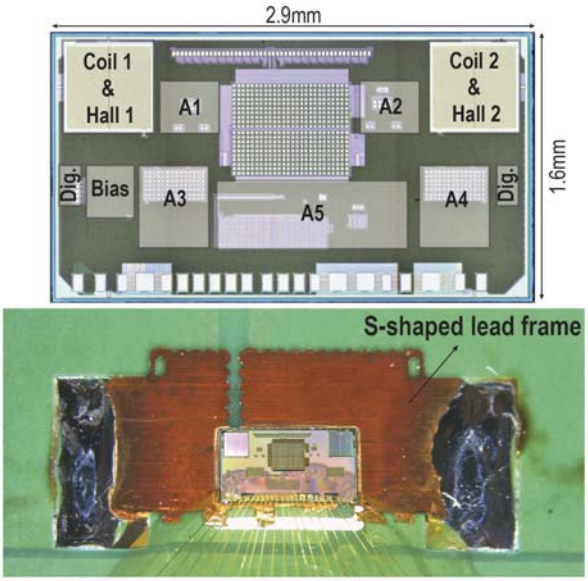

Figure 5.6.7: Die micrograph (top), Sensor die on a copper lead-frame (bottom).

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