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A ±2A/15A Current Sensor with 1.4 µA Supply Current and ±0.35%/0.6% Gain Error From −40 to 85 ˚C using an Analog Temperature-Compensation Scheme

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Abstract

This paper presents a ±2A fully-integrated current sensor with a 20 mΩ on-chip shunt (resistor). It employs an energy-efficient hybrid sigma-delta ADC with an FIR-DAC and consumes only 1.4 µA, a 3× improvement on the state-of-the-art. A tunable analog non-linear temperature-compensation scheme (TCS) allows ±2A currents to be digitized with 0.35% gain error from −40 to 85 ˚C. With a 3 mΩ PCB shunt, ±15A currents can be digitized with slightly more (0.6%) gain error. In a 0.18 µm CMOS process, the sensor occupies 1.6 mm^2.

Introduction

Coulomb counting demands accurate, low power, and low-cost current sensors [1,2,3]. In [1], both low power (5µA) and gain error (0.5%) are achieved with a low temperature coefficient (TC) off-chip shunt (resistor). Low-cost alternatives are PCB traces or integrated metal shunts [2,3], but both have high TCs (~0.3%/°C). In [3], a digital temperature-compensation scheme (TCS) based on an on-chip temperature sensor achieves 0.3% gain error but draws 13µA. In [1], the use of an ADC and a PTAT reference voltage (V_{REF}) draws less current (11µA), but only partially compensates for the TC of its integrated shunt, resulting in 0.9% gain error and even larger errors (4%) with a PCB shunt [6]. This work proposes using an energy-efficient ADC and a TC-tunable V_{REF}, which can then be flexibly used to obtain low gain error with both PCB traces and integrated shunts.

Current Sensor

The block diagram of the proposed current sensor is shown in Fig. 1a. An ADC uses a temperature-dependent V_{REF} to digitize the voltage V_S across a shunt. $V_{REF} = V_{PTAT}+V_{CTAT}/\lambda$ where λ can be tuned to match the shunt's TC (Fig.1b). Two different shunt types are used in this work: a 20 mΩ on-chip shunt based on four metal layers [1,3], and a 3 mΩ PCB shunt.

Fig. 2a shows the generation of V_{PTAT} (ΔV_{BE} ~65mV at 27°C) with a pair of NPNs and V_{CTAT} (V_{GS} ~50mV at 27°C) with a Dynamic Threshold-Voltage MOSFET (DTMOST). Fig. 4 shows the simulated variation of the digital output (D_{OUT}) over temperature; setting $V_{REF} = V_{PTAT}$ results in a gain error of 0.8% from −40 to 85 ˚C. To correct the systematic non-linearity due to the higher-order TCs of the on-chip shunt [3], a slightly non-linear V_{PTAT} is generated by combining NPNs with different units emitter areas. Adding V_{CTAT}/λ to the non-linear V_{PTAT} reduces the gain error to 0.1%.

Fig. 3 shows a single-ended block diagram of the fully-differential readout circuit. It is based on a 1st order ΔΣ ADC, which has a uniform impulse response and a time-independent response to input pulses. Its summing node consists of a capacitively-coupled instrumentation amplifier (CCIA), which allows the modulator to handle beyond-the-rail CM input voltages. In the 0.18µm process used, the combination of series-connected ESD diodes and a 3.8V I/O pad supply limits the CM voltage range to -0.3V to 5 V, which covers most of the single-cell battery applications.

An 8-tap FIR-DAC reduces the CCIA's input swing, which can then be based on an energy-efficient current-reuse OTA [4]. The CCIA is followed by a switched-capacitor integrator (Fig. 3). Its kT/C noise is suppressed by the CCIA's gain (25x), allowing the use of small sampling capacitors (C_A = 100 fF and C_B = 800 fF). By exploiting the FIR-DACs NTF notches, the CCIA (A_1, 400 nA) can be chopped at $f_{CH} = f_S/8$ without incurring quantization-noise folding. The integrator (A_2, 200 nA) is also chopped ($f_{CH2} = f_S/16$) to reduce its input-referred offset and 1/*f* noise. Finally, system-level chopping (SLC) is used ($f_{SLC} = f_S/256$) to further reduce the residual offset.

Since the scaling factor λ is quite large, it is realized via two feedback paths. One via the CCIA, consists of the V_{PTAT}-referenced FIR-DAC, and a second via the integrator, consists of a V_{CTAT}-referenced 1-bit DAC. λ is then the product of the CCIA's gain (25x) and the C_A/C_B's capacitor ratio.

Measurement Results

The current sensor was fabricated in a standard 0.18 µm CMOS process (Fig. 5) and draws 1.4 µA from a 1.8 V supply, of which the on-chip logic draws 600 nA. The decimator was implemented off-chip for flexibility. At a clock frequency of 32 kHz, the current sensor has a resolution of 5.4 μV_{RMS} in a conversion time of 15.625 ms.

Figs. 7 and 8 show the decimated output D_{OUT} of typical samples with on-chip and PCB shunts, respectively, for three different V_{REF} choices after a 25ºC gain trim. Using only V_{PTAT} results in a D_{OUT} variation of 0.8%/5%, using the non-linear V_{PTAT} reduces the systematic non-linearity, and, finally, adding V_{CTAT}/λ results in a D_{OUT} variation of less than 0.2%/0.5%.

After a 25ºC gain trim and with a fixed λ = +500, the measured gain error with the on-chip shunt was less than 0.35% for currents up ±2A from −40 to 85 ˚C (Fig. 9). With the PCB shunt and an adjusted λ = -50, this increased to 0.6% over a wider (±15A) current range (Fig. 10). As in [3], a D_{OUT}^2 correction factor reduces the effect of PCB shunt self-heating, which is not accurately sensed due to the imperfect thermal coupling between the PCB trace and the chip. The offset with (<500nV) and without SLC (<40µV) is shown in Fig. 11 for CM input voltages ranging from -0.3 to 5 V.

Table 1 summarizes the sensor's performance. Compared to the state-of-the-art, it requires 3x less supply current and achieves competitive gain error and offset with both PCB and integrated shunts.

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[3] S. Shalmany,*et.al.,JSSC*,2017 [4] R. Theertham,*et.al.*, *VLSI, 2019.*
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[6] L. Xu, *et al., SSCL, 2018*.

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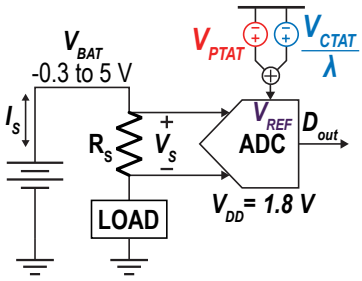

Fig. 1a: System block diagram.

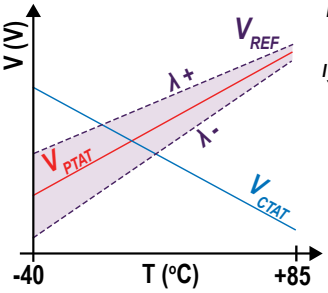

Fig. 1b V_{REF} over temperature.

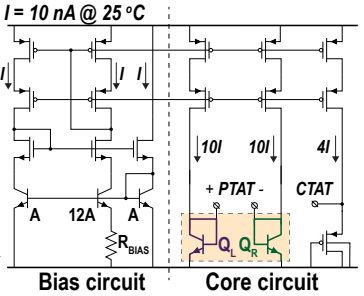

Fig. 2a: V_{REF} generation.

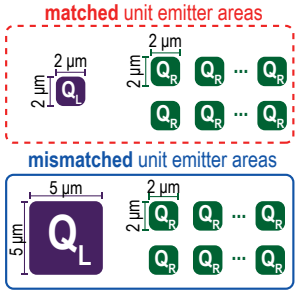

Fig. 2b: BJT layout options.

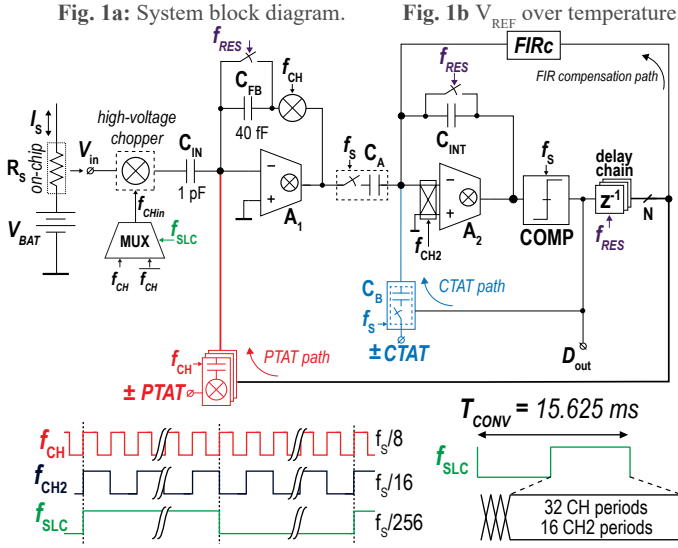

Fig. 3: Single-ended block diagram of the current sensor.

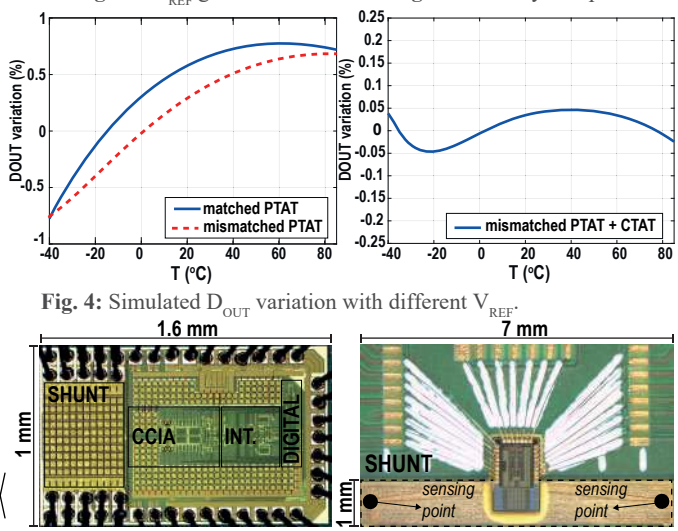

Fig. 4: Simulated D_{OUT} variation with different V_{REF}.

Fig. 5a: Chip micrograph. **Fig. 5b:** Chip on PCB trace.

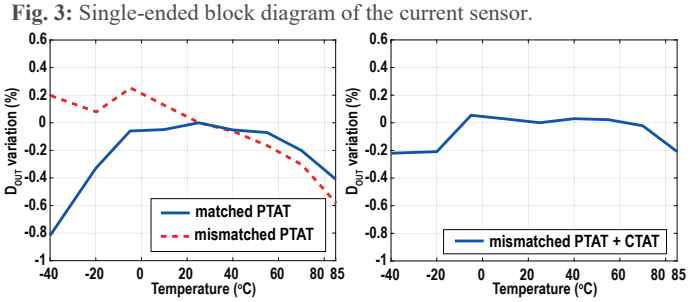

Fig. 7: Measured D_{OUT} variation: ***On-chip shunt***.

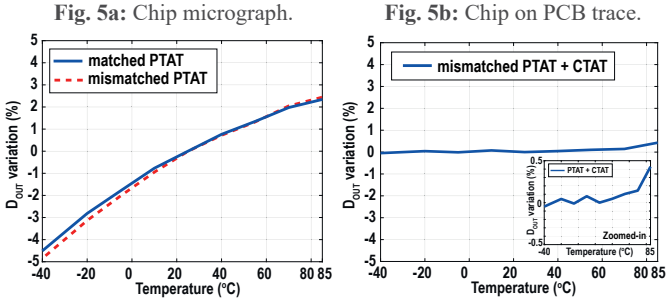

Fig. 8: Measured D_{OUT} variation: ***PCB shunt***.

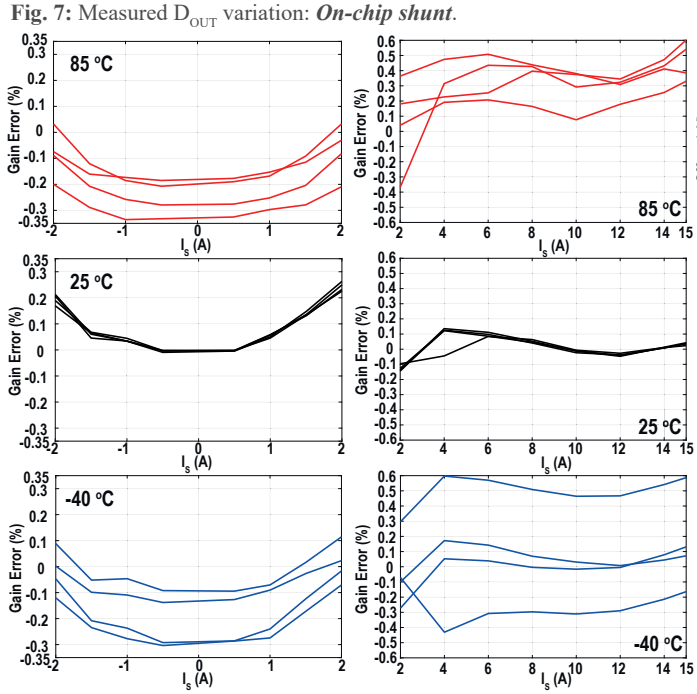

Fig. 9: Current sensor's gain error using the on-chip shunt.

Fig. 10: Current sensor's gain error using the PCB trace.

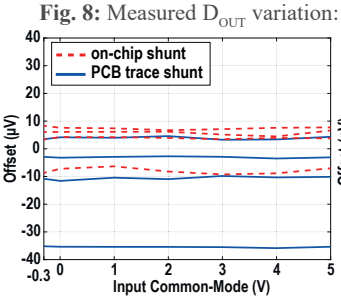

Fig. 11a: Offset w/o SLC.

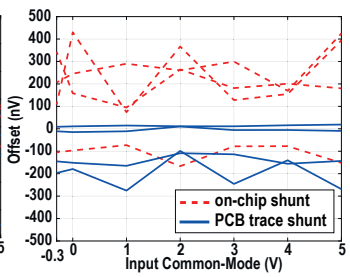

Fig. 11b: Offset with SLC.

Table. 1: Performance summary and comparison.

	This Work		ISSCC 20 [1]	ISSCC 18 [2]	JSSC 17 [3]		INA 260 [5]
I_{SUPPLY}	1.4 µA		< 5 µA	10.9 µA	13 µA		310 µA
Gain Error	on-chip	±0.35%	±0.5%*	±0.9%	on-chip	±0.3%§	±0.5%*
	PCB trace	±0.6%			lead-frame	±0.3%§	
I_{RANGE}	on-chip	±2A	±1A	±4A	on-chip	±5A	±10A
	PCB trace	±15A			lead-frame	±36A	
Shunt	on-chip	20 mΩ	50 mΩ*	10 mΩ	on-chip	10 mΩ	2 mΩ*
	PCB trace	3 mΩ			lead-frame	260 µΩ	
Offset	on-chip	25 µA	< 100 µA	40 µA	on-chip	4 µA	5 mA
	PCB trace	100 µA			lead-frame	400 µA	
ICMR	-0.3 to 5 V		0 to 60 V	0 to 25 V	0 to 0.75 V		0 to 36 V
V_{SUPPLY}	1.8 V		1.7 to 60 V	1.5 to 2 V	1.3 to 1.7 V		2.7 to 5.5 V
T_{RANGE}	-40 to 85°C		-50 to 125°C	-40 to 85°C	-40 to 85°C		-40 to 125°C
Tech.	0.18		0.18 BCD	0.18 BCD	0.13		

** Uses a custom/off-chip low-TCR shunt.*

§ Uses an extra ADC for temperature sensing allied with an extensive calibration.

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