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An Energy-Efficient 3.7-nV/ $\sqrt{\text{Hz}}$ Bridge Readout IC With a Stable Bridge Offset Compensation Scheme

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Abstract—This paper describes an energy-efficient bridge readout IC (ROIC), which consists of a capacitively coupled instrumentation amplifier (CCIA) that drives a continuous-time delta-sigma modulator (CTΔΣM). By exploiting the CCIA's ability to block dc common-mode voltages, the bridge's bias voltage may exceed the ROIC's supply voltage, allowing these voltages to be independently optimized. Since bridge output is typically much smaller than bridge offset, a digital to analog converter (DAC) is used to compensate this offset before amplification and thus increase the CCIA's useful dynamic range. Bridge loading is reduced by using a dual-path positive feedback scheme to boost the CCIA's input impedance. Furthermore, the CCIA's output is gated to avoid digitizing its output spikes, which would otherwise limit the ROIC's linearity and stability. The ROIC achieves an input-referred noise density of 3.7 nV/ $\sqrt{\text{Hz}}$, a noise efficiency factor (NEF) of 5, and a power efficiency factor (PEF) of 44, which both represent the state of the art. A pressure sensing system, built with the ROIC and a differential pressure sensor (AC4010), achieves 10.1-mPa (1σ) resolution in a 0.5-ms conversion time. The ROIC dissipates about 30% of the system's power dissipation and contributes about 6% of its noise power. To reduce the sensor's offset drift, a temperature compensation scheme based on an external reference resistor is used. After a two-point calibration, this scheme reduces bridge offset drift by 80× over a 50 °C range.

Index Terms—Beyond the rails, bridge offset compensation, bridge sensor, capacitively coupled (CC) chopper, CC instrumentation amplifier (CCIA), continuous-time delta-sigma modulator (CTΔΣM), energy efficient, readout IC (ROIC), temperature compensation.

I. INTRODUCTION

WHEATSTONE bridges are widely used to read out impedance sensors that monitor physical parameters such as temperature, pressure, and humidity [1]–[12]. As shown in Fig. 1, their output can be digitized by a readout IC (ROIC), which consists of an instrumentation amplifier (IA) and an analog to digital converter (ADC). To maximize the accuracy of the resulting sensing system, the ROIC should have low input-referred noise, low-temperature drift, high

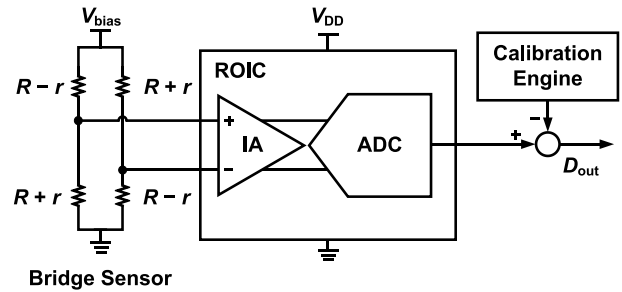


Fig. 1. Precision sensing systems.

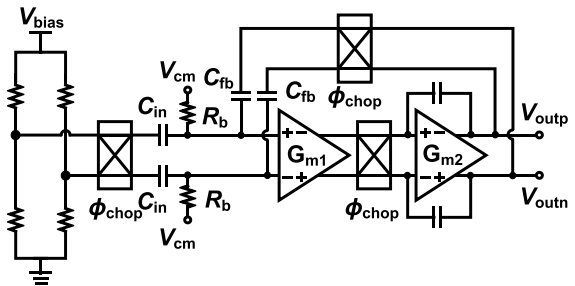


Fig. 2. Bridge readout using a CCIA.

input impedance, high linearity, and high common-mode rejection ratio (CMRR) [2], [13]. It should also have high energy efficiency to facilitate its use in battery-powered applications and in precision mechatronic systems where self-heating may be an issue [14].

An ROIC's energy efficiency will usually be determined by its IA, since this sets its input-referred noise. Recently, capacitively coupled (CC) IAs have been shown to be particularly energy efficient [3]. As shown in Fig. 2, a CCIA consists of an input chopper, which up-modulates differential input voltages to a chopping frequency, f_{chop} , allowing them to be amplified by an inverting amplifier with capacitive feedback elements. Since they only require one noise-critical input stage, CCIA's are generally more energy efficient than three-Opamp and current-feedback (CF) IAs [15]. Moreover, their input capacitors naturally block common-mode (CM) input voltages, allowing them to handle CM levels much larger than their supply voltages [4]. In bridge readout applications, this means that the bridge and the ROIC can be powered from different voltage supplies, allowing the ROIC's supply voltage to be optimized for energy efficiency. Last but not the least,

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since CCIA's are inherently chopped, their $1/f$ noise and offset are also quite low.

A major drawback of CCIA's is that they generate output spikes at their chopping transitions, i.e., at $2f_{\text{chop}}$ [3]. These should not be digitized since their amplitude is usually not a linear function of the input signal. In the case of a discrete-time ADC, this can be readily achieved by sampling the output of the CCIA just before the chopping transitions [3]. The CCIA's bandwidth then needs to be wide enough to ensure complete settling, which increases noise aliasing and thus degrades the ROIC's overall energy efficiency [5]. Furthermore, the ADC's sampling frequency f_s is now the same as $2f_{\text{chop}}$, which limits design flexibility. In [6], a dynamic filter has been used to limit the noise bandwidth while maintaining settling accuracy, but at the expense of increased design complexity.

This paper describes a pressure sensing system that consists of an energy-efficient ROIC and a bridge-type pressure sensor [16]. The ROIC uses a gated continuous-time delta-sigma modulator (CT $\Delta\Sigma$ M) to digitize the CCIA's output while avoiding its output spikes. To maximize the CCIA's useful dynamic range, the bridge offset is compensated by a passive digital to analog converter (DAC) referred to the bridge biasing voltage. This ratio-metric approach ensures that the compensating signal only depends on capacitor and resistor ratios, and so is stable over temperature and bias voltage variations. Implemented in a standard CMOS 180-nm process, the ROIC achieves a state-of-the-art noise efficiency factor (NEF) of 5. It dissipates about 30% of the system's power and contributes about 6% of its noise power, resulting in a resolution of 10.1 mPa (rms) with a range of ± 100 Pa in a 0.5-ms conversion time.

The rest of this paper is organized as follows. Section II discusses the main techniques used in the ROIC to achieve high energy efficiency and high precision. Section III describes the implementation details of the ROIC, while the experimental results of the ROIC and pressure sensing system with temperature calibration are presented in Section IV. Section V provides the conclusion.

II. SYSTEM DESIGN OF THE ROIC

Differential pressure sensors with a range of ± 100 Pa are required in air gages for industrial applications [7]. The AC4010 is a high-resolution bridge-type piezo-resistive pressure sensor that can cover this range. To achieve a resolution of 10 mPa (rms) over 1-kHz bandwidth, its biasing voltage V_{bias} should be at least 5 V, thus resulting in a sensitivity of about $45 \mu\text{V}/\text{Pa}$. However, this will be superimposed on a bridge offset of about 100 mV, due to the mismatch of its piezo-resistive elements (nominally $3.7 \text{ k}\Omega$ each), to ensure that the ROIC does not limit the sensor's performance, it should be designed to meet the specifications in Table I.

A. Dual-Supply Sensing System

Conventionally, the supply voltage of an ROIC must be somewhat larger than the bridge's CM level, despite the fact that the bridge's output is quite small [2], [9], [10], [17]. This

TABLE I
TARGET SPECIFICATIONS OF THE ROIC

Specifications	Value
Input noise density	4 nV/ $\sqrt{\text{Hz}}$ ($\sim 1 \text{ k}\Omega$)
Conversion time	0.5 ms
Input CM level	2.5 V
Input range	$\pm 100 \text{ mV}$ (offset), $\pm 10 \text{ mV}$ (signal)
Gain	≈ 100
Input impedance	$> 370 \text{ k}\Omega$ (for $< 0.1\%$ gain error)
Offset drift	$< 10 \mu\text{V}/^\circ\text{C}$
Power dissipation	$< 6.8 \text{ mW}$
INL	$< 50 \text{ ppm}$

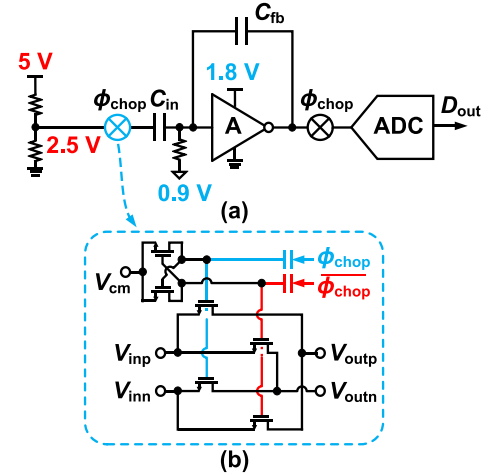


Fig. 3. (a) Proposed dual-supply sensing system (single-ended representation). (b) CCIA's CC input chopper.

constraint leads to a tradeoff between bridge sensitivity and ROIC power dissipation.

One way of avoiding this tradeoff is to exploit the beyond-the-rails capability of a CCIA. As shown in Fig. 3(a), the bridge can then be powered from a 5-V supply, while the ROIC can be powered from a 1.8-V supply voltage. The only active components exposed to the bridge's 2.5-V CM voltage are the switches of the CCIA's CC input chopper [Fig. 3(b)], which can be realized with deep n-well CMOS (DMOS) transistors or I/O devices [18]. The CCIA's input capacitors can be implemented by metal-insulator-metal (MIM) capacitors, which, in most processes, are capable of handling even higher voltages.

B. Compensating the Bridge Offset

Due to bridge mismatch, however, increasing V_{bias} will also increase bridge offset. Since this can be quite large, it will limit the IA's useful output range, and hence its gain. As a result, the succeeding ADC will need to have a wider dynamic range and lower input-referred noise, both of which will result in increased power dissipation.

To avoid this problem, bridge offset should be compensated before amplification. This can be done by using: 1) an external offset compensation network to trim the bridge [19] and 2) a current DAC to inject a programmable current into the bridge [20]. However, the bridge and the compensation

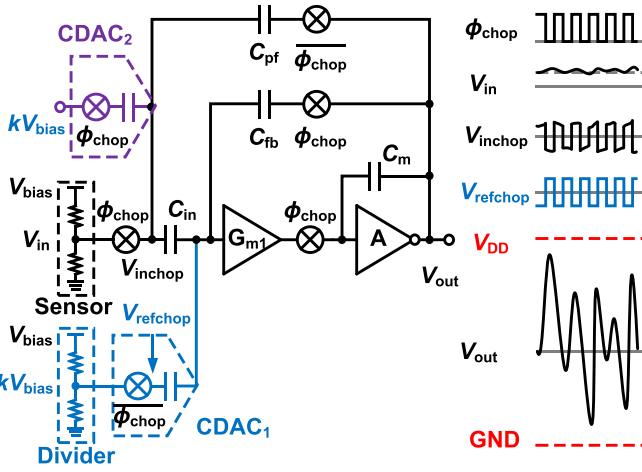


Fig. 4. Block diagram of the CCIA illustrating the operation of the bridge offset compensation and dual-path input impedance boosting loops.

circuitry will inevitably have different temperature dependencies, leading to significant temperature drift.

In this paper, the CCIA is used to implement a ratio-metric offset-compensation scheme (Fig. 4). The bridge output V_{in} is added to an offset-compensating signal generated by a capacitive DAC (CDAC₁), which is referred to V_{bias} via a resistive divider. By implementing both C_{in} (input capacitor of the CCIA) and CDAC₁ with MIM capacitors, both the bridge output V_{in} and the divider's output kV_{bias} will respond in the same way to temperature and V_{bias} variations.

Note that the residual bridge offset and bridge sensitivity will still drift over temperature. As shown in Fig. 1, such errors can be absorbed by an overall system calibration. However, the proposed bridge offset compensation minimizes the errors contributed by the ROIC, ensuring that the overall system accuracy is mainly limited by the bridge sensor.

C. Dual-Path Input Impedance Boosting Scheme

A known drawback of CCIA's is that they output spikes at twice the chopping frequency ($2f_{chop}$) [3]. This is because C_{in} must be rapidly charged and discharged at the chopping transitions. To reduce the amplitude of these spikes, most of the required charge can be provided from the output of the CCIA via a positive feedback path [3] or by an auxiliary pre-charge path [6], which also boosts the CCIA's input impedance. Although the boosting effect of a positive feedback path is limited by parasitic capacitors and stability considerations [3], it is more appealing in this design, as a pre-charge path requires active buffers which would compromise the CCIA's beyond-the-rails capability.

As shown in Fig. 4, a positive feedback path can be realized with an extra capacitor C_{pf} which should provide a compensation charge Q_{com} [3], given by

$$Q_{com} = C_{pf} V_{out} \approx C_{in} V_{in} = Q_{in} \quad (1)$$

where V_{in} consists of two parts, the useful bridge signal V_{sig} and the bridge offset V_{os} . However, in the proposed design (Fig. 4), V_{os} will be partially canceled by CDAC₁ before amplification. To still provide a charge proportional to the compensated offset, a capacitive DAC (CDAC₂) is added, and

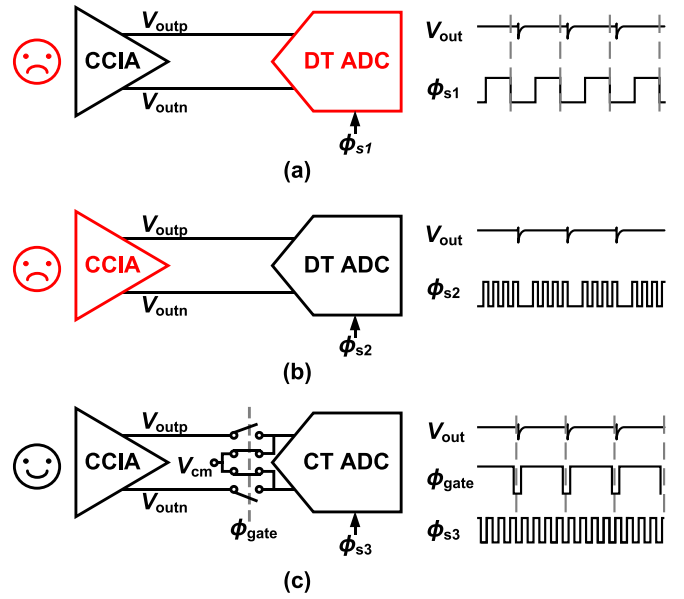


Fig. 5. Different ways to avoid digitizing the spikes of a CCIA by (a) using $f_s = 2f_{chop}$, (b) oversampling at quiet moments, and (c) using gated continuous-time integration.

driven by the same code as CDAC₁. The total compensation charge is now given by

$$Q_{com} = C_{pf} V_{out} + Q_{DAC} \approx C_{in} (V_{sig} + V_{off}) = Q_{in}. \quad (2)$$

D. Gating the Output of the CCIA

The CCIA's residual output spikes can be avoided by using a discrete-time $\Delta\Sigma$ modulator (DT $\Delta\Sigma$ M) to synchronously sample the CCIA's output. The modulator's sampling frequency f_s will then be equal to $2f_{chop}$, as shown in Fig. 5(a) [3], [5]. Assuming that the CCIA is a single pole system without slew rate limitations, a minimum bandwidth BW is needed to achieve sufficient settling [21]

$$BW \geq 2 \cdot (m + 1) \cdot f_s \cdot \ln 2 \quad (3)$$

where m is the target resolution of the ROIC in bits. Due to the sampling process, noise within a bandwidth of $\pi/2 \cdot BW$ will fold back to baseband, increasing the CCIA's in-band noise power density. This significantly decreases the ROIC's energy efficiency [5]. A dynamic RC filter can be used to limit the noise bandwidth before sampling [Fig. 5(b)] at the expense of increased design complexity [6].

In this design, the CCIA's residual spikes are avoided by gating the input of a CT $\Delta\Sigma$ M [4]. As shown in Fig. 5(c), the input of the CT $\Delta\Sigma$ M is connected to the CM voltage for the duration of the spikes, after which it is connected to the output of the CCIA. In this way, the errors associated with the CCIA's spikes are reduced without noise fold back. Compared to a switched-capacitor (SC) load, the resistive load presented by the modulator significantly relaxes the requirements on the CCIA's driving capability and thus further improves the ROIC's energy efficiency. Since the CCIA's output is effectively duty cycled, these benefits are acquired at the expense of a small reduction (2.5%) in its effective gain.

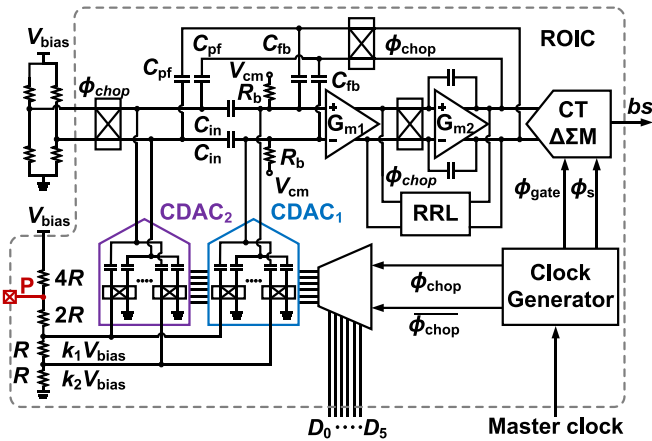


Fig. 6. Simplified circuit diagram of the bridge ROIC.

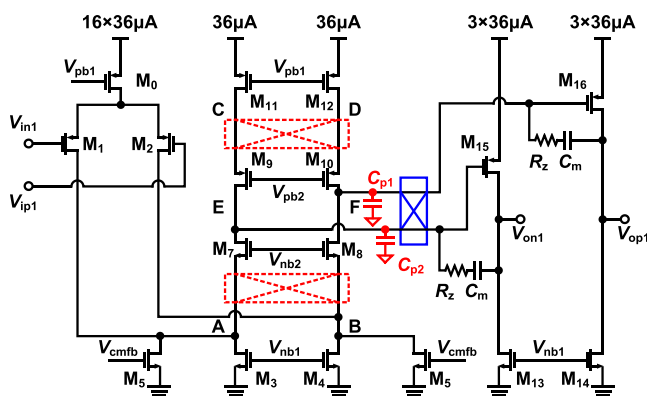


Fig. 7. Schematic of the CCIA main amplifier with demodulating chopper. (Bias circuits and CM feedback loop circuits are not shown.)

III. ROIC IMPLEMENTATION DETAILS

A simplified circuit diagram of the proposed ROIC is shown in Fig. 6. It consists of a CCIA with bridge offset-compensation circuitry and a gated CT $\Delta\Sigma$ M. In this section, the implementation of these blocks will be discussed in detail.

A. CCIA

The gain of the CCIA is set at 40 dB. To achieve high linearity, the CCIA is built around a two-stage Miller compensated amplifier, with a dc gain of about 124 dB. The bridge has an equivalent source resistance of 3.7 k Ω , corresponding to a noise density of 7.8 nV/ $\sqrt{\text{Hz}}$. The CCIA's input-referred noise should then be lower than this, which is quite challenging. The first stage consists of a chopped folded-cascode amplifier with a very large PMOS input pair (1280 μm /0.2 μm) that is biased in weak inversion to efficiently realize a trans-conductance of about 6.7 mS. As shown in Fig. 7, the input pair consuming most of the current of the amplifier. To mitigate the noise gain penalty due to the input pair's parasitic capacitance (1.3 pF), the CCIA's input capacitors C_{in} were set to 10 pF [3].

In this design, the offset and $1/f$ noise of the 1st stage is mitigated by chopping, while that of the 2nd stage is suppressed by the gain of the 1st stage. Often [2], [22], and [23], the demodulating chopper (drawn with dotted lines in Fig. 7) is located at nodes A and B and C and D. In this case,

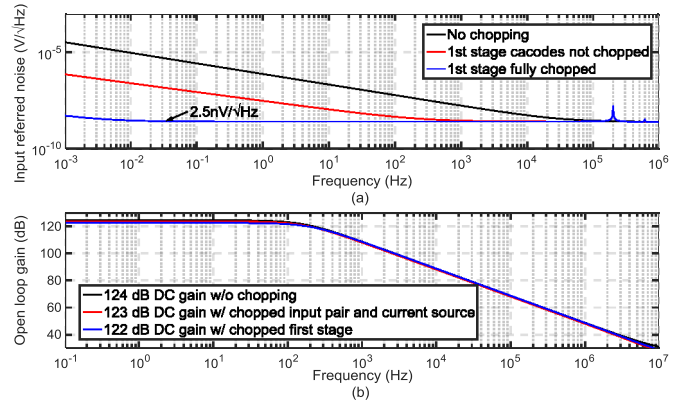


Fig. 8. Simulation results. (a) Amplifier's input-referred noise PSD. (b) Amplifier's open-loop gain.

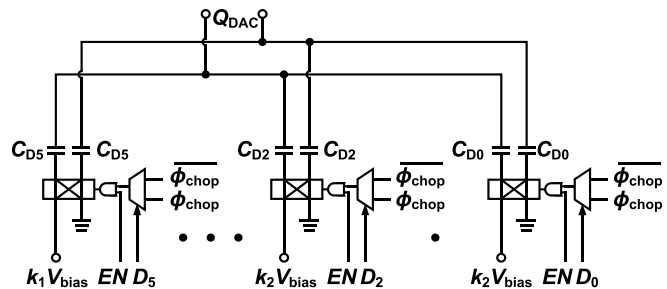


Fig. 9. Simplified circuit diagram of the offset compensation DAC.

the cascodes are not chopped and their $1/f$ noise becomes dominant, as shown in Fig. 8(a).

This can be addressed by moving the chopper to the output of the 1st stage, i.e., nodes E and F in Fig. 7. As shown in Fig. 8(a), chopping at 200 kHz results in a simulated 3.2 mHz $1/f$ noise corner. However, the chopped parasitic capacitors ($C_{p1,2}$) at these nodes will form an SC resistance, which, in turn, will reduce the gain of the 1st stage. To mitigate this, the cascode transistors were made relatively small ($M_{7,8}$: 24 $\mu\text{m}/1.8 \mu\text{m}$ and $M_{9,10}$: 60 $\mu\text{m}/1.2 \mu\text{m}$), and the layout was optimized. In this way, chopping only reduces the open-loop gain by 2 dB [Fig. 8(b)].

To minimize their noise contribution, the CCIA's bias resistors R_b should be in excess of 250 M Ω . To conserve area, they are implemented as SC resistors to achieve good linearity and stability over process and temperature variations [18]. The input chopper consists of capacitively driven DMOS transistors, allowing the input of the CCIA to handle bridge CM voltages up to 3.3 V (limited by the ESD-protection diodes) while operating from a 1.8-V supply.

B. Offset Compensation DAC

The bridge offset-compensation circuit consists of a 5-bit (D_{5-1}) binary weighted DAC with a redundant LSB (D_0) and a bank of chopper switches (Fig. 9). It is controlled by an external trimming code (D_{5-0}). The DAC compensates the bridge offset by effectively adding a scaled and chopped version of V_{bias} to the output of the bridge.

The total DAC capacitance should be kept small to minimize its impact on the CCIA's noise gain [18]. With a 5-V bias, a ± 100 -mV bridge offset can be expected. To bring the

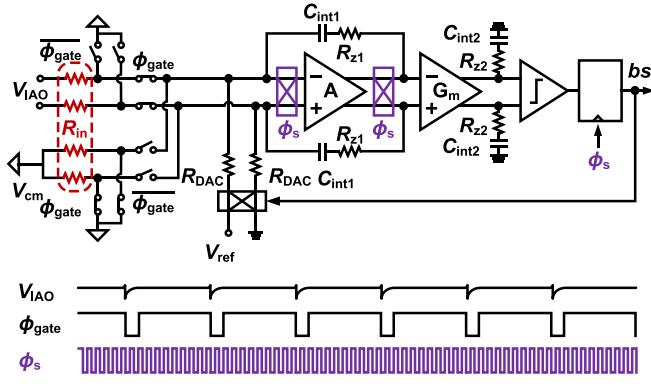


Fig. 10. Gated 2nd-order CTΔΣM.

offset into the input range of the CCIA, two references, $k_1 V_{bias}$ (1.25 V for D_{5-3}) and $k_2 V_{bias}$ (0.625 V for D_{2-0}), are derived from V_{bias} by a resistive divider. In this way, the DAC capacitance is reduced from 1.6 to 0.87 pF, $11.4\times$ smaller than C_{in} , ensuring that the divider's noise contribution is much less than the CCIA. The unity capacitances are 49.1 fF for D_{5-1} and 35.6 fF for D_0 (the smallest in the process).

The resistive divider has a total resistance of 36 kΩ, and is made from polysilicon resistors, which can handle bridge bias voltages up to 6.6 V. The chopper switches are protected by connecting the node P to an ESD-protected pad to ensure that the chopper gates are not exposed to voltages above the supply (Fig. 6). The polarity of the compensating signal can be inverted via the choppers, so the CCIA's output can be expressed as $(V_{in}C_{in} \pm Q_{DAC1})/C_{fb}$. The simulations show that the CCIA, including the DAC, achieves an input-referred noise density of 3.4 nV/√Hz and a $1/f$ noise corner of 18 mHz.

C. Gated CTΔΣM

As shown in Fig. 10, the CTΔΣM employs an energy-efficient 2nd-order feedforward topology. It consists of a gated RC integrator (1st stage), a G_m -C integrator (2nd stage), a 1-bit quantizer, and a resistive feedback DAC. The modulator's sampling frequency $f_s = 2$ MHz, which is enough to achieve the target resolution.

The 1st integrator, consuming about 190 μA, employs a folded-cascode OTA (A) with an 82-dB dc gain and a trans-conductance of about 0.86 mS. R_{in} and R_{DAC} , each 200 kΩ, are the main thermal noise sources of the CTΔΣM. R_{Z1} (0.74 kΩ) is added, in series with C_{int1} (35 pF), to compensate the right-half plane zero of OTA-based RC integrator. The 1st integrator is also chopped to reduce the impact of its $1/f$ noise on the ROIC's input-referred noise. Its chopping frequency is set at f_s to minimize quantization noise fold back [24]–[26]. Although this is much higher than the 1st integrator's $1/f$ corner, the associated drawbacks, such as reduced input impedance, reduced output impedance, and increased residual offset, are suppressed by the gain of the preceding CCIA.

The 1st integrator is gated by periodically swapping its input between the CCIA's output and the CM voltage. For linearity, the associated switches are located at the integrator's virtual ground to ensure that their ON-resistance is signal independent. As shown in Fig. 10, the gating scheme ensures that the

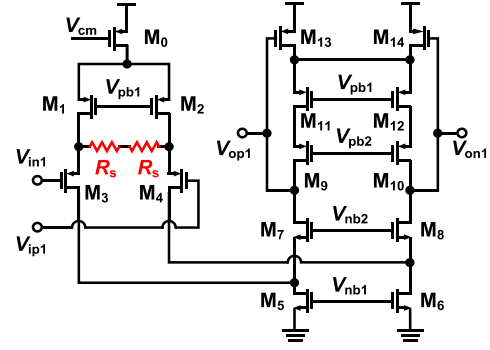


Fig. 11. Source degenerated OTA of the 2nd integrator.

CCIA's output is always loaded by the input resistors R_{in} , and thus minimizes gating transients. In this paper, the gating period is 2.5% of each chopping phase, resulting in a proportional decrease in the CCIA's equivalent gain. This gain is well-defined as ϕ_{gate} , ϕ_{chop} , and ϕ_s are derived from a 16-MHz external clock.

As shown in Fig. 11, the 2nd integrator employs a G_m -C topology based on a 310 source degenerated OTA (G_m in Fig. 10). The 2nd integrator employs a G_m -C topology based on a source degenerated OTA (G_m in Fig. 10). Since the 2nd integrator's noise will be suppressed by the gain of the 1st, the OTA only draws 20 μA.

The feedforward path of the 2nd-order ΔΣM is realized by adding R_{Z2} (110 kΩ) in series with integration capacitor C_{int2} (8 pF), with the value of the coefficient being well-defined by the ratio between the degeneration resistors R_s (100 kΩ) and the feedforward resistors R_{Z2} . Thus, the transfer function $H(s)$ from the input to the output of 2nd integrator can be expressed as

$$H(s) = g_{m2} \left(R_{Z2} + \frac{1}{sC_{int2}} \right) \approx \frac{R_{Z2}}{R_s} + \frac{1}{sR_sC_{int2}} \quad (4)$$

where g_{m2} is the transconductance of the OTA G_m shown in Fig. 10.

The jitter of the sampling clock will translate into input-referred noise, thus degrading the signal-to-noise ratio (SNR) of the CTΔΣM. However, the jitter requirement is relaxed by the relatively narrow signal band. The SNR_{jdc} determined by the sampling clock jitter σ_{jdc} is given by [1]

$$SNR_{jdc} = 10 \cdot \log \left(\frac{1}{16 \cdot OSR \cdot f_b^2 \cdot \sigma_{jdc}^2} \right) \quad (5)$$

where over sampling ratio (OSR) is 1000, and f_b is 1 kHz. Assuming 10-ps (rms) jitter, SNR_{jdc} is 118 dB, which is sufficient for bridge readout. In the worst case, 42-ps (rms) jitter would result in a noise level close to that of the ROIC. However, this noise power contribution, caused by clock jitter, to the pressure sensing system is less than 6%.

Similarly, the jitter of the gating clock σ_{jgate} in the 1st integrator also degrades the modulator's in-band noise performance. SNR_{jgate} determined by this jitter is given by [27]

$$SNR_{jgate} = 10 \cdot \log \left(\frac{1}{4 \cdot (V_{IAO}/V_{ref})^2 \cdot f_b \cdot f_{gate} \cdot \sigma_{jgate}^2} \right) \quad (6)$$

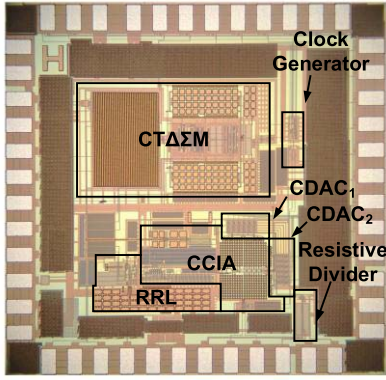
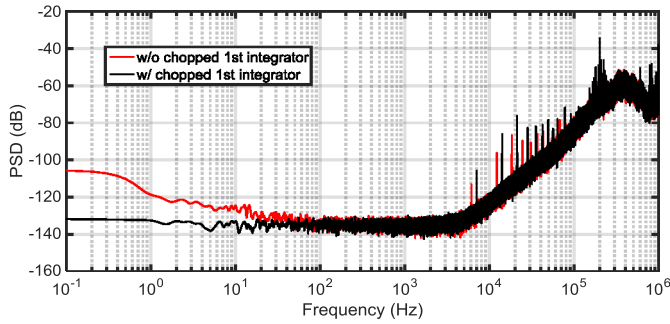


Fig. 12. Micrographs of the ROIC.

Fig. 13. Measured PSD of the ROIC's bitstream with 2×10^7 samples. (8× averaging was applied, and the residual offset was subtracted.)

where V_{IAO} is the CCIA output signal, and f_{gate} is 400 kHz. In the worst case, when V_{IAO} is ± 1 V, the resulted SNR_{jgate} with 10-ps (rms) jitter is 133 dB, 15 dB lower than the SNR_{jdac} .

IV. MEASUREMENT RESULTS

The ROIC was implemented in a 180-nm standard CMOS technology and has an active area of 0.73 mm^2 (Fig. 12). The core of the ROIC, including the CCIA, $\text{CT}\Delta\Sigma\text{M}$, CDAC_1 , CDAC_2 , and clock generator, consumes 1.2 mA from a 1.8-V supply. The on-chip resistive divider is supplied by the bridge bias voltage V_{bias} , which may be as high as 6.6 V.

The performance of the ROIC and that of the entire pressure sensing system have been characterized experimentally. The digital processing of the calibration has been done in MATLAB. The results will be described in Sections IV-A and IV-B.

A. Electrical Measurements

The fast Fourier transform (FFT) plots of the ROIC's output bitstream, based on 2×10^7 samples, is shown in Fig. 13. It can be seen that the modulator's 1st integrator must, indeed, be chopped to ensure that the ROIC's noise spectrum becomes flat from 0.1 Hz to 2 kHz. The spectrum corresponds to a $3.7\text{-nV}/\sqrt{\text{Hz}}$ noise level. By decimating the ROIC's output with an off-chip sinc^3 filter and then acquiring 2×10^8 samples of the filter's output over 100 s, its $1/f$ corner frequency was found to be about 0.04 Hz.

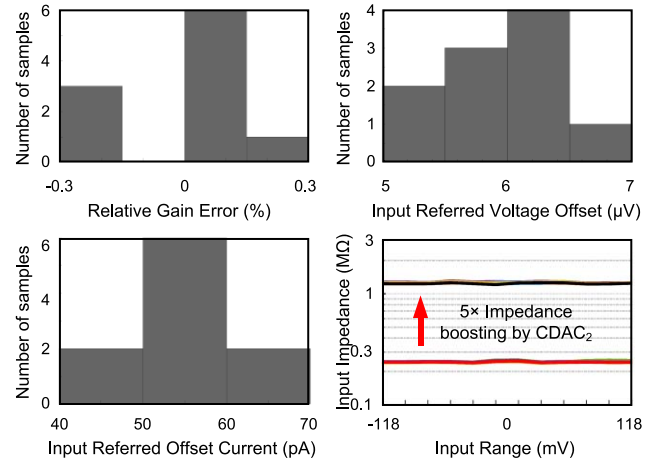


Fig. 14. Measured relative gain error, offset voltage, offset current, and the input impedance of the ROIC.

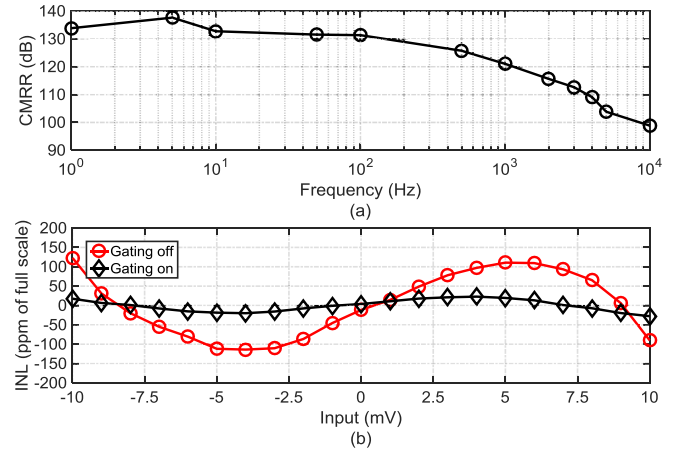


Fig. 15. Measured CMRR of (a) ROIC and (b) INL.

Measurements on 10 samples show that the ROIC achieves 0.3% relative gain error and $7\text{-}\mu\text{V}$ voltage offset (Fig. 14). Enabling CDAC_2 reliably boosts its input impedance by a factor of 5 (Fig. 14). The CMRR of the ROIC is shown in Fig. 15(a).

To test the effectiveness of the gating technique, a 118-mV signal with 2-k Ω source impedance was applied to the inputs of the ROIC when the resistive voltage divider was biased at 6 V. Gating the $\text{CT}\Delta\Sigma\text{M}$ reduces the ROIC's gain temperature drift from 74.6 to 8.9 ppm/ $^\circ\text{C}$, and reduces its offset temperature drift from 105 to 12.5 nV/ $^\circ\text{C}$. As shown in Fig. 15(b), gating the $\text{CT}\Delta\Sigma\text{M}$ also improves the ROIC's INL from 105 to 28 ppm.

The ROIC's performance is summarized in Table II and compared with the state of the art. It achieves both high accuracy and energy efficiency for $\pm 10\text{-mV}$ bridge signals, while accommodating up to 3.3-V input CM voltage. With a $3.7\text{-nV}/\sqrt{\text{Hz}}$ input-referred noise PSD, it achieves an NEF (in [28]) of 5 and a power efficiency factor (PEF) (in [29]) of 44.

B. System Measurements and Temperature Calibration

The ROIC was combined with an AC4010 pressure sensor to realize a pressure sensing system. As shown in Fig. 16(b),

TABLE II
STATE-OF-THE-ART ROICs

	This work	JSSC 2016 [1]	JSSC 2012 [2]	ISSCC 2018 [5]	JSSC 2017 [6]	ISSCC 2011 [8]	ESSCIRC 2012 [9]	VLSI 2017 [10]	L-SSC 2018 [11]
Architecture	CCIA + CTAEM	3-Opamp + DTAEM	CFIA + DTAEM	CCIA + DTAEM	CCIA + DTAEM	SHA + DTAEM	Gm-C CTAEM	CC-C TAEM	CC-C TAEM
Input stage	PMOS	PMOS	PMOS	PMOS	NMOS	PMOS	PMOS	PMOS	PMOS
Technology (nm)	180 nm	180 nm	700 nm	130 nm	180 nm	350 nm	700 nm	40 nm	180 nm
Active area (mm ²)	0.73	0.5	6	0.88	0.53 ²	1.2	3	0.06	0.75
Supply Voltage (V)	1.8	1.55	5	3	3.3	3.3	5	1.2	1.8
Supply Current (mA)	1.2	1.56	0.27	0.326 ¹	0.075 ²	2	0.24	0.0175	1.2
DC CMRR (dB)	134	--	140	124	109	--	120	--	137
CM Input Range (V)	0–3.3	--	0–2.5	--	0–3	0–3	0–2.5	--	0–3.3
INL (ppm)	28	--	5	--	5	--	15	79 ³	15
Gain Drift (ppm/°C)	8.9	--	0.7	--	0.81	--	--	--	7.7
Offset (μV)	7	--	0.05	2.4	1.8	--	1	300	72
Offset Drift (nV/°C)	12.5	--	6	--	70	--	--	--	12.3
Input noise density (nV/√Hz)	3.7	8.2	16.2	16	19	6.7	20	140	4.5
NEF ⁴ /PEF ⁵	5.0/44	12.5/242	10.4/541	11.1/372	6.41/136	11.6/444	12/720	22.6/613	6.1/67

1. Without taking account the current consumption of 1.5V supply. 2. Without taking account the ADC. 3. Estimated from THD. 4. $NEF = v_n \sqrt{2 \cdot I_{tot} / \pi \cdot U_T \cdot 4kT \cdot BW}$. 5. $PEF = NEF^2 \cdot V_{DD}$.

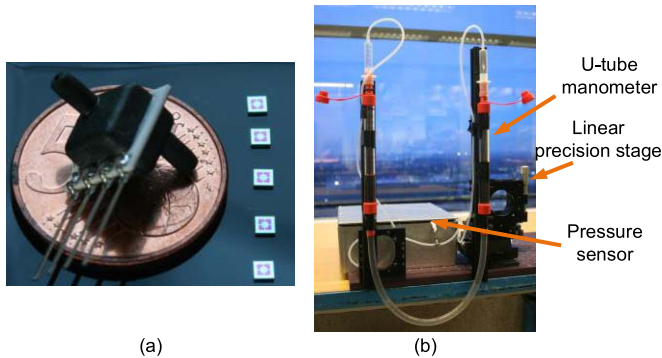


Fig. 16. (a) AC4010. (b) Differential pressure measurement setup.

the water-level difference in a U-tube manometer was precisely controlled by a linear stage to create a well-defined differential pressure [30].

Moving the right leg of the U-tube manometer relative to the left one by ± 10 mm with a 2.5-mm step, then results in ± 100 -Pa pressure change. The real-time response of the sensing system is shown in Fig. 17(a). The pressure sensing system has a pressure sensitivity of 0.0025 (1/Pa). To evaluate the system's resolution, the inputs of the differential pressure sensor were shorted to avoid mechanical interference from the environment. The pressure resolution, obtained from the standard deviation of 5000 samples (decimated by sinc³ filter with a length of 1000), is found to be 10.1 mPa

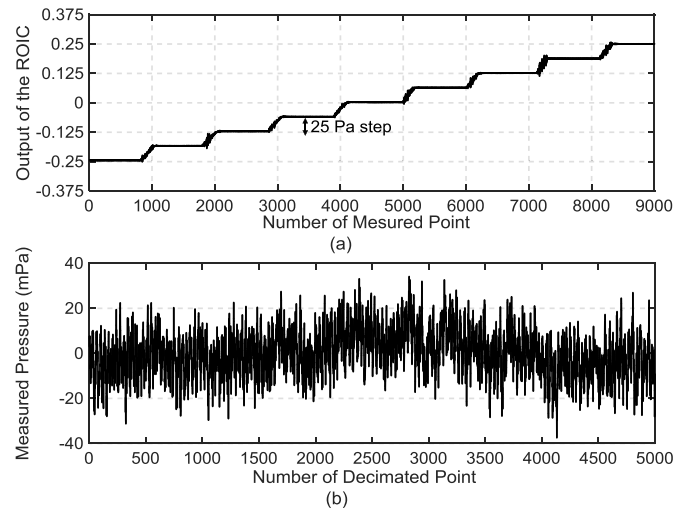


Fig. 17. Measurement results of the sensing system. Decimated output of the ROIC (a) with swept pressure input (the residual offset has been subtracted) and (b) with zero pressure input (shorted, the residual offset has been subtracted).

with a 0.5-ms conversion time for each decimated sample [Fig. 17(b)].

In practice, the temperature drift of a bridge sensor can be corrected by system calibration (Fig. 1). This usually involves exposing the bridge sensor to at least two well-defined temperature levels and measuring its output. The sensor's drift can then be corrected if the ambient temperature is known,

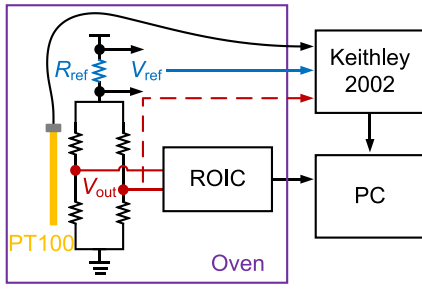


Fig. 18. Bridge sensor with reference resistor for temperature calibration.

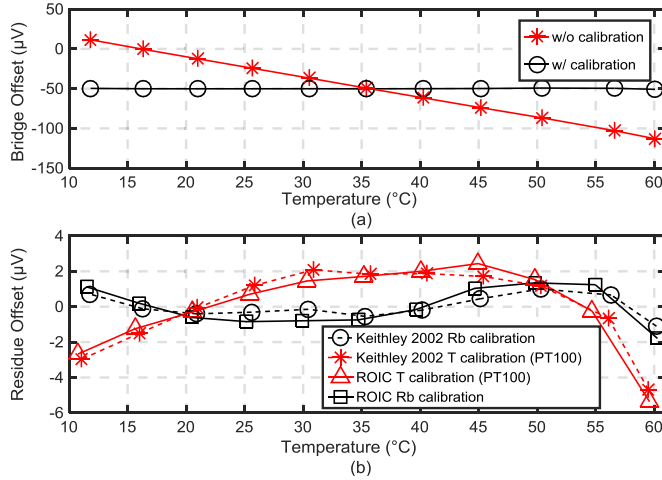


Fig. 19. Measured bridge offset drift (a) before and after calibrations and (b) residual offset drift.

e.g., by realizing a temperature sensor in the ROIC. However, the accuracy of this approach is limited by bridge self-heating, which can create temperature differences between the bridge and temperature sensor.

A more accurate approach is to use the bridge itself as a temperature sensor, by measuring its temperature-dependent resistance. To calibrate the bridge resistance over temperature, both the bridge sensor and the ROIC were placed in an oven-stabilized aluminum block next to a PT100 thermometer (Fig. 18). A reference resistor ($100\ \Omega$, $\pm 3\ \text{ppm}/^\circ\text{C}$ [31]) was placed in series with the bridge as a shunt current sensor. The voltage across the reference resistor was read out by Keithley 2002. In this way, the bridge resistance, and thus, the temperature on the bridge can be measured.

The effectiveness of the resulting calibration was tested by measuring the bridge sensor's offset drift over temperature. After a two-point calibration, the offset drift decreases from $244\ \mu\text{V}$ over a $50\ ^\circ\text{C}$ range, to about $3\ \mu\text{V}$ [Fig. 19(a)].

To compare the results of both methods and the output of the bridge is measured by both the ROIC and a Keithley 2002 (Fig. 18). As shown in Fig. 19(b), the residual offset with monitoring the bridge resistance (red curves) is about $2\times$ better than that obtained by monitoring the bridge temperature using PT100 thermometer (black curves). The residual errors obtained by the ROIC (solid curves) are in good agreement with that obtained by the Keithley 2002 (dashed curves).

V. CONCLUSION

An energy-efficient ROIC for a differential pressure sensing system has been presented. To maximize bridge sensitivity with high energy efficiency, the beyond-the-rails capability of a CCIA is exploited to allow the bridge biasing voltage to exceed the ROIC's supply voltage. A bridge offset compensation is implemented in a ratio-metric manner, which is robust to variations in temperature and bridge biasing voltage. A dual positive feedback path scheme is used to boost the input impedance of the ROIC. A gated-input CT $\Delta\Sigma$ M is proposed to digitize the amplified signal and avoid the error caused by the output spikes of the CCIA. Measurements show that the ROIC achieves both precision and energy efficiency with an NEF of 5, which represents the state of the art. The ROIC was tested together with a piezo-resistive differential pressure sensor. The experimental results show that the applied techniques are effective. The resulting pressure sensing system achieves 10.1-mPa (1σ) resolution with a 0.5-ms conversion time. The ROIC dissipates about 30% of the system's power dissipation and contributes about 6% of its noise power. Moreover, a temperature calibration, to reduce the bridge temperature dependence, has shown a factor of $80\times$ improvement on the system's offset drift over a $50\ ^\circ\text{C}$ range.

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