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A 10-to-12 GHz 5 mW Charge-Sampling PLL Achieving 50 fsec RMS Jitter, -258.9 dB FOM and -65 dBc Reference Spur

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***Abstract*— This paper presents a charge-sampling PLL (CSPLL), that demonstrates the best reported jitter-power FOM of -258.9 dB thanks to its high phase-detection gain and to the removal of the power-hungry buffer driving the phase detector. It also achieves -65 dBc of reference spur by both minimizing the modulated capacitance seen by the VCO tank and reducing the duty cycle of the sampling clock. Without requiring any RF dividers, a 50 μW frequency tracking loop is also introduced to robustly lock the CSPLL to a 100 MHz reference. Fabricated in 40-nm CMOS, the 0.13 mm^2 CSPLL achieves an RMS jitter of 50 fsec at 11.4 GHz while consuming 5 mW.**

***Keywords*— Charge-sampling PLL, charge-sampling phase detector, low-jitter, divider-less frequency tracking loop.**

I. Introduction

Low-jitter and low-spur PLLs are required for high-speed, high-resolution data converters, wireline, and wireless transceivers. A PLL using a sub-sampling phase detector (SSPD) can achieve low jitter while dissipating low power, as it eliminates the feedback divider and suppresses the charge pump and the phase detector noise thanks to its high phase-detection gain [1]. Unfortunately, the direct sampling of the VCO waveform by a low-frequency reference (REF) can introduce large reference spurs due to the periodic tank-capacitance perturbation, reference clock feedthrough, and charge injection from the sampling switch to the VCO. Reference spurs can be mitigated by minimizing the modulated capacitance (C_{MOD}) seen by the VCO tank and reducing the duty cycle of the reference (D_{REF}) [1]. However, decreasing the sampling capacitance to lower C_{MOD} can degrade the in-band phase noise (PN), whereas narrowing D_{REF} would require a massive switch to speed up the sampling transient, thus increasing both clock feedthrough and charge injection.

An isolation buffer with a resistive [1], or an inductive load [2] (Fig. 1 (a)) between the VCO and the SSPD can reduce C_{MOD}. However, this buffer operates at the VCO frequency (F_{VCO}), resulting in a substantial penalty in the PLL area, power consumption (P_{DC}), and jitter. Duty-cycled operation of this buffer by reducing D_{REF} can partially alleviate spurs and P_{DC} overhead [3], [4] (Fig. 1 (b)). Nevertheless, the transistors in the buffer should be wide to provide a high detection gain and a low noise at F_{VCO}. Hence, they draw relatively large current when the REF is high. Considering the size of the buffer devices, their input capacitance changes significantly when switching from the off-state to saturation and vice versa. Consequently, the VCO experiences a large C_{MOD}, limiting the PLL spur performance. In addition, the clock feedthrough issue still exists through the parasitic capacitance of the isolation buffer [4]. On the other hand, the REF pulse width (T_P) cannot be shorter than a few cycles (e.g., 5-10) of the VCO period (T_{VCO}) to ensure that the resonant buffer reaches its steady-state amplitude before the sampling instants. In the case of the resistive buffer, the common-mode settling time sets the shortest possible T_P. Consequently, even by using a gated isolation buffer, the improvement in the spur level and the power overhead is limited due to the clock feedthrough and the constraints on the minimum achievable C_{MOD} and D_{REF}.

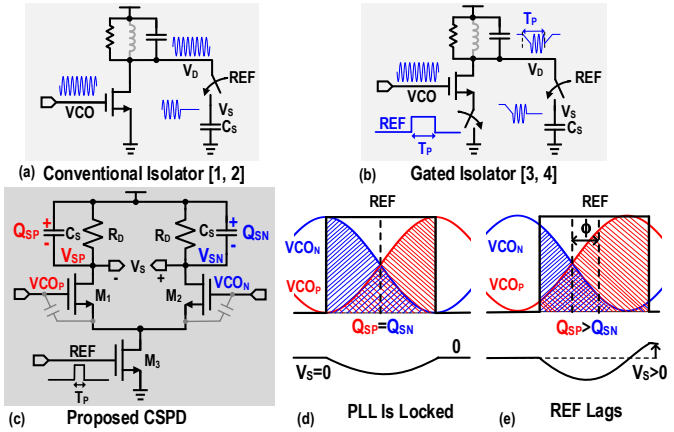

Fig. 1. Schematics of (a) the conventional isolator, (b) the gated isolator, and (c) the proposed CSPD, and input and output waveforms of CSPD (d) without and (e) with a phase error.

To solve the above-mentioned issues, we propose a charge-sampling PLL, which achieves a jitter-power FOM of -258.9 dB thanks to its high phase-detection gain and elimination of the power-hungry isolation buffer. It also demonstrates a reference spur of -65 dBc by simultaneously minimizing both C_{MOD} and D_{REF}. Furthermore, a 50 μW highly-digital frequency tracking loop without the usage of any RF divider is proposed to guarantee PLL's robust operation.

II. Proposed Charge-Sampling Phase Detector

Fig. 1 (c) shows the schematic of the proposed charge-sampling phase detector (CSPD). When the REF is high, $M_{1,2}$ convert the VCO's output voltage VCO_P-VCO_N=$2A_{VCO}\cdot\cos(\omega_{VCO}t+\phi)$ into a differential RF current, creating a charge difference Q_S=Q_{SP}-Q_{SN} $\propto \int_0^{T_P}(VCO_P - VCO_N)dt$, on the sampling capacitors (C_S), since $R_D \gg 1/C_S\omega_{VCO}$. If the VCO zero-crossings are at the center of the REF pulse, Q_S is zero, since the shaded blue and red areas are the same, as shown in Fig. 1 (d). Hence, the sampled differential voltage V_S (=V_{SN}-V_{SP}) remains zero

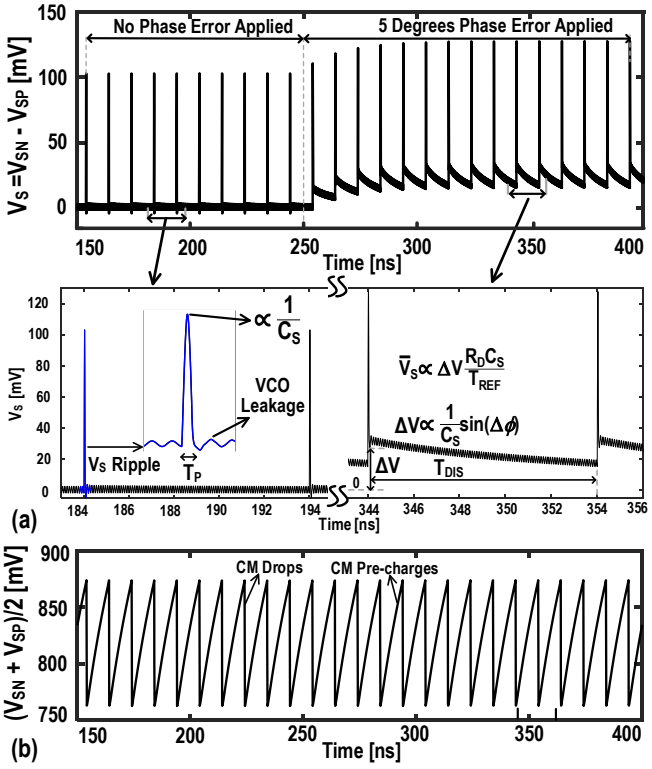

Fig. 2. Simulated transient response of the proposed CSPD to a 5 degrees phase step: (a) differential-mode response; (b) common-mode response.

after the phase comparison, corresponding to the ideal locking condition of the PLL. If there is any phase error (ϕ), as shown in Fig. 1 (e), the CSPD converts it into a non-zero Q_S and V_S, thus indicating that the PLL is not locked. Following the phase comparison, the REF becomes low for a duration of T_{DIS}=T_{REF}-T_P, and the sampling charge on C_S is *partially* discharged through the load resistance, R_D.

Fig. 2 shows the simulated transient waveforms of the CSPD output when a 5° phase step is applied to the VCO at 250 ns. It can be shown that the phase detection gain (K_{PD}) is approximately $2G_MA_{VCO}R_D\sin(0.5\omega_{VCO}T_P)/(\pi N)$, where G_M is the large-signal transconductance of $M_{1,2}$, and N is the frequency multiplication factor. K_{PD} is a periodic function of T_P and reaches its maximum at T_P=$0.5T_{VCO}$. Interestingly, K_{PD} does not depend on C_S, which can be intuitively explained as follows. The average value of V_S, thus K_{PD}, is mainly determined by its waveform in the discharging phase, since $T_{DIS} \gg T_P$. Note that the average value of a periodically decaying exponential function is proportional to its peak value ($\propto 1/C_S$) and time constant (R_DC_S). Consequently, C_S terms are cancelled in the K_{PD} expression.

As can be gathered from Fig. 2 (a), V_S experiences a ripple during each phase comparison even if the PLL is locked, introducing reference spurs. Since C_S value does not affect K_{PD}, V_S ripple can be easily suppressed by increasing C_S as long as the PLL phase margin is not degraded by the R_DC_S delay. For example, by considering a VCO tuning gain K_{VCO}=50 MHz/V, and choosing C_S>100 fF, the simulated spur due to V_S ripple can be reduced to <-90 dBc.

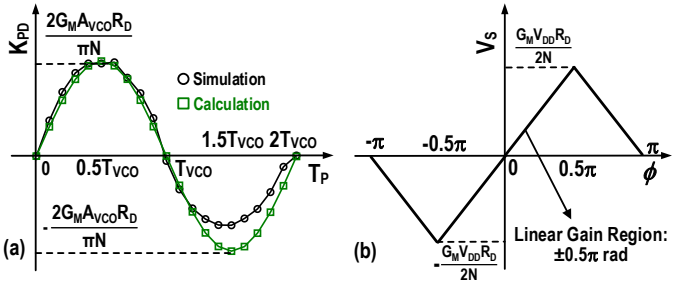

Fig. 3. (a) K_{PD} vs. the pulse width of the sampling clock when the oscillation voltage is sinusoidal. (b) CSPD output voltage vs. phase error when the oscillation voltage is square wave.

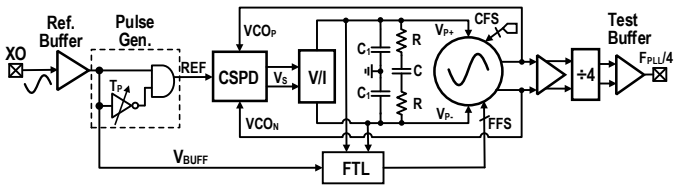

Fig. 4. Block diagram of the proposed CSPLL.

It should be mentioned that the common-mode (CM) voltage of the CSPD output drops when the REF is high, see Fig. 2 (b). K_{PD} would be potentially compromised if $M_{1,2}$ enter the triode region, as shown in Fig. 3 (a), where the simulated K_{PD} deviates from its theoretical value if a larger T_P is used. Therefore, a large C_S and very narrow pulse width (e.g., $0.5\,T_{VCO}$) for REF *must* be used to keep $M_{1,2}$ in saturation during each phase comparison. When the REF is low, the CM output voltage is pre-charged to a high level such that $M_{1,2}$ can be turned on very fast (i.e., <15 ps), only limited by the on-resistance and parasitic capacitance of the tail switch M_3.

By considering the PLL stability, area, spur, and jitter, K_{PD} is chosen to be ~0.3 V/rad, achieved by R_D=100 kΩ and $(W/L)_{1,2}$=2 μm/40 nm. Utilizing such small devices significantly reduces C_{MOD}. Besides, D_{REF} (=T_P/T_{REF}) can be as low as 0.5/N (e.g., ~0.5%), further alleviating the reference spurs by 36 dB. Thanks to the achieved high K_{PD}, the simulated PLL in-band PN introduced by R_D and $M_{1,2}$ (considering both flicker and thermal noise) is <-133 dBc/Hz at 200 kHz offset from a 10 GHz carrier.

At first glance, the proposed CSPD seems similar to the isolated-sub-sampling phase detector [3], and active-mixer-adopted sub-sampling phase detector [4]. However, there are substantial differences. Firstly, due to the large time constant R_DC_S ($\gg 1/\omega_{VCO}$), the hold switches at the sampler output are not needed, while they are essential in [3], [4], since the phase error information gets lost right after the sampling due to the small R_DC_S time constant ($\sim 1/\omega_{VCO}$). Secondly, since the REF transition occurs near the peak of the VCO waveforms when the PLL is locked (see Fig. 1 (d)), the clock feedthrough mainly introduces an amplitude error instead of a phase error, lowering the spurs. On the contrary, the sampling edge in [3], [4] occurs exactly at the VCO zero-crossings, intensifying the spurs. Thirdly, when the oscillation voltage is a square wave, the CSPD

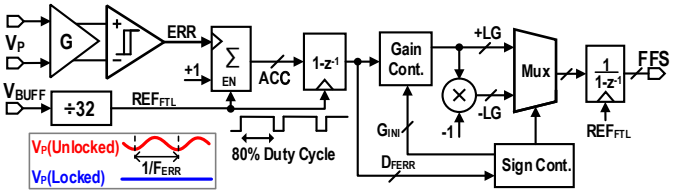

Fig. 5. Block diagram of the frequency tracking loop.

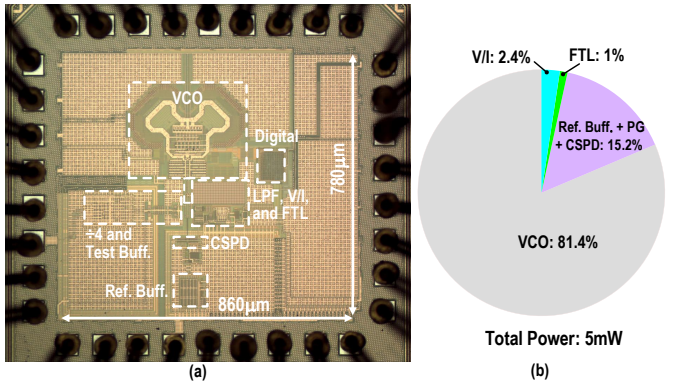

Fig. 6. (a) Chip micrograph and (b) measured power breakdown.

works properly and even exhibits a larger linear gain range (see Fig. 3 (b)). However, similar to the conventional SSPD, the phase detector range in [3], [4] becomes too narrow, thus requiring a power-hungry slope generator. Lastly, due to the integration operation [5], the *uncorrelated* noise of the falling and rising edges of the charge-sampling clock is multiplied by $N^2/2$ when transferred to the CSPLL output[1].

III. Charge-Sampling Phase-Locked Loop

The proposed PLL in Fig. 4 is composed of a continuous-time frequency tracking loop (FTL) and a type-II charge-sampling PLL (CSPLL). A reference buffer similar to [1] is employed to convert an off-chip 100 MHz sine wave into a square wave, which a pulse generator (PG) uses to realize a narrow pulse signal as the PLL reference. The pulse width of the PG (∼35-to-55 ps) can be digitally adjusted by a 4-b switched-capacitor bank. At the PLL start-up, a coarse frequency selector (CFS) first brings the VCO frequency close to the lock-in range of the PLL. The CSPD converts the phase error between the VCO and REF into a differential voltage, V_S. A fully differential V/I stage then rejects the common-mode ripples on the CSPD output and converts its desired differential-mode signal into a current, which is further filtered by the loop filter to generate a fine-tuning voltage V_P ($=V_{P+}$-V_{P-}) for the VCO.

Since the lock-in range of the CSPLL is limited ($\sim\pm7$ MHz), an FTL is required for a robust operation under PVT variations. In contrast to prior art [1]–[4], the proposed FTL consumes only $\sim 50\,\mu$W during the locking process, as it does not rely on any power-hungry RF dividers (see

[1]This alleviates the noise requirement of the pulse generator. However, the noise of the reference buffer is still multiplied by N^2, since both edges of the charge sampling clock are generated from the rising edge of the reference buffer output.

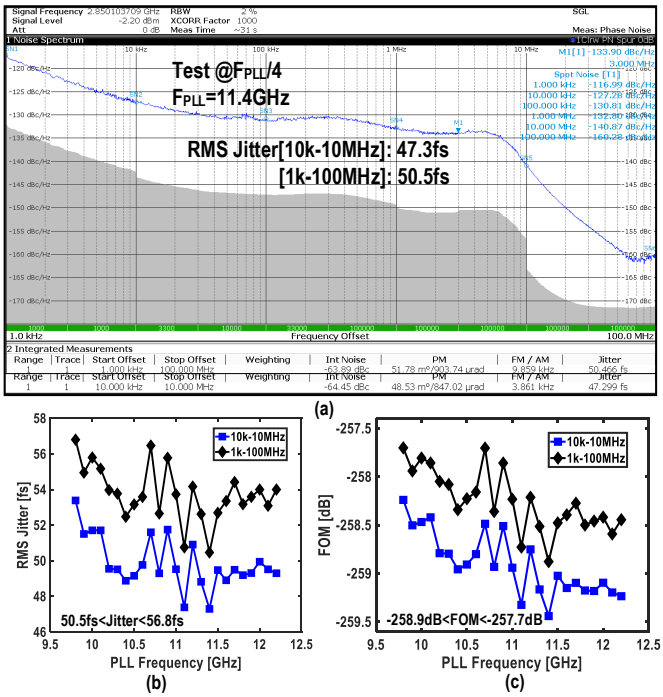

Fig. 7. (a) Measured phase noise at 11.4 GHz after an on-chip divide-by-4; (b) RMS jitter and (c) FOM across the tuning range.

Fig. 5). Once the CSPLL gets unlocked, an aliasing signal with a frequency of F_{ERR}=NF_{REF}-F_{VCO} is generated at V_P nodes instantly [6]. An amplifier and a Schmitt trigger are employed to convert this analog signal (with ∼20-to-40 mV amplitude) to a digital bitstream (ERR). Note that FTL should first determine F_{ERR} sign since ERR does not provide that information. Consequently, after sensing F_{ERR}, FTL is set to decrease the F_{VCO}. Depending on whether the frequency error is decreasing or increasing (by monitoring D_{FERR}), the initial loop sign is kept or flipped. To speed up the frequency locking process, FTL loop gain (LG) is adaptively controlled based on D_{FERR} value. Once FTL brings F_{VCO} into the lock-in range of the PLL, the CSPLL rapidly locks the VCO phase to REF, forcing a nearly constant V_P. Hence, ERR stops toggling due to insufficient gain of the amplifier, eliminating the power of the digital logic.

A frequency divider generates the FTL clock (REF_{FTL}) from the reference. The rising edge of ERR is counted only when the REF_{FTL} is high to ensure that the following digital blocks are synchronized with REF_{FTL}. As a result, REF_{FTL} frequency and duty cycle determine the minimum detectable F_{ERR}, which must be smaller than CSPLL lock-in range to ensure a seamless frequency locking operation.

IV. Measurement Results

The CSPLL was fabricated in an LP 40-nm CMOS process, and the core circuit occupies 0.13 mm^2, as illustrated in Fig. 6 (a). It dissipates ∼5 mW from 1.1 V and 0.6 V (for the VCO) power supplies, and its power breakdown is shown in Fig. 6 (b). The power and area overhead of the CSPD and FTL are negligible compared to the VCO.

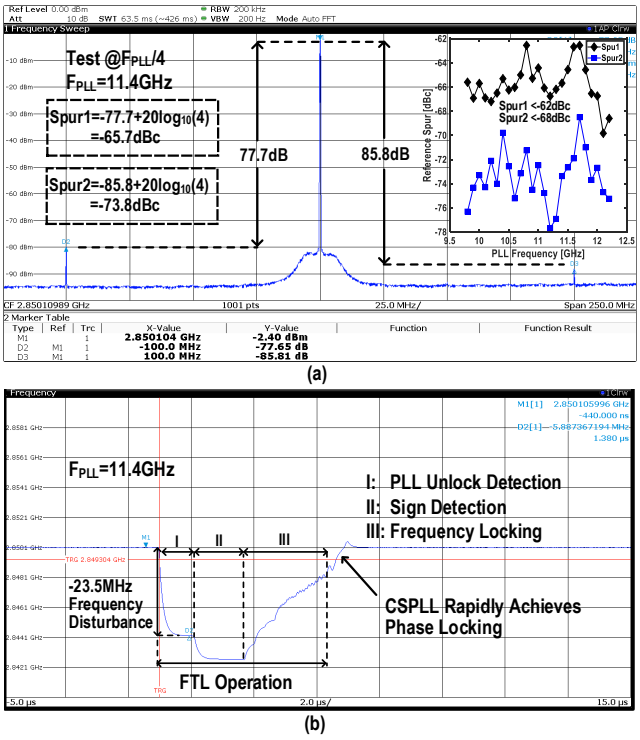

Fig. 8. (a) Measured CSPLL spectrum after an on-chip divide-by-4 and spur level across TR; (b) measured frequency recovery behavior.

Fig. 7 shows the measured PN and jitter after an on-chip divide-by-4. The restored in-band PN is -119 dBc/Hz at a 100 kHz offset from an 11.4 GHz carrier. Thanks to the high K_{PD} offered by the CSPD, the in-band PN is dominated by the reference buffer. The minimum integrated jitter is 50.5 fs (integrated from 1 kHz to 100 MHz but excluding the reference spurs) and varies by <7 fs across the tuning range (TR). This corresponds to a peak FOM of -258.9 dB. Note that T_P tuning code is initially adjusted to achieve the highest K_{PD} in the middle of the PLL TR (i.e., 11 GHz). Since K_{PD} varies <10 % across the PLL TR (i.e., 9.8-to-12.2 GHz) and shows a negligible (<1.5 fs) impact on the integrated jitter, T_P code is fixed during the measurements. However, to compensate for VCO gain variations, and to optimize jitter performance, the PLL bandwidth was digitally regulated at ∼7 MHz by adjusting the resistance of the loop filter and the transconductance of the V/I converter.

Fig. 8 (a) shows the measured reference spur across the TR. The worst-case spur is <-62 dBc, which is 10 dB lower than the integrated phase noise (∼-52 dBc). Hence, the impact of the spurs on integrated jitter is marginal. Since the negative and positive offset spurs are asymmetric, the origin of the -62 dBc spur is probably due to direct coupling (e.g., from the reference buffer to the VCO inductor), and not to up-conversion within the CSPLL [7]. EM simulations also confirm this hypothesis and show that a proper floor plan of the bond-pads, and shielding of the input reference clock would reduce the spurs level. Fig. 8 (b) shows the response of the FTL to an external frequency disturbance of ∼23 MHz injected to the VCO. The FTL successfully re-locks the VCO within 10 μs.

Table 1. Comparison with the state-of-the-art Integer-N PLLs.

	This Work	[2] ISSCC'19	[3] ISSCC'19	[4] JSSC'19	A. Sharkia ISSCC'18	J. Sharma ISSCC'18	J. Kim ISSCC'19
PLL Architecture	Type-II CSPLL	Type-II SSPLL	Type-II iSSPLL	Type-II SSPLL	Type-I SSPLL	Type-I RSPLL	Type-II SSPLL
F_{REF} [MHz]	100	200	103	100	100	50	100
F_{PLL} [GHz] FTR [GHz]	11.4 9.8-12.2	14 12-16	26.4 25.4-29.5	2.4 NA	5 4.6-5.6	2.55 2.05-2.55	3.8 3.3-4.3
Ref. Spur [dBc]	-65.7	-64.6	-63	-67	-64.1	-63	-75
Spur Jitter, σ_{spur} [fs]	10.2	9.5	6	41.9	28.1	61.8	10.5
RMS Jitter, σ_{rms} [fs] [Int. Bandwidth]	50.5 [1k-100MHz]	56.4 [1k-100MHz]	71 [1k-100M]	161 [10k-100M]	185.3 [10k-50MHz]	110 [10k-100M]	72 [1k-30MHz]
Total Jitter, σ_T [fs]	51.6	57.2	71.3	166.4	187.4	126.2	72.8
Power, P_{DC} [mW]	5	7.2	15.3 ^	0.9 #	1.1	3.7	19.1
*FOM [dB]	-258.9	-256.4	-251.1	-256.3	-254.2	-253.5	-250.1
**FOM_T [dB]	-258.8	-256.3	-251.1	-256	-254.1	-252.3	-250
***FOM_N [dB]	-279.5	-274.9	-275.4	-269.8	-271	-270.6	-265.8
Core Area [mm²]	0.13	0.234	0.24	0.42	0.01	0.36	0.21
Process [nm]	40	40	65	65	65	65	65

*$FOM = 20*\log_{10}(\sigma_{rms}/1s) + 10*\log_{10}(P_{DC}/1mW)$ **$FOM_T = 20*\log_{10}(\sigma_T/1s) + 10*\log_{10}(P_{DC}/1mW)$

***FOM_N = FOM + $10*\log_{10}(F_{REF}/F_{PLL})$ defined in K. M. Megawer, ISSCC'2018

^Reference buffer power of 5.08mW excluded #FTL power excluded

Table 1 summarizes the performance and compares it with the prior art. The proposed CSPLL shows the lowest jitter and a 2.5 dB improvement in FOM and 4.6 dB in FOM_N, thanks to the proposed CSPD and low-power FTL. It also occupies the smallest area compared to other type-II PLLs. The deterministic jitter due to reference spurs is 12 dB lower than [4] and is slightly higher than [2], [3], where a power/area hungry isolation buffer with an inductive load is used.

V. Conclusion

This paper demonstrates a compact, low-jitter, and power-efficient frequency synthesizer thanks to the proposed charge-sampling phase detector and a highly-digital frequency tracking loop. Fabricated in a 40-nm CMOS process, the 0.13 mm^2 prototype synthesizer generates a 9.8-to-12.2 GHz carrier using a 100 MHz sine wave reference. The CSPLL achieves 50 fs RMS jitter, and -65 dBc spur at 11.4 GHz carrier frequency, while consuming 5 mW. It corresponds to a jitter-power FOM of -258.9 dB, outperforming the state-of-the-art by 2.5 dB.

Acknowledgment

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