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A 210nW BJT-based Temperature Sensor with an Inaccuracy of ±0.15°C (3σ) from −15°C to 85°C

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Abstract

This paper presents a 210nW BJT-based temperature sensor that achieves an inaccuracy of ±0.15°C (3σ) from −15°C to 85°C. A dual-mode front-end (FE), which combines a bias circuit and a BJT core, halves the power needed to generate well-defined CTAT (V_{BE}) and PTAT (ΔV_{BE}) voltages. The use of a tracking ΔΣ ADC reduces FE signal swing and further reduces system power consumption. In a 180-nm BCD process, the prototype achieves a 15mK resolution in 50ms conversion time, translating into a state-of-the-art FoM of 2.3pJK^2.

Introduction

To extend the battery life of portable devices, the demand for low power temperature sensors is increasing. Although sub-1μW MOSFET/resistor-based temperature sensors have been reported, they require a 2-point trim to achieve good accuracy, which increases cost [1-2]. In this work, we propose a 210nW BJT-based temperature sensor that only requires a 1-point trim to achieve ±0.15°C (3σ) inaccuracy from −15°C to 85°C.

Proposed Design

The frontend (FE) of a BJT-based temperature sensor typically consists of a bias circuit and a BJT core that generate V_{BE} and ΔV_{BE} (Fig. 1(a)). Although minimizing I_{BIAS} would reduce FE power, to ensure the linearity of ΔV_{BE}, it should be much larger than the BJT's saturation current I_s (Fig. 1(b)). In this work, a single, reconfigurable dual-mode FE (DMFE) generates I_{BIAS}, V_{BE}, and ΔV_{BE}, thus saving significant power (Fig. 2). During an initial pre-charge phase ($\Phi_{AFE} = 1$), it is configured as a bias circuit that generates PTAT currents I_{BIAS} and pI_{BIAS} ($p = 7$). These are then sampled by storing the gate voltages of $M_{A,B}$ on a capacitor C_S (=5pF). During the conversion phase ($\Phi_{AFE} = 0$), the DMFE is configured as a BJT core, and the sampled currents are used to generate V_{BE} and ΔV_{BE}. Compared to the use of a separate bias circuit and BJT core, this approach nearly halves FE power dissipation, since the pre-charge phase is much shorter (2ms) than the total conversion time (50ms). Fig. 3(a) shows a detailed schematic of the DMFE. An accurate 1:7 current ratio is achieved by applying dynamic element matching (DEM) to 8 current sources $M_{S1\text{-}8}$. R_{BIAS} (10MΩ) sets I_{BIAS} = 5nA at room temperature (RT) ensuring that I_S related errors are less than 0.04°C at 85 °C. Instead of using separate devices, the cascodes of the current sources are reused as DEM switches (Fig. 3(b)), thus halving the bias current errors due to MOSFET leakage. A bootstrapped sampling switch SW_1 ($M_{1\text{-}3}$ and two capacitors $C_{1,2}$ = 1pF), is used to limit the leakage of the sampled charge in C_S via the off-resistance and bulk connection of the main switch M_1 (Fig. 3(c)).

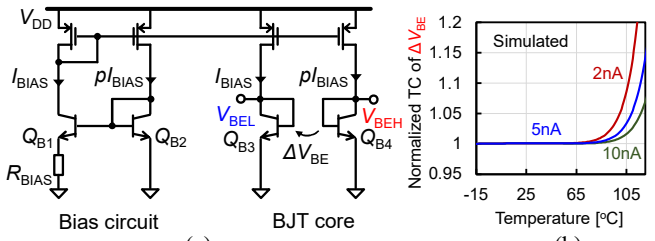
The output of the DMFE can be efficiently digitized by a charge-balancing ΔΣ modulator, which adjusts the gain K of a switched-capacitor (SC) DAC so that $K \times \Delta V_{BE} = V_{BE}$ on average. In [3], a 2nd order zoom ADC is used, which combines a coarse SAR ADC and a fine ΔΣ modulator. However, its two-step operation requires a complex and power-hungry digital controller. To reduce power, this work employs a tracking ΔΣ modulator [4]. As shown in Fig. 4, this consists of a correlated double sampling (CDS)-based 1st integrator (Fig. 5(a)), followed by a comparator and a digital loop filter (DLF), whose multi-bit output drives the DAC. Each half of the SC DAC is implemented by 19 unit caps (C_{DAC} = 60fF), allowing K to be varied from 1 to 19 (Fig. 5(b)). In addition, half steps in K are realized by using different gain factors in the two halves of the DAC, i.e., by alternating between $K_1 = N$ and $K_2 = N + 1$, or $K_1 = N + 1$ and $K_2 = N$, thus realizing a $0.5\Delta V_{BE}$ differential DAC swing, while maintaining an average CM swing of zero. As shown in Fig. 6, this is 4x less than the swing in the zoom ADC of [3], allowing the SC integrator to be efficiently implemented as a current-reuse OTA (Fig. 5(c)). Moreover, the single-step operation of the tracking ΔΣ modulator lowers the complexity and power of the digital controller. Compared to the zoom ADC of [3], the number of sampling switches per unit cap is halved by creating the ΔV_{BE} transitions needed to transfer charge to the integrator by re-using the DEM switches in the DMFE to swap the bias currents of the BJTs. This halves bias current errors due to switch leakage. In addition, PMOS, rather than the usual NMOS, T-switches are used (Fig. 5(b)), allowing their body and drain-source leakages to be minimized by connecting them to V_{BEH_R}, which is a replica of the largest V_{BE} ($V_{BEH} = V_{BEL} + \Delta V_{BE}$) generated by Q_{BR} biased at I_{BIAS} in the DMFE.

Measurement Results

The prototype is fabricated in a 180-nm BCD process (Fig. 7) and occupies 0.058mm^2. The digital controller and the DLF are synthesized from standard digital cells. With a 1.25V supply and a 5 kHz system clock, the sensor consumes 210nW at room temperature, with 121nW/79nW/9nW consumed in the analog core, the digital controller and loop filter, and the clock generator, respectively. The line sensitivity is 0.07°C/V for supply voltages ranging from 1.2V to 1.8V. The sensor achieves a thermal-noise limited resolution of 15mK (RMS) in a 50ms conversion time (Fig. 8), which translates into a state-of-the-art FoM of 2.3pJK^2. Measurements on 20 samples packaged in ceramic DIL packages resulted in ±0.4°C (3σ) and ±0.15°C (3σ) inaccuracy from −15°C to 85°C without/with 1-point offset trimming, respectively (Figs 9). As expected, the sensor's characteristic becomes non-linear at high temperature (>85°C), due to the increase in I_S, while at low temperatures, it exhibits more spread as both I_{BIAS} and the OTA gain decrease. Table I compares the performance of the proposed sensor with those of other 1-point trimmed sub-μW temperature sensors. This design simultaneously achieves the lowest power consumption and the best accuracy.

References

[1] K. Yang *et al*., *IEEE ISSCC*, 2017. [2] A. Jain *et al*., *IEEE T-CAS II*, 2021. [3] K. Souri *et al*., *IEEE ISSCC*, 2014. [4] M. Motz *et al*., *IEEE ISSCC*, 2006. [5] T. Zhang *et al*., *IEEE J. SENSOR*, 2018. [6] H. Xin *et al*., *IEEE SSC-L*, 2018. [7] Z. Tang *et al*., *IEEE SSC-L*, 2021.



(a) (b)

Fig. 1 (a) Schematic of a conventional FE. (b) Simulated I_{BIAS} vs. normalized temperature coefficient (TC) (@ −15°C) of ΔV_{BE}.

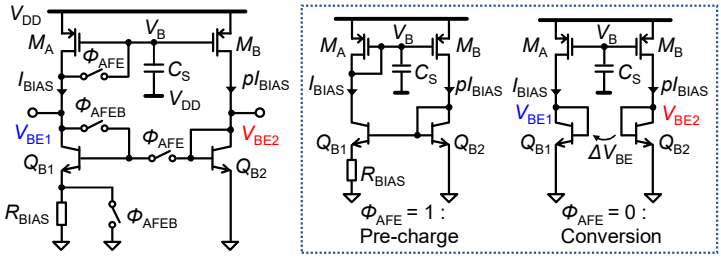


Fig. 2 Concept of the proposed DMFE.

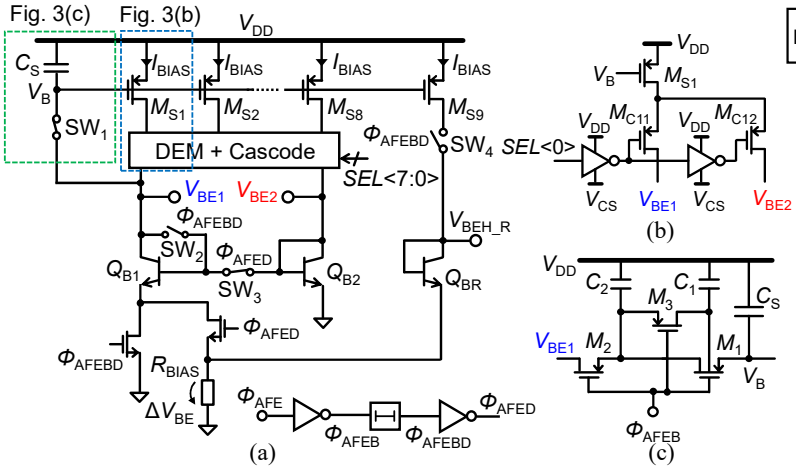


Fig. 3 Schematic of (a) DMFE, (b) cascode combined with DEM switch, and (c) sample and hold circuit based on a passive bootstrap switch.

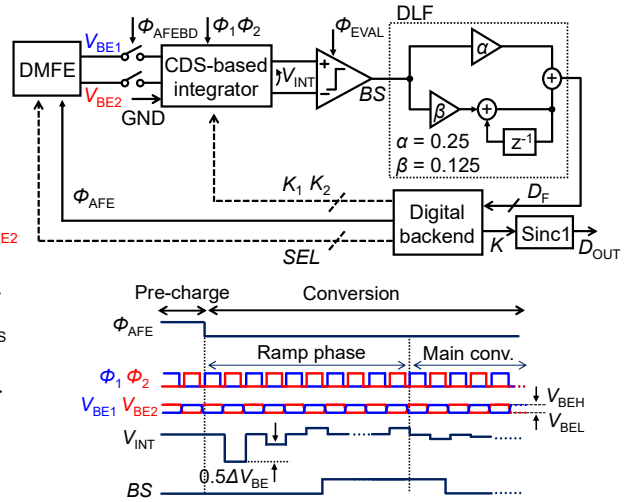


Fig. 4 Temperature sensor block diagram and timing waveforms.

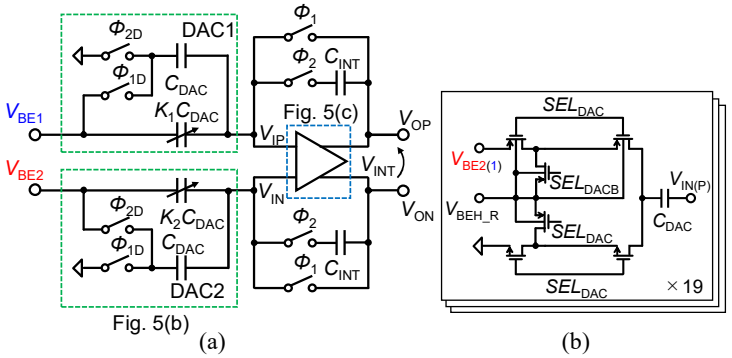


Fig. 5 Schematic of (a) CDS-based integrator, (b) cells of DAC, and (c) current-reuse OTA.

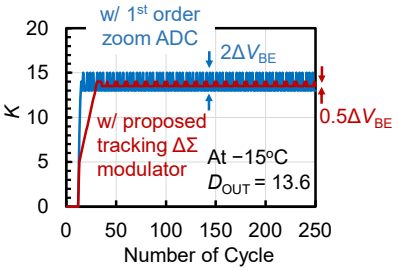


Fig. 6 Swing of DAC gain.

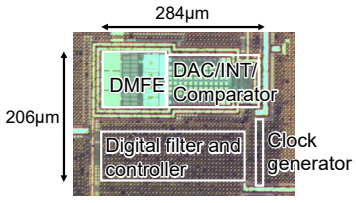


Fig. 7 Die micrograph of the fabricated temperature sensor.

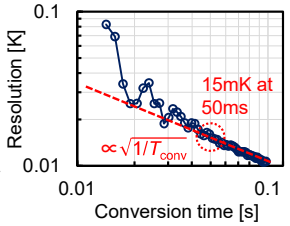


Fig. 8 Measured resolution vs. conversion time.

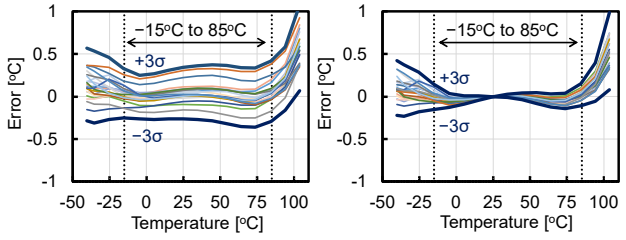


Fig. 9 Measured inaccuracy of 20 samples (a) without and (b) with 1-point offset calibration.

TABLE I
Performance Summary and Comparison with the state-of-the-art

	This work		Zhang [5] JSensor18	Xin [6] SSCL18	Souri [3] ISSCC14		Tang [7] SSCL21
Sensor type	BJT		BJT	Resistor	DTMOS		MOS
Process	180nm		180nm	65nm	160nm		55nm
Area [mm²]	0.058		0.18	0.06	0.085		0.0024
Fully integrated?	Yes		Yes	Yes	External digital controller		External 1MHz reference
Power [nW] (Supply V_{DD})	210 (1.25V)		720 (1.0V)	488 (1.0V)	600 (0.85V)		860 (0.8V)
Temp. Range [°C]	−15 to 85		0 to 100	0 to 100	−40 to 125		−40 to 85
Inaccuracy [°C] (Trim. Point)	±0.4*1 (0)	±0.15*1 (1)	±0.2*1 (1)	−1.1/1.5*2 (1)	±1.0*1 (0)	±0.4*1 (1)	±0.8*1*3 (1)
R-IA [%]	0.8	0.3	0.4	2.6	1.3	0.5	1.3
Resolution [mK]	15		40	610	63		17
Conv. time [ms]	50		40	0.01	6		1
FoM*4 [pJ·K²]	2.3		46	1.8	14.1		0.26
PSS [°C/V] (V_{DD} range)	0.07 (1.2 to 1.8V)		N/A	N/A	0.45 (0.85 to 1.2V)		5.8 (0.8 – 1.3V)

*1 3σ inaccuracy
*2 Peak-to-peak inaccuracy
*3 Polynomial fitting is applied.
*4 FoM = (Resolution)² × (Energy/conversion)