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Comparison of Two and Three-Level AC-DC Rectifier Semiconductor Losses with SiC MOSFETs Considering Reverse Conduction

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Keywords

«AC-DC converter», «Analytical losses computation», «Conduction losses», «Silicon Carbide (SiC)», «Shunt current».

Abstract

This paper presents the semiconductor losses analytical equations in closed form for two-level voltage source converter, three-level neutral point clamped (NPC) and three-level T-Type PFC topologies in high power applications. The reverse parallel current conduction between the SiC MOSFETs channel and body diode is considered. A circuit simulation model is built in PLECS to estimate the semiconductor losses and to verify the accuracy of the developed analytical model. A calculation example of the semiconductor losses of a 200 kW three-phase rectifier is shown.

Introduction

With the popularity of electric vehicles, there is a growing need to have fast charging infrastructures. The power rating for DC fast charger is typically rated at 50 kW, and chargers with power rating up to 350 kW is also available from ABB [1]. Power factor correction circuits are used as a front-end converter in these applications.

Semiconductor losses of two and three-level converters with IGBTs are well studied in literature such as in [2], therefore, it is not covered here. In order to increase the power density, SiC MOSFETs (modules) are preferred due to its superior switching performance. The semiconductor losses study of these SiC MOSFETs based three-level converters when the reverse conduction current is distributed between the channel and body diode is not commonly seen. Reference [3] shows the analysis of SiC technology used in two and three-level converters without considering the reverse parallel current conduction. References [4, 5, 6, 7] consider the reverse conduction and blanking time influence in a two-level converter. Reverse parallel current conduction of different modulation schemes in SiC-based inverters is discussed in [8] while this phenomenon is also described in high-power bidirectional converters [9].

The main contribution of this paper is to extend this analysis to three-level rectifiers to provide an accurate losses calculation model, especially for the conduction losses calculation. Besides, a simulation circuit will also be given which can be easily modified to simulate semiconductor losses under more complicated situations such as deadtime influence, third harmonic injection, etc.

AC-DC PFC Topologies

Fig. 1 shows one arm of the AC-DC converters studied in this paper with MOSFETs as active switches. A complete three-phase converter will have three arms. Sinusoidal Pulse-Width-Modulation (SPWM) scheme is assumed in this paper. With SPWM applied to two-level, three-level T-Type and NPC rectifier, Fig. 2 could be used to show the circuit operation [10].

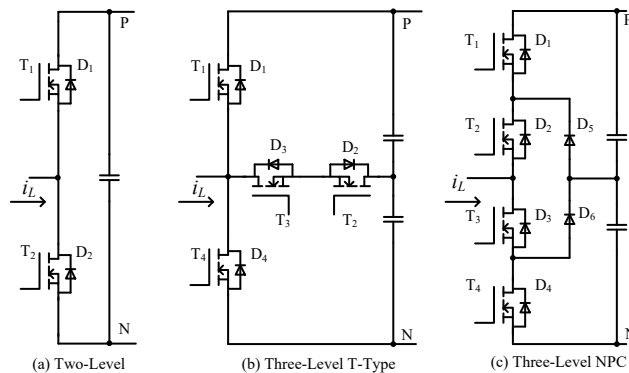


Fig. 1: PFC topologies studied in this paper.

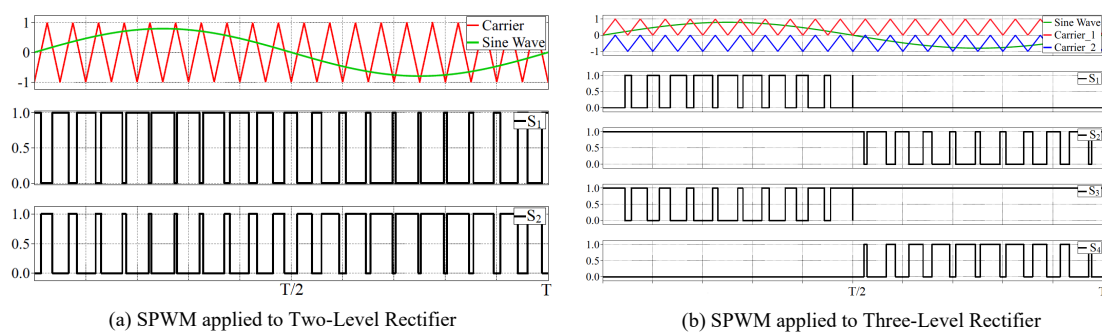


Fig. 2: SPWM applied to two-level and three-level rectifiers.

In Fig. 2, S_1 - S_4 are PWM signals applied to the switches T_1 - T_4 .

Semiconductor Losses Analysis

The semiconductor losses can be divided into conduction losses and switching losses. The MOSFET channel's conduction can also be turned on by applying a gate-source voltage above the threshold voltage to reduce the reverse conduction losses which is also called active or synchronous rectification technique. When the current is high enough to a certain extent, the current will be distributed between the body diode and channel. The circuit model of a MOSFET is shown in Fig. 3. Fig. 4 shows the current through the MOSFET channel and body diode, the deadtime is not considered. T_1 and T_2 , D_1 and D_2 are given in Fig. 1.

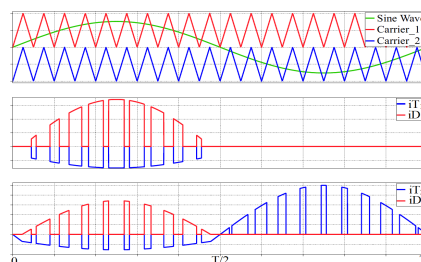
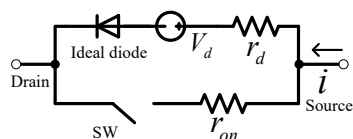


Fig. 3: MOSFET model, during reverse conduction Fig. 4: Parallel current conduction between MOSFET channel and diode, T-Type rectifier.

For MOSFETs operating in reverse conduction state, when $r_{on}i > V_d$, the current through r_{on} and r_d are:

$$i_{r_{on}} = \frac{r_d i + V_d}{r_{on} + r_d}, \quad i_{r_d} = \frac{r_{on} i - V_d}{r_{on} + r_d}. \quad (1)$$

r_{on} and r_d are the channel and body diode on-resistances, V_d is the body diode forward voltage, i is the summed reverse current shown in Fig. 3. Note, that when $r_{on}i < V_d$, the anti-parallel diode does not conduct current.

Semiconductor Conduction Losses

To calculate the conduction losses of MOSFETs, the rms and average current value of the body diode and rms current value of the MOSFET channel need to be known. To simplify the formulae expression, the three functions below will be adopted:

$$\begin{aligned} \int_{\alpha}^{\pi-\alpha} \sin^2 \theta d\theta &= \frac{\pi-2\alpha+\sin 2\alpha}{2} = f_1(\alpha), \quad \int_{\alpha}^{\pi-\alpha} \sin^3 \theta d\theta = \frac{3}{2} \cos \alpha - \frac{1}{6} \cos 3\alpha = f_2(\alpha) \\ \int_0^{\alpha} \sin^3 \theta d\theta &= \frac{1}{12} \cos 3\alpha - \frac{3}{4} \cos \alpha + \frac{2}{3} = f_3(\alpha). \end{aligned} \quad (2)$$

α is a variable with a value between 0 and $\frac{\pi}{2}$. Several conditions were assumed for the calculation: the switching frequency is much higher than the grid frequency, the line current is sinusoidal with small ripple and the deadtime is neglected.

Two-Level Rectifier

Below, I_{avg_X} is average current while I_{rms_X} is rms current, $\hat{i}_L$ is the peak input current shown in Fig. 1 and M is the modulation index.

$$\begin{aligned} I_{avg_D1,D2} &= \frac{1}{2\pi} \int_{\varphi}^{\pi-\varphi} \frac{r_{on} \hat{i}_L \sin \theta - V_d}{r_{on} + r_d} \frac{1 + M \sin \theta}{2} d\theta \\ &= \frac{1}{4\pi(r_{on} + r_d)} [2 \cos \varphi (r_{on} \hat{i}_L - MV_d) + r_{on} \hat{i}_L M f_1(\varphi) + V_d(2\varphi - \pi)]. \end{aligned} \quad (3)$$

In (3), $\varphi = \arcsin \frac{V_d}{r_{on} \hat{i}_L}$. If $V_d > r_{on} \hat{i}_L$, then $\varphi = \frac{\pi}{2}$. The definition of φ applies to the rest of this two-level rectifier section.

$$\begin{aligned} I_{rms_D1,D2} &= \sqrt{\frac{1}{2\pi} \int_{\varphi}^{\pi-\varphi} \left(\frac{r_{on} \hat{i}_L \sin \theta - V_d}{r_{on} + r_d} \right)^2 \frac{1 + M \sin \theta}{2} d\theta} = \\ &= \sqrt{\frac{1}{4\pi(r_{on} + r_d)^2} [k^2 M f_2(\varphi) + (k^2 - 2kV_d M) f_1(\varphi) + 2 \cos \varphi (V_d^2 M - 2kV_d) + V_d^2(\pi - 2\varphi)]}. \end{aligned} \quad (4)$$

In (4), $k = r_{on} \hat{i}_L$.

Through piecewise integral,

$$\begin{aligned} I_{rms_T1,T2} &= \sqrt{\frac{1}{2\pi} [\hat{i}_L^2 (\frac{\varphi}{2} + \frac{\pi}{4} - \frac{\sin 2\varphi}{4} - \frac{2M}{3}) + \hat{i}_L^2 M f_3(\varphi)] + \frac{1}{4\pi(r_{on} + r_d)^2} [q^2 M f_2(\varphi) + \\ &+ \sqrt{(q^2 + 2qV_d M) f_1(\varphi) + 2 \cos \varphi (2qV_d + V_d^2 M) + V_d^2(\pi - 2\varphi)}]}. \end{aligned} \quad (5)$$

In (5), $q = r_d \hat{i}_L$.

Three-Level T-Type Rectifier

Suppose the MOSFET parameters of $T_1(D_1)$ and $T_4(D_4)$ are r_{on1} , r_{d1} and V_{d1} . The parameters of $T_2(D_2)$ and $T_3(D_3)$ are r_{on2} , r_{d2} and V_{d2} .

$$I_{avg_D1,D4} = \frac{1}{2\pi} \int_{\varphi}^{\pi-\varphi} \frac{r_{on1} \hat{i}_L \sin \theta - V_{d1}}{r_{on1} + r_{d1}} M \sin \theta d\theta = \frac{1}{2\pi(r_{on1} + r_{d1})} [r_{on1} \hat{i}_L M f_1(\varphi) - 2 \cos \varphi V_{d1} M]. \quad (6)$$

In (6), $\varphi = \arcsin \frac{V_{d1}}{r_{on1}\hat{i}_L}$.

$$\begin{aligned} I_{avg_D2,D3} &= \frac{1}{2\pi} \int_{\beta}^{\pi-\beta} \frac{r_{on2}\hat{i}_L \sin \theta - V_{d2}}{r_{on2} + r_{d2}} (1 - M \sin \theta) d\theta \\ &= \frac{1}{2\pi(r_{on2} + r_{d2})} [2 \cos \beta (r_{on2}\hat{i}_L + MV_{d2}) - r_{on2}\hat{i}_L M f_1(\beta) + V_{d2}(2\beta - \pi)]. \end{aligned} \quad (7)$$

In (7), $\beta = \arcsin \frac{V_{d2}}{r_{on2}\hat{i}_L}$. φ and β have the same definition below for T-Type rectifier section.

$$\begin{aligned} I_{rms_D1,D4} &= \sqrt{\frac{1}{2\pi} \int_{\varphi}^{\pi-\varphi} \left(\frac{r_{on1}\hat{i}_L \sin \theta - V_{d1}}{r_{on1} + r_{d1}} \right)^2 M \sin \theta d\theta} \\ &= \sqrt{\frac{1}{2\pi(r_{on1} + r_{d1})^2} [k_1^2 M f_2(\varphi) - 2k_1 V_{d1} M f_1(\varphi) + 2 \cos \varphi V_{d1}^2 M]}. \end{aligned} \quad (8)$$

$$\begin{aligned} I_{rms_T1,T4} &= \sqrt{\frac{1}{2\pi} [2 \int_0^{\varphi} (\hat{i}_L \sin \theta)^2 M \sin \theta d\theta + \int_{\varphi}^{\pi-\varphi} \left(\frac{r_{d1}\hat{i}_L \sin \theta + V_{d1}}{r_{on1} + r_{d1}} \right)^2 M \sin \theta d\theta]} \\ &= \sqrt{\frac{1}{\pi \hat{i}_L^2} M f_3(\varphi) + \frac{1}{2\pi(r_{on1} + r_{d1})^2} [k_2^2 M f_2(\varphi) + 2k_2 V_{d1} M f_1(\varphi) + 2 \cos \varphi V_{d1}^2 M]}. \end{aligned} \quad (9)$$

$$\begin{aligned} I_{rms_D2,D3} &= \sqrt{\frac{1}{2\pi} \int_{\beta}^{\pi-\beta} \left(\frac{r_{on2}\hat{i}_L \sin \theta - V_{d2}}{r_{on2} + r_{d2}} \right)^2 (1 - M \sin \theta) d\theta} \\ &= \sqrt{\frac{1}{2\pi(r_{on2} + r_{d2})^2} [-k_3^2 M f_2(\beta) + (k_3^2 + 2k_3 V_{d2} M) f_1(\beta) - 2 \cos \beta (2k_3 V_{d2} + M V_{d2}^2) + V_{d2}^2 (\pi - 2\beta)]}. \end{aligned} \quad (10)$$

$$\begin{aligned} I_{rms_T2,T3} &= \sqrt{\frac{1}{2\pi} \hat{i}_L^2 \left(\frac{\pi}{2} + \beta - \frac{\sin 2\beta}{2} \right) - \frac{1}{2\pi} M \hat{i}_L^2 \left[\frac{4}{3} + 2f_3(\beta) \right] + \frac{1}{2\pi(r_{on2} + r_{d2})^2} [-k_4^2 M f_2(\beta) +} \\ &\quad \sqrt{(k_4^2 - 2k_4 V_{d2} M) f_1(\beta) + 2 \cos \beta (2k_4 V_{d2} - M V_{d2}^2) + V_{d2}^2 (\pi - 2\beta)]}. \end{aligned} \quad (11)$$

In (8), (9), (10), (11), $k_1 = r_{on1}\hat{i}_L$, $k_2 = r_{d1}\hat{i}_L$, $k_3 = r_{on2}\hat{i}_L$, $k_4 = r_{d2}\hat{i}_L$.

Three-Level NPC Rectifier

Suppose the four MOSFETs in one NPC rectifier arm are of the same type with parameters r_{on} , r_d and V_d .

$$I_{avg_D5,D6} = \frac{1}{2\pi} \int_0^{\pi} \hat{i}_L \sin \theta (1 - M \sin \theta) d\theta = \hat{i}_L \left(\frac{1}{\pi} - \frac{M}{4} \right). \quad (12)$$

$$I_{avg_D1,D2,D3,D4} = \frac{1}{2\pi} \int_{\varphi}^{\pi-\varphi} \frac{r_{on}\hat{i}_L \sin \theta - V_d}{r_{on} + r_d} M \sin \theta d\theta = \frac{1}{2\pi(r_{on} + r_d)} [r_{on}\hat{i}_L M f_1(\varphi) - 2 \cos \varphi V_d M]. \quad (13)$$

In (13), $\varphi = \arcsin \frac{V_d}{r_{on}\hat{i}_L}$. φ has the same definition below for NPC rectifier section.

$$I_{rms_D5,D6} = \sqrt{\frac{1}{2\pi} \int_0^{\pi} (\hat{i}_L \sin \theta)^2 (1 - M \sin \theta) d\theta} = \hat{i}_L \sqrt{\frac{1}{4} - \frac{2M}{3\pi}}. \quad (14)$$

$$\begin{aligned} I_{rms_D1,D2,D3,D4} &= \sqrt{\frac{1}{2\pi} \int_{\varphi}^{\pi-\varphi} \left(\frac{r_{on}\hat{i}_L \sin \theta - V_d}{r_{on} + r_d} \right)^2 M \sin \theta d\theta} \\ &= \sqrt{\frac{1}{2\pi(r_{on} + r_d)^2} [k_1^2 M f_2(\varphi) - 2k_1 V_d M f_1(\varphi) + 2 \cos \varphi V_d^2 M]}. \end{aligned} \quad (15)$$

In (15), $k_1 = r_{on}\hat{i}_L$.

$$I_{rms_T1,T4} = \sqrt{\frac{1}{2\pi} [2 \int_0^\pi (\hat{i}_L \sin \theta)^2 M \sin \theta d\theta + \int_\pi^{2\pi} \left(\frac{r_d \hat{i}_L \sin \theta + V_d}{r_{on} + r_d} \right)^2 M \sin \theta d\theta]} = \sqrt{\frac{1}{\pi} \hat{i}_L^2 M f_3(\varphi) + \frac{1}{2\pi(r_{on} + r_d)^2} [k_2^2 M f_2(\varphi) + 2k_2 V_d M f_1(\varphi) + 2 \cos \varphi V_d^2 M]}. \quad (16)$$

$$I_{rms_T2,T3} = \sqrt{\frac{\hat{i}_L^2}{4} + \frac{1}{\pi} \hat{i}_L^2 M [f_3(\varphi) - \frac{2}{3}] + \frac{1}{2\pi(r_{on} + r_d)^2} [k_2^2 M f_2(\varphi) + 2k_2 V_d M f_1(\varphi) + 2 \cos \varphi V_d^2 M]}. \quad (17)$$

In (16) and (17), $k_2 = r_d \hat{i}_L$.

Note, when φ and β are $\frac{\pi}{2}$ when there is no parallel current distribution between the MOSFETs channel and body diode, then, the above equations degrade into the situation that all the reverse conduction current only goes through the MOSFETs channel.

Semiconductor Switching Losses

The reverse recovery losses of the SiC MOSFETs body diode will be neglected in this paper. The turn-on (E_{on}) and turn-off (E_{off}) losses are curve fitted by a second order polynomial at a reference drain source voltage:

$$E_{on} = a_1 i^2 + b_1 i + c_1, E_{off} = a_2 i^2 + b_2 i + c_2. \quad (18)$$

i is the current through the MOSFET channel at the transient moment.

Two-Level Rectifier

The switching losses of T_1 and T_2 are:

$$\begin{aligned} P_{s_T1,T2} &= \frac{f_s V_{dc}}{2\pi V_{ref}} \int_0^\pi [(a_1 + a_2) \hat{i}_L^2 \sin^2 \theta + (b_1 + b_2) \hat{i}_L \sin \theta] d\theta + \frac{f_s V_{dc}}{2V_{ref}} (c_1 + c_2) \\ &= \frac{f_s V_{dc}}{2V_{ref}} \left[\frac{(a_1 + a_2) \hat{i}_L^2}{2} + \frac{2(b_1 + b_2) \hat{i}_L}{\pi} + (c_1 + c_2) \right]. \end{aligned} \quad (19)$$

In (19), f_s is the switching frequency, V_{ref} is the reference voltage [11] [12], V_{dc} is the dc link voltage between P and N shown in Fig. 1.

Three-Level T-Type Rectifier

There are no switching losses of T_1 and T_4 . Similar to (19), the switching losses of T_2 and T_3 are:

$$P_{s_T2,T3} = \frac{f_s V_{dc}}{4V_{ref}} \left[\frac{(a_1 + a_2) \hat{i}_L^2}{2} + \frac{2(b_1 + b_2) \hat{i}_L}{\pi} + (c_1 + c_2) \right]. \quad (20)$$

In (20), a_1 , a_2 , b_1 , b_2 , c_1 and c_2 are the parameters of T_2 (T_3).

Three-Level NPC Rectifier

Diodes D_5 and D_6 have no reverse recovery losses if SiC diodes are used. The switching losses of T_2 and T_3 are:

$$P_{s_T2,T3} = \frac{f_s V_{dc}}{4V_{ref}} \left[\frac{(a_1 + a_2) \hat{i}_L^2}{2} + \frac{2(b_1 + b_2) \hat{i}_L}{\pi} + (c_1 + c_2) \right]. \quad (21)$$

Simulation Model

The simulation model for semiconductor losses in PLECS is given in Fig. 5 which is a modification and simplification of [13].

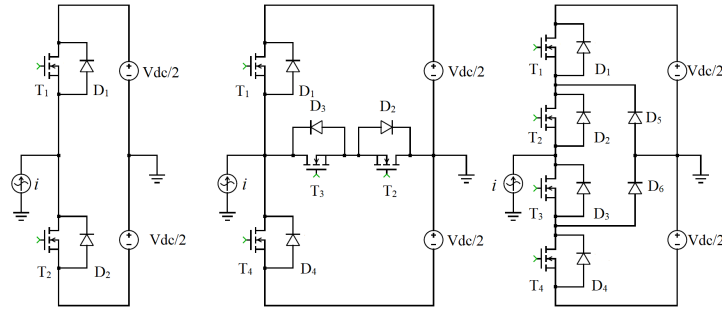


Fig. 5: Semiconductor losses simulation model in PLECS.

In order to simulate the losses in a simpler way, the input source is set to be a current source. The PWM strategy is given in Fig. 2. Due to the thermal analysis principle adopted by PLECS, the operation status of the MOSFETs channel and diode needs to be known to calculate their losses, therefore, the electrical parameters of r_{on} , r_d and V_d should be applied first and will keep the same during simulation. Device parameters from datasheets will be applied to the software thermal domain as a form of a lookup table.

Results

As an analysis example, the DC link voltage is set to be 1400 V which is adopted at applications when a high DC link voltage is needed such as high-power wireless power transfer systems, three-phase power is 200 kW and line-to-line rms voltage is set to be 650 V which means the modulation index M is 0.758. The devices selected for each topology are given in Table I. The semiconductor losses may be different with different devices, the intention of this example analysis is to show the losses based on today's SiC technology and to benchmark the losses between different topologies.

Table I: Selected devices for analysis in this paper with voltage and current rating at $T_{case}=25^\circ\text{C}$

Topology	Device Selection	Device Name	Manufacturer	$V_{rating}(V)$	$I_{rating-T}$	$I_{rating-D}$
Two-Level	$T_{1,2}, D_{1,2}$	CAS300M17BM2	CREE	1700	325	556
T-Type	$T_{1,4}, D_{1,4}$	CAS300M17BM2	CREE	1700	325	556
	$T_{2,3}, D_{2,3}$	C3M0016120K	CREE	1200	115	112
NPC	T_{1-4}, D_{1-4}	CAS300M12BM2	CREE	1200	423	-
	$D_{5,6}$	SKM125KD12SC	Semikron	1200	-	264

For T-Type rectifier, both T_2 (D_2) and T_3 (D_3) have three C3M0016120K MOSFETs in parallel to increase current capacity.

Conduction losses difference between different models

This subsection will show the conduction losses difference with the derived model (method 1) and also the one assuming that all the reverse conduction current passes through the channel (method 2). To verify the correctness of the derived equations for current stress calculations, the simulation results from PLECS are given in the tables with switching frequency at 10 kHz, maximum step size is 1 μs , relative tolerance is 1e-4, pure sinusoidal current is used as input source. The device parameters at junction temperature of 150°C through curve fitting are (In Table II, $a = a_1 + a_2$, $b = b_1 + b_2$, $c = c_1 + c_2$):

Table II: Device parameters to estimate the semiconductor losses through curve fitting

	$r_{on} (m\Omega)$	$r_d (m\Omega)$	$V_d (V)$	a	b	c	$V_{ref} (V)$
CAS300M17BM2	19.59	5.13	0.78	5.628e-8	9.077e-5	2.791e-3	1200
CAS300M12BM2	8.43	4.59	0.77	3.560e-8	2.440e-5	1.411e-3	600
C3M0016120K	39.8	16.85	3.15	1.104e-7	7.532e-6	1.910e-4	600
SKM125KD12SC	-	5.65	0.79	-	-	-	-

Table III-V show the calculated rms and average current of the device and the three phase conduction losses.

Table III: Calculated current value and three phase conduction losses of two-level rectifier

	$I_{rms_T1,T2}$ (A)	$I_{rms_D1,D2}$ (A)	$I_{avg_D1,D2}$ (A)	Losses (W)
Method 1	67.49	72.89	39.27	883
Method 2	125.62	0	0	1855
Simulation	67.49	72.89	39.27	-

Table IV: Calculated current value and three phase conduction losses of NPC rectifier

	$I_{rms_T1,T4}$ (A)	$I_{rms_T2,T3}$ (A)	$I_{avg_D1,D4}$ (A)	$I_{rms_D1,D4}$ (A)	$I_{avg_D5,D6}$ (A)	$I_{rms_D5,D6}$ (A)	Losses (W)
Method 1	63.66	98.37	16.88	38.01	32.35	75.00	1270
Method 2	100.77	125.62	0	0	32.35	75.00	1656
Simulation	63.66	98.37	16.88	38.01	32.35	75.00	-

Table V: Calculated current value and three phase conduction losses of T-Type rectifier

	$I_{rms_T1,T4}$ (A)	$I_{rms_D1,D4}$ (A)	$I_{avg_D1,D4}$ (A)	$I_{rms_T2,T3}$ (A)	$I_{avg_D2,D3}$ (A)	$I_{rms_D2,D3}$ (A)	Losses (W)
Method 1	36.05	65.08	30.15	35.22	0.057	0.382	1316
Method 2	100.77	0	0	35.35	0	0	2089
Simulation	36.05	65.08	30.15	35.22	0.057	0.382	-

Note in Table V, the current for T_2 (T_3) and D_2 (D_3) are the current through each device, since three are put in parallel to increase the current rating.

From the above results, it can be seen that firstly, the simulation results match the theoretical equations as expected which proves the correctness of the derived formulae. Secondly, the conduction losses between these two methods differ much. If defining error percentage as: $\text{error} = \frac{\text{Losses}(\text{Method 2}) - \text{Losses}(\text{Method 1})}{\text{Losses}(\text{Method 1})}$, then the error is 110%, 30.4% and 58.74%. Therefore, the more accurate models should be used to estimate the losses if there is reverse current distribution between the MOSFET channel and its paralleling diode.

Simulation and theoretical semiconductor losses

The switching losses will be included. Based on the previous equations derived for the switching losses, the results are given in Fig. 6 below at 10 kHz switching frequency:

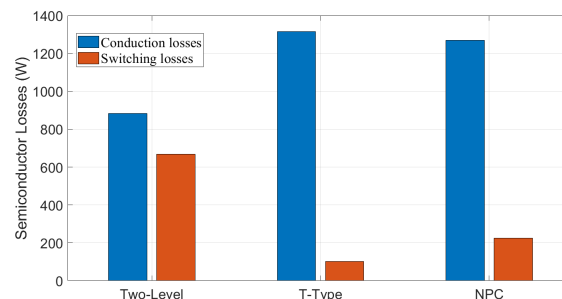


Fig. 6: Semiconductor losses of different rectifier types.

As a verification example, the simulation result of the two level rectifier is shown in Fig. 7 below:

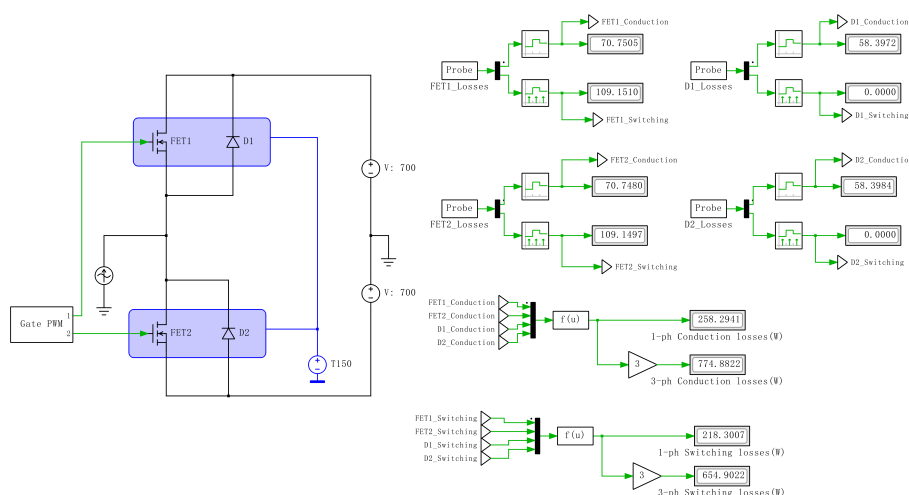


Fig. 7: Semiconductor losses simulation results of a two-level rectifier.

From the simulation results, the switching losses match well with the theoretical values while the conduction losses have some differences. As mentioned previously, in order to calculate the losses of each component, the electrical operation status of each component needs to be known first due to the losses calculation mechanism of PLECS itself, therefore, the on-resistance of the channel is applied while the losses simulation is based on lookup table, so, this difference is expected and acceptable.

Conclusion

Analytical equations considering the reverse current parallel conduction between MOSFETs channel and body diodes are given to facilitate a quick calculation of semiconductor losses for high power three-phase rectifiers. The situation that the MOSFET channel conducts all the current will then become a special case. A losses simulation model is also provided which can be adapted easily to study more complicated situations as discussed in introduction. The studied example shows the necessity to use a more accurate model for conduction losses estimation.

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