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Transceiver ASIC Design for High-Frame-Rate 3D Intracardiac Echocardiography

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Background, Motivation and Objective

Intra-cardiac echocardiography (ICE) procedures are currently evolving from 2D to 3D imaging to enhance their field of view. The applied 3D probes commonly contain a chip to enhance signal quality while reducing the number of cables from the required 2D transducer matrix. The latter is typically achieved with the aid of subarray beamforming, combining subarray signals by means of delay-and-sum onto one cable. As only one set of delays can be applied per acquisition, this however limits its field of view and multiple acquisitions are required to construct a full volume, hampering the use of emerging high-frame-rate modes like electromechanical wave imaging. To provide this in future probes, an imaging rate of 1000 vol/s is desired but yet to be achieved due to the challenge of reducing the beamformer size while still providing enough space for all required circuitry in the transducer pitch and low enough channel-count to enable compatibility with mm-diameter catheters.

In this work, an architecture enabling 3D high-frame-rate imaging with all necessary transmit and receive electronics and sufficient channel-count reduction is shown.

Statement of Contribution/Methods

A subarray beamformer size of just 3 elements is chosen to facilitate the targeted frame-rate at 10 cm imaging depth. To still maintain a suitable cable count, the subarray outputs are digitized and four of them are time-division-multiplexed onto one channel. The applied novel analog-to-digital converter is implemented as a hybrid between a successive-approximation and a slope stage, which, combined with hardware sharing between neighboring stages, leads to the most area- and power-efficient design reported so far. This enables the integration with area-hungry 65-V pulsers, analog frontends with 54 dB time-gain-compensation and the subarray beamformer in a pitch-matched fashion. [1]

Results/Discussion

Electrical and acoustic verification were obtained with an 8×9 element prototype fabricated in a 0.18µm HV process with a transducer matrix directly manufactured on its surface. Fig. 1 shows a micrograph of the prototype, the characterization of the receive path to a dynamic range of 91dB and a 3D-render of the acquisition of a 3-needle phantom at the intended frame-rate.

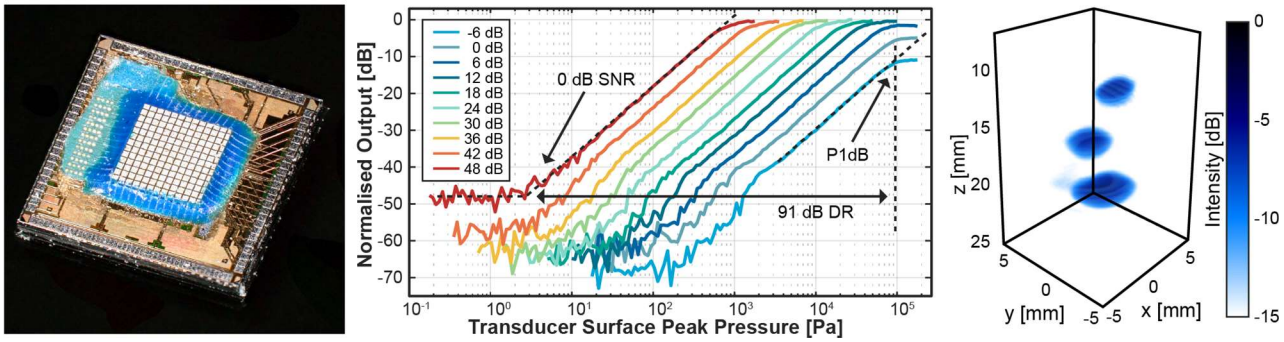

Fig. 1.: Micrograph of the manufactured prototype with receive channel characterization across ten gain settings and high-frame-rate imaging experiment showing a three-needle phantom in 3D-space.

[1] Y. Hopf et al., "A Pitch-Matched ASIC with Integrated 65V TX and Shared Hybrid Beamforming ADC for Catheter-Based High-Frame-Rate 3D Ultrasound Probes," 2022 IEEE International Solid- State Circuits Conference (ISSCC), 2022, pp. 494-496.