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A 2.5-μW Beyond-the-Rails Current Sensor With a Tunable Voltage Reference and ±0.6% Gain Error From −40 °C to +85 °C

Roger Zamparette, *Member, IEEE*, and Kofi Makinwa, *Fellow, IEEE*

***Abstract*—This letter presents a low-power, fully integrated current sensor for Coulomb-counting. It employs a hybrid delta–sigma modulator (ΔΣM) with an FIR-DAC to digitize the voltage drop across a shunt. The modulator's first stage consists of a capacitively coupled chopper amplifier, which enables a beyond-the-rails (−0.3 to 5 V) input common-mode voltage range from a 1.8-V supply. A tunable voltage reference is used to accurately compensate for the large temperature coefficient (∼3500 ppm/°C) of low-cost metal shunts. With a 20-mΩ on-chip shunt, ±2 A currents can be digitized with 0.35% gain error from −40 °C to 85 °C, after a 1-point trim. With a 3-mΩ PCB trace, currents up to ±15 A can be digitized with 0.6% gain error over the same temperature range. Fabricated in a standard 0.18-μm CMOS process, the sensor occupies 1.6 mm^2 and consumes 2.5 μW, which is 3× less than the state of the art. It also achieves competitive energy efficiency, with a figure of merit (FoM) of 149 dB.**

***Index Terms*—Coulomb-counting, current sensor, FIR-DAC, fully integrated, high-side, hybrid delta–sigma modulator, on-chip shunt resistor, PCB trace shunt resistor.**

I. Introduction

Coulomb-counting is a well-known technique for estimating battery state of charge (SOC). It involves measuring and integrating battery current to determine the net influx of charge. Shunt-based current sensors are often used to achieve the required accuracy and dynamic range [1], [3], [5]. These should be configured for high-side sensing to avoid adding extra resistance between the battery and the system ground. However, this requires instrumentation amplifiers or ADCs with a wide input common-mode range (ICMR), ∼5 V, for the lithium batteries employed in IoT and wearable devices. Low *instantaneous* power consumption is another key requirement in such applications since Coulomb-counting current sensors are always on. Minimizing their power consumption is a major target of this letter.

Accurate current sensors often employ precision off-chip shunts. To reduce cost, metal shunts made from CMOS interconnect [3], lead-frame metal [4], or PCB traces [5] can also be used. However, they have two main disadvantages. First, their nominal resistance may spread significantly (±30%). Second, their large temperature coefficients (TCs ∼3500 ppm/°C) result in significant resistance variations over temperature. Although their nominal spread can be trimmed, their large TCs require the use of temperature compensation schemes.

In [4], an on-chip temperature sensor is used to sense and digitize shunt temperature. This information is then used to correct the current sensor output digitally. Although it achieves a gain error of 0.3% over the industrial temperature range (−40 °C to +85 °C), it requires a complex trimming scheme and consumes 20 μW.

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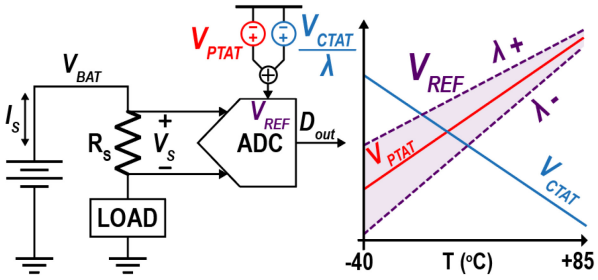

Fig. 1. Block diagram of the proposed current sensor.

In [3], rather than directly measuring the shunt temperature, the TC of a metal shunt is compensated by applying a proportional-to-absolute-temperature (PTAT) voltage reference to the current sensor's ADC. However, it consumes 25 μW and only achieves a gain error of 0.9% with an on-chip metal shunt. Furthermore, accurately correcting a PCB trace's slightly different TC still requires using a (relaxed) temperature sensor [5].

However, the current consumption of the aforementioned sensors is still too high for IoT and wearable applications. In [6], a Coulomb-counter that consumes less than 8.5 μW is presented, but it relies on a precision off-chip shunt to achieve good accuracy over temperature. A recent work [7] presents a current sensor with a TC-tunable voltage reference, making it suitable for different types of shunts, but its 0.5-mW power consumption is too high.

This letter, an extended version of [8], presents a high-side current sensor that achieves low power consumption and high accuracy with low-cost metal shunts. This is achieved by combining an energy-efficient hybrid ΔΣ modulator with a TC-tunable voltage reference. This approach obviates the need for an extra temperature sensor and a complex digital back-end. It consumes only 2.5 μW, representing a 3× improvement on the state of the art while achieving competitive gain error (<0.6%) and energy efficiency figure of merit (FoM) (149 dB).

II. Temperature Compensation

The proposed TC-tunable voltage reference (V_{REF}) is realized by adding a PTAT voltage (V_{PTAT}) to a complementary-to-absolute-temperature (CTAT) voltage (V_{CTAT}) scaled by an appropriate factor ($\pm\lambda$), thus allowing a low gain error to be achieved for a broad range of shunts. The block diagram of the resulting current sensor is shown in Fig. 1, where the TC-tunable V_{REF} is given by

$$V_{\mathrm{REF}} = V_{\mathrm{PTAT}} \pm \frac{V_{\mathrm{CTAT}}}{\lambda} \tag{1}$$

and V_S is the voltage drop across the shunt. The λ factor can then be tuned to match the TCs of different types of low-cost metal shunts.

Fig. 2 depicts the circuit that generates V_{PTAT} and V_{CTAT}. A differential V_{PTAT} (ΔV_{BE}) is generated by two NPNs with different current densities. An NPN-based bias circuit generates a well-defined PTAT current I (10 nA @ 25 °C), which is then used to bias the core circuit that generates V_{PTAT} and V_{CTAT}. Compared to using a PNP-based bias circuit, this obviates the need for an extra opamp to force ΔV_{BE}

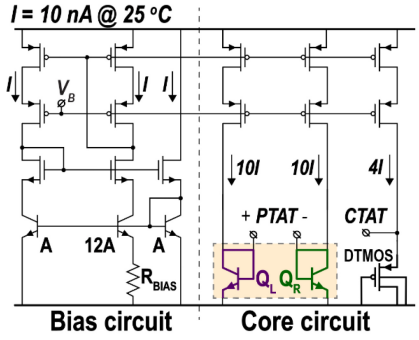

Fig. 2. V_{REF} generation.

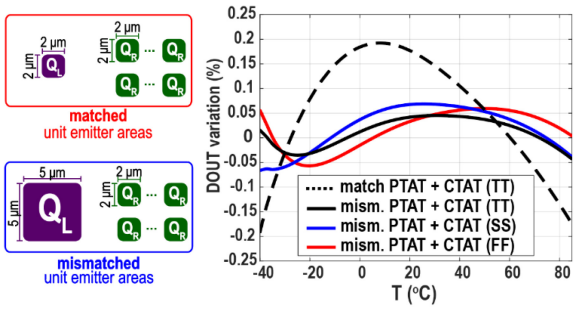

Fig. 3. Effect of the nonlinear PTAT on the D_{OUT} variation of the on-chip shunt for different process corners.

across R_{BIAS}, thus reducing power consumption. Also, in the chosen 180-nm process, NPNs have a larger current gain, which reduces base-current-related biasing errors.

However, if V_{CTAT}/λ (typically <1 mV) is derived from the base-emitter voltage of a BJT (V_{BE} ~650 mV @ 25 °C), λ may have to be quite large (>1000) to achieve the target TC. To relax this, a dynamic threshold-voltage MOS transistor (DTMOST) based on a low-threshold device is used to generate a smaller V_{CTAT}(V_{SG} ~ 65 mV @ 25 °C). As a result, λ can be significantly reduced.

In addition to the mismatch between the shunt's first-order TC (TC1) and V_{REF}, the shunt's second-order TC (TC2) will also limit the achievable gain error. In this letter, the on-chip shunt, similar to the one used in [3], has an expected TC2 of ~ −1 ppm/K^2. To mitigate this, a systematic nonlinearity can be introduced in V_{PTAT} by using NPNs with mismatched unit emitter areas, as shown in Figs. 2 and 3. This mismatch leads to different base resistances, resulting in a small second-order nonlinearity. As shown in Fig. 3, this significantly reduces the variation of D_{OUT} (= V_S/V_{REF}) over temperature. For comparison purposes, two V_{PTAT} cores were designed, one with matched NPN emitter areas and one with mismatched areas.

III. Readout Circuitry

The block diagram of the readout is shown in Fig. 4. It is built around a first-order ΔΣM with an 8-tap FIR-DAC. This has a uniform impulse response, which facilitates accurate Coulomb-counting even with dynamic currents. The use of an FIR-DAC reduces the swing at the virtual ground of the loop filter and thus enables the use of a continuous-time (CT) gain stage (25 V/V) before the discrete-time (DT) integrator. This reduces the input-referred kT/C noise of the DT integrator and thus increases energy efficiency. The PTAT portion of V_{REF} is fed back through an equally weighted (1/8) 8-tap FIR-DAC via the first stage, while the CTAT portion of V_{REF} is fed back through the first tap of the FIR-DAC via the DT integrator. The gain of the first stage is thus part of the large λ.

To avoid instability due to the extra delay introduced by the FIR-DAC, a compensation FIR-DAC is connected to the output of the first stage. The k_i coefficients [0, 0.87, 0.75, 0.62, 0.5, 0.37, 0.25, 0.12] are

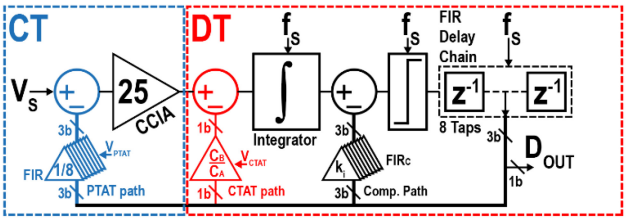

Fig. 4. Block diagram of the current sensor.

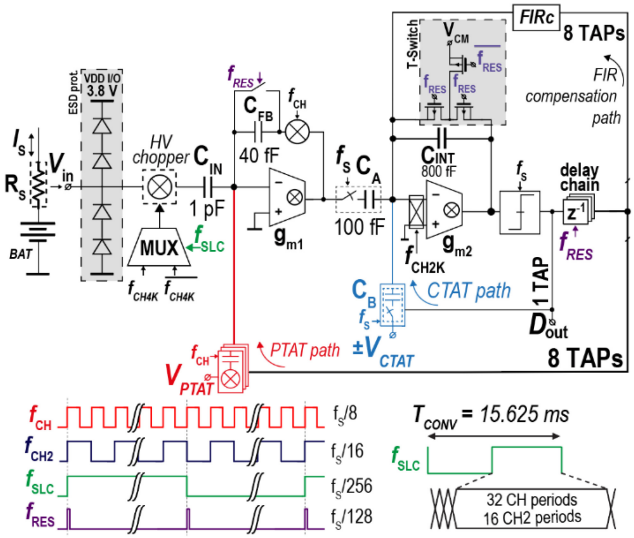

Fig. 5. Single-ended representation of the readout circuit.

chosen to make the sampled impulse response of the resulting loop filter the same as that of an integrator driven by a 1-bit DAC [10].

A single-ended representation of the proposed fully differential current sensor is shown in Fig. 5. Its input stage consists of a capacitively coupled instrumentation amplifier (CCIA) [11], which efficiently amplifies the voltage drop across the shunt resistor V_S, inherently suppressing offset and 1/f noise, while also isolating its virtual ground voltage from the battery's voltage.

Thanks to the FIR-DAC, the error swing at the CCIA input is reduced by 6× to around ~20 mV. The CCIA can then be realized as an energy-efficient single-stage current-reuse OTA g_{m1} (400 nA) with a closed-loop gain of 25 V/V (= C_{FB}/C_{IN}).

The CCIA is followed by a chopped switched-capacitor (SC) integrator built around g_{m2}, also implemented by another current-reused OTA (200 nA). It serves as a summing node for the tunable $\pm V_{CTAT}/\lambda$ feedback signal, as well as the output of a second 8-tap FIR-DAC that compensates for the extra delay caused by the feedback FIR-DAC. The λ factor is then defined by

$$\lambda = A_{CCIA} \cdot \frac{C_A}{C_B}. \tag{2}$$

Since A_{CCIA} = 25 V/V, this approach results in a reasonable ratio between the capacitors C_A and C_B, where C_A is the sampling capacitor of the integrator and C_B is the feedback CDAC of the CTAT path. To tune λ, C_A (60–140 fF) and C_B (5–25 fF) are 5-bit and 3-bit trimmable capacitors, respectively. An extra bit is responsible for controlling the polarity of the λ. This strategy allows the TC of V_{REF} to be tuned from 3000 to 4000 ppm/°C. This trimming range allows the λ factor to handle different low-cost shunt resistors and to reduce the resulting first-order gain error to less than 0.1%.

Fig. 6(a) shows the FIR-DAC. It consists of eight sets of two capacitors connected to the virtual ground of the CCIA. The V_{PTAT} is then injected through switches connected to the eight different terminals generated by the delay chain (Fig. 5). The V_{CTAT} voltage is injected

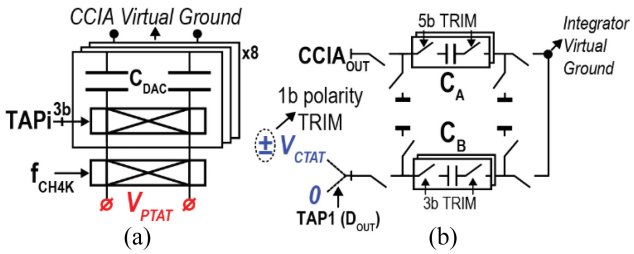

Fig. 6. (a) FIR-DAC injecting V_{PTAT} into the virtual ground of the CCIA. (b) Single-ended representation of the SC DAC injecting V_{CTAT} into the virtual ground of the integrator.

into the loop through an SC DAC, where a single-ended representation is shown in Fig. 6(b). Depending on D_{OUT} (the first tap of the delay chain), $\pm V_{CTAT}$ or 0 is feedback. The combination of both DACs generates the V_{REF} described in (1).

To achieve low offset, both the CCIA and the integrator are chopped. The chopping frequency f_{CHOP} should be greater than the OTA's 1/f-noise corner, but as low as possible to reduce residual offset due to chopping artifacts. However, due to the CT front-end, the chopping frequency f_{CHOP} should be set to $f_S/2$ or f_S to avoid quantization noise-folding, which happens at $2f_{CHOP}$. Conveniently, the equally weighted 8-tap FIR-DAC creates notches in the modulator's noise transfer function (NTF), which allows f_{CHOP} to be safely set to multiples of $f_S/2Nt$, where Nt is the number of taps [10]. The CCIA and the integrator are chopped in this design at $f_{CH4K} = f_S/8$ and $f_{CH2K} = f_S/16$, respectively.

The modulator's residual offset is suppressed by system-level chopping (SLC). This is done by inverting the clock of the CCIA's input chopper [4] and refreshing the memory storage elements (integrator and flip-flops) at every reset phase. A timing diagram of this operation is shown in Fig. 5.

A problem related to the use of CCIAs is the output ripple generated by their offset [11]. As shown in Fig. 5, there is no dc feedback path for this offset, which means that it is amplified by the open-loop gain of g_{m1} and can potentially cause clipping. To deal with this issue, reset switches were added in parallel with the feedback capacitors. These switches close at every reset phase of the $\Delta\Sigma$M operation, when gm_1 is also auto-zeroed by storing the offset at C_{IN}. Although switch leakage will cause the output ripple to increase slowly, this is limited to less than 100 mV_{pp} during a conversion time of 16 ms.

The input switches can handle an ICMR from -15 to 15 V. However, in practice, this is limited by ESD protection. In this design, two diodes were placed in series between the input terminals and the ESD supply rail, allowing the ICMR to be extended by approximately 1.4 V beyond the ESD supply rail. In the 0.18-μm process used, the combination of series-connected ESD diodes and a 3.8-V I/O pad supply limits the CM voltage range to -0.3 to 5 V, which covers most single-cell battery applications.

The CCIA's gain suppresses the input-referred kT/C noise of the SC integrator, allowing for a small sampling capacitor ($\sim$100 fF). However, this low capacitor value and the low sampling frequency of this design impose a high off-impedance requirement for the integrator's reset switch; which would otherwise limit the integrator's dc gain and hence, the modulator's noise floor. To avoid this issue, the reset switch was implemented as a T switch (Fig. 5). This reduces switch leakage significantly, thus preserving the integrator's dc gain.

IV. Measurement Results

The current sensor prototype, shown in Fig. 7(a), was designed and fabricated in a standard 0.18-μm CMOS process. It occupies 1.6 mm^2 and draws 1.4 μA from a 1.8-V source, where the digital logic consumes 600 nA. At a sampling frequency of 32 kHz, the ADC has a 5.4 μV of resolution at $\sim$16-ms conversion time.

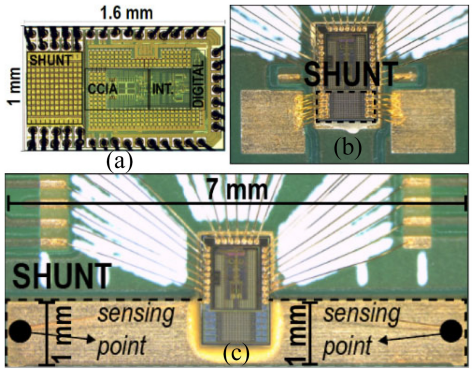

Fig. 7. Chip micrograph. (a) Die micrograph. (b) Die mounted for on-chip measurements. (c) Die mounted over a PCB trace shunt.

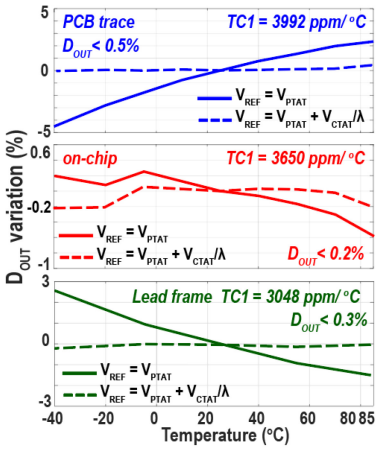

Fig. 8. D_{OUT} variation for different kinds of shunt resistors.

For the on-chip shunt (20 mΩ) measurements [Fig. 7(b)], four chips were mounted on a PCB. Ten bond wires (<1 mm) were connected to each terminal of the shunt to minimize their series resistance and self-heating, which could create a significant temperature gradient between the shunt and the temperature-sensing transistors. In the case of the PCB shunt (3 mΩ) measurements [Fig. 7(c)] four chips were mounted directly onto the PCB trace with a thermally conductive (1 W/mK) and electrically isolating glue to improve thermal contact and maintain galvanic isolation. Similarly, a sample mounted on a lead-frame copper shunt (300 $\mu\Omega$) was also measured.

After a gain trim at 25 °C, the sensor was characterized from -40 °C to 85 °C. A fixed value of λ was used for each type of shunt. Fig. 8 shows the typical decimated output D_{OUT} over temperature for an on-chip shunt, a PCB shunt, and a lead-frame shunt. To demonstrate the sensor's flexibility, results are shown for $V_{REF} = V_{PTAT}$ and $V_{REF} = V_{PTAT} + V_{CTAT}/\lambda$. For the PCB and lead-frame shunts, less than 0.5% of D_{OUT} variation was measured. As shown in Fig. 8, this drops to less than 0.2% for the on-chip shunt, mainly due to the reduced D_{OUT} curvature obtained with the mismatched NPN PTAT core, Fig. 9.

After a gain trim at 25 °C, multiple samples of the sensor were characterized with on-chip and PCB shunts. With $\lambda = +500$, the gain error of four on-chip shunt samples remained below 0.35% for currents up to ± 2 A from -40 °C to 85 °C (Fig. 10). With $\lambda = -50$, four PCB shunt samples were measured over a wider (± 15 A) current range. An additional $D_{OUT}{}^2$ correction factor [3] was added to reduce caused by the combination of shunt self-heating and the finite thermal resistance between the PCB trace and the chip. The gain error then remains below 0.6% (Fig. 11). The offset with ($\leq$500 nV) and without SLC ($\leq$40 μV) are shown in Fig. 12 for CM input voltages ranging from -0.3 to 5 V.

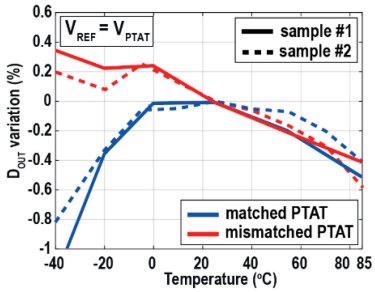

Fig. 9. On-chip shunt D_{OUT} variation for the matched/mismatched cases.

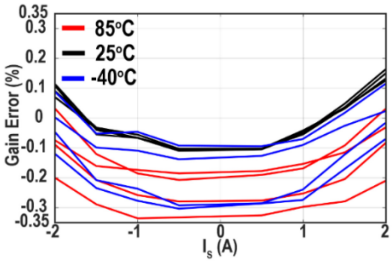

Fig. 10. Gain error for the on-chip shunt.

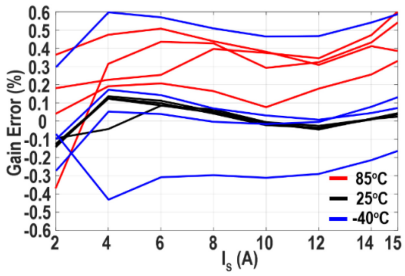

Fig. 11. Gain error for the PCB trace shunt.

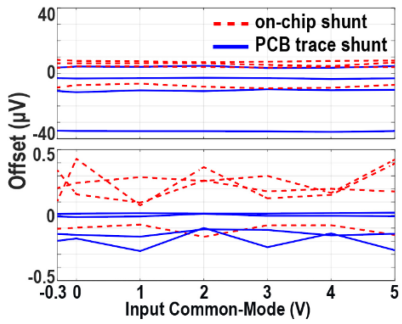

Fig. 12. Offset measurements.

Table I summarizes the sensor's performance and compares it to the state of the art. The proposed sensor requires 3× less supply current and achieves competitive gain error with three types of shunts. Due to its beyond-the-rails ICMR (−0.3 to 5 V), the sensor can be used for battery monitoring in most single-cell battery applications.

V. Conclusion

A flexible current sensor for low-power Coulomb-counting has been presented. An ADC with a TC-tunable V_{REF} enables the accurate compensation of the TCs of various low-cost shunt resistors, resulting in gain errors <0.6% over the industrial temperature range. This approach does not require an explicit temperature sensor, resulting in significant power savings. Moreover, using a CCIA front-end combined with an 8-tap FIR-DAC enables an energy-efficient design while allowing a beyond-the-rails ICMR. The current sensor draws 3× less power (2.5 μW) than the state of the art while maintaining a competitive energy efficiency FoM of 149 dB and beyond-the-rails ICMR of 5 V. These characteristics make it well suited for low-cost Coulomb-counting in single-cell battery-operated IoT/wearable applications.

TABLE I
Performance Summary and Comparison Table

	This Work		Vroonhoven ISSCC 20 [6]	Xu JSSC 18 [3]	Shalmany JSSC 17 [4]		Z. Tang ISSCC 22 [7]
I_{SUPPLY}	2.5 µW		< 9 µW	19.6 µW	19.5 µW		477 µW
Gain Error	on-chip	±0.35%	±0.5%*	±0.9%	on-chip	±0.3%§	±0.25%
	PCB trace	±0.6%			lead-frame	±0.3%§	
I_{RANGE}	on-chip	±2A	±1A	±4A	on-chip	±5A	±25A
	PCB trace	±15A			lead-frame	±36A	
Shunt	*on-chip*	20 mΩ	50 mΩ*	10 mΩ	on-chip	10 mΩ	2 mΩ
	PCB trace	3 mΩ			lead-frame	260 µΩ	
Offset	on-chip	25 µA	< 100 µA	40 µA	on-chip	4 µA	3 mA
	PCB trace	100 µA			lead-frame	400 µA	
ICMR	-0.3 to 5 V		0 to 60 V	0 to 25 V	low-side		low-side
V_{SUPPLY}	1.8 V		1.7 to 60 V	1.5 to 2 V	1.3 to 1.7 V		1.8 V
T_{RANGE}	-40 to 85°C		-50 to 125°C	-40 to 85°C	-40 to 85°C		-40 to 85°C
Resolution	5.4 μV_{RMS}		-	1.5 μV_{RMS}	2 μV_{RMS}		8.5 μV_{RMS}
T_{CONV}	16 ms		-	2 ms	10 ms		0.1 ms
FoM**	149 dB		-	162 dB	155 dB		149 dB
Tech.	0.18		0.18 BCD	0.18 BCD	0.13		0.18

** Uses a custom/off-chip low-TCR shunt*
*** FoM=Dynamic Range + 10log(Bandwidth/Power)*
§ Uses an extra ADC for temperature sensing allied to an extensive calibration.

Acknowledgment

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