A 1-to-4GHz Multi-Mode Digital Transmitter in 40nm CMOS Supporting 200MHz 1024-QAM OFDM signals with more than 23dBm/66% Peak Power/Drain Efficiency

Beikmirza, Mohammadreza; Shen, Yiyu; de Vreede, Leo C.N.; Alavi, Morteza S.

DOI
10.1109/CICC53496.2022.9772797

Publication date
2022

Document Version
Final published version

Published in
2022 IEEE Custom Integrated Circuits Conference, CICC 2022

A 1-to-4GHz Multi-Mode Digital Transmitter in 40nm CMOS Supporting 200MHz 1024-QAM OFDM signals with more than 23dBm/66% Peak Power/Drain Efficiency

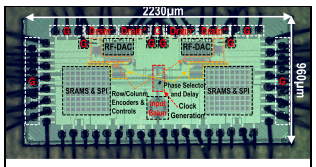
Mohammadreza Beikmirza, Yiyu Shen, Leo C.N. de Vreede, Morteza S. Alavi

Delft University of Technology, Delft, The Netherlands

To support wideband complex modulated signals and comply with the stringent requirements of modern communication standards in an energy-efficient manner, recently, digital transmitters (DTXs) have been explored to fully benefit from the high-speed switching and integration capabilities of nanoscale CMOS technologies [1-5]. These DTXs are primarily exploiting a polar or Cartesian architecture. In a polar DTX [1,2], two eigenvectors of amplitude (ρ) and phase (Φ) are generated from the in-phase (I) and quadrature (Q) baseband signals using non-linear coordinate rotation transformations (i.e., CORDIC). Provided that ρ is constant, the achievable drain efficiency (DE) is constant (Fig. 1 top). However, polar DTXs cannot manage large modulation bandwidth due to their non-linear I/Q to ρ/ Φ conversion. Moreover, their phase and amplitude paths must recombine at the output stage without any delay mismatch to maintain linear operation. In contrast, Cartesian DTX variants can handle signals with large modulation bandwidth [3]. Nevertheless, their DE is lower than their polar counterparts owing to the linear combination of orthogonal I/Q vectors, yielding a 3-dB worst-case output power loss at the orthogonal (I/Q) axes. Alternatively, a multi-phase operation can be utilized that compromises polar and Cartesian features by mapping the I/Q signals into two non-orthogonal basis vectors with 45° relative phase difference and magnitudes of I_{MP}=I-Q, Q_{MP}=$\sqrt{2}$Q [4]. This architecture inherits the advantages of the cartesian DTX, such as wideband operation, symmetrical, and synchronized I/Q paths along with a DE behavior that imitates the polar case. This paper presents a multi-mode DTX that uses both Cartesian and multi-phase operation modes to target applications requiring large modulation bandwidth, decent spectral purity and average efficiency.

Fig. 2 illustrates the detailed operating modes of the proposed DTX. It features various operational modes comprising Cartesian and multi-phase configurations utilizing LO clocks with different duty cycles (12.5/25/50%). The multi-phase mode exploits the I/Q to multi-phase mapping. The related LO clocks with the 45° phase difference are selected based on the octant where the IQ baseband point is located (Fig. 2). Each configuration operates in interleaving and non-interleaving modes. In the interleaving mode, for each DPA, the upconverted baseband signals are digitally combined while sharing a single power cell (Mode-1/Mode-3). In the non-interleaving mode, one of the DPAs is allocated to only I (I_{MP}), and the other DPA is assigned to merely Q (Q_{MP}), and thus, their outputs are combined at the output drain nodes of the power cell (Mode-2/Mode-4).

Fig. 3 exhibits the implemented chip's block diagram. An off-chip single-ended clock at 4×f_C is applied to an on-chip transformer to convert this clock into its differential counterparts. These high-speed differential clocks are then applied to a divide-by-2 circuit to generate four quadrature clocks at 2×f_C with 50%-LO clocks (i.e., 2×$f_{LO,k\_50\%}$, k=0, 90, 180, 270). A following divide-by-2 circuit is employed to generate the desired carrier frequency at f_C with 50%-LO clocks and 45° phase differences (i.e., $f_{LO,k\_50\%}$, k=0, 45, …, 315). Depending on the intended operational mode, an arrangement whereby the 50%-LO clocks at f_C have 12.5%-LO or 25%-LO overlaps are selected. The duty-cycle generation circuit produces the related 12.5%-LO or 25%-LO clocks by bit-wise AND operation of the corresponding LO pairs to generate the required 8 phases ($f_{LO,k}$, k=0, 45, …, 315). Besides, to modulate the LO clock properly, a phase selector (sign-bit mapper) is exploited whose control signals in Cartesian modes are I/Q sign bits ($Sign_I$/$Sign_Q$). Based on this 2-bit selection code, the complementary LO clock pairs can be swapped, and thus the entire four quadrants of the constellation diagram are covered. The multi-phase operation modes demand 3-bits selection control signals to cover 8-octant, two of which are $Sign_I$/$Sign_Q$ bits, and the third one is generated in the digital domain based on the multi-phase mapping operation ($SB_{,UP}$). Furthermore, data-aware clock gating circuitry is employed to reduce the power consumption at power back-off. An alternative sampling clock, generated from another off-chip clock source, can also set the modulation bandwidth independent of the LO clock. Every bank comprises 4-bit binary (LSB) and 7-bit unary (MSB) segmented sub-cells, each consisting of a bit-wise AND upconverter. This chip is combined with an off-chip Class-E-like matching network. Since in Class-E, the drain voltage can go up to 2-to-3 times the supply voltage, a cascode power cell topology was adopted in this design to prevent reliability violations.



Die micrograph.

The DTX is realized in a 40nm CMOS, occupying 2.23×0.96mm^2, including pads and SRAMs. The baseband data of each DPA is independently applied to the DTX using four parallel on-chip 1-K SRAMs running at 600MHz. The power consumption of all blocks (except SRAMs) is included in the reported system efficiency (SE). The measured peak output power (P_{Out}), DE, and SE for different operational modes versus frequency are shown in Fig.4. With a 1.1V supply, in Mode-1, the DTX delivers 23.18dBm peak P_{Out} with 66.26/52.59% DE/SE at 2.1GHz. The peak P_{Out} and DE vary in different operational modes. Namely, in Mode-1, the effective duty-cycle of the combined vectors can be as high as 50% when using a 25% LO clock, while in Mode-4, the combined duty-cycle reduces to 37.5%, yielding a significant efficiency improvement. Overall, the DTX achieves a 3dB bandwidth 1.35GHz in a 1.65-to-3GHz band while maintaining decent performance.

A 400-point static measurement is performed using 20 samples for each I/Q symbol (first I/Q quadrant) at 2.4GHz. In Fig. 4, measured DE contours for different operational modes are extracted for the four-quadrant plane. Generally, the Cartesian configuration has 4-petal-like efficiency contours along the diagonal lines of the IQ plane. In contrast, the multi-phase operation has 8-petal-like efficiency contours where multiples of 22.5° lines are located, imitating polar contours, thus reducing the phase dependency of the efficiency. The dashed gray circle on the IQ plane represents the average power region for a 160MHz 256-QAM OFDM signal. The enhanced efficiency performance is evident in multi-phase operation modes as it has higher efficiency on the gray circle than its Cartesian DTX.

Utilizing a simple memory-less DPD, for a 160MHz 4-channel 64-QAM OFDM signal, the DTX delivers an average P_{Out} of 13.5/11.4/7.7/9.4dBm, achieving an ACLR of better than -42/-40/-40/-38dBc and an average EVM of -36/-34/-34/-32dB, operating in modes-1/2/3/4, respectively (Fig. 5). The average ACLR and EVM of the DTX in different modes of operation are verified with various 1-to-4-channel 40MHz 64-QAM OFDM signals. Generally, the ACLR is better than -38dBc, and the EVM is better than -32dB. Finally, a 200MHz single-channel 256(1024)-QAM OFDM signal at 2.4GHz in Mode-1/-4 is applied. The average delivered output power is 14.11/9.29(12.23/7.32)dBm, while the ACLR and EVM are better than -42/-41(-43/-43)dBc and -34.6/-33.1(-33.5/33.9)dB, respectively. The performance of the multi-mode DTX is summarized in Fig. 6. Compared to the DTXs without efficiency enhancement techniques, the proposed DTX exhibits the highest data rate, reasonable average efficiency, and high peak output power, suitable for wireless communication systems.

Acknowledgment: This work has been supported by Ampleon under project DIPLOMAT.

References:

[1] A. Ben-Bassat et al., "10.5 A Fully Integrated 27dBm Dual-Band All-Digital Polar Transmitter Supporting 160MHz for WiFi 6 Applications," ISSCC, Feb. 2020.

[2] M. Hashemi et al., "An intrinsically linear wideband polar digital power amplifier," IEEE JSSC, vol. 52, no. 12, Dec. 2017.

[3] M. Beikmirza et al., "A Wideband Four-Way Doherty Bits-In RF-Out CMOS Transmitter," IEEE JSSC, vol. 56, no. 12, Dec. 2021.

[4] W. Yuan and J. Walling, "A Multiphase Switched Capacitor Power Amplifier," IEEE JSSC, vol. 52, no. 5, pp. 1320-1330, May 2017.

[5] D. Zheng et al., "24.5 A 15b Quadrature Digital Power Amplifier with Transformer-Based Complex-Domain Power-Efficiency Enhancement," ISSCC Feb. 2020.

2022 IEEE Custom Integrated Circuits Conference (CICC) | 978-1-6654-0756-4/22/$31.00 ©2022 IEEE | DOI: 10.1109/CICC53496.2022.9772797

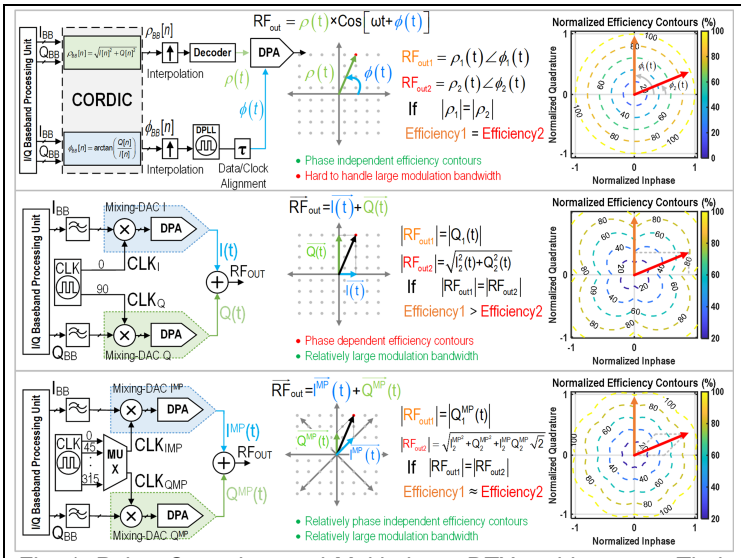


Fig. 1. Polar, Cartesian, and Multi-phase DTX architectures. Their operational concepts and corresponding efficiency countors' phase dependency comparison.

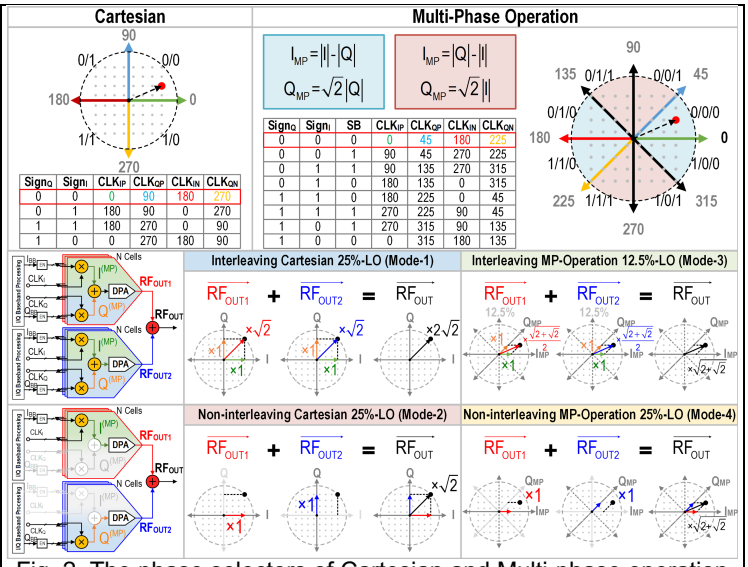


Fig. 2. The phase selectors of Cartesian and Multi-phase operation (top) and different (Non-)interleaving operating modes (bottom).

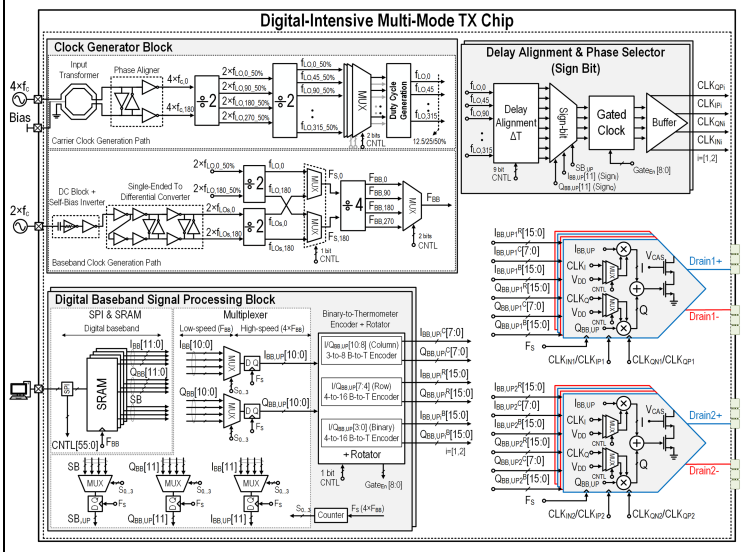


Fig. 3. The detailed block diagram of the proposed digital multi-mode transmitter.

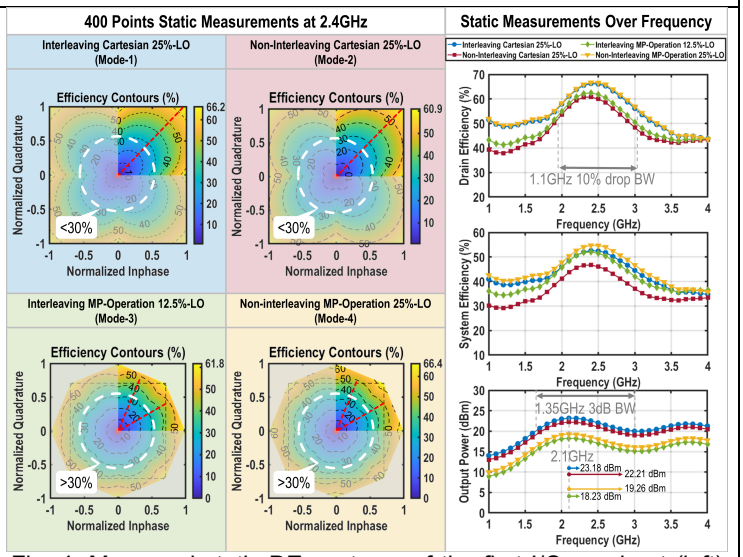


Fig. 4. Measured static DE contours of the first I/Q quadrant (left) and frequency responses, DE, SE, P_{Out}, (right) for different operational modes.

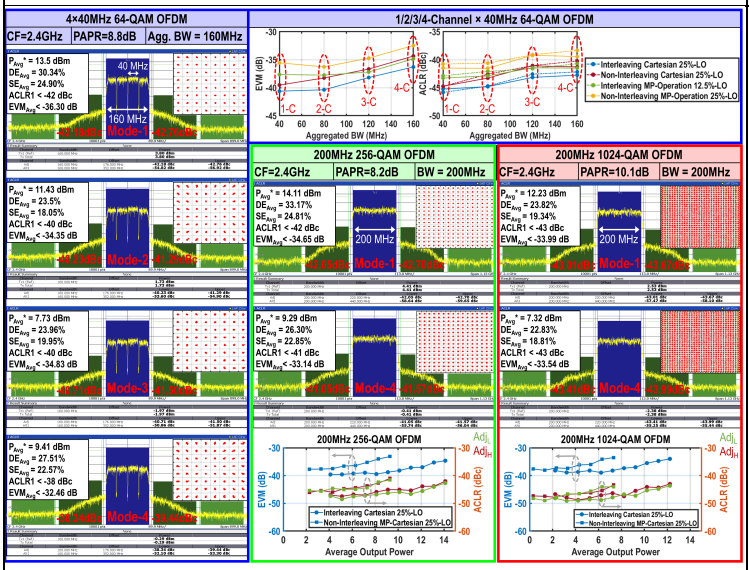


Fig. 5. Measured 4-carrier 160MHz 64-QAM OFDM (blue frame), single-carrier 200MHz 256/1024-QAM OFDM (green/red frames).

Specifications	This Work		ISSCC 2020 A. Bassat	ISSCC 2017 M. Hashemi	JSSC 2017 W. Yuan	JSSC 2021 M.R. Beikmirza	ISSCC 2020 D. Zheng	JSSC 2020 S.W. Yoo	ISSCC 2021 B. Yang	
Technology	CMOS 40nm		CMOS 28nm	CMOS 40nm	CMOS 130nm	CMOS 40nm	CMOS 55nm	CMOS 60nm	CMOS 40nm	
Architecture	Multi-mode DTX*		Polar	Polar	Multi-phase SCPA	Quadrature 4-way Doherty	Quadrature	TI-Doherty /Class G	Quadrature SCPA /Hybrid Doherty	
Die Area (mm²)	2.1 (0.72 ‡)		4 ¥	0.45	3.7	3.55 (1.5 ‡)	NA (1.19 ‡)	3.36	2.2	
Supply (V)	1.1		1.4	0.5	3	1	1.2 / 2.4	2.5	1.2/2.4	
Frequency (GHz)	2.4		2.5 5	2.2 **	1.8	5.4	0.85	2.4	2.4	
3dB Power BW	1.35 GHz		N/A	1.5 GHz *	750 MHz	1.3 GHz	1 GHz *	N/A	1.1GHz **	
Peak P_{out} (dBm)	(Mode-1) 23.18	(Mode-4) 19.26	27	27	14.6	26	27.4	29.3	30	30.3
Peak DE (%)	66.2	66.4	N/A	N/A	43.8	N/A	47.4	N/A	40.2	41.3
Peak SE (%)	52.59	54.73	53	35	28.8 †	24.9	30.66	43.1	N/A	36.5
Modulation scheme	1024-QAM OFDM	1024-QAM OFDM	MCS11	MCS11	64-QAM @2GHz	64-QAM @2GHz	64-QAM LTE	256-QAM OFDM	256-QAM OFDM	64-QAM LTE	1024-QAM	64-QAM OFDM	256-QAM	1024-QAM
Bandwidth (MHz)	200	200	40	160	20	40	10	40	240	10	10	10	60	40
PAPR (dB)	10.1	10.1	6.9	7.8	8		5.1	8.64	9.68	5.7	6.8	10.9	6.98	9.86
Avg. P_{out} (dBm)	12.23	7.32	20.1	19.2	6.1 §		20.9	18.9	17.8	23.6	23.2	19.1	23.3	20.4
Avg. DE (%)	23.82	22.83	N/A	N/A	17.5 §		N/A	43.1	41.2	N/A	36.2%	30.3%	30.7%	22.6%
Avg. SE (PAE) (%)	19.34	18.81	(28.9)	(21.2)	14.3 §†		15.2	24.5	22.1	24.4	N/A	N/A	N/A	N/A
EVM (dB)	-33.99	-33.54	-35	-35	NA	-31	-29.1	-40	-32.2	-25.6	-44.5	-41.7	-31.9	-35.9
ACLR (dBc)	-43.0/-43.6	-43.4/-43.9	N/A	N/A	-43/-49	-40/-45	-30.3/-31.7	-47/-47	-39/-39	-31/-32	N/A	N/A	-32/-30	-35/-34
Linearization	DPD		DPD		NO		DPD	DPD		NO	NO		DPD	

- * Off-chip matching network.
- ** Estimated from reported figures and plots.
- ‡ Core area.
- ¥ Area including Digital front end, DPLL, and LB/HB DTX.
- † Excluding LO generation.
- § For a 10MHz QAM signal with PAPR = 8-9dB.

Fig. 6. Performance summary and comparison with state-of-the-art works.