A TCAD Simulation Study on the Short-circuit Performance of 650V P-pillar Offset Super-junction MOSFET

Yuan, Wucheng ; Liu, Ke ; Wang, Shaogang; Tan, Chunjian; Ye, Huaiyu

DOI
10.1109/ICEPT56209.2022.9873366

Publication date
2022

Document Version
Final published version

Published in
Proceedings of the 2022 23rd International Conference on Electronic Packaging Technology (ICEPT)

A TCAD Simulation Study on the Short-circuit Performance of 650V P-pillar Offset Super-junction MOSFET

1st Wucheng Yuan
School of Microelectronic
Southern University of Science and Technology
Shenzhen, China
12132485@mail.sustech.edu.cn

2nd Ke Liu
School of Microelectronic
Southern University of Science and Technology
Shenzhen, China
12132459@mail.sustech.edu.cn

3rd Shaogang Wang
Fac.EEMCS
Delft University of Technology
Delft, Netherlands
S.Wang-10@tudelft.nl

4th Chunjian Tan
Fac.EEMCS
Delft University of Technology
Delft, Netherlands
c.tan@tudelft.nl

5th Huaiyu Ye*
School of Microelectronicsn
Southern University of Science and Technology
Shenzhen, China
yehy@sustech.edu.cn

2022 23rd International Conference on Electronic Packaging Technology (ICEPT) | 978-1-6654-9905-7/22/$31.00 ©2022 IEEE | DOI: 10.1109/ICEPT56209.2022.9873366

***Abstract*—The limitation of Silicon based power MOSFET was broken by the super-junction (SJ) structure, which can provide lower specific on-resistance and higher breakdown voltage compared with the conventional power MOSFET structure. Multi-epitaxial and multi-ion-implant technology, as a mature manufacturing process of the SJ structure, has been widely used in the field of SJ-MOSFET. Therefore, this process is applied to construct the cell structure of 650V SJ-MOSFET in our study. Based on practical application, high current caused by unexpected short circuit will induce an increasing of the internal temperature of SJ-MOSFET, which leads to an irreversible damage in the SJ-MOSFET devices. However, the short-circuit robustness of SJ-MOSFET is still unstable, and the structure needs to be further improved. In our study, the electrical performance of a 650V SJ-MOSFET with offset P-pillar is theoretically investigated by means of technology computer aided design (TCAD) when the SJ-MOSFET is short-circuited. The results clearly show that the optimized SJ-MOSFET can withstand the source-drain voltage of 400V for at least 10 μs in the case of the short-circuit. The thermal distribution and peak temperature of the cell structure of SJ-MOSFET are also simulated to assist in the analysis of the short circuit capable of the device. In addition, the hole current density distribution of two SJ-MOSFETs is considered to gain insight into the effect of P-pillar parameters on the short-circuit robustness. The result represents that the structure with offset P-pillar can effectively improve the short-circuit capability.**

Keywords—: Super-junction structure; Short circuit; P-pillar offset; TCAD simulation

I. INTRODUCTION

Power semiconductor MOSFETs are widely used in the power-electronics applications as an efficient power switch. Power semiconductor devices with low on-resistance and high breakdown voltage are ideal goals pursued by scholars and engineers. Conventional vertical double-diffused MOSFETs (VDMOSFETs) are widely used in practice. In terms of mechanism, in order to improve the breakdown voltage (BV) of silicon-based devices, it is necessary to increase the thickness of the drift region of the VDMOSFET, or reduce the doping concentration of the drift region, which will sacrifice the on-state resistance (R_{on}) of the device. Thus, the "silicon limit" is existed, which indicates the trade-off relationship between R_{on} and BV of the VDMOSFET [1]. New construction of power MOSFET, named Super-Junction MOSFET (SJ-MOSFET), was proposed about thirty years ago, which is based on the charge-compensation theory [1, 2]. The principle of SJ-MOSFET at on-state is similar to that of the VDMOSFET, but the N-drift region is replaced by alternating vertical PN junction with higher doping concentration. By introducing this structure, the electric field within the MOSFET is added horizontal component, not just vertical electric field in the VDMOSFET. Thus, the SJ-MOSFET can withstand a sufficiently high BV, and provide a lower R_{on} compared with the conventional VDMOSFET, which effectively break the "silicon limit". Although wide-bandgap semiconductor materials have made significant progress in the field of power devices in the application field of around 650V, silicon-based SJ-MOSFETs still occupy the vast market due to the cost advantages, and the optimization of their structures is still of great significance.

During the operation of the power MOSFET, the device may inevitably encounter non ideal situations because of some unexpected accident. One example is short circuit (SC) condition. The MOSFET is suffering high drain-source current and voltage while operating in SC conditions, which will generate much heat within the device. The device may be failure due to overheating. Therefore, the capability of SC has received more attention in the practical application areas. According to the failure mechanisms induced by SC condition, the SC capability of SJ-MOSFET needs to be improved.

There are two types of SC mode in actual condition. One is hard switching fault (HSF), where the load is in short-circuit before the MOSFET operating under on-stage. After the device is turned on, it is directly subjected to short-circuit current. The other condition is fault under load (FUL), the load is in short-circuit while the switch is fully turned on [3]. The SJ-MOSFET under HSF condition is studied in this paper. To characterize the SC capability, short-circuit withstand time (SCWT) needs to be measured. Besides, the peak temperature is also required to analysis during the SC period.

The withstanding ability and failure mechanisms of the SJ-MOSFET operating under SC condition have been reported in several previous studies [3-7]. The SC capability requirement for a 650 V MOSFET is the SCWT greater than 10 μs at 400 V DC bus voltage. However, a few studies focus on enhancing

the withstanding ability of SC of SJ-MOSFET through improving the structure of device [8].

In this paper, a possessing optimized offset P-pillar planar gate Si SJ-MOSFET is proposed by technology computer aided design (TCAD) simulation. The offset P-pillar is obtained by changing the implantation windows. The SJ-MOSFET with optimized P-pillar possesses a better SC capability, meanwhile, retains good BV and R_{on}. This paper is structured as follows. Firstly, the structures of normal SJ-MOSFET and the proposed device are presented in Sec. II. Then, the electrical characteristic of two devices under static operation and SC condition are investigated in Sec. III. Finally, the paper ends with a conclusion.

II. DEVICE STRUCTURE

Fig. 1(a) and (b) are the cross-section diagrams of the SJ-MOSFET and proposed device, respectively. The multi-epitaxy and multi-ion-implantation technology are used to fabricate the SJ-MOSFET [2]. The device grows a buffer layer with high doping concentration on the substrate, and then repeats the steps of epitaxial growth and ion implantation 11 times. To form the device with optimized structure, the window of Boron implant should be offset slightly on several N-doped layers near top. The offset direction is different between two adjacent epitaxial layers. And the offset direction of every other epitaxial layer is the same. The offset distance of P-pillar is controlled by changing the ion implantation windows, i.e., changing the photomask, as shown in Fig. 1(c). The detail parameters of the device are listed in Table I.

Several physical models are considered in the simulation process for ensuring the accuracy of the results. The models include carrier mobility models (the Philips unified mobility model, high-field saturation, the doping-dependent and transverse field–dependent portion of the inversion accumulation layer mobility (IALMob)) and recombination models (Shockley-Read-Hall, Auger recombination, avalanche generation (Okuto–Crowell)) and effective intrinsic density model (OldSlotboom). Besides, due to the significance of high temperature during the SC process, the thermodynamic model is considered.

III. SIMULATION RESULT AND DISCUSSION

A. Static Electrical Parameters

Fig. 2(a) shows the BV waveforms of the conventional SJ-MOSFET and proposed device at 25 °C. The voltage are 798.4 V and 754.3 V while the drain-source current (I_{DS}) is 50 μA. The *I-V* waveform is shown at Fig. 2(b). The measured R_{on} are 563 mΩ and 598 mΩ. Fig. 2(c) illustrates two similar V_{th} curves. When the I_{DS} is 0.08 mA, the V_{th} are 3.11 V and 3.12 V. Besides, Fig. 2(d) shows that the saturation current are 20.98 A and 18.65A while V_{ds} is 200 V. Compared with conventional SJ-MOSFET, the BV, R_{on} and saturation current of the proposed device are a little degenerated but still close.

B. Short-Circuit Simulation Result and Analysis

Fig. 3 shows the schematic of circuit used for testing SC capability of devices. Here, the V_{dc} provides 400 V input DC bus voltage. The gate driver (V_g) applies single pulse voltage (10 V / 0 V) to control the device under test (DUT) turn on or off. Meanwhile, a 10 Ω resistance (R_g) is connected in series with the pulse voltage and the gate of device. The parasitic inductance *L* is 10 nH.

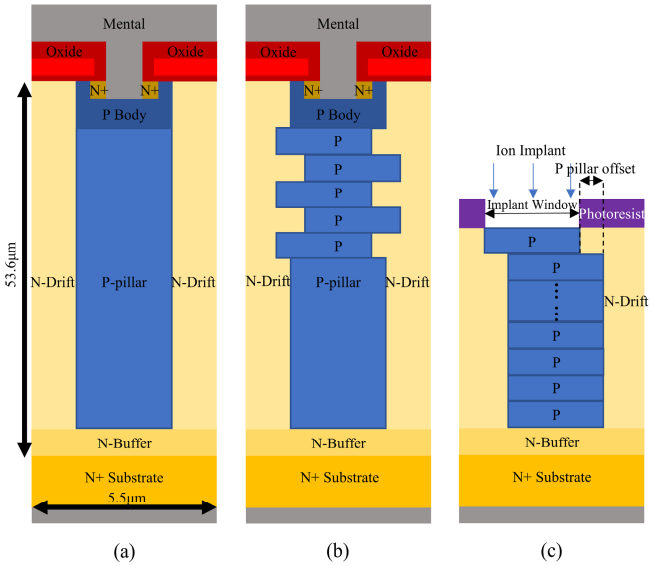


Fig. 1. The cross-section schematics of (a) the conventional SJ-MOSFET, (b) the proposed P-pillar offset SJ-MOSFET, and (c) the fabricated process of P-pillar offset.

TABLE I. DETAIL PARAMETERS OF DEVICES

Parameters	SJ-MOSFET	Proposed Structure
N+ substrate doping (cm^{-3})	2.2×10^{19}	
N buffer implant (cm^{-2})	4×10^{15}	
N buffer epi thickness (μm)	12	
N epi doping (cm^{-3})	4.27×10^{13}	
N epi implant (cm^{-2})	7.75×10^{12}	
N drift epi thickness (μm)	3.5	
P-pillar implant (cm^{-2})	3.83×10^{13}	
P-pillar implant window (μm)	1.1	
Number of epi layer	11	
P body implant (cm^{-2})	1×10^{13}	
Gate oxide thickness (μm)	0.1	
Poly Si thickness (μm)	0.5	
Cell pitch (μm)	5.5	
P-pillar implant offset (μm)	N.A.	0.4
P-pillar offset layers	N.A.	5

The SC waveforms of conventional SJ-MOSFET and proposed device under different SC time are illustrated in Fig. 4. Specifically, the SC current of two devices rises rapidly to 16.5 A and 14.0 A at the beginning of the SC process, respectively. With the gate pulse width is applied, the total temperature also rises because of the self-heating effects and the drain-source current decreases because of reduction of electron mobility caused by high temperature. If the applied gate pulse voltage is turned off in the safe operate time range, the SC current can be switched off successfully. However, if the short-circuit time of the device exceeds the limitation of the short-circuit safe operating area, its drain-source current will rise again and cannot be turned off.

This phenomenon is caused by the parasitic BJT latch-up within the SJ-MOSFET [9, 10]. With the internal temperature of the SJ-MOSFET increasing, the hole concentration in the

P-pillar also increases. While the hole concentration achieves a specific level, the hole current flows into the N+ source region, causing the parasitic BJT latch-up. Therefore, the gate voltage could no longer control the drain-source current. Finally, the devices are thermal breakdown. The SCWT of the conventional SJ-MOSFET in this paper is 8 μs, and the P-pillar offset SJ-MOSFET has a SCWT of 10 μs, which is better than the conventional device. The lattice temperature distribution and maximum temperature at t_{SC} is 8 μs are shown in Fig. 5. The maximum temperature regions are observed near the bottom of the P-pillar inside the device, respectively. Particularly, due to the lower drain-source current, the maximum temperature of the P-pillar offset SJ-MOSFET is 50 K lower than the conventional SJ-MOSFET.

Due to the significance of parasitic BJT latch-up to SC failure, analyzing the hole current is necessary. The hole current density distribution in the different devices at the 9th μs of SC process are illustrated in Fig. 6(a) and Fig. 6(b). The hole current is mainly observed in the P-pillar and P body regions. As shown in Fig. 6(c), the hole current density of the conventional SJ-MOSFET is significantly higher than the P-pillar offset SJ-MOSFET, including in the vertical direction of P-pillar and horizontal direction of P body near N+ source. Due to the lower hole current density, fewer holes could pass through the P body near the N+ source, thus the parasitic BJT is more difficult to activate.

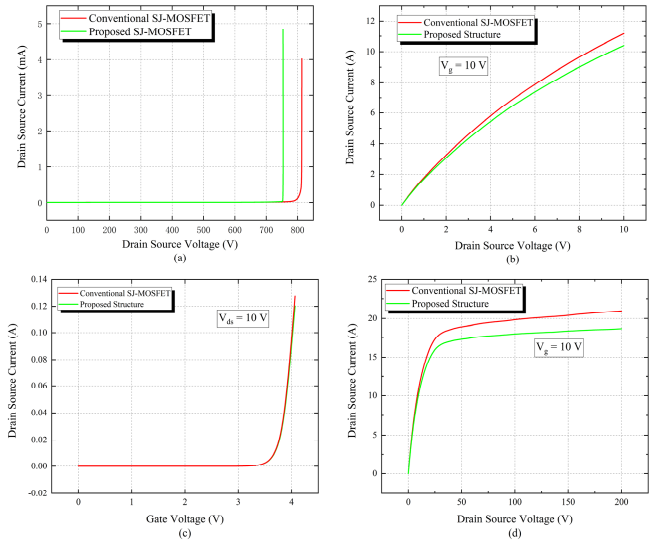


Fig. 2. The comparison of (a) the breakdown voltage, (b) the forward *I-V* characteristic, (c) the threshold voltage, and (d) saturation characteristic.

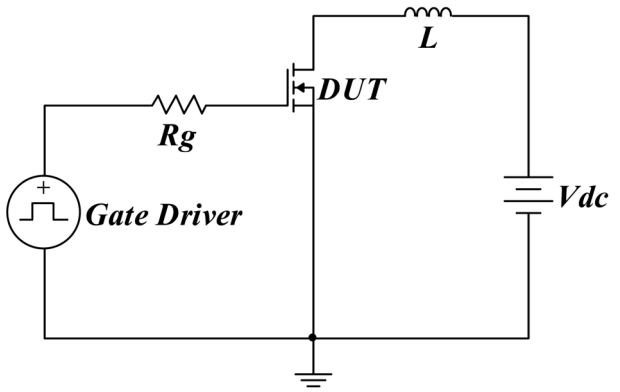
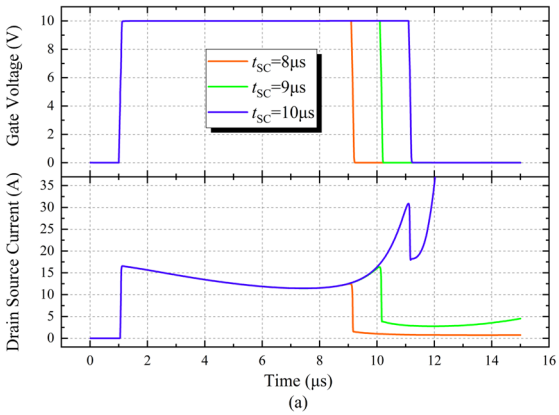


Fig. 3. Schematic of the test circuit for SC.



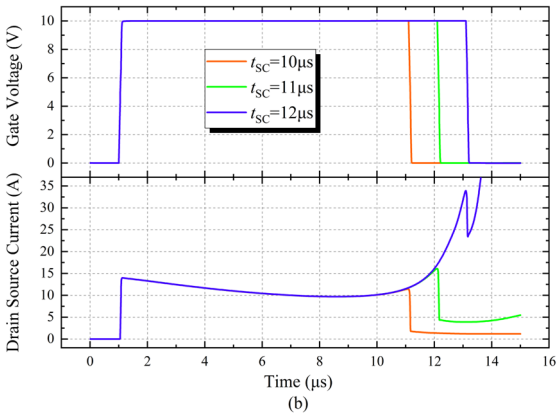


Fig. 4. SC simulated characteristic results of (a) the conventional SJ-MOSFET and (b) the proposed P-pillar offset SJ-MOSFET under 400 V dc bus voltage with different SC time.

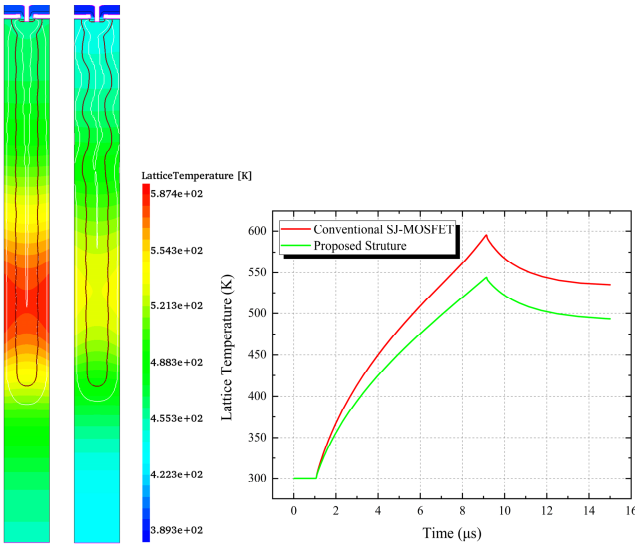
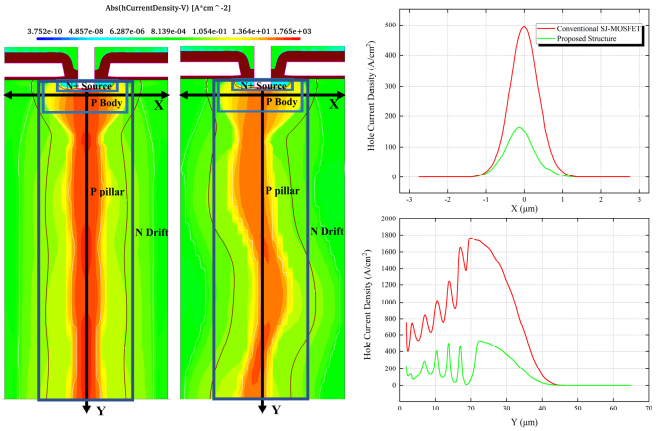


Fig. 5. (a) Lattice temperature distribution of two devices at 8 μs after SC process beginning and (b) temperature variation of two devices with time.



(a) (b) (c)

Fig. 6. Distribution figures of hole current density near the N+ source of (a) the conventional SJ-MOSFET and (b) the P-pillar offset SJ-MOSFET; (c) The hole current distribution in the horizontal and vertical direction.

IV. Conclusion

This paper presents a 650 V, 598 mΩ P-pillar offset super-junction MOSFET (SJ-MOSFET) for improving short-circuit (SC) capability. Compared with the conventional silicon-based SJ-MOSFET, the device proposed in this paper achieves a longer short-circuit withstand time (from 8 μs to 10 μs) during short circuit period with minimal consumption of static characteristics, and effectively reduces the internal peak temperature of the device (from 595 K to 544 K). Specifically, the offset P-pillar structure effectively reduces the hole current density near the N+ source, thereby suppressing the parasitic BJT latch-up effects of the SJ-MOSFET, which enhances the short-circuit capability.

Acknowledgment

This work is supported by the Shenzhen Fundamental Research Program (JCYJ20200109140822796), and the NSQKJJ under grant K21799119.

References

[1] C. Xing Bi, "Breakthrough to the "Silicon limit" of power devices," in 1998 5th International Conference on Solid-State and Integrated Circuit Technology. Proceedings (Cat. No.98EX105), 23-23 Oct. 1998 1998, pp. 141-144, doi: 10.1109/ICSICT.1998.785827.

[2] G. Deboy, N. Marz, J. P. Stengl, H. Strack, J. Tihanyi, and H. Weber, "A new generation of high voltage MOSFETs breaks the limit line of silicon," in International Electron Devices Meeting 1998. Technical Digest (Cat. No.98CH36217), 6-9 Dec. 1998 1998, pp. 683-685, doi: 10.1109/IEDM.1998.746448.

[3] H. Qin et al., "A comprehensive study of the short-circuit characteristics of SiC MOSFETs," in 2017 12th IEEE Conference on Industrial Electronics and Applications (ICIEA), 18-20 June 2017 2017, pp. 332-336, doi: 10.1109/ICIEA.2017.8282866.

[4] M. Pfost, C. Unger, G. Cretu, M. Cenusa, K. Büyüktas, and U. Wahl, "Short-circuit safe operating area of superjunction MOSFETs," in 2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD), 12-16 June 2016 2016, pp. 335-338, doi: 10.1109/ISPSD.2016.7520846.

[5] M. Okada et al., "Superior Short-Circuit Performance of SiC Superjunction MOSFET," in 2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD), 13-18 Sept. 2020 2020, pp. 70-73, doi: 10.1109/ISPSD46842.2020.9170126.

[6] J. Roig, E. Stefanov, and F. Morancho, "Thermal behavior of a superjunction MOSFET in a high-current conduction," IEEE Transactions on Electron Devices, vol. 53, no. 7, pp. 1712-1720, 2006, doi: 10.1109/TED.2006.876277.

[7] N. Badawi, A. E. Awwad, and S. Dieckerhoff, "Robustness in short-circuit mode: Benchmarking of 600V GaN HEMTs with power Si and SiC MOSFETs," in 2016 IEEE Energy Conversion Congress and Exposition (ECCE), 18-22 Sept. 2016 2016, pp. 1-7, doi: 10.1109/ECCE.2016.7855410.

[8] X. Zuo et al., "Improvement on short-circuit ability of SiC super-junction MOSFET with partially widened pillar structure," Chinese Physics B, 2022.

[9] T. Chirilă, W. Kaindl, T. Reimann, M. Rüb, and U. Wahl, "Analysis of the role of the parasitic BJT of Super-Junction power MOSFET under TLP stress," Microelectronics Reliability, vol. 55, no. 9, pp. 1481-1485, 2015/08/01/ 2015, doi: https://doi.org/10.1016/j.microrel.2015.06.108.

[10] M. Okawa et al., "First Demonstration of Short-Circuit Capability for a 1.2 kV SiC SWITCH-MOS," IEEE Journal of the Electron Devices Society, vol. 7, pp. 613-620, 2019, doi: 10.1109/JEDS.2019.2917563.