

## 23.7 A BJT-Based Temperature Sensor with $\pm 0.1$ C( $3\sigma$ ) Inaccuracy from $-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$ and a $0.85\text{pJ}\cdot\text{K}^{-2}$ Resolution FoM Using Continuous-Time Readout

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### 23.7 A BJT-Based Temperature Sensor with $\pm 0.1^\circ\text{C}$ ( $3\sigma$ ) Inaccuracy from $-55^\circ\text{C}$ to $125^\circ\text{C}$ and a $0.85\text{pJ}\cdot\text{K}^2$ Resolution FoM Using Continuous-Time Readout

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BJT-based temperature sensors are widely used due to their high accuracy over a wide temperature range with a low-cost 1-point trim. Although resistor-based sensors can achieve better energy efficiency, they typically require a 2-point trim to achieve comparable accuracy, while thermal-diffusivity based sensors achieve superior accuracy at the cost of energy efficiency [1]. This paper presents a BJT-based temperature sensor that achieves both excellent accuracy and energy efficiency. To avoid the  $\text{KT}/\text{C}$  noise limitations of conventional discrete-time (DT) readout schemes [2,3], it employs a compact continuous-time (CT) front-end. Component mismatch, which often limits the accuracy of CT front-ends [4,5], is mitigated by a combination of dynamic element matching (DEM) and a low-cost resistor-ratio self-calibration scheme. As a result, the sensor achieves a resolution FoM of  $0.85\text{pJ}\cdot\text{K}^2$ , and a competitive inaccuracy of  $\pm 0.1^\circ\text{C}$  ( $3\sigma$ ) from  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  after a 1-point trim. This makes it  $4\times$  more energy-efficient than state-of-the-art BJT-based sensors with similar accuracy [2,4,5].

The operating principle of the sensor is illustrated in Fig. 23.7.1. Two identical PNPs  $Q_{1,2}$ , biased at a current-ratio  $p = 7$ , are used to generate a PTAT voltage  $\Delta V_{\text{BE}}$ , which is forced across a resistor  $R_1$  by an opamp ( $A_1$ ) to generate a PTAT current  $I_{\text{PTAT}} = \Delta V_{\text{BE}}/R_1$ . This current is then mirrored to the current DAC (IDAC) of a  $\Delta\Sigma$  modulator ( $\Delta\Sigma\text{M}$ ), which balances either  $a^* I_{\text{PTAT}}$  or  $b^* I_{\text{PTAT}}$ , where  $a$  and  $b$  are constants, against a CTAT current  $I_{\text{CTAT}} = V_{\text{BE}}/R_2$ . The latter is efficiently generated by using the  $1^{\text{st}}$  integrator of the  $\Delta\Sigma\text{M}$  to force  $V_{\text{BE}}$  across resistor  $R_2$ . Compared to [5], this implementation requires one less amplifier, and eliminates the power-hungry CClA used in [4].

As shown in Fig. 23.7.1, the modulator's bitstream average  $\mu$  will vary from 0, when  $b^* I_{\text{PTAT}} = I_{\text{CTAT}}$ , to 1, when  $a^* I_{\text{PTAT}} = I_{\text{CTAT}}$ . In this work, the choice of  $a = 1$ ,  $b = 4$ , and  $R_1/R_2 = 6$  ensures that  $\mu$  varies from  $-0.1$  to  $-0.9$  as temperature varies from  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  (Fig. 23.7.1 bottom). Although  $\mu$  is a non-linear function of temperature, it is a linear function of  $X = V_{\text{BE}}/\Delta V_{\text{BE}}$ , which means that the PTAT spread of  $V_{\text{BE}}$  can be conveniently corrected by a digital offset trim [2], and that a linear function of temperature  $\mu_{\text{lin}}$  can be expressed as  $\mu_{\text{lin}} = \alpha / (\alpha + X)$ , where  $\alpha$  ( $\sim 11$ ) is a digital constant.

To ensure that the PTAT spread in  $V_{\text{BE}}$  is the dominant source of error, and thus facilitate 1-point trimming,  $\Delta V_{\text{BE}}$  errors due to the offset and overdrive of the bias opamp  $A_1$  should be minimized. As shown in Fig. 23.7.2, the offset of  $A_1$  (cascode telescopic amplifier) is mitigated by chopping, while its gain ( $>83\text{dB}$  over PVT) is high enough to ensure that its static overdrive ( $\sim 8\mu\text{V}$  at room temperature, RT) adds negligible error. The mismatch of the current mirrors and PNPs is mitigated by applying DEM. As in [5], Kelvin connections are used to prevent  $\Delta V_{\text{BE}}$  sensing errors due to the IR drop across the associated PNP DEM switches. To mitigate errors due to DAC, DEM, and chopping transients, which will accumulate in the proposed CT front-end, unused current-mirror branches of the IDAC are routed to a current dumper that replicates  $V_{\text{BE}}$ , and the unity-gain bandwidth of  $A_1$  (UGBW  $\sim 220\text{kHz}$ ) is high enough to limit the duration of the remaining transients to a few microseconds over PVT.

Another source of error is the spread in the  $R_1/R_2$  ratio, which should be smaller than  $0.01\%$  to ensure a BJT-dominated inaccuracy. As this cannot be realized by layout techniques alone, a low-cost resistor-ratio self-calibration scheme is proposed. As shown in Fig. 23.7.2, it involves using either  $V_{\text{BE}1}$  or  $V_{\text{BE}1} + \Delta V_{\text{BE}}$  to set the voltage across  $R_2$ . By making successive ADC conversions, and assuming that die temperature, and hence,  $V_{\text{BE}1}$  and  $\Delta V_{\text{BE}}$  are constant, the actual value of the  $R_1/R_2$  ratio can be accurately determined (Fig. 23.7.2, bottom). The measured resistor mismatch can then be compensated in the digital domain. However, detecting  $0.01\%$  mismatch requires an equivalent temperature sensing resolution of  $\sim 1.5\text{mK}$  ( $3\sigma$ ), which, in turn, requires a relatively long conversion time. To achieve the necessary resolution, while also suppressing errors due to ambient temperature drift, the resistor ratio is determined by averaging 10 pairs of short, but still thermal-noise-limited conversions of 40ms.

By relying on the accuracy of  $\Delta V_{\text{BE}}$ , the spread of  $V_{\text{BE}}$  can be determined by a voltage calibration scheme [6], which can replace the time-consuming temperature trim. This involves replacing  $V_{\text{BE}1}$  with an external reference voltage  $V_{\text{CAL}}$ , allowing  $\Delta V_{\text{BE}}$ , and thus, die temperature, to be determined. The combination of resistor-ratio and voltage calibration enables the sensor to be calibrated at low-cost, since neither an accurate temperature reference nor stringent temperature stability is required.

As shown in Fig. 23.7.2, a single-ended  $2^{\text{nd}}$ -order DSM is used to digitize the CT current signals generated in the BJT front-end. It is sampled at  $f_s = 50\text{kHz}$ , which provides a good balance between conversion time and errors caused by switching transients. Its

CT  $1^{\text{st}}$  integrator is built around a 2-stage Miller-compensated opamp ( $A_2$ ) and an integration capacitor  $C_{\text{int}}$  ( $= 60\text{pF}$ ), which limits integrator swing.  $A_2$  (UGBW  $= 600\text{kHz}$ ) is fast enough to ensure that the integrated error due to switching transients at its input is always less than  $80\mu\text{V}$  and thus contributes negligible error compared to the voltage ( $V_{\text{BE}}$ ) across  $R_2$ . Its DC gain ( $>110\text{dB}$  over PVT) suppresses the noise of the  $2^{\text{nd}}$  integrator, allowing this to be implemented with area-efficient switched-capacitor circuitry that draws  $4\times$  less power than the  $1^{\text{st}}$  stage.

The resolution of the proposed sensor is mainly determined by the thermal noise generated by the PNPs and the resistors (46%), the PMOS current mirrors (16%), and the bias opamp  $A_1$  (38%). As shown in Fig. 23.7.2, the  $1/f$  noise of  $A_1$  and  $A_2$  is mitigated by chopping at  $f_s$  without incurring quantization-noise (Q-noise) folding, while the  $1/f$  noise of the current mirrors is mitigated by DEM. Due to current-mirror mismatch, the use of barrel-shifting DEM would cause periodic variations in  $I_{\text{PTAT}}$ , which would be effectively multiplied by the bitstream and give rise to significant Q-noise folding. This can be avoided by applying bitstream-controlled (BSC) DEM, which ensures that every DEM state has a similar occurrence for both BS states, effectively averaging out the mismatch errors [6]. In this work, BSC DEM is realized by utilizing two independent barrel-shifting registers for all current mirrors. The PNP DEM frequency was set to  $f_s/1000$  (50Hz), which mitigates the PNP's  $1/f$  noise, and is also low enough to avoid significant Q-noise folding.

Two sensors were fabricated on the same die in a  $0.18\mu\text{m}$  CMOS process, enabling the use of differential measurements to cancel ambient temperature drift during resolution measurements. Each sensor occupies only  $0.12\text{mm}^2$  and draws  $9.5\mu\text{A}$  ( $8.9\mu\text{A}$  analog and  $0.6\mu\text{A}$  digital) from a  $1.7\text{V}$  supply. The DEM and chopping signals are generated by on-chip logic, while the  $\text{sinc}^2$  decimation filter is implemented off-chip for flexibility.

Twenty chips (40 sensors) in ceramic DIL packages were characterized from  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  in a temperature-controlled oven. To minimize ambient temperature drift, they were mounted in good thermal contact with a large aluminium block. Figure 23.7.3 (top left) shows the temperature spread of the measured  $\mu$  after linearization (with  $\alpha = 11.44$ ) and batch calibration, which result in an inaccuracy of  $\pm 0.45^\circ\text{C}$  ( $3\sigma$ ). The chosen value of  $\alpha$  ensures that the sensor's systematic residual non-linearity is below  $\pm 0.015^\circ\text{C}$  over the entire temperature range. After a room-temperature trim, this improves to  $\pm 0.2^\circ\text{C}$  ( $3\sigma$ ) (Fig. 23.7.3, top right). Applying the proposed resistor-ratio calibration scheme reduces this even further, to  $\pm 0.1^\circ\text{C}$  (Fig. 23.7.3, bottom left). The low-cost combination of voltage calibration and resistor-ratio calibration results in an inaccuracy of  $\pm 0.2^\circ\text{C}$  (Fig. 23.7.3, bottom right), which is sufficient for many applications.

An FFT of the sensor's output bitstream is shown in Fig. 23.7.4 (top). As expected, the use of barrel-shifting DEM causes significant Q-noise folding, which is eliminated when BSC DEM is used. Below  $100\text{Hz}$ , the resolution of the sensor is thermal-noise-limited, while its  $1/f$  corner is well below  $100\text{mHz}$ . The PNP DEM tones at harmonics of  $50\text{Hz}$  are removed by the notches of a  $\text{sinc}^2$  decimation filter. Figure 23.7.5 (bottom) shows the measured temperature resolution plotted against conversion time, where thermal- and Q-noise-limited operation can clearly be observed. This sensor achieves a  $1.1\text{mK}$  resolution in 40ms, resulting in a resolution FoM of  $0.85\text{pJ}\cdot\text{K}^2$ .

Figure 23.7.5 (left) shows the normalized spread in the ratio  $R_1/R_2$  determined by resistor-ratio calibration. It has a standard deviation of  $0.045\%$ , which agrees with the results of Monte Carlo mismatch simulations, and confirms the need for the proposed resistor-ratio calibration scheme. The measured supply sensitivity (at RT) is  $0.01^\circ\text{C}/\text{V}$  from  $1.7\text{V}$  to  $2.2\text{V}$  (Fig. 23.7.5, right), which is on par with the state-of-the-art.

In Fig. 23.7.6, the performance of the proposed CT BJT-based temperature sensor is summarized and compared with that of state-of-the-art BJT-based designs. Compared to the other high-accuracy sensors (relative inaccuracy  $< 0.2\%$ ) in the table, it achieves the best FoM ( $0.85\text{pJ}\cdot\text{K}^2$ ), while its inaccuracy ( $\pm 0.1^\circ\text{C}$  ( $3\sigma$ ) from  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ ) and supply sensitivity are comparable to the state-of-the-art.

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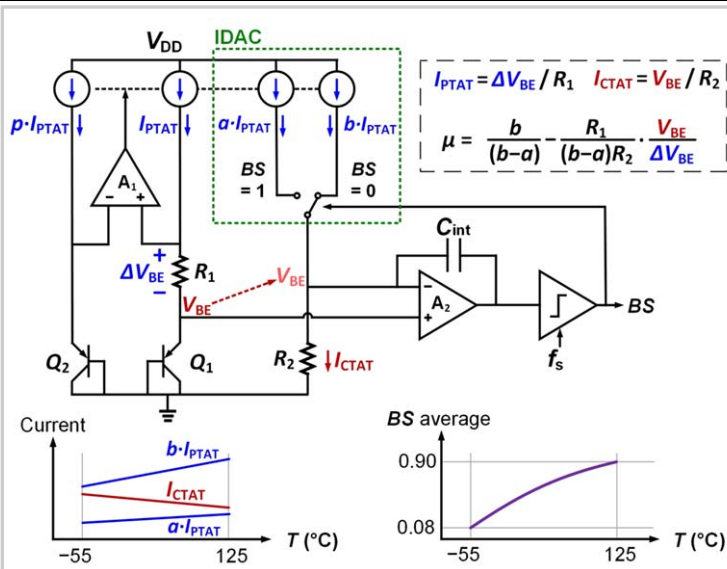


Figure 23.7.1: Operating principle of the proposed BJT sensor (top), and the current signals and bitstream average plotted over temperature (bottom).

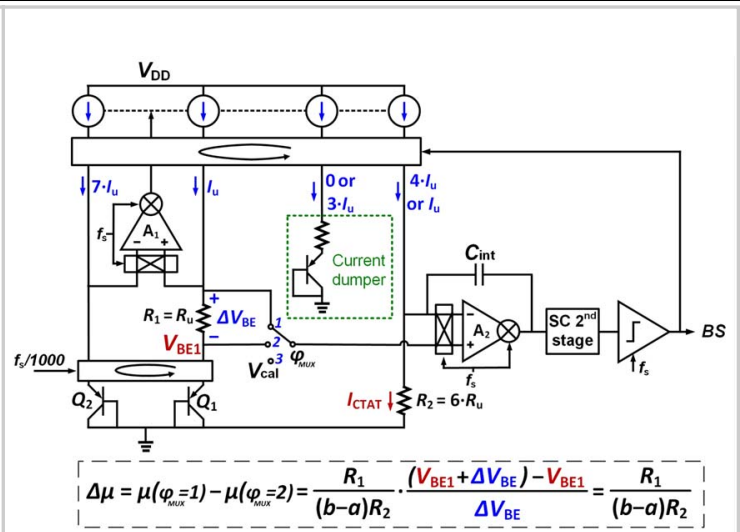


Figure 23.7.2: Simplified schematic of the proposed sensor (top), and the expression used when applying resistor-ratio calibration (bottom).

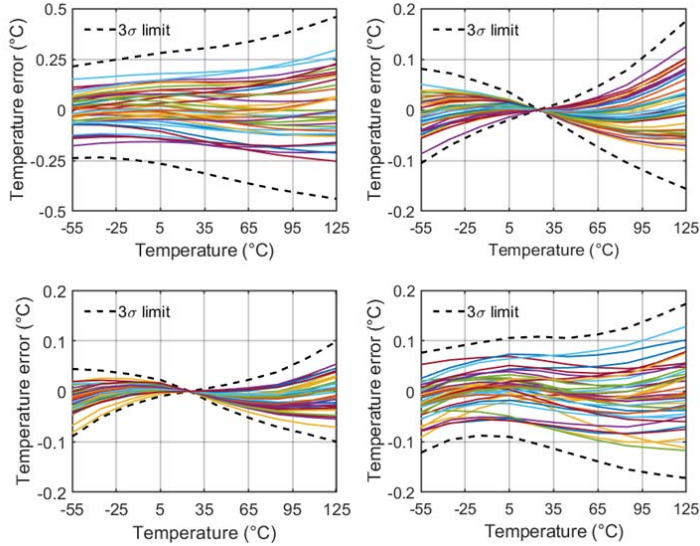


Figure 23.7.3: Measured temperature spread of 40 sensors before trimming (top left), with RT trim (top right), with RT trim and resistor-ratio calibration (bottom left), with voltage- and resistor-ratio calibration (bottom right).

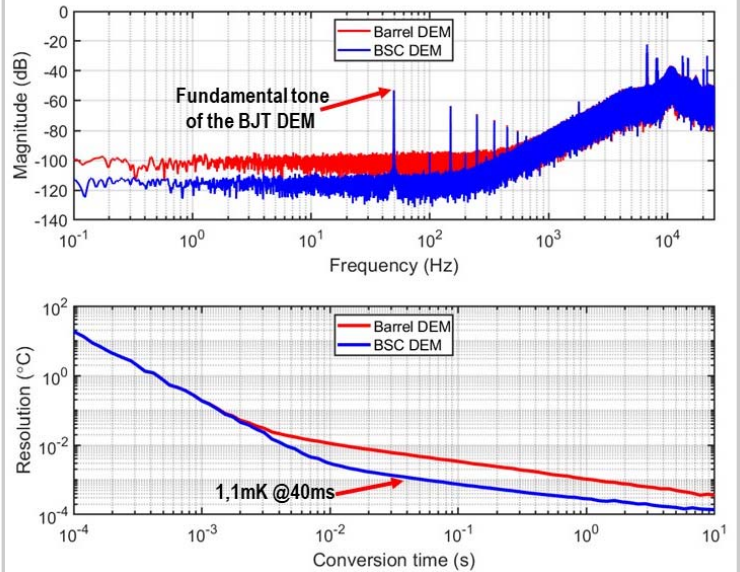


Figure 23.7.4: FFT of the bitstreams generated with barrel-shifting DEM and bitstream-controlled DEM (top), and the resolution vs. conversion time (bottom).

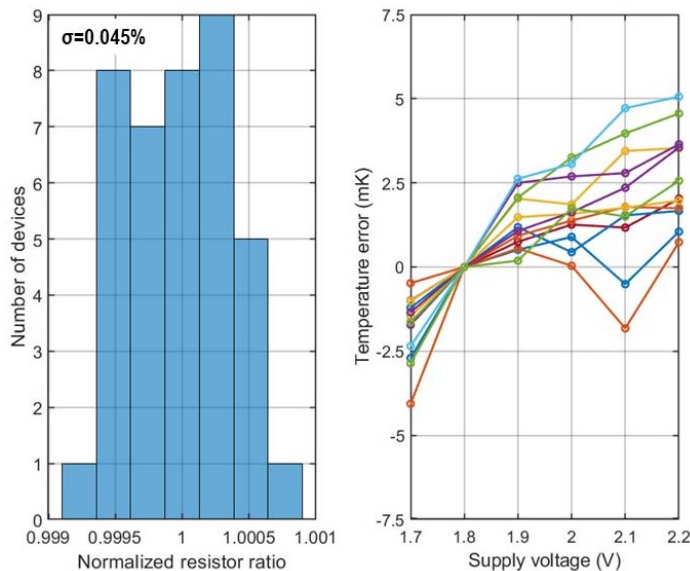


Figure 23.7.5: Normalized spread in the measured resistor ratio of 40 samples (left), the power-supply sensitivity at RT of 12 samples (right).

	JSSC'17 [2]	VLSI'22 [3]	ISSCC'14 [5]	ASSCC'19 [4]	ISSCC'20 [7]	This work
Sensor type	PNP	NPN	PNP	NPN	NPN	PNP
Architecture	DTΔΣM	DTΔΣM	DCM <sup>2</sup>	CTΔΣM	CTΔΣM	CTΔΣM
Technology	0.16μm	0.18μm	0.7μm	0.18μm	0.11μm	0.18μm
Chip area [mm <sup>2</sup> ]	0.16	0.058	0.8	0.35	0.2	0.12
Supply current [μA]	4.6	0.17	55	5.5	550	9.5
Supply voltage [V]	1.5 to 2	1.25	2.9 to 5.5	1.6 to 2.2	1.125	1.7 to 2.2
Supply sensitivity [°C/V]	0.01	0.07	0.1	0.01	-	0.01
Temperature range	-55°C to 125°C	-15°C to 85°C	-45°C to 130°C	-40°C to 125°C	-35°C to 95°C	-55°C to 125°C
3σ Inaccuracy [°C] after a 1-pt trim	±0.06 <sup>3</sup>	±0.15	±0.15 <sup>3</sup>	±0.13 <sup>3,4</sup>	-	±0.1
Relative inaccuracy [%]	0.07	0.3	0.17	0.16	-	0.11
Resolution [mK]	15	15	3	1.27	0.65	1.1
Conversion time [ms]	5	50	2.2	320	0.72	40
Resolution FoM <sup>1</sup> [pJ°C <sup>2</sup> ]	7.8	2.3	3.6	5.4	0.19	0.85

<sup>1</sup>FoM = Energy / Conversion x (Resolution)<sup>2</sup>  
<sup>2</sup>DCM = Duty-Cycle Modulation  
<sup>3</sup>After systematic non-linearity removal  
<sup>4</sup>After CClA gain calibration

Figure 23.7.6: Performance summary and comparison with state-of-the-art energy-efficient BJT sensors.

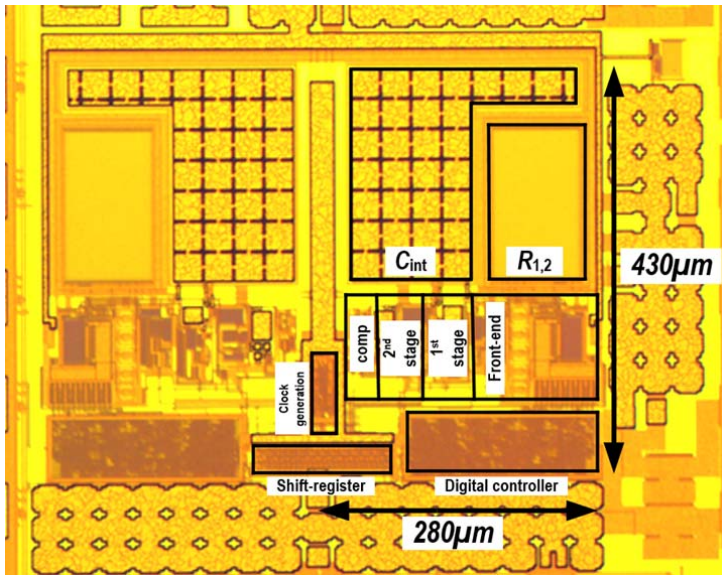


Figure 23.7.7: Die micrograph of the fabricated sensor pair.