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DOI
10.1117/12.2652248

Publication date
2023

Document Version
Final published version

Published in
Quantum Sensing and Nano Electronics and Photonics XIX

PROCEEDINGS OF SPIE

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SPIE.

Event: SPIE OPTO, 2023, San Francisco, California, United States

LinoSPAD2: a 512×1 linear SPAD camera with system-level 135-ps SPTR and a reconfigurable computational engine for time-resolved single-photon imaging

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ABSTRACT

The LinoSPAD2 camera combines a 512×1 linear single-photon avalanche diode (SPAD) array with an FPGA-based photon-counting and time-stamping platform, to create a reconfigurable sensing system capable of detecting single photons. The read-out is fully parallel, where each SPAD is connected to a different FPGA input. The hardware can be reconfigured to achieve different functionalities, such as photon counters, time-to-digital converter (TDC) arrays and histogramming units. Time stamping is performed by an array of 64 TDCs, with 20 ps resolution (LSB), serving 256 channels by means of 4:1 sharing. At sensor level, the pixel pitch is 26.2 μm with a fill factor of 25.1%. The median dark count rate of each SPAD at room temperature is below 100 cps at 6V excess bias, the single-photon timing resolution (SPTR) of each channel is 50 ps FWHM, and the peak photon detection probability reaches ~50% at 510 nm at the same excess bias. The fill factor can be increased by 2.3× by means of microlenses, with good spatial uniformity and flat spectral response above 400 nm. At system level, the average instrument response function (IRF) is 135 ps FWHM. The LinoSPAD2 camera enables a wide range of time-of-flight and time-resolved applications, including 3D imaging, fluorescence lifetime imaging microscopy (FLIM), heralded spectroscopy, and compressive Raman imaging, to name a few. Thanks to its features, LinoSPAD2 is a novel generation of reconfigurable single-photon image sensors capable of adapting their read-out and processing to match application-specific requirements, and combining SPAD arrays with advanced, massively-parallel computational functionalities.

Keywords: Single-photon avalanche diodes (SPADs), Time-resolved imaging, Reconfigurable camera system, Time-to-digital converters (TDCs) on FPGA, Microlenses, Heralded spectroscopy, Compressive Raman imaging

1. INTRODUCTION

Single-photon avalanche diodes (SPADs) are photodetectors capable of generating a digital pulse from a single photon event with picosecond timing precision, in addition to photon-counting capability[1]. Since the first demonstration of SPADs in standard CMOS technology[2], a wide range of single-photon imagers with different levels of integration and varying number of pixels have been explored. SPADs are p-n junctions, biased above breakdown and equipped with a quenching mechanism, so as to operate in Geiger mode.

Various SPAD pixel architectures have been implemented over the years, having in common an avalanche detection, quenching, and recharge mechanism. The pixel is generally equipped with a counter and/or a time-stamping circuitry, while gating may also be used for various purposes[3]. Array architectures vary in size and complexity as well, whereas one-dimensional or linear arrays simplify connectivity and optimize fill factor by implementing pixel circuitry outside the photosensitive area. Two-dimensional arrays on the contrary enable 2D imaging without scanning, at the cost of higher read-out complexity, lower fill factor and less functionality at pixel level. The majority of image sensors are 2D arrays with pixel counts up to millions of pixels and with integrated gating or timing electronics at pixel or column level[3],[4],[5].

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Quantum Sensing and Nano Electronics and Photonics XIX, edited by Manijeh Razeghi, Giti A. Khodaparast, Miriam S. Vitiello, Proc. of SPIE Vol. 12430, 124300K · © 2023 SPIE
0277-786X · doi: 10.1117/12.2652248

The timing precision of SPAD-based imagers has led to a wide range of time-resolved applications, such as fluorescence lifetime imaging microscopy (FLIM), Förster resonance energy transfer (FRET), near-infrared optical tomography, non-line-of-sight imaging, ghost imaging, and quantum random number generation. Time-uncorrelated high-speed imaging, faster than 100 kfps, has also been demonstrated, as well as novel computational imaging approaches that fully exploit the quantum nature of light. All these applications, hitherto implemented mostly with monolithic imagers, have varying needs in terms of processing of the photon data, while recurring to common data acquisition and processing blocks, such as photon counting, histogram generation, coincidence detection or peak finding.

Traditional SPAD image sensor architectures embed fixed circuits, which are partly programmable, so as to enable some degree of operational flexibility, like a variable dead time. Several sensors allow the selection of time-correlated vs. time-uncorrelated photon counting operation by means of pixel-level time-to-digital converters (TDCs) or counters. Usually, some degree of circuit sharing is used to minimize silicon real estate[6],[7],[8]. Other typical degrees of freedom include selecting the start and the end of a gating window[9],[10], masking of noisy pixels[11], and enabling/disabling on-chip data compression[12],[13]. Other types of partially reconfigurable circuits were also explored in a 144×252 SPAD array for LiDAR applications, where full histograms could be reduced to partial histograms and data was compressed[14]. Programmability has also been exploited in [15] relying on digital processing units connected to a backside-illuminated SPAD array. In-pixel reconfigurable logic has been used in [16] to allow photon counting, timestamping, or gating modes. Modular photon processors have been integrated in an advanced 3D-stacked design[17],[18] allowing several intensity and time-resolved operating modes, possibly with some tradeoffs needed in the spatial and temporal resolution.

It would, however, be appealing to move one step beyond and achieve hardware reconfigurability, possibly in real-time. This approach is pursued in this paper, where a field-programmable gate-array (FPGA) is combined to a large SPAD array. In the latter, each SPAD's digital output is coupled directly to an independent input of the FPGA. In this embodiment, the SPAD array consists of a linear 512×1 SPAD sensor, known as LinoSPAD2. The approach is similar to that of [19],[20], except for a larger array and better performing SPAD[21],[22]. Several trade-offs were considered in the FPGA, such as accuracy versus speed, data-rate versus processing power, or timing versus counting. Another advantage of FPGAs is the continuous advances of the underlying CMOS technology, which enables doubling of speed and functionality roughly every 2 years. By contrast, SPADs are implemented in older CMOS technology nodes, which enable better sensitivity and lower noise. The overall system can therefore benefit from smaller transistors for the digital logic thereby achieving higher speed and lower power consumption, while achieving better SPAD performance.

LinoSPAD2 represents a first step towards fully reconfigurable image sensor architectures based on natively digital SPAD arrays, combined with reconfigurable pixel and processing logic. Such sensors will ultimately allow the user to combine high spatial granularity with direct access to information at the single photon level, exploiting SPADs' photon counting capabilities and exquisite timing resolution, as well as the absence of read-out noise.

2. SPAD PIXEL AND IMAGE SENSOR ARCHITECTURES

SPAD pixels can be schematically differentiated in three classes[3],[23],[24], shown in Figure 1a-c from the most simple, comprising quenching, recharge, and interface circuitry to the most complex, comprising time-stamping electronics, such as TDCs. Figure 1 also shows layout examples of published SPAD pixels. The tradeoffs available in the organization of pixel electronics are shown in Figure 1d-f, whereas it can be placed entirely off-pixel (Figure 1d), entirely in-pixel (Figure 1e), and partially in-pixel and partially off-pixel (Figure 1f).

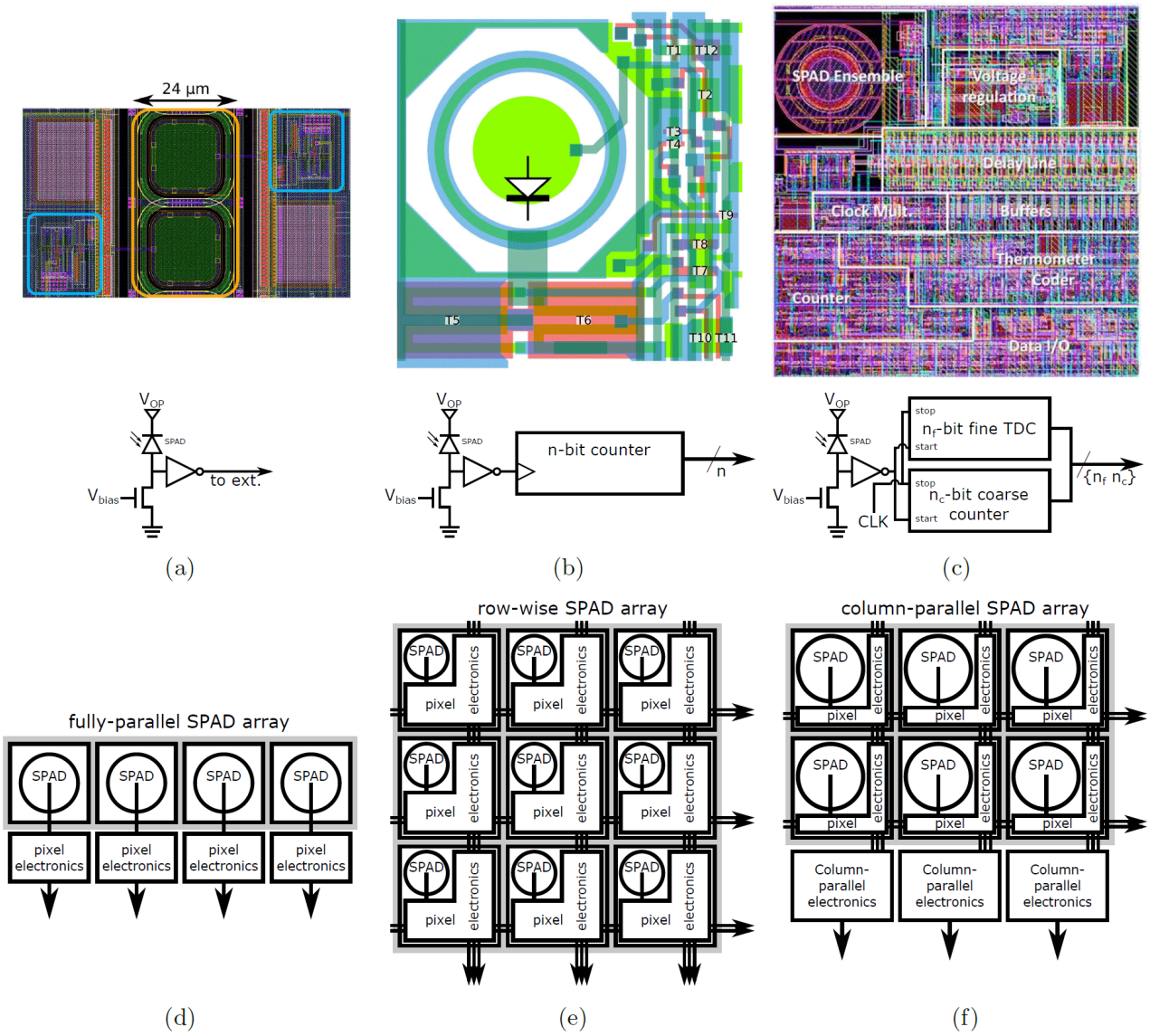

Figure 1. Different SPAD pixel designs: (a) a basic pixel and corresponding schematic[19],[25], (b) pixel with counter and corresponding schematic[9], (c) pixel with a complete TDC[6],[26],[27]. The different layouts illustrate the trade-off between active area and pixel complexity. SPAD array architectures: (d) line sensor with off-pixel electronics, (e) fully parallel pixels with in-pixel electronics, (f) column-parallel electronics with minimal in-pixel electronics.

Basic pixels (Figure 1a) offer the highest flexibility in terms of reconfigurable sensor electronics, as only the essential circuit is fixed and the remainder of the electronics, such as a photon counter or TDC, can be implemented at system run-time. However, as each pixel has a separate output, the total number of pixels is limited both by physical interconnects and by available system bandwidth. A possible remedy to reduce the interconnection complexity consists in reducing parallelism by sharing a common output line among multiple pixels, by means of multiplexing or serializing data streams, at the price of a significant increase in the frame read-out time. An alternative solution is to include fixed functionality in the pixel electronics, such as memory elements or counters (Figure 1b), and reading out data serially after a fixed integration time. This allows the implementation of larger arrays that can still measure in parallel[9],[28], at the price of a reduction in timing resolution and acquisition speed. Finally, time-stamping electronics such as TDCs can also be implemented in each pixel, or at column level, to increase the timing precision (Figure 1c). The former does

indeed significantly enhance the timing performance, but at the cost of requiring a significant amount of fixed electronics, not only limiting pixel fill factors, but also limiting the amount of reconfigurable options at system level.

To make a functional imager array, the independent pixel circuits described above need to be combined and operated together. An array of basic pixels, each with a separate output (Figure 1d), is quickly limited by the amount of required physical interconnects; even with current bonding, PCB and CMOS technologies, arrays exceeding several hundreds of pixels are hard to assemble. Therefore, larger arrays require some form of physical interconnect sharing by means of multiplexing or serializing data streams. Both pixels with built-in counters and TDCs are generally read row-wise (Figure 1e) to significantly reduce parallelism, bandwidth and thus interface connections. By placing shared electronics at the column level (Figure 1f), a serialization is implicitly included, as only a limited number of rows can be active at the same time. This architecture can be combined with event-driven readout, where the columns operate independently and use the available bandwidth efficiently, because they are only active when data is being processed. However, the amount of reconfigurability that can be applied in such a sensor is generally more limited, since a large part of the electronics has to be fixed to allow for the serialization.

3. LINOSPAD2 RECONFIGURABLE SINGLE-PHOTON IMAGER SYSTEM

The LinoSPAD2 sensor, containing a linear array of 512×1 SPAD pixels implemented in a 0.18 μm CMOS process, is shown in Figure 2a. Each pixel includes only the core circuitry required for SPAD operation, i.e. a passive quenching and recharge circuit, and an inverter for the conversion of the analog into a digital pulse. Each digital pixel output is connected to a separate pad, together with pads for quenching voltage, power and ground. The chip is bonded on a carrier PCB (Figure 2b), which in turn connects to a main board with the reconfigurable logic.

The main board hosts a Spartan6 XC6SLX150 FPGA from Xilinx with 150k logic elements packed in 20k slices, the largest amount of reconfigurable logic available in this class of FPGAs. A total of 498 user I/O pins are available, sufficient to interconnect 256 SPAD outputs, i.e. one half of the sensor, to a dedicated FPGA input. Two main boards are therefore needed to read out the full sensor, if required. Experience has indeed shown that most applications can make use of a restricted number of pixels, possibly selected in such a way as to avoid “hot” ones. In such cases, one readout board is perfectly sufficient. This board is the same as developed for the LinoSPAD system[19],[20],[25], whereas the firmware and software build on top of the previous versions. For interfacing the board with a computer, a Cypress FX3 USB3.0 transceiver chip is implemented, enabling to continuously stream up to 3 Gbps to the host PC. The key characteristics of the full LinoSPAD2 imager system are highlighted in Table 1.

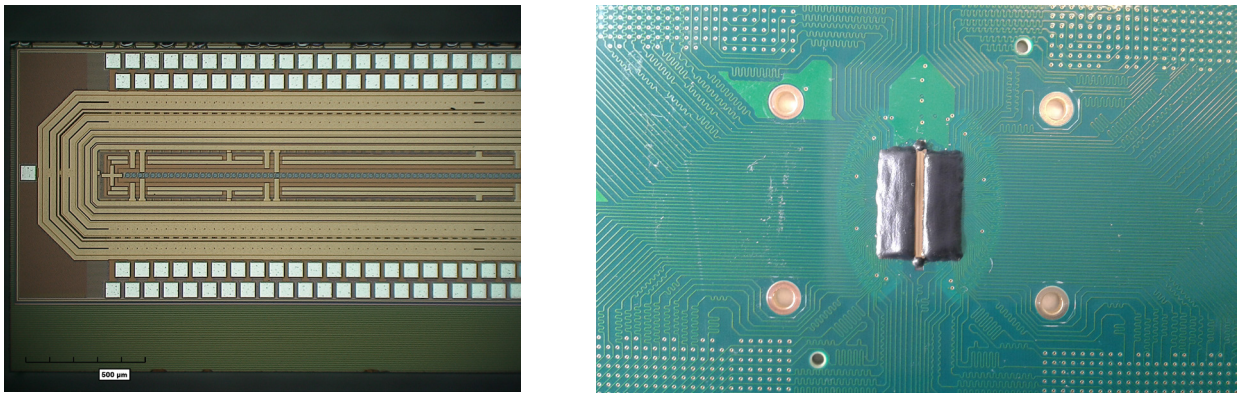

Figure 2. (a) Detail of LinoSPAD2, with top alignment cross integrated in the metal stack. Each pixel has a dedicated digital output. (b) Sensor bonded on a carrier PCB, which is then connected to a custom FPGA board.

Table 1. LinoSPAD2 main characteristics and specifications. IRF: Instrument Response Function; PDP: Photon Detection Probability.

Level	Specification	Value
Chip	Size [mm^2]	14.3×1.1
	Pixel array	512×1
	CMOS process [μm]	180 nm
	Breakdown / Excess bias voltage [V]	25.0 / up to 6.5 V
Pixel	Pitch [μm]	26.2
	Fill factor native / microlenses [%]	25.1 / 2.3×
	Peak PDP [%]	~50% @510 nm
	Dead time [ns]	20-50 ns
	Dark count rate @ 25 C [cps]	<100 @6 V
	Intrinsic jitter [ps FWHM]	50-60
FPGA (typical config.)	Logic utilization	71%
	Register utilization	43%
	Memory utilization	94%
System (typical config.)	Bandwidth [MB/s]	>200
	Number of TDCs	64 (4:1 sharing)
	TDC resolution [ps]	20
	TDC range [ms]	4.5
	TDC rate [MHz]	133
	IRF [ps FWHM]	135

The reconfigurable processing system enables various topologies to be implemented in quasi real-time, ranging from counters per pixel towards TDC arrays with on-the-fly histogram generation. In Figure 3, four different representative processing architectures are shown, namely basic photon counting, time-gated photon counting, shared photon time-stamping and shared photon time-stamping combined with histogram generation. Early implementations have been presented in [20]. For the first one (Figure 3b), 256 counters are implemented in the FPGA fabric, each connected to one SPAD output of one sensor half. This implementation is suitable for applications that require high throughput, at the cost of limited timing resolution. The 256 counters operate in parallel at a frequency of 100 MHz and employ a double-buffering memory scheme to ensure that no events are missed. The circuit thus provides accurate photon counts for integration times down to a few microseconds. To measure photon counts on shorter integration times, gates can be implemented, potentially with multiple counters (Figure 3c). Using programmable delay elements within FPGAs, it is possible to implement accurate time gates with a precision better than 100 picoseconds. For time correlated single-photon counting (TCSPC) applications, TDCs are required that can be implemented in the FPGA's carry chains[29],[30] (Figure 3d). As TDC blocks are significantly larger than simple counters in FPGAs, a single TDC per pixel implementation is not possible in a Spartan6; however, a TDC can be shared among multiple SPADs, only slightly impacting system performance. To further enhance system efficiency and limit the bandwidth with the host interface, a histogram generation engine can be coupled with the TDCs (Figure 3g). This unit enables on-the-fly generation of time-of-arrival histograms from raw TDC data.

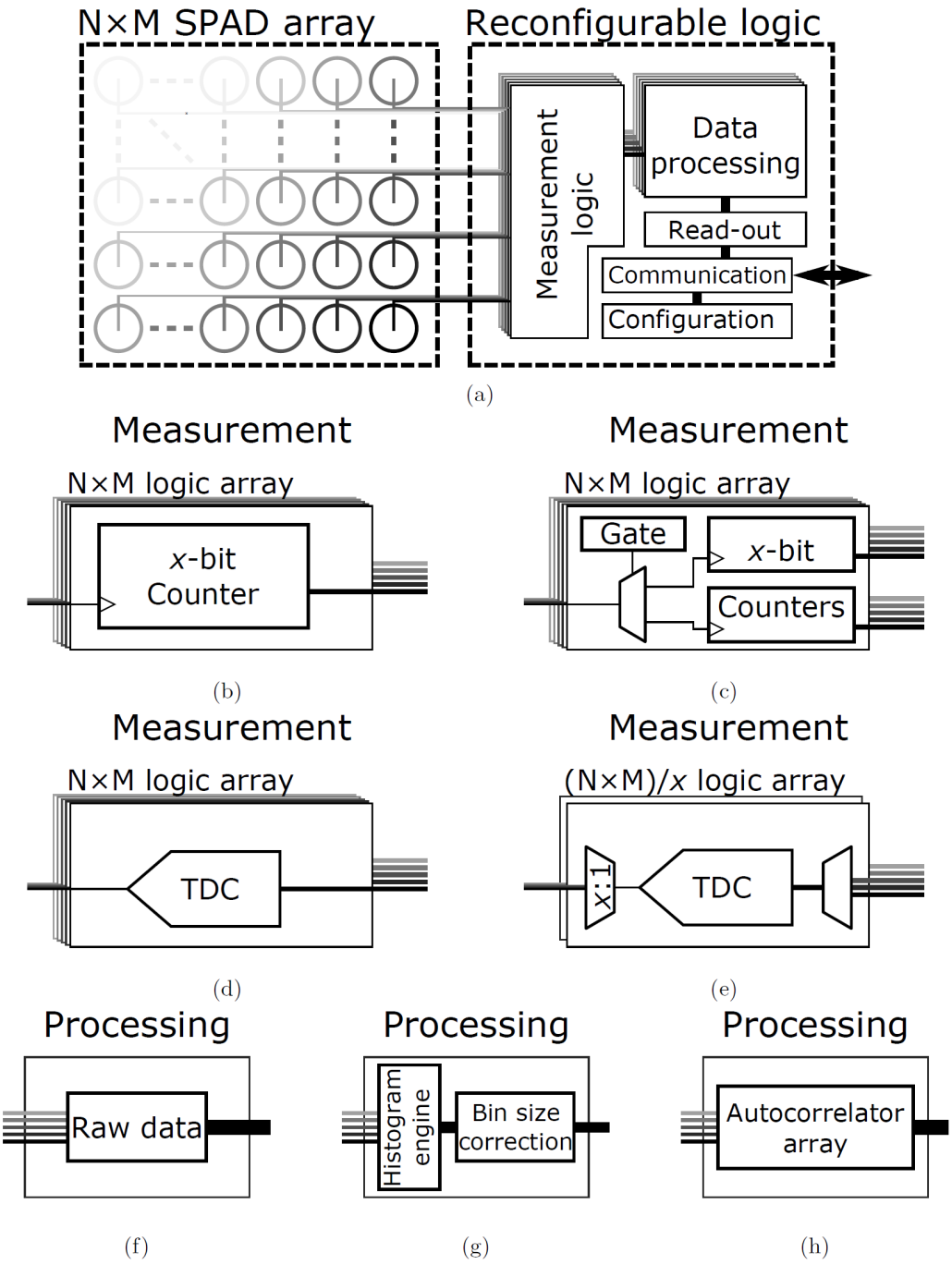

Figure 3. Various topologies for a general reconfigurable imaging sensor concept (a), as demonstrated with our LinoSPAD2 system. (b) A basic photon counting system with per pixel counters. (c) Time-gated photon counting, implemented with several counters and a picosecond delayable gate. (d) A time-correlated single-photon counting implementation with a single TDC per pixel (not achievable for all 256 SPADs in one sensor half). (e) A similar TDC array with sharing among 4 pixels to meet logic density constraints. (f-h) Different ways of acquiring the measured data, such as raw data read-out, histogramming the TDC outputs or applying a logic function, such as an autocorrelator. For all topologies, configuration data is sent through a daisy-chain to the modules while command signals are routed in parallel to every unit. The read-out occurs serially using a daisy-chain as well to route measurement data through processing modules to the serial output.

For our projects, we opted for a fixed firmware functionality tailored to the target application; however, FPGAs offer the possibility of dynamic or run-time reconfiguration to change circuit functionality on-the-fly. Run-time reconfiguration can be used to increase FPGA processing power by swapping in and out circuitry that is not used all the time. For further enhancements, several real-time post-processing steps can be considered for inclusion in the FPGA, such as mean time-of-arrival estimation, peak intensity extraction, lifetime estimation for FLIM or a 32×32 autocorrelator array (Figure 3h) for diffusion estimation[31].

The versatility of our reconfigurable single-photon camera is illustrated by its use in various applications realized in collaboration with research groups across the world. We highlight some of these applications in Table 2, together with the firmware requirements targeted to each of them. Most of the application results could be further improved in terms of photon collection efficiency and acquisition times by further optimizing the reconfigurable FPGA circuitry.

Table 2. Applications in which the LinoSPAD2 or LinoSPAD reconfigurable cameras have been employed together with specific firmware requirements. Firmware blocks (referring to Figure 3) that are used for the application are given in parenthesis. The reference column provides further information on the application and (when available) specific results obtained with the LinoSPAD2 or LinoSPAD cameras. N/A: not yet available (work in progress).

Application	Firmware requirements (Fig. 3 blocks)	Refs. (LinoSPAD)	Refs. (general)
Transient imaging, non-line-of-sight imaging, 3D scanning	High acquisition speed (d,f) / (d,e)	[32]	[33]
True (quantum) random number generation	High timing resolution (e, extractor)	[34]	[35],[36]
Heralded spectroscopy	Parallel time-stamping (synchronous) (d,f)	[21],[22]	[37]
Quantum astrometry/ spectroscopy	Data-driven time-stamping (asynchronous) (d,f)	N/A	[38],[39]
Compressive Raman	Parallel high speed counting (b)	[40],[41]	[42],[43]
Spectral dynamics in quantum emitters	Parallel time-stamping (synchronous) (d,f)	N/A	[44]
Drop flow time-resolved fluorescence analysis	Photon throughput (e,g)	N/A	[45],[46]

4. FULLY RECONFIGURABLE SPAD ARRAY ARCHITECTURES

The principle of a fully reconfigurable SPAD-based image sensor and its corresponding reuse of logic resources is an attractive way to repurpose a camera system for multiple applications. In practice, to the best of the authors' knowledge, no fully reconfigurable SPAD imaging system has been presented, to date. Although many systems are programmable to a certain extent, the logic on the sensor and in the pixels is mainly fixed. We believe that 3D CMOS architectures, which are now fast maturing, are the key technology enabler towards fully reconfigurable single-photon imaging and computing platforms. They allow to independently optimize photon absorption on one hand and information processing on the other hand, combined with the ability to process large data volumes generated by SPADs on a limited power budget, thanks to the proximity between data generation and processing. According to Moore's law, the transistor density roughly doubles every two years, and, since SPAD imagers employ relatively mature processes (e.g. 0.13 and 0.18 μm), they are about 15 years behind in logic density scaling. Thus, when stacking a SPAD top-tier with a modern logic process at the bottom, one can integrate roughly 100× more transistors/area for each pixel to process the SPAD data, e.g. over 10 T/μm^2 in a 28 nm CMOS technology node. An additional benefit is the capability of reducing pixel pitch and enhancing fill factor in modern SPAD sensors.

Indeed, only 3D integration achieves a high fill factor for the SPAD front-end in combination with enough reconfigurable logic and interconnects for each pixel. This solution is shown in Figure 4 left next to a possible single-layer solution (Figure 4b center).

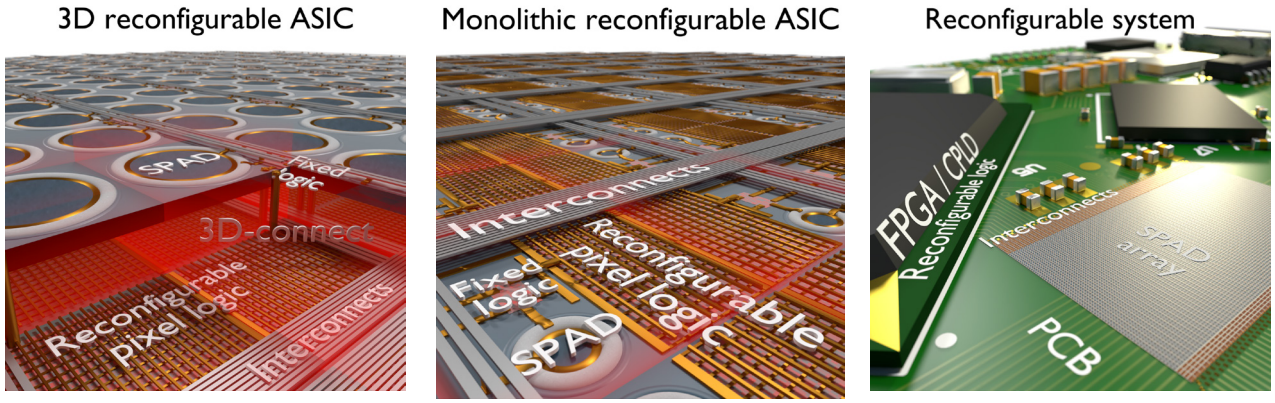

Figure 4. Different possibilities for the combination of the fixed and reconfigurable components of a SPAD-based imager. The main underlying assumption is that the only fixed electronics is represented by the SPAD circuit with quenching. The avalanche pulse from an impinging photon is immediately digitized and fed into the reconfigurable circuit. *Left*: 3D combination of an optimized, mature, low-noise process for the SPAD front-end with a high-density logic process for the reconfigurable back-end, which would offer the ultimate performance. *Center*: monolithic (i.e. single-layer) alternative. *Right*: development platform enabling proof-of-concept demonstrators, such as LinoSPAD2.

5. CONCLUSIONS

The LinoSPAD2 time-resolved camera combines a 512×1 SPAD array with an FPGA-based photon-counting and/or time-stamping platform. The sensor read-out is fully parallel, and its companion FPGA firmware can be reconfigured to different functionalities, such as photon counters, histogramming units, and time-to-digital converter arrays. The 26.2 µm SPADs feature a median DCR below 100 cps, intrinsic timing precision of 50 ps, and peak PDP of ~50%. The average IRF is 135 ps FHWM. Microlenses increase the sensitivity by 2.3×.

LinoSPAD2 embodies a proof-of-concept reconfigurable, high-sensitivity single-photon camera system capable of adapting the read-out and processing chains to match application specific requirements. As such, it represents a first step towards fully reconfigurable image sensor architectures based on natively digital single-photon avalanche diode arrays, combined with reconfigurable pixel and processing logic, as in FPGAs. Image sensor reconfigurability allows to adjust read-out and processing chains on the one hand, and spatial and temporal granularity on the other, to match application-specific requirements, thereby overcoming recurring limitations in bandwidth and power by processing photon information closer to its origin. Fully reconfigurable SPAD-based cameras would ultimately be built using 3D-stacking technologies, whereby SPADs would be employed as photon-to-digital conversion elements, stacked onto CMOS-based, reconfigurable circuitry in an FPGA-like bottom tier.

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