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Fieback, Moritz; Münch, Christopher; Gebregiorgis, Anteneh; Cardoso Medeiros, Guilherme; Taouil, Mottaqiallah; Hamdioui, Said; Tahoori, Mehdi

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Moritz Fieback[1], Christopher Münch[2], Anteneh Gebregiorgis[1],
Guilherme Cardoso Medeiros[1], Mottaqiallah Taouil[1], Said Hamdioui[1], Mehdi Tahoori[2]
[1] EEMCS, Delft University of Technology, Delft, The Netherlands
[2] Department of Computer Science, Karlsruhe Institute of Technology (KIT), Karlsruhe, Germany
Email: m.c.r.fieback@tudelft.nl, christopher.muench@kit.edu, s.hamdioui@tudelft.nl, mehdi.tahoori@kit.edu

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***Abstract*—Emerging non-volatile resistive memories like Spin-Transfer Torque Magnetic Random Access Memory (STT-MRAM) and Resistive RAM (RRAM) are in the focus of today's research. They offer promising alternative computing architectures such as computation-in-memory (CiM) to reduce the transfer overhead between CPU and memory, usually referred to as the memory wall, which is present in all von Neumann architectures. A multitude of architectures with CiM capabilities are based on these devices, due to their inherent resistive behavior and thus their ability to perform calculation directly within the memory, and thus without invoking the CPU at all. However, emerging memories are sensitive to Process, Voltage and Temperature (PVT) variations. This sensitivity has an even larger impact on CiM architectures. In this paper, we analyze and compare the impact of PVT variations on STT-MRAM and RRAM-based CiM architectures. We perform a sensitivity analysis to identify which parts of the CiM structure are most susceptible to PVT variations, for each technology. Based on these analyses, we recommend that STT-MRAM is used in high-performance CiM, while RRAM is used for edge CiM.**

***Index Terms*—Computation-in-Memory (CiM), PVT, emerging memories, STT-MRAM, RRAM, reliability**

I. Introduction

Current computing architectures are reaching performance limits caused by limited memory bandwidth, called the memory wall [1, 2]. Hence, new computing architectures are required that alleviate this bottleneck. One of these promising architectures is *computation-in-memory* (CiM) based on emerging memory technologies [3–5]. Here, memristive devices such as *spin-transfer torque magnetic random-access memory* (STT-MRAM) and *resistive random access memory* (RRAM or ReRAM) are used to perform compute operations directly *in the memory itself*, thereby mitigating the bandwidth issue completely. These memory technologies are used because they are non-volatile, faster, more energy-efficient, and can be fabricated denser than traditional memory technologies such as Flash and DRAM [6, 7]. In a CiM architecture, the analog properties of the memristive devices are used to perform the compute operations. For example, analog comparison of two bit cells can be used to perform logic operations [3], or vector-matrix multiplications can be performed in one cycle by storing the matrix as a resistance [5]. A drawback of emerging memory devices is that they suffer from *process, voltage and temperature* (PVT) variations that affect the resistance of the devices and thereby the performance of the CiM scheme. In order to design CiM architectures that benefit from these emerging technologies, the effects of PVT variations need to be well understood.

Resistive variations in STT-MRAM and RRAM devices have been studied before [6, 8–10]. In STT-MRAM, sources of variation include the stochastic switching of the device and the high resistance variation of the stack due to variations in the device dimensions [11]. This has a direct impact on its behavior when used for a CiM capable memory. Therefore, mitigations are needed which introduce an additional overhead in form of, e.g., additional error correction, to build a CiM capable memory [12]. Variations in RRAM devices are attributed to the stochastic growth and nature of its conductive filament [8]; higher temperatures and higher write currents decrease the variability [8, 9]. It was shown that the variations in the RRAM device have a strong impact on the CiM performance [13]. It is clear that the performance of a CiM architecture is strongly affected by variations. However, it remains unclear which device technology, i.e., STT-MRAM or RRAM, is better to use when designing a reliable CiM architecture, and which mitigation techniques are best suited for each technology.

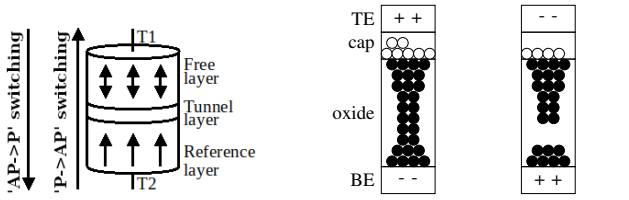
In this work, we analyze the impact of PVT variations on the compute performance of STT-MRAM and RRAM logic CiM architectures. This analysis allows CiM designers to properly understand the trade-offs that are involved when designing such architectures. In short, the contributions of this work are:

- Complete analysis of STT-MRAM and RRAM PVT variations on the performance of logic CiM.
- Sensitivity analysis to identify the parts that are most susceptible to PVT variations for these technologies.
- Design and mitigation recommendations to use STT-MRAM for high-performance CiM.
- Design and mitigation recommendations to use RRAM for edge CiM.

This paper is structured as follows. Section II presents the technology background of STT-MRAM and RRAM. Section III introduces CiM based on these technologies. Section IV describes the experimental set-up. Section V presents the results. Section VI analyzes the design trade-offs for CiM based on emerging memories. Finally, Section VII concludes this paper.

II. Background

This section introduces the STT-MRAM and RRAM.



(a) MTJ (b) RRAM SET (c) RRAM RESET

Fig. 1: MTJ stack and conductive filament in bipolar RRAM.

A. STT-MRAM

The main storage device of STT-MRAMs is the *Magnetic Tunnel Junction* (MTJ) [14, 15] as shown in Fig. 1a. It is a stack of two ferromagnetic layers, which are separated by a thin tunnel layer. The *Reference Layer* (RL) is manufactured with a fixed magnetic orientation, whereas the magnetic orientation of the *Free Layer* (FL) can be changed. The FL has two stable magnetic states, one in the same magnetic orientation as the RL, the *Parallel* (P) state and one in the opposite magnetic direction, the *Anti-Parallel* (AP) state, corresponding to *Low* and *High Resistance States* (LRS and HRS), respectively. By applying a *write current* (I_w) above the device-dependent *critical write current* (I_c) the magnetic orientation of the FL can be switched either to P or AP, depending on the direction of I_w. The resistance of the MTJ can be evaluated and treated as binary information, by Using a small *read current* (I_{read}) $I_{read} << I_c$. Process variation (PV) can lead to *device-to-device* (D2D) variations in the resistive behavior which are more severe in the AP state than the P-state of a device and varying I_c, thus impacting the write operation. MTJs are affected by temperature, both in their read an write behavior. The resistance of an MTJ at higher temperatures is slightly reduced for P-state MTJs and significantly reduced for AP-state MTJs. Writing the MTJ becomes easier with higher temperatures, thus lower currents or less write time are needed to switch the state [16].

B. RRAM

An RRAM device is a device that can change its resistance by applying voltages to it. Fig. 1 schematically shows an RRAM device that is a stack consisting of a *bottom electrode* (BE), a metallic oxide (oxide), a capping layer (cap), and a *top electrode* (TE), also called an OxRAM. When a positive voltage is applied between the TE and the BE that is higher than V_{SET}, some of the bonds between the oxygen and metal ions break [6, 7]. Then, the oxygen ions are attracted to the capping layer and leave behind a conducting chain of vacancies that is called a *conductive filament* (CF), as shown in Fig. 1b. This LRS is called the SET state or logic '0'. When a negative voltage is applied that is lower than V_{RESET}, some of the oxygen ions move back into the oxide and rupture the CF, leaving a gap in the CF, as shown in Fig. 1c. This HRS is called the RESET state or logic '1'. Note that, in this paper, '0' and '1' are defined this way to align with the STT-MRAM convention. The current through a RRAM device is strongly influenced by the temperature.

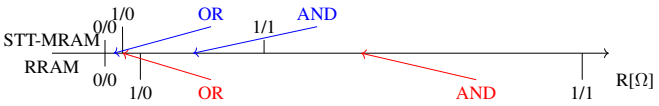


Fig. 2: Resistive behavior for multiple active cells in different HRS/LRS state combination and the needed reference resistance for the according binary operations. Relative to 0/0 state for the individual technology.

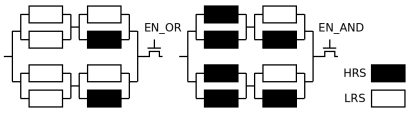


Fig. 3: Generic compound references based on resistive memory cells for CiM-OR (left) and CiM-AND (right) operations.

Higher temperatures decrease the switching thresholds, thus speeding up the switching process [9]. Furthermore, higher temperatures increase the conductivity of the device, which increases the self-heating of the device [17].

The growth and dissolution of the CF is a stochastic process [8]. Hence, the shape of the CF will change every time it forms or dissolves, leading to variations in the device resistance. PV during the manufacturing of the RRAM devices lead to D2D variations between multiple RRAM devices, while variations per SET or RESET cycle lead to *cycle-to-cycle* (C2C) variations.

III. CiM Based on Emerging Memories

First, we introduce the concept of CiM. Second, we illustrate one specific CiM architecture.

A. CiM Architectures and Challenges

CiM architectures perform computations in the memory chip directly, thereby alleviating the need to move data to and from the processor. CiM architectures are classified based on the location where the result of the computation is produced, i.e., in the memory array (CiM-A) or in the peripheral circuits (CiM-P) [18]. Some examples of CiM-A architectures are Snider logic [19] and Majority-oriented logic [20]. Some examples of CiM-P are Scouting logic [3] and Boolean Matrix Multiplication on memristive crossbars [5]. CiM-A stores its results in the array itself, which introduces a high write load on the cells that limits the lifetime of the circuit. In contrast, CiM-P uses only read operations to perform computations and thus does not suffer from this problem. For this reason, in this work, we study Scouting logic.

For a CiM circuit, the most important performance criteria are the error rate, the energy consumption, and the sensing delay. All these factors are affected by variations in the resistance of the memory cell. Hence, a CiM circuit can only be made reliable when the effects of the resistance variations on the chosen cell technology are understood.

B. CiM-P Scouting Logic Example

CiM-P scouting logic senses the equivalent resistance of two memory cells and compares the resulting current to a reference current using a *sense amplifier* (SA) [3]. By changing this reference, different logic operations can be performed. Fig. 2 shows how an AND and OR operation can be implemented

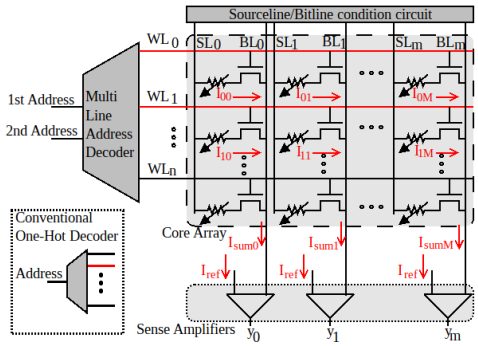


Fig. 4: Generic Scouting Architecture using a core array with resistive memory cells, a multi-word line address decoder to select the CiM operands, a Source line / Bit line condition circuit to write the cells and set the proper states for performing read/CiM operations with the SAs.

for both STT-MRAM and RRAM by setting the reference to a *specific* resistance. The difference between the STT-MRAM states is smaller than the difference between the RRAM states, due to the intrinsic lower device resistance.

There are multiple ways to generate the reference. On one hand, they can be implemented with large conventional CMOS process-based resistors like the polysilicon resistor. On the other hand, it is possible to create a compound reference [21] with a mix of multiple devices of a specific memristive technology to generate the required resistance value for a specific CiM operation. As shown in Fig. 2, in case of an OR operation, the reference resistance is placed between the equivalent resistance of two cells that store a '0', and two cells that store a '0' and a '1'. This reference resistance is realized by connecting a total of eight devices as shown in Fig. 3 on the left side, in addition with an access transistor to select the operation during the sense phase. Likewise, realizing the AND operation places the reference resistance between the equivalent resistance of two cells that store a '0' and '1', and two cells that store a '1', as shown in Fig. 3 on the right side.

IV. Experimental Set-Up

In this section, we introduce the evaluated architecture and its parameters. Then, we describe the performed experiments.

A. CiM Array Architecture

Fig. 4 shows how a conventional memory can be modified to perform Scouting logic [3]. The main adjustments are at the address decoder, which needs to address and enable multiple word lines concurrently and select the reference resistances reflecting the different operations. For our experiments, we assumed a two-address concurrent decoding, allowing for two-operand operations, and a conventional pre-charge SA. The reference resistances for the binary AND and OR operations are generated using the compound reference scheme as described in Section III-B.

B. Performed Experiments

To study the impact of resistive variations on the CiM performance, we perform all possible 2-bit AND and OR operations, with varying operating conditions. We vary the *ambient temperature* (T) and the *supply voltage* (V_{DD}). Based on the nominal corner at 300 K and V_{DD} of 1.5 V, we investigate the fixed voltage corners with varying temperature (273 K and 358 K) and the fixed temperature corners with varying V_{DD} (1.4 V and 1.6 V). For every combination, we perform a sensitivity analysis to study the influence of six different component PV combinations in the circuit: cell transistor only (CT), cell memristive device (CM), cell transistor and memristive device (CTM), reference transistor (RT), reference memristive devices (RM), and reference transistor and memristive device (RTM). For every temperature, voltage and component variation combination, we perform 1000 Monte Carlo (MC) simulations. For the transistor variations, we use the variation models included in the TSMC 40nm LP process development kit, while for STT-MRAM and RRAM device variations, we set up the models according to [22] and [17], respectively. We study D2D variations for both devices and for RRAM we include C2C variations. We initialize the cells to the opposite value of the desired value to include the D2D variation. Subsequently, we write the correct value to the cell before we perform the logic operation to include the C2C variation. To illustrate, if the desired operation is 1 AND 1, we initialize the cells to '0', then write a '1' to them and perform the CiM operation.

TABLE I: Parameters and simulation set-up.

Parameter	Value
Nominal VDD	1.5V
Nominal Temperature	300 K
CMOS library	TSMC 40nm low-power
MTJ model	[22]
MTJ radius	20 nm
Free/Oxide layer thickness	1.3/1.48 nm
RA and TMR @ 0V	7.5 $\Omega\mu m^2$ and 150%
AP'/'P' resistance	15 kΩ/6 kΩ
STT-MRAM access transistor L/W	40 nm/0.8 µm
RRAM Model settings	Same as in [17]
RRAM stack	Pt/HfO2 (3 nm)/TiOx (13 nm)/Pt
LRS/HRS resistance	2 kΩ/40-100kΩ
RRAM access transistor L/W	270 nm/3.2 µm

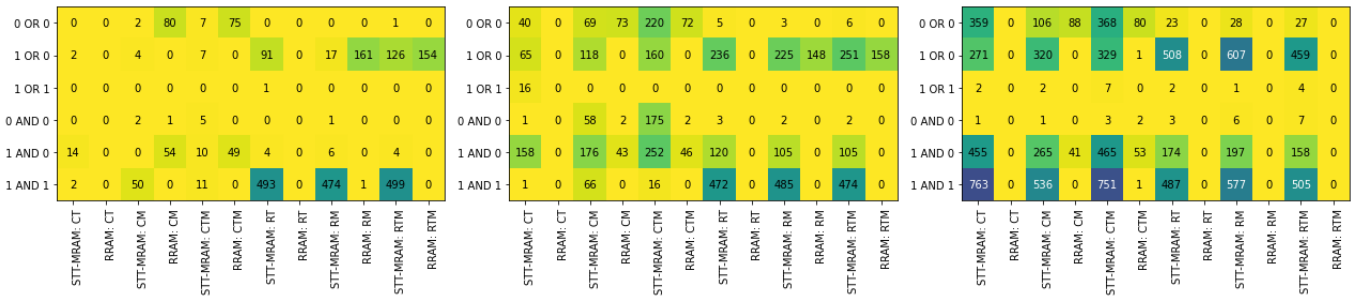
For every MC iteration, we record three metrics: 1) Number of operation errors (number of operations that fail to produce the correct answer) 2) Energy consumption (energy consumption of the complete circuit during the read operation) and 3) Sensing delay (the delay between the start of the sensing operation and the output crossing $V_{\mathrm{DD}}/2$).

V. Results

This section presents the result of the PVT analysis. First, we present the results for the nominal case. Second, we present the results for the temperature variations. Third, we present the results for the voltage variations.

A. Nominal Case: No Voltage/Temperature Variations

1) Number of Operation Errors: Fig. 5a lists the number of operation errors for the nominal case, i.e., $T = 300\,\mathrm{K}$ and $V_{\mathrm{DD}} = 1.5\,\mathrm{V}$. The x-axis lists the cell technology with the varied component combination, e.g., *STT-MRAM: CTM* denotes that the cell technology is STT-MRAM and the components that are varied are the cell transistor and the cell STT-MRAM device. The y-axis lists the performed operations, e.g., 1 OR 0. We observe the following:



(a) $T = 300\,\mathrm{K}$, $V_{\mathrm{DD}} = 1.5\,\mathrm{V}$, nominal (b) $T = 273\,\mathrm{K}$, $V_{\mathrm{DD}} = 1.5\,\mathrm{V}$ (c) $T = 358\,\mathrm{K}$, $V_{\mathrm{DD}} = 1.5\,\mathrm{V}$

Fig. 5: Number of operation errors for varying temperature. Each data point refers to 1000 Monte Carlo simulations points.

TABLE II: Mean CiM Energy Consumption [pJ]

	STT-MRAM					RRAM				
	A	B	B	C	C	A	B	B	C	C
T [K]	300	273	358	300	300	300	273	358	300	300
V_{DD} [V]	1.5	1.5	1.5	1.4	1.6	1.5	1.5	1.5	1.4	1.6
0 OR 0	2.47	2.53	2.46	2.94	2.97	7.41	7.29	7.94	6.15	8.82
1 OR 0	2.38	2.41	2.37	1.85	2.86	7.19	6.95	7.76	5.88	8.56
1 OR 1	2.09	2.07	2.12	1.70	2.52	6.40	6.16	6.97	5.22	7.72
0 AND 0	2.16	2.31	2.19	1.76	2.59	6.42	6.28	7.05	5.14	7.73
1 AND 0	2.16	2.29	2.19	1.75	2.59	6.27	6.03	6.96	5.10	7.58
1 AND 1	2.10	2.09	2.13	1.70	2.54	6.08	5.81	6.69	4.97	7.39

TABLE III: Mean CiM Sensing Delay [ps]

	STT-MRAM					RRAM				
	A	B	B	C	C	A	B	B	C	C
T [K]	300	273	358	300	300	300	273	358	300	300
V_{DD} [V]	1.5	1.5	1.5	1.4	1.6	1.5	1.5	1.5	1.4	1.6
0 OR 0	516	510	532	592	467	708	664	746	784	651
1 OR 0	512	501	525	586	461	737	709	777	833	672
1 OR 1	503	496	516	575	454	606	585	628	681	563
0 AND 0	515	506	527	588	457	620	581	645	676	574
1 AND 0	519	510	531	592	465	627	607	650	684	580
1 AND 1	518	505	529	596	465	638	619	661	700	592

- STT-MRAM is more susceptible to PV than RRAM.
- More errors are observed when the equivalent cell resistance is closer to the reference resistance.
- STT-MRAM is susceptible to AND operation failures.
- There are no RRAM access transistor faults.

They will be discussed in detail below. The two device technologies differ in their behavior for cell and for reference variation in the nominal design corner, as shown in Fig. 5a. We can see that STT-MRAM is more susceptible to PV than RRAM, as the total number of operation errors is higher for the former technology. This can be explained by the fact that the resistance difference between the different STT-MRAM states is smaller than for RRAM, as shown Fig. 2, i.e., the margin between the equivalent cell resistance and the reference resistance is smaller. To illustrate, the equivalent resistance of two cells storing '1' and '0' is closer to the OR reference resistance than two cells storing '1' and '1'. Hence, variations will cause more operation errors in STT-MRAM than in RRAM. Because of this smaller resistance window, STT-MRAM is very susceptible to AND operation faults. Finally, the figure shows that there are no RRAM access transistor faults. This is caused by the fact that this transistor is relatively large, and thus PV here has a relatively small effect on the performance [23]. As the STT-MRAM transistor sizes are much smaller, variation in them has a noticeable effect on the CiM functionality.

2) Energy Consumption: Table II lists the mean energy consumption results in columns A. The table shows that the lower the equivalent and reference resistance is, the more energy is consumed. This can be explained by the fact that lower resistance will discharge the nodes of the SA further before the difference is sensed than higher resistances. Furthermore, the table shows the energy consumption is 3X lower for STT-MRAM cells than for RRAM cells. This can be explained by the fact that the RRAM peripheral circuits need to be stronger and thus larger in order to minimize the voltage drop when performing write operations.

3) Sensing Delay: Table III lists the mean sensing delay results in columns A. Due to space constraints, we again chose to only list the sensing delay per operation, as there was more variation here than per component combination. The table shows that STT-MRAM cells allow for about 21% faster sensing in average. This is due to the smaller access transistor that introduces less capacitance in the circuit. Further, the table shows that the sensing delay is the shortest when the equivalent cell and reference resistance are farther from each other. This can be explained by the larger voltage difference that will develop during the sensing phase, which will lead to a faster sensing operation.

B. Temperature Dependence

1) Number of Operation Errors: The number of operation errors for the three studied temperatures is shown in Fig. 5. From the figures the following observations can be made.

- STT-MRAM is strongly affected by temperature.
- Temperature has a limited effect on RRAM cells.

These will be discussed next. STT-MRAM cells suffer more from temperature changes than RRAM. This can be attributed to the fact that for elevated temperatures, the AP and P state move closer to each other [24], while for lower temperature, the transistor will conduct less current due to its increased threshold voltage. This moves the equivalent cell and reference resistances closer to each other. Both these factors reduce the resistance window between the equivalent and reference resistances and lead to operation errors. In addition, HRS and LRS of STT-MRAM cells are affected by temperature variation differently, the LRS is nearly unaffected by temperature, whereas the HRS resistance is reduced with an increasing temperature. This results in an asymmetric change of resistance for memory and reference cells, and thus increased

error rates for non-nominal scenarios. As the AND reference is composed of more HRS devices, STT-MRAM is more prone to temperature variations for the AND operation than for the OR operation. The reduced number of errors in RRAM cells for higher temperatures can be attributed to the fact that with higher temperatures there is less resistance variation for RRAM cells [9]. Hence, the impact of these temperature variations is marginal for RRAM cells.

2) Energy Consumption: The results on the energy consumption are shown in Table II in columns A and B. The table shows that, due to the change in transistor threshold voltage, less energy is consumed when the temperature decreases, and more energy is consumed when it increases. Furthermore, the same trends from the nominal case are seen at these two temperature corners as well.

3) Sensing Delay: The results on the sensing delay are shown in Table III in columns A and B. For both technologies lower temperatures decrease the sensing delay, as the SA is able to operate faster. Further, the operation dependability seen in the nominal case still applies.

C. Voltage Dependence

1) Number of Operation Errors: The number of operation errors for varying V_{DD} is shown in Fig. 6. The following observations can be made:

- Lower voltages lead to more operation errors.
- Higher voltages lead to STT-MRAM operation errors.

This will be explained next. Lower voltages introduce more operation errors, as the transistor current is reduced. This increases the equivalent resistance of the cells and thus lowers the difference with the reference resistance, leading to operation errors. For RRAM, lowering V_{DD} also decreases the voltage over the RRAM device, which increases its switching time. This is more severe for the RESET process, i.e., writing '1', and thus more errors will occur when an operation contains a '1'. Note that the difference between the OR reference resistance and the equivalent resistance of two cells that store '1' is large enough so that no errors occur for this operation. Higher voltages do not affect the RRAM performance, as there is sufficient voltage to reliably write the cells. However, a lower voltage has a comparably significant impact on the performance of STT-MRAM due to a significant increase in write errors. Moreover, increasing the voltage also increases the sensibility of the SA, therefore increasing the error rate in case the reference is close to the sensed cells, thus increasing the probability of a sense failure.

2) Energy Consumption: The effects of voltage variations on the energy consumption are listed in Table II in columns A and C. As expected, it decreases when the voltage decreases, and it increases when the voltage increases. Furthermore, the operation dependability is similar to the nominal case. These observations hold for both technologies.

3) Sensing Delay: The effects of voltage variations on the sensing delay are listed in Table III in columns A and C. Lower voltages will result in a slower SA, and thus increase the sensing delay, while higher voltages will speed up the sensing and thus reduce the sensing delay. Furthermore, the operation dependability is similar to the nominal case. The observations above hold for both technologies.

VI. Design Considerations and Improvements

In this section, first we present design considerations when developing CiM based on emerging memory technologies. Second, we propose improvements to make emerging memory-based CiM more resilient against PVT variations.

A. Design Considerations

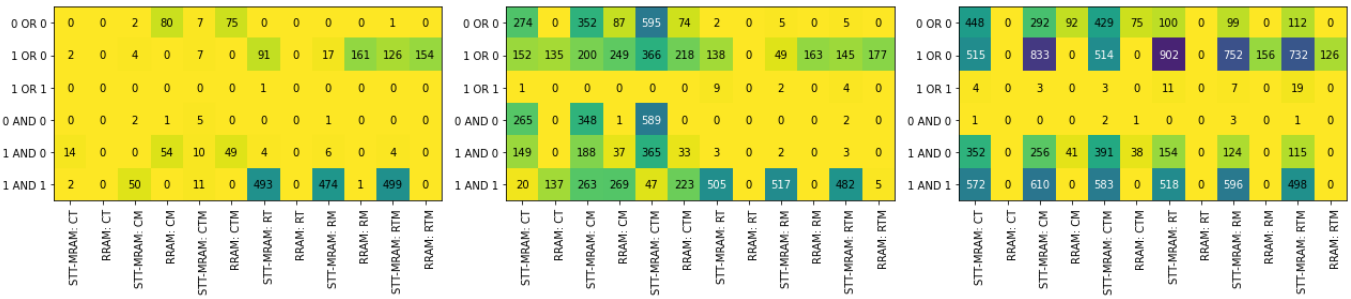
This section uses the results to identify and compare the strengths and weaknesses of every technology. We define five qualities that a CiM designer may aim for based on our results. These are the process sensitivity (ability to withstand PV), the temperature sensitivity (ability to withstand temperature changes), the voltage sensitivity (ability to withstand voltage changes), the energy consumption (energy consumed when performing a CiM operation) and the sensing delay (how fast the SA produces a result). Furthermore, there are four other important qualities for CiM that we consider: Cell area, Cell write energy, Write delay, Multilevel storage.

Fig. 7 shows how STT-MRAM and RRAM compare on these qualities, relative to each other, based on the results from the previous section and the data in Table I. In addition, we evaluated the average write energy and time which was 2.6pJ for the 10ns write operation in STT-MRAM and $41\,\mu$J for the 1ms write operation in RRAM. The more outward a point is on this graph, the better the given technology performs on this quality. The figure shows that STT-MRAM is more sensitive to PVT variations than RRAM. Hence, if it is known that the CiM architecture will be used in noisy or temperature varying environments, it is better to implement the CiM architecture using RRAM cells. However, STT-MRAM performs better in terms of area, sensing delay, and energy consumption. Therefore, if larger memories are required on which many operations need to be performed fast, it is better to use STT-MRAM. Based on these observations for a CiM-P architecture, we suggest that STT-MRAM cells are better suited to be used in CiM architectures that implement large database structures in a controlled environment, e.g., in large data centers, while RRAM cells are better suited in smaller circuits that are more prone to PVT variations, e.g., edge computing. The observations also apply for other CiM-P architectures, as these also use STT-MRAM or RRAM cells to generate the reference [18]. For CiM-A, the analysis should be focused on write reliability, as this is the operation that performs the logic.

B. Improvement

This section discusses improvements to reduce the impact of PVT variations on the CiM performance.

- Increase the LRS/HRS ratio: Increasing this ratio increases the difference between the two references and the closest equivalent cell resistances. This can be implemented in RRAM by changing the cell drivers that are used for writing. For STT-MRAM, the device stack can be tailored



(a) $T = 300\,\mathrm{K}$, $V_{\mathrm{DD}} = 1.5\,\mathrm{V}$, nominal (b) $T = 300\,\mathrm{K}$, $V_{\mathrm{DD}} = 1.4\,\mathrm{V}$ (c) $T = 300\,\mathrm{K}$, $V_{\mathrm{DD}} = 1.6\,\mathrm{V}$

Fig. 6: Number of operation errors for varying V_{DD}. Each data point refers to 1000 Monte Carlo simulations points.

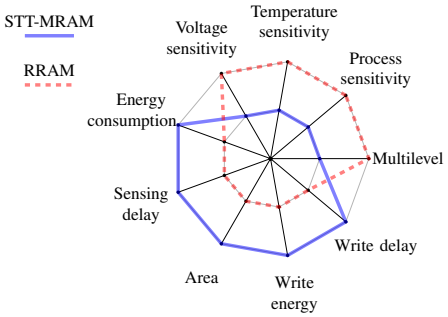


Fig. 7: Quality comparison between. More outward is better.

specifically so that the difference between HRS and LRS becomes larger, thus increasing the HRS/LRS ratio [25].

- Change the operation: The number of operation errors depends strongly on the difference between the reference and the equivalent cell resistance. Hence, many errors can be mitigated if the operation with the largest difference is favored. In this work, this means that the AND operations should be preferred for RRAM, while for STT-MRAM OR operations should be preferred. Additionally, changing the operand encoding to HRS/LRS=0/1 allows reusing the initial OR operation to reliably implement the AND operation.
- Modify cell structure: In [13], the authors propose to add a second access transistor, word and bit line, to increase the difference between the equivalent cell and reference resistance. This can be effective, but decreases the density of the CiM capable memory, which increases its cost.

VII. Conclusion

In this work, we have analyzed the effects of PVT variations on the performance of CiM architectures that are based on either STT-MRAM or RRAM cells. We observed that in general STT-MRAM cells are more susceptible to PVT than RRAM cells. Therefore, RRAM is preferred when the environment is noisy or the temperature changes frequently. However, CiM based on STT-MRAM cells is faster, can be fabricated denser and is generally more energy efficient. Therefore, STT-MRAM is preferred in controlled environments where more memory and higher speeds are desired.

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