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Ganeshpure, Dhanashree Ashok; Soeiro, Thiago Batista; Gagic, Mladen; Niasar, Mohamad Ghaffarian; Bauer, Pavol; Vaessen, Peter

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Demonstration of Scalable Series-Connected Submodule of Modular-Multilevel-Converter-Based Arbitrary Wave Shape Generator Used for High-Voltage Testing From Off-the-Shelf Component

DHANASHREE ASHOK GANESHPURE [1] (Student Member, IEEE), THIAGO BATISTA SOEIRO [2] (Senior Member, IEEE), MLADEN GAGIC [1], MOHAMAD GHAFFARIAN NIASAR [1], PAVOL BAUER [1] (Senior Member, IEEE), AND PETER VAESSEN [1,3] (Member, IEEE)

[1]Delft University of Technology, 2628 CD Delft, The Netherlands
[2]University of Twente, 7522 NB Enschede, The Netherlands
[3]KEMA Laboratories, 6812 DE Arnhem, The Netherlands

CORRESPONDING AUTHOR: DHANASHREE ASHOK GANESHPURE (e-mail: d.a.ganeshpure@tudelft.nl)

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ABSTRACT To test high-voltage (HV) equipment with increasingly complex transients obtained from various power system studies, this article demonstrates a hardware implementation of a medium-voltage (MV) submodule (SM) to be used in a modular multilevel converter (MMC)-based HV arbitrary wave shape generator (AWG). The MV SM is scalable with its own onboard auxiliary power supply (APS), and it is constructed by connecting three full-bridge SMs in series from the commercially available component. The designed MV SM can be operated for a wide voltage range of 0.8–2.7 kV to incorporate different test objects ranging from HV insulation material to MV equipment and generate a wide output range of 0.12–1.2 kV. Considering the hardware nonidealities in the APS, gate driver, and switches, the series operation of three SMs is ensured using an arm energy controller. Based on the current-based model of APS, SM capacitance design criteria are updated for variable-frequency output waveform, and the minimum dc-link voltage is calculated for the proper start-up of this scalable MMC module. Apart from the variable voltage per SM, the HV AWG application poses different conditions, such as a low value of SM capacitance value and the HV dc sources with a current rating of a few tens of milliamperes. Hence, this article proposes exclusive design guidelines for the proper start-up, steady-state, and shutdown operation of the MMC-based AWG. In addition, this article dives deeper analytically into the soft start-up algorithm to understand its working principle and to design the average charging current within the limit for any number of SMs of the arm. In the end, their performance is showcased with a single MV SM per arm, operating at a different voltage (0.8–2.7 kV) and frequency levels (1–600 Hz) and generating different wave shapes, such as triangular, sinusoidal with different harmonics, and pulse waveforms. In addition, the fault ride-through capability is verified for the MMC-based HV AWG.

INDEX TERMS Arbitrary wave shape generator, high-voltage (HV) testing, modular multilevel converter (MMC), off-the-shelf component, scalable medium-voltage (MV) submodule design.

I. INTRODUCTION

Medium-voltage (MV) and high-voltage (HV) equipment in the electrical power system, such as switchgear, cables, and transformers, are experiencing new electrical stresses due to the rise of distribution generation systems and grid

integration of large amounts of renewable energy interfaced via power electronic converters [1], [2]. For this reason, HV equipment must more often endure the higher dV/dt stresses effect of solid-state switching, which can degrade the reliability of the electrical power system by weakening the dielectric material of the electric power grid assets [3], [4]. In addition, conventional HV test sources, i.e., transformers (cascaded and resonant), impulse generators, and rectifier circuits, face many limitations. First, they do not have the flexibility to generate different wave shapes. Second, HV test sources have limited current capability in the range of a few milliamperes. Finally, building a customized test setup is time consuming when multiple HV test sources are used to generate complex waveforms. It has been shown that a modular multilevel converter (MMC) is a promising solution to realize an HV arbitrary wave shape generator (AWG) [5] to address the abovementioned problems. Fig. 1 shows the schematic of an MMC-based HV AWG. The advantages of an MMC as an AWG have been studied analytically, with MATLAB/Simulink simulations, and with a scaled-down experimental setup with 12 submodules (SMs) [5]. This article demonstrates an MV SM design, which is scalable and can be realized from commercially available components.

Though MMC is a vastly discussed converter topology in power electronics, its SM hardware design is rarely discussed in the literature. Among the few lab-scaled MV MMC demonstrators, ABB has designed an MV MMC with hot swap capability at 3.4-kV dc-link voltage and 0.55-MW output with 12 SMs and with a wireless auxiliary power supply (APS) [6]. Here, the main focus of the demonstrator was its hot swap capability, and all the design aspects, such as APS, cooling system, and communication system, are adapted accordingly. Another MV MMC demonstrator with 10-kV dc-link voltage and 0.5-MVA power rating is assembled in the Power Electronics Laboratory of EPFL, and Christe et al. [7] discuss mainly the insulation design of the MMC structure. The hardware design of an MV MMC, including its control, is discussed in detail in [8], where the authors have developed a 7-kV MMC with 1.7-kV silicon carbide (SiC) MOSFET. However, in their setup, the APS for each MMC SM is taken externally using a large isolated power supply rated for 10 kV. This limits the output voltage to 7 kV and makes the MMC setup challenging to scale up with the voltage. This article proposes a scalable MV SM design that can be realized using commercially available components.

Before diving into the MV SM design, it is important to highlight that the MMC-based HV AWG has many different design requirements compared to the high-voltage direct current (HVDC) transmission application of MMC. First and foremost, there is no intended active power transfer from the input to the output side for the HV AWG application since the equivalent load with this new application is capacitive [5]. Hence, the power efficiency of the MMC is not the most relevant performance parameter, and the performance of the HV AWG is measured using the voltage efficiency in terms of the total harmonic distortion (THD). Such an MMC-based

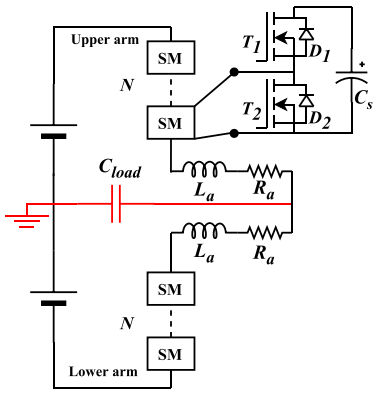


FIGURE 1. Schematic of MMC-based HV AWG.

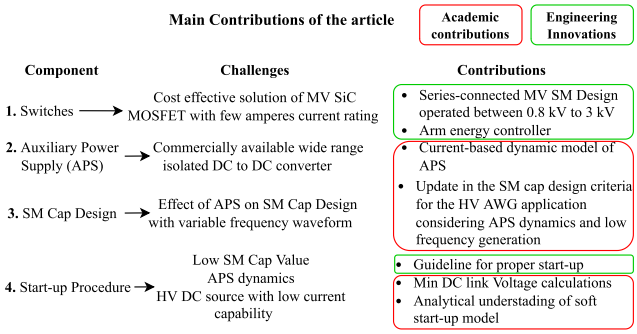


FIGURE 2. Main contributions of this article.

HV test source is used to perform dielectric testing on different MV/HV insulation materials to characterize them and to perform type tests on various MV equipment to ensure reliable operation. Hence, the MMC-based HV AWG needs to generate output voltage ranging from 10 to 100 kV to incorporate the MV/HV insulation material to MV distribution transformer [5]. If the MMC SM is designed for the highest voltage rating of 100 kV, the low voltage of 10 kV can be generated with a very low modulation index of 0.1. This will drastically reduce the number of levels in the output voltage and affect the voltage waveform quality. Hence, it is critical to design the MMC SM that can operate for a wide voltage range to maintain the quality of the generated voltage waveforms as per standards of HV testing. However, the variable SM voltage requires the onboard APS to operate for a wide input range from hundreds of volts to a few kilovolts and can step down from a few kilovolts to low voltage such as 12, 15, or 24 V. Hence, the main contribution of this article is summarized as follows. Since, this article is a combination of engineering innovations and academic investigations, both are highlighted in Fig. 2.

1) The hardware design of a scalable series-connected MMC SM that can operate for a wide voltage range (0.8–2.7 kV) with onboard APS. The aforementioned

SM design is comprised of commercially available components, keeping its cost low and making it possible to realize a full-scale prototype.

2) Equal voltage sharing among the series-connected SMs is ensured using the arm energy controller to compensate for the nonidealities in the APS, switches, and gate driver.
3) The start-up procedure is devised by modeling the APS dynamics as a current sink and how it affects the SM capacitor choice for the given value of dc-link voltage for this particular HV testing application. In addition, a soft start-up algorithm is studied analytically to understand its working principle and to design the average charging current within the limit for any number of SMs of the arm.
4) The performance of the proposed MV SM design and the proposed start-up, steady-state, and shutdown procedure is demonstrated in an MMC configuration with a single MV SM in each arm. Different arbitrary wave shapes, such as triangular and sinusoidal with different harmonics, are generated for the designed wide voltage range and the wide range of output frequency (1–600 Hz).

The rest of this article is organized as follows. Section II explains the HV AWG application in detail and summarizes the requirements and the challenges for the MV SM design. Later, the hardware design of the MV MMC SM is proposed in Section III from the off-the-shelf component. Next, Section IV gives an exhaustive summary of the hardware and control challenges present in the proposed design of MV SM with unique solutions suitable for the application. Afterward, the performance of the proposed design is demonstrated in Section V with a single MV SM in each arm of the MMC-based HV AWG. In addition, Section VI briefly summarizes the guidelines for realizing a full-scale prototype with the stacking of more of these MV SMs. Finally, Section VII concludes this article with future recommendations.

With this article, the research in the MMC-based HV AWG reaches the Technology Readiness Level (TRL) 4, where the MMC prototype is validated in the laboratory environment. Earlier, TRL 1 was achieved with the preliminary analytical and simulation studies of the MMC-based HV AWG [9]. The next step of TRLs 2 and 3 was achieved where exhaustive design tradeoffs were discussed analytically, with MATLAB/Simulink simulations and scaled-down MMC prototype [5]. The current status of the research work in the HV AWG is shown in Fig. 3.

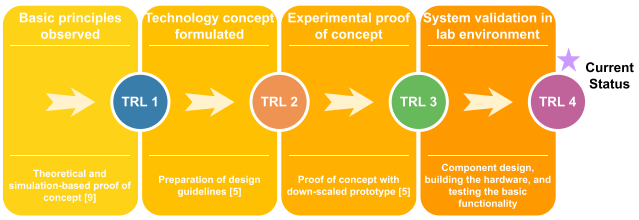


FIGURE 3. Current status of the research work.

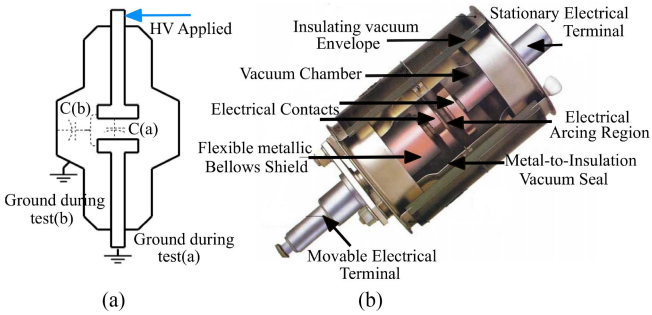


FIGURE 4. MV vacuum circuit breaker [26]. (a) Simplified HV test. (b) Construction detail.

II. HV AWG APPLICATION

To ensure reliable operation, power grid equipment undergoes mechanical, thermal, and dielectric property testing prior to integration into the grid. HV tests measure the dielectric strength, partial discharge behavior, and dielectric losses of MV and HV insulation materials [10]. During these dielectric tests, the equipment insulation behaves electrically as a capacitance [11]. The history of testing power grid equipment spans over a century [12] and is standardized by organizations such as IEC and IEEE for specific voltage classes. As per the standard [13], MV equipment has operating voltages of 1 and 36 kV, and they need to be tested for higher voltage of such as 100 and 250 kV. The HV equipment ranges from 36 to 150 kV and will need extra high voltage levels for the test. Therefore, testing of MV equipment is naturally the first target application where the MMC-based HV AWG needs to generate the output voltage up to 100 kV.

Figs. 4–8 provide images of commonly certified MV power grid equipment, namely, circuit breaker, distribution transformer, cable, and instrument transformer. Instrument transformers can be categorized into two types, namely, potential transformer (PT) and current transformer (CT). These figures illustrate the construction details of the aforementioned equipment and simplified diagrams of how HV tests are performed with respect to the applied HV potential and grounding parts. They also show the equivalent dielectric capacitances that may impact the tests. It is worth noting that there are significant differences in construction and operation between a distribution transformer and an instrument transformer (PT and CT) [14]. Consequently, the dielectric tests performed on the distribution transformer and PT differ in their test circuit, as shown in Figs. 5 and 7. While the test connections are the same for the distribution transformer and the CT, there is only a single turn in the primary winding of a CT with a toroidal core, as shown in [15], as opposed to a standard E core in the distribution transformer [16].

Table 1 provides the capacitance range of the power grid equipment mentioned earlier. The IEC standards are used to

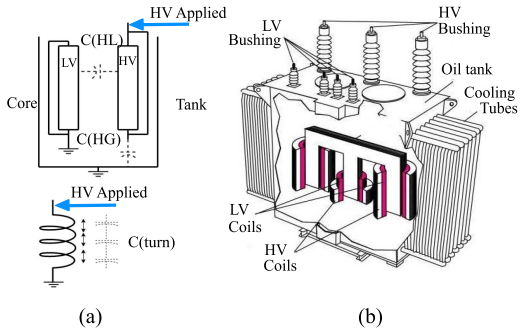


FIGURE 5. MV distribution transformer [27]. (a) Simplified HV test circuit. (b) Construction detail.

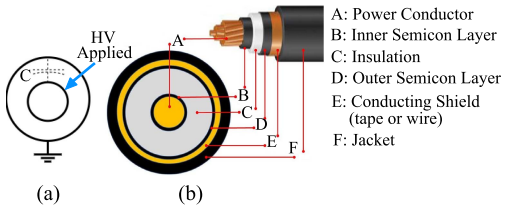


FIGURE 6. MV AC cable [28]. (a) Simplified HV test circuit. (b) Construction detail.

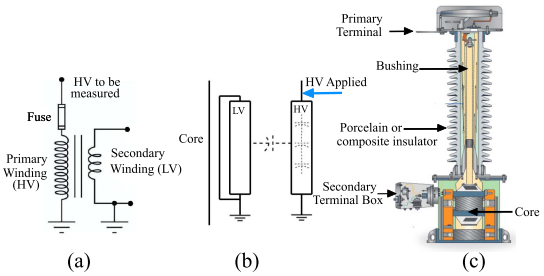


FIGURE 7. MV potential transformer [29]. (a) Simplified circuit. (b) Simplified HV test circuit. (c) Construction detail.

TABLE 1. Typical Range of the Equivalent Capacitance of Dielectric Insulation Materials

Vacuum Circuit Breaker [23]	Distribution Transformer [23]	AC Cable [24]	Instrument Transformer [25]
C(a) = 50 pF C(b) = 50 pF	C(HG) = 12–16 nF C(LG) = 19–26 nF	C = 1–10 nF	C(PT) = 1 nF C(CT) = 0.25 nF

test this equipment in the EU [17], [18] [19], [20], which involve sinusoidal and lightning impulse test waveforms [21]. Sinusoidal waveforms have a frequency of 50 or 60 Hz, while lightning impulses have a 1.2-μs rise time and a 50-μs tail time. Power frequency tests for MV class equipment are carried out at voltages higher than the equipment's rated voltage due to different switching transients [10]. For example, a 3-kV equipment is tested at 10 kV, and a 36-kV rated equipment is tested at 70–80 kV [19]. Manufacturers or owners of the device under test can also customize tests to push the limits of their equipment with higher voltages than the standardized values. Lightning impulse tests are performed at six to seven times higher voltage than the rated voltage of the equipment, depending on the voltage class of the equipment. For instance, a 36-kV transformer is tested with 170–220 kV lightning impulses [19]. PTs are also tested for their accuracy in measuring higher order voltage harmonics and need to be evaluated for this purpose. Therefore, the AWG should generate higher order harmonics up to the 50th harmonic [22].

Apart from equipment, HV tests are performed on different insulation materials to determine their dielectric properties before being used in HV equipment. These material tests require much lower voltages, such as 10 kV. This gives the final output voltage range for the MMC-based HV AWG as 10 to 100 kV. In addition, the output frequency range is considered between 1 Hz and 2.5 kHz considering the challenges of generating higher frequencies by means of the MMC-based HV AWG [5], [30]. In summary, the required specifications for the HV AWG are as follows:

1) Output voltage range: 10–100 kV;
2) Output frequency range: 1 Hz to 2.5 kHz;
3) Load capacitance range: 50 pF to 10 nF.

The HV AWG application has some significant differences from the existing energy transmission application of MMC, and they are summarized in the following section.

A. DIFFERENCE BETWEEN HV AWG AND ENERGY TRANSMISSION APPLICATION

1) *The magnitude of power transfer:* In the case of the AWG, the capacitive load range that has been specified will only require a relatively low output current, which typically ranges up to a few amperes. This low output current is responsible for transferring reactive power to the equivalent capacitive load. As a result, the active power requirement for the AWG is also low, and it only accounts for losses within the converter and test object. This is in sharp contrast to the active power flow in the megawatt range that is typically observed in HVDC transmission application range [31].
2) *Test object behavior:* In HV testing, there is a risk of test object experiencing breakdown or flashover. As a result, it is critical that the test source is capable of providing sufficient energy for the breakdown while also rapidly protecting itself within a few microseconds or milliseconds. On the other hand, in power applications such as renewable energy generation and battery energy systems, it may be necessary for power electronics to supply energy in a coordinated manner during a fault condition that lasts for a relatively long time, typically several milliseconds, without disconnection. An example of this is low-voltage ride-through [32].
3) *Operational Frequency:* Typically, a power electronic converter that is incorporated into the grid is designed for continuous operation. On the other hand, a test source is used only for a limited time period during regular working hours. When it comes to dielectric testing, the standard duration of the test usually ranges

from 1 min to 4 h, except for prequalification tests and long-term testing.

4) *Performance parameter:* While power efficiency is crucial when it comes to power electronic converters for energy transmission, voltage accuracy/efficiency is the top priority during HV testing. This is because active power transfer is not intentionally involved in HV testing, and therefore, the design requirements are primarily focused on factors such as output voltage and current, slew rate, and small- and large-signal bandwidth.

B. CHALLENGES FOR REALIZING MV MMC SM

Apart from the abovementioned technical differences, the following two points make designing and realizing the MV MMC SM challenging.

1) *Variable dc-link Voltage:* Since the output voltage needs to vary between 10 and 100 kV, the dc-link voltage needs to be varied from 20 to 200 kV for a constant modulation index in MMC implemented with half-bridge (HB) SM topology. The dc voltage variation needs the SM to operate with that large voltage range for the constant modulation index to avoid the poor quality of generated wave shapes. This is especially an issue for the onboard APS, because the APS needs to convert a large range of voltage to 12, 15, or 24 V.
2) *Low-current dc input power supply:* The MMC-based HV AWG needs two full-rated dc voltage sources as the input or one full-rated dc source with two capacitors to make a midpoint connection for bipolar waveforms. As explained earlier, the dielectric tests do not require high currents. Hence, the current rating of available HVDC sources is low, in the approximate range of tens of milliamperes. This condition gives additional challenges in the start-up procedure of the MMC-based HV AWG.

III. MV SM DESIGN DETAILS

Two essential constraints that dictate the MV SM design are available switches and the APS, and their choices are discussed below to create the MV SM structure.

A. SWITCHES

A very high switching frequency is critical to generate accurate voltage waveforms from the MMC-based HV AWG. Hence, SiC MOSFET is an ideal choice over Si-based MOSFETs, or insulated gate bipolar transistors [5]. Though CREE-Wolfspeed has developed a predeveloped version of 6.5-, 10-, and 15-kV SiC MOSFETs [33], they are not commercially available as of the writing of this article. Some interesting commercially available SiC MOSFETs are summarized in Table 2, which are more cost-effective solutions compared to MV SiC MOSFETs even when they become available in the future. The highest voltage blocking capability of these commercially available SiC MOSFETs is 3.3 kV. The TO-263-7 package is chosen considering the advantages of the Surface Mount Technology, such as high-density packaging and lower parasitics. SiC MOSFETs with 1.2 and 1.7 kV are available for a wide current range, and the devices in Table 2 are chosen based on the current required for this application.

TABLE 2. Switches Considered

Switches	Blocking Voltage	Continuous Current Id @ 25 °C
G2R120MT33 J	3300	35 A
G3R450MT17 J	1700	9 A
G3R350MT12 J	1200	11 A

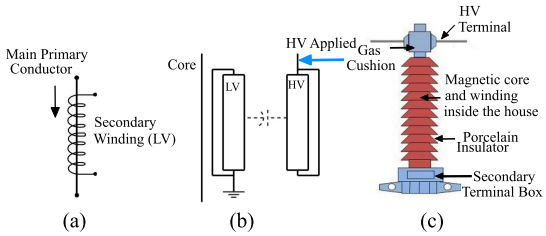


FIGURE 8. MV current transformer [15]. (a) Simplified circuit. (b) Simplified HV test circuit. (c) Construction detail.

B. AUXILIARY POWER SUPPLY

For the HV application, drawing the auxiliary power for the printed circuit board (PCB) from the onboard SM capacitance is expedient. Otherwise, the APS of the topmost SM will need isolation from the total dc-link voltage. This limits the output voltage, as discussed in [34] and [35], and makes the converter design nonscalable. Hence, the implementation of APS becomes critical, especially when the power supply needs to convert a wide range of SM voltage to a relatively small voltage of 12 V. For this requirement of APS, many converter topologies are studied in the literature, such as flyback [36], input series output parallel [37], or other variants [6], [38]. As discussed in many of these publications, implementing such an APS is challenging due to isolation requirements, series operation of switches, etc. Since the APS of the SM impacts critical factors such as reliability, safety, and cost-effectiveness, it has been decided to go with the commercially available solutions for the MMC-based HV AWG.

Two isolated dc-to-dc converters are found that satisfy the application criteria commercially. The first converter named PV15-27B12R3 from Mornsun Power has input voltage range of 0.1–1 kV, and it step downs it to 12 V. The other converter named AE15-EW-S12 from CUI Inc. has a wider input range from 0.2 to 1.5 kV. In addition, Mornsun is developing a converter with an even wider input range converter from 0.25 to 3.3 kV. It is called PV75-36D15400-01, and a sample of this product is available for research. The photos of all three auxiliary power supplies are shown in Fig. 9, and their description is compared in Table 3.

C. STRUCTURE OF MV SM

Based on the current availability of the switches and the APS, the highest voltage per SM can be 1.5 kV with 3.3-kV SiC MOSFETs switches and AE15-UW-S12 APS. However, this low voltage per SM creates a challenge for the controller and

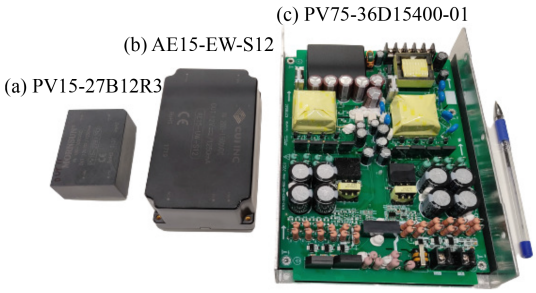


FIGURE 9. Commercially available auxiliary power supplies.

TABLE 3. Details of Commercially Available Auxiliary Power Supplies

	Manufacturer	Power	Efficiency (Typ.)
0.1–1 kV PV15-27B12R3	Mornsun Power	15 W	81%
0.2–1.5 kV AE15-UW-S12	CUI Inc	15 W	71%
0.25–3.3 kV PV75-36D15400-01	Mornsun Power	32 W	70%

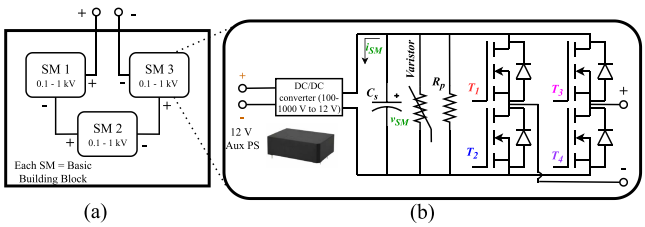


FIGURE 10. MV SM structure. (a) 3-kV MV SM. (b) 0.1–1 kV SM structure.

communication since it means that one needs a minimum of 134 SMs per arm without considering redundancy. As discussed in [5], the minimum of 67 SMs with 3 kV can be an optimum solution. The 3-kV switch can be realized either using series combination of three 1.7 kV or series combination of two 3.3 kV. Since the current rating requirement of the HV testing application is quite less than 35 A, stray capacitances in the 3.3-kV switches will not give optimum switching performance at the current level such as 1 A. Since the high-switching frequency is crucial to the application, low-current-rated 1.7-kV switches are chosen, which is also much cheaper solution compared to 3.3-kV switches. Though it is possible to connect 1.7-kV switches in series to create a 3-kV switch, the APS is not available commercially, which converts 3 kV to low voltage. Even if the PV75-36D15400-01 APS gets available commercially, the APS is much larger and will consume more space than the SM capacitance on the MMC module. Hence, it is not an optimal solution for the application. Hence, a 3-kV MV SM is realized using three 1-kV SMs connected in series, as shown in Fig. 10.

Fig. 10(b) shows a zoomed picture of a single SM that can operate between 0.1 and 1 kV rating, and it is called the basic fundamental block in the further part of the article. The basic fundamental block is realized using a 1.7-kV rated SiC MOSFET and using PV15-27B12R3 APS. The structure of the single SM in Fig. 10(b) consists of a full-bridge (FB) SM topology, SM capacitance (C_s), parallel resistor (R_p), PV15-27B12R3 APS, and varistor. Note that the isolation capability of this APS is 4 kV, which ensures that the proposed MV SM design can be stacked on each other to build a 100-kV MMC-based HV AWG. The FB topology is chosen for the HV AWG application since it gives more flexibility to control the SM capacitance voltages and offers the advantage of obtaining the peak output voltage the same as dc-link voltage compared to the HB topology [39]. It means that the dc-link voltage requirement is reduced by half, which is a great advantage, especially for this HV application. However, in this article, the FB is operated as HB to demonstrate this MV SM design. Hence, when all the SMs in series connection are counted as N in each arm, the number of levels obtained in the output voltage will be $2(N/3)+1$ since $N/3$ SMs are operated as one MV SM.

IV. HARDWARE AND CONTROL CHALLENGES

There were four significant challenges faced in realizing this scalable MV SM design. The first challenge is creating equal voltage sharing among the series operation of three SMs due to the hardware's nonidealities. The second is about the start-up issues faced due to the installed APS and the low-current rating HVDC source. The third is about the SM capacitance design considering the effect of the installed APS. The last discussed part is about the protection design for the HV AWG in case of any fault within or outside the converter.

A. HARDWARE NONIDEALITIES

There are three SMs connected in series, and they must share the voltage equally, which can be disturbed by either of the following four factors. They are discussed in detail with possible solutions to ensure equal voltage sharing.

1) GATE PULSES

Though gate pulses of all the SMs are controlled synchronously, three SMs connected in series can have different time delays. The delay can be attributed to the controller, the communication hardware, and/or the gate driver design. A real-time simulator from OPAL-RT OP5600 is used as a controller and sends synchronized gate pulse signals. In addition, the fiber-optic connection keeps the delay to a few nanoseconds. All four switches are controlled independently using an ACPL-344JT gate driver IC with a typical value of the propagation delay as 100 nS.

2) SWITCHES

Switches in different SMs can have different parasitic capacitances that take different times to turn ON and OFF even though they receive the gate pulses simultaneously.

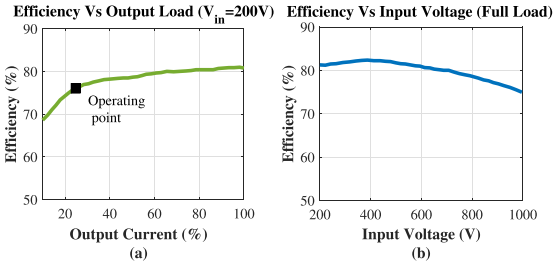


FIGURE 11. APS—PV15-27B12R3. (a) Efficiency versus output load. (b) Efficiency versus input voltage.

3) AUXILIARY POWER SUPPLY

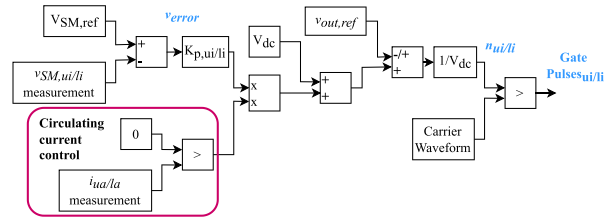
This isolated dc–dc converter is connected parallel to the SM capacitance. It can greatly influence the voltage sharing of the series connection. The current consumption by the APS (i_{SM}) can be calculated as

$$P_{APS} = v_{SM} i_{SM} \eta_{APS}. \tag{1}$$

Here, P_{APS} is the power consumption of APS for that SM PCB board, and v_{SM} is the voltage across the SM capacitance. In addition, η_{APS} is the efficiency of the APS. The multiple APSs connected to three SMs in series can have different η_{APS} and different P_{APS}. Hence, even if they start with the same initial voltage $v_{SM,initial}$, eventually, they will start deviating from $v_{SM,initial}$ since i_{SM} will be different, which will deplete the SM voltage differently. Since i_{SM} increases as v_{SM} reduces, there is a positive feedback loop. It means that the SM that has lower SM voltage consumes higher i_{SM}, leading to a faster reduction in v_{SM}. Hence, without any control, the unequal voltage sharing will worsen faster.

Fig. 11 shows the efficiency of the converter as per P_{APS} and v_{SM}. The load of the onboard APS is the PCB consumption around 3.6 W. This amount is 24% of 15 W, which is the full power capability of the APS. Fig. 11(a) highlights the operating point as per the percentage of full load, and it is clear that the efficiency is less than 80%. As per the voltage graph in Fig. 11(b), the highest efficiency is achieved at 50% of the highest possible voltage. Lower efficiencies at higher voltages are not a problem since the current consumption will be drastically reduced, making it easier to balance the series operation.

Among the three discussed nonidealities in the hardware, the difference in the APS consumption (i_{SM}) affects equal voltage sharing the most since the APS consumption can be different dynamically and during steady state since v_{SM} varies as per the output voltage to be produced. It is possible to use a parallel resistor (R_p) to assist in equal voltage sharing among series-connected SMs. However, the value of this R_p needs to be tuned as per the APS consumption, i_{SM}. Since this consumption varies by so many factors, as mentioned above, it is tedious to tune R_p for different cases. In addition, it is more beneficial to utilize the control rather than the power connection for safety and reliability. Hence, the individual



No.	Description	Symbol	No.	Description	Symbol
1.	Reference of SM Capacitor Voltage	$V_{SM,ref}$	5.	DC link Voltage	V_{dc}
2.	SM Capacitor Voltage Measurement of i^{th} module from upper/lower arm	$V_{SM,ui/li}$	6.	Error in the reference and measurement of the SM Cap Voltage	v_{error}
3.	Upper/lower arm current	$i_{ua/la}$	7.	Output Voltage Reference	$v_{out,ref}$
4.	Proportional gain of i^{th} SM from upper/lower arm	$K_{p,ui/li}$	8.	Insertion indices for the ith submodule fro upper/lower arm	$n_{ui/li}$

FIGURE 12. Arm energy controller per SM.

SM-based arm energy controller is proposed to ensure equal voltage sharing among series-connected SMs.

A simple proportional controller is designed for equal voltage sharing during the steady-state operation, and its implementation for a single SM is shown in Fig. 12. All the SM capacitor voltages are measured and compared with the reference value. The output of the proportional controller is added or subtracted from the dc voltage. The decision of addition or subtraction is made based on the arm's current direction. Since the average circulating current in the steady-state operation of the MMC-based HV AWG is zero, the effect of the circulating current is taken into the arm energy controller by changing the sign. The sign of the arm current decides whether the controller output is added or subtracted from the dc-link voltage. This variation in the dc-link voltage changes the reference waveform, which changes, in turn, the gate pulses. This adjustment counteracts the APS current consumption and other hardware nonidealities, resulting in equal voltage sharing among the SMs. As discussed in [5], a phase-shift carrier modulation technique is used to generate gate pulses from the reference waveform with a switching frequency as a noninteger multiple of the fundamental frequency.

B. START-UP PROCEDURE

The MMC-based HV AWG needs a black-start capability since SMs do not have auxiliary power until the voltage per SM reaches roughly 100 V. Using the antiparallel diodes of the MOSFETs, it is possible to charge the SM capacitor voltages to 100 V. However, the series operation of APS has the following major issues.

1) The voltage at which different APS turns ON is quite wide and varies between 60 and 85 V [40].
2) The inrush current drawn by the APS can be as high as 200 mA when the input voltage is 100 V and SM capacitance (C_s) is 75 μF, as shown in Fig. 13.
3) Different APSs have a different delay to start-up even when the SM capacitor voltage is the same in all the SMs.

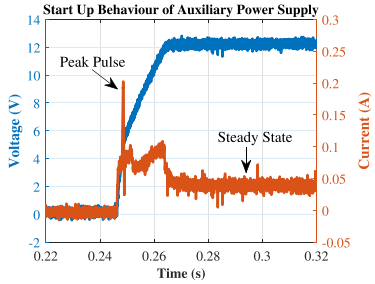


FIGURE 13. Start-up behavior of APS with $V_{SM} = 100$ V and $C_s = 75$ μF.

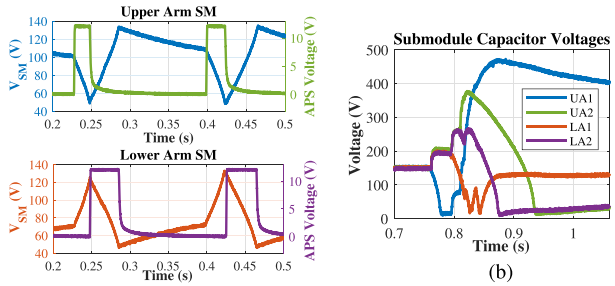


FIGURE 14. Issue with the APS at $C_s = 75$ μF. (a) One SM at each arm. (b) Two SMs at each arm.

These issues combined create problems in the start-up, as shown in Fig. 14, for one SM in each arm and two SMs connected in series in each arm with SM capacitance of 75 μF and $v_{SM,initial}$ of roughly 100 V. Fig. 14(a) shows the SM capacitor voltage and the output of the APS for the upper arm (UA) and lower arm (LA). The APS from UA turns ON at 0.23 s. However, it experiences a considerable voltage drop due to the in-rush current of the APS. Hence, when LA gets its auxiliary power, the APS from UA turns OFF. A similar problem occurs for two SMs in each arm, as shown in Fig. 14(b), with the four SM capacitor voltages. It is important to point out that the second SM from UA (UA2) gets its auxiliary power last, which is 50 ms after the first SM gets its APS. This time difference in receiving the auxiliary power for different SMs can be different depending on many system parameters, such as SM capacitance value, the current capability of the dc source, etc. The solution to this problem is multifold. First of all, it needs to have a proper start-up procedure. Second, the choice of SM capacitance and initial SM capacitor voltage ($v_{SM,initial}$) needs to be done properly considering all the abovementioned nonidealities in the APS. The following section addresses all these challenges to ensure a proper start-up and steady-state operation of the MMC-based HV AWG.

1) START-UP GUIDELINE

To avoid the issues shown in Fig. 14, the following guidelines are important to follow.

1) Directly apply the dc-link voltage with current-controlled mode to charge the SMs to a minimum voltage of 100V fast and simultaneously.

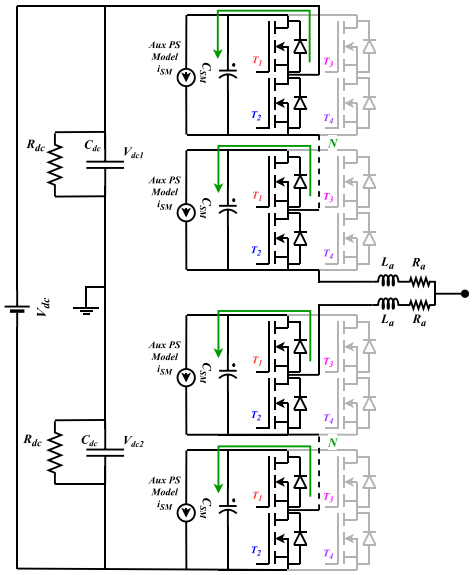


FIGURE 15. Schematic of MMC during the start-up.

2) As discussed earlier, most HVDC sources can supply only up to a few tens of milliamperes. Hence, it is important to implement a soft start-up to charge the SM capacitor voltages from $V_{DC}/2N$ to V_{DC}/N without requiring large inrush current.
3) The SM that gets the APS first is kept inserted, so the SM capacitor voltage is maintained even after the transient and steady current drawn by the APS.

To be on the safe side, gate pulses as per particular reference waveform are inserted after 5–20 ms after all the SMs receive auxiliary power. This methodology of insertion of SMs ensures that the circulating current maintains the SM capacitor voltage, while the APS is draining the current (i_{SM}). The path for charging the SMs is shown with a schematic in Fig. 15. Also, it limits the SM capacitor voltages whose APSs are not turned ON, unlike in Fig. 14(b).

2) SOFT START-UP IMPLEMENTATION

The SM capacitor voltages are charged to $V_{DC}/2N$ with current limiting mode on the HVDC source where the antiparallel diodes are conducting the charging current. It is assumed that the APSs of all SMs are turned ON before implementing the soft start-up algorithm, and this stage is considered Stage 0. At the instant of soft start-up algorithms begins (T_{s1}), all N SMs are inserted. The soft start-up algorithm charges the SM capacitor voltages to V_{DC}/N by changing the inserted SMs per arm from N to $N/2$, as described in [41]. This soft start-up algorithm differs from using a proportional–integral controller to keep the charging current constant in [42] and [43]. However, the former start-up algorithm is chosen, considering that it does not produce any output voltage or current during the soft start-up. It is ideal to apply the desired dielectric voltage stress directly. The charging algorithm can be achieved in two stages for $N = 3$. In the first stage, two SMs from each

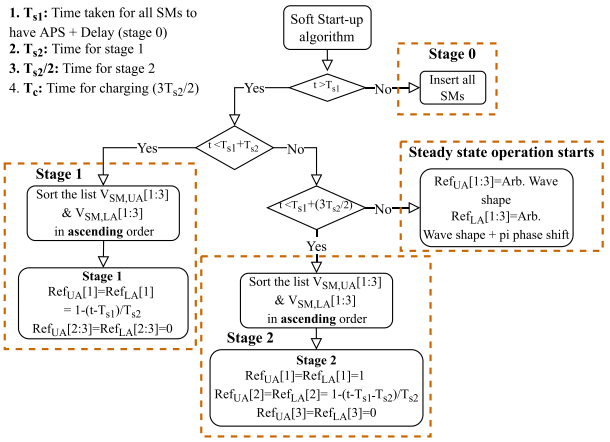


FIGURE 16. Soft start-up algorithm for $N = 3$.

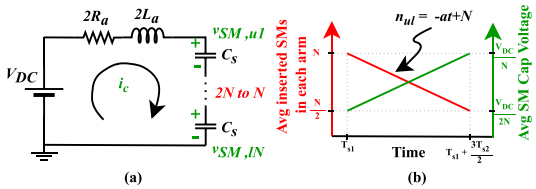


FIGURE 17. Working principle of the soft start-up algorithm. (a) Circulating current circuit. (b) Insertion index.

arm are always inserted, and single SM from each arm is switching with varying duty ratios from 1 to 0 in T_{s2} duration. During this first stage, the total inserted SMs from both arms changes from six to four. In the second stage, one SM from each arm are always inserted, one SM from each arm is always bypassed, and one SM from each arm is switching with varying duty ratios from 1 to 0.5 in $T_{s2}/2$ duration. During both the stages, SMs are sorted to decide which one to be inserted based on the SM capacitor voltages. Hence, any variations present in the SM capacitor voltages at T_{s1} time instant are disappeared, and equal voltages are obtained among series-connected SMs when the reference waveform is being generated, which helps the arm energy controller. Fig. 16 shows the exact soft-start algorithm for $N = 3$.

The basic working principle of this soft start-up algorithm is shown in Fig. 17 when N can be any number more than three. From the circulating current circuit shown in Fig. 17(a), [5], it is clear that the soft start-up algorithm is influenced by the passive element values such as the arm inductance, the arm resistance, and the SM capacitance. In addition, Fig. 17(b) shows the overall dynamics of the SM insertion in both arms and how the SM capacitor voltages are charged from $V_{\mathrm{DC}}/2N$ to V_{DC}/N. The dynamic of the SM insertion is linear with a negative slope of "a," and it can be represented in (2), assuming $T_{s1} = 0$. Another equation can represent the same equation, where the integer part of n_{ul} is "n" and its decimal part is "d." The desired rise in the SM capacitor voltages for three SMs is obtained in two stages, as explained above. In the first stage, $n = 2$, and d varies from 1 to 0. In the second stage,

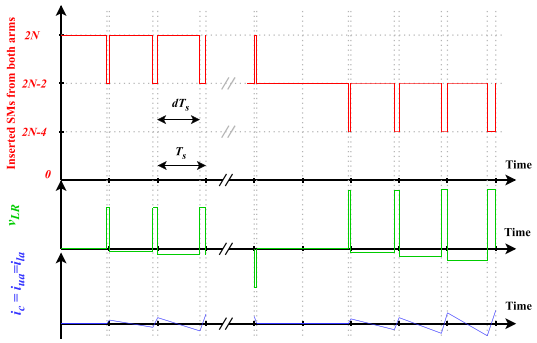


FIGURE 18. Waveforms during the soft start-up.

n is reduced to 1, and d varies from 1 to 0.5, where n_{ul} reaches 1.5. More stages would be needed to reduce the inserted SMs from N to $N/2$ for a higher number of SMs

$$n_{ul} = -at + N = n + d. \tag{2}$$

Fig. 18 shows the detailed switching behavior of all SMs from both arms with variable duty and how the charging current is generated. Here, the switching frequency is T_s, and the duty ratio "d" is the same as the decimal part mentioned above. As soon as the inserted SM is reduced from $2N$ to $2N - 2$, a positive voltage is built across the arm inductance and arm resistance, resulting in a positive charging current i_c. When n_{ul} reaches $N/2$, then the algorithm stops. The dynamics behind this soft start-up algorithm can be understood analytically with (3)–(7). First, it is important to find the relation between the average instantaneous voltage of SM capacitor voltage and dc-link voltage, and it is shown in (3). For any integer value of n_{ul} (n), it is possible to write two equations for charging current and for discharging current, as shown in (4) and (5), respectively. Since the dynamics of charging current are linear, it is possible to derive the peak charging current using (6), and it is simplified in (7)

$$V_{\mathrm{SM,avg},t} = \frac{V_{\mathrm{DC}}}{2n_{ul}} = \frac{V_{\mathrm{DC}}}{2n + 2d} \tag{3}$$

$$2R_a i_c + 2L_a \frac{di_c}{dt} = V_{\mathrm{DC}} - (2n + 2)V_{\mathrm{SM,avg}} \tag{4}$$

$$2R_a i_c + 2L_a \frac{di_c}{dt} = V_{\mathrm{DC}} - 2nV_{\mathrm{SM,avg}} \tag{5}$$

$$2R_a I_{pp} + 2L_a \frac{I_{pp}}{(1-d)T_s} = V_{\mathrm{DC}} - 2n\frac{V_{\mathrm{DC}}}{2n + 2d} \tag{6}$$

$$I_{pp} = \frac{d(1-d)T_s V_{\mathrm{DC}}}{4(n+d)(L_a + R_a(1-d)T_s)}. \tag{7}$$

The maximum peak current for this charging can be derived when the integer part (n) is the lowest, and the minimum value of n can be calculated for any number of SMs, as shown in (9). In addition, it is possible to derive the maximum value of I_{pp} with respect to the decimal part (d), and its value is derived, as shown in (10). Hence, the maximum value of I_{pp} can be

calculated from (8). Note that this instantaneous peak current is supplied by the dc-link capacitors (C_{dc}), and the average charging current is provided by the dc source. Calculating the average current drawn by the dc source is possible, assuming the energy conservation principle. In addition, when the capacitors are charged through a resistor, it is well known that the energy supplied by the dc source is split equally between the resistor and the capacitor. With this assumption, it is possible to calculate the average charging current (I_c) using the equation shown in (11). Here, T_c is the time to charge the SM capacitors. It is related to the slope of the insertion index as $T_c = a/N$. Depending upon the current capability of the HVDC source, the time for charging should be calculated from (12)

$$I_{ppm} = \frac{d_m(1-d_m)T_s V_{DC}}{4(n_m+d_m)(L_a+R_a(1-d_m)T_s)} \tag{8}$$

$$n_m = \text{floor}\left(\frac{N-1}{2}\right) \tag{9}$$

$$d_m = -(R_a T_s * n_m + L_a n_m + \sqrt{(L_a R_a T_s n_m^2 + L_a^2 n_m^2 + L_a R_a T_s n_m + L_a^2 n_m)})/(-R_a T_s n_m + L_a) \tag{10}$$

$$V_{DC} I_c T_c = 2\frac{1}{2}(2N)C_s\left[\left(\frac{V_{DC}}{N}\right)^2 - \left(\frac{V_{DC}}{2N}\right)^2\right] \tag{11}$$

$$T_c = \frac{2NC_s}{V_{DC} I_c}\left[\left(\frac{V_{DC}}{N}\right)^2 - \left(\frac{V_{DC}}{2N}\right)^2\right]. \tag{12}$$

C. SM CAPACITANCE CHOICE

The SM capacitance value is one of the most critical parameters in determining voltage efficiency, size, and cost of the MMC-based HV AWG. All advantages offered by MMC come with the challenge of balancing SM capacitance voltages. Generally, the SM capacitance value is designed according to the total energy stored in all SM capacitance per MVA rating of the converter or to keep the capacitor voltage ripple within a limit. In [5], the capacitor voltage ripple is derived for HV AWG application, and it has been proven that 10 μF is enough to generate accurate voltages. However, that design guideline did not include the series operation of SMs or the effect of the onboard APS. In addition, the start-up issues shown in Section IV-A can be solved with the right design of the SM capacitance value and the initial voltage of the SM. These issues are not seen in typical HV MMC hardware since the SM capacitance lies in millifarad range. As described in [44], the SM capacitance takes 50% of the total volume of the SM. Hence, for this HV AWG application, it is not wise to increase the SM capacitance to millifarad range since it can drastically increase the size and cost of the MMC-based HV AWG. In addition, a larger SM capacitance value requires a longer time to charge the SM to $v_{SM,initial}$, which is especially problematic since most HVDC sources cannot provide current more than a few tens of milliamperes.

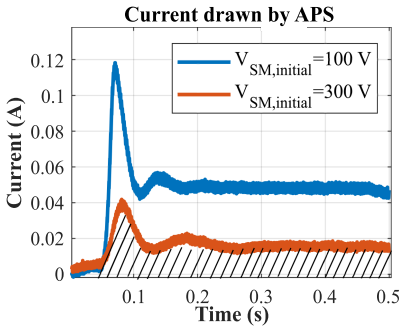


FIGURE 19. SM capacitance design.

The APS current consumption affects both the start-up and steady-state operation of the MMC-based HV AWG if the SM capacitance value is not large enough. During the start-up, APS draws an inrush current of 200 mA, which creates the first voltage drop ($\Delta v_{SM,1}$) in the SM capacitor voltage. Then, the SM capacitor voltage needs to be maintained until all SMs get the APS working, creating a second voltage drop of $\Delta v_{SM,2}$. Combining both voltage drops, the SM capacitor voltage should not drop less than 75 V, where the APS turns OFF [40]. In Fig. 14(a), the SM capacitor voltage drop from 100 to 50 V in the first 20 ms and the APS turns OFF. This clearly shows that $\Delta v_{SM,1}$ itself is 50 V. This should be reduced to 12.5 V so that $\Delta v_{SM,2}$ can be 12.5 V and the SM capacitor voltage will not drop below 75 V. Since $\Delta v_{SM,1}$ needs to be reduced from 50 to 12.5 V, the SM capacitance value needs to be increased roughly four times from 75 to 310 μF as per (13). With the higher value of SM capacitance, the APS has a different dynamic performance, as shown in Fig. 19. It draws less peak current with a relatively smoother current wave shape compared to the 75-μF capacitance. Also, it is important to note that the in-rush peak current reduces as $V_{SM,initial}$ is increased.

In the experiments, it has been observed that the mismatch in start-up delay of different APSs can be as high as 300–450 ms when six SMs are present with 310-μF capacitance and an HVDC source with limited current capability. Instead of increasing the SM capacitance further, the $V_{SM,initial}$ voltage is varied from 100 to 300 V to find an optimum point where the total SM capacitor voltage drop is not below 75 V. Using (13) and (14), the minimum value of $V_{SM,initial}$ is calculated to be 130 V for 310 μF with 450-ms delay between first and last APS to turn ON. The integration in (14) is obtained from the area under the curve from Fig. 19

$$i_{SM} = C_s \frac{dv_{SM}}{dt} \tag{13}$$

$$\Delta v_{SM} = \frac{1}{C_s}\int_0^{t=0.45} i_{SM}\, dt. \tag{14}$$

Apart from the start-up, the APS consumption disturbs the charge time product during the steady state, creating a larger SM capacitor voltage ripple for lower frequency waveform. Hence, it is important to have enough SM capacitance for

lower frequency waveform to keep the voltage ripple around 10% of the average SM voltage value [45], [46]. The ripple is largest when the SM capacitor voltage is lowest since the APS consumption is highest. For $V_{\text{SM,initial}} = 130$ V, the steady-state SM capacitor voltage is 260 V. Hence, I_{SM} is calculated to be 17.8 mA from (1), considering 78% efficiency. Considering 10% of 260 V, the allowed capacitor voltage ripple is 26 V. It is possible to calculate the minimum possible frequency from (15). Δt in (15) is half of the period. The minimum possible frequency is 1.1 Hz. The MMC-based AWG can go low frequency since there is almost negligible active power transfer to the load, and the transferred reactive power is also low, drawing only a few amperes of arm current and zero average circulating current

$$\Delta t = \frac{\Delta V_{\text{SM}} C_s}{I_{\text{SM}}} = \frac{26 \times 310 \times 10^{-6}}{0.0178} = 0.42 \text{ s}. \tag{15}$$

D. PROTECTION DESIGN

Apart from proper start-up, steady state, and shutdown operation of the HV AWG, it is essential to protect the converter from undesired fault scenarios. Among many possible failures in the converter, the breakdown of the inductor can create extremely severe di/dt and peak amplitude of the current in the particular arm since there is no limiting inductor. Hence, it is crucial to protect the switches and other components on the SMs from these extreme currents and voltages. The installed gate driver (ACPL-344JT) can detect the high current magnitudes and di/dt flowing through switches. Apart from that, each SM PCB has overvoltage protection. One SM among each arm has the current sensor and can detect overcurrent scenarios. The fault signal from the gate driver, overvoltage fault signal, and overcurrent fault signal are sent to an AND gate on each SM to generate a fault signal, which is sent to the central controller. In case of any fault on any SM, all SMs will be disabled together to avoid any damage. The controller is implemented in the real-time simulator (OPAL-RT), and it can disable the switches as fast as 20 μs. Hence, the fault-ride through (FRT) capability is not present in the implemented protection system design since the switches are blocked right after the fault occurs. In addition, it is essential to discharge the dc link in case of a fault condition and turn OFF the dc source. Hence, an HV relay is installed to discharge the dc-link capacitance through the fault resistor and disable the HV power supply. This relay can be operated manually. Fig. 20 shows the updated schematic of the MMC-based HV AWG with the implemented protection. In addition, the overall timeline of operation of the MMC-based with a single MV SM is shown in Fig. 21.

E. GENERAL MMC PARAMETERS

After designing the SM capacitance, the design tradeoffs of arm inductance and arm resistance are analyzed with the output current circuit shown in Fig. 22. The switching harmonics present in the MMC (v_s) are removed from the output voltage

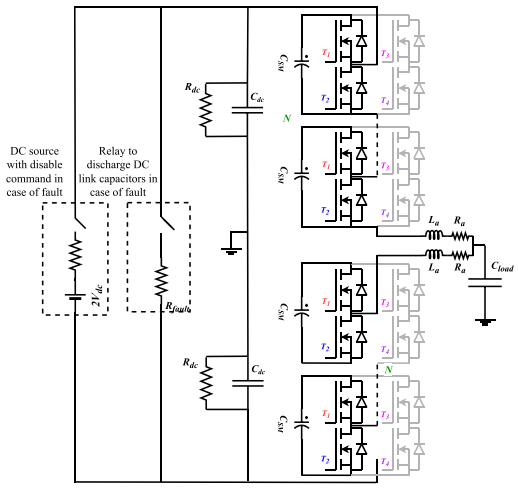


FIGURE 20. Protection circuit of the MMC-based AWG with a single MV SM.

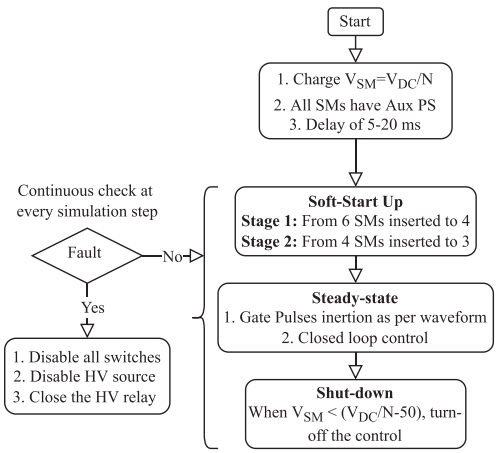


FIGURE 21. Overview of the MMC-based AWG with single MV SM operation.

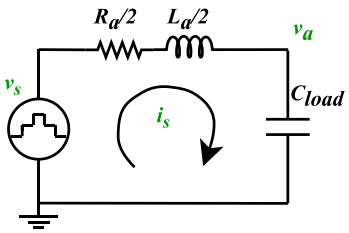
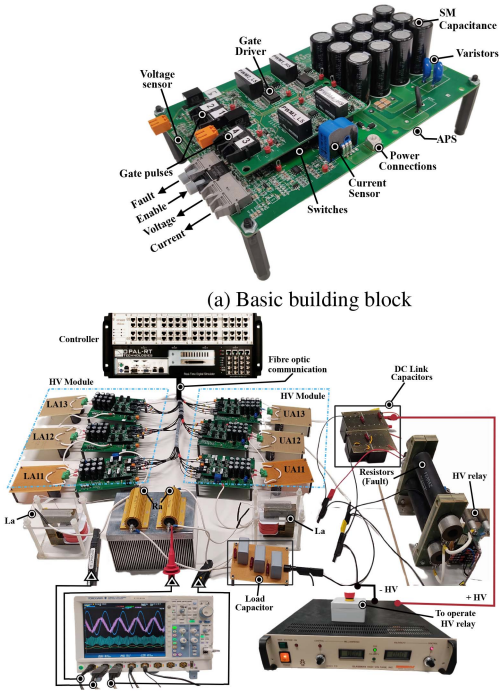


FIGURE 22. Passive element design.

(v_a) by the first order created by the load capacitor (C_{load}), arm inductance (L_a) and arm resistance (R_a). In this *RLC* circuit, the resonance created between L_a and C_{load} is damped using the arm resistor, and its minimum value is shown in (16) as per damping requirement [5]. When the MMC prototype contains only a single SM per arm, the switching frequency (F_s) in v_s does not shift farther than ($2F_s$). Hence, this puts higher requirements on the single-order low-pass filter, resulting in



(a) Basic building block

(b) MMC-based AWG with Single MV SM

FIGURE 23. Experimental setup. (a) Basic building block. (b) MMC-based AWG with single MV SM.

the higher value of L_a

$$R_a \geq \sqrt{\left(\frac{8L_a}{C_{\text{load}}}\right)}. \tag{16}$$

V. HARDWARE SETUP AND RESULTS

The design of this series-connected MV SM is verified with the experimental setup, as shown in Fig. 23, with one MV SM in each arm. This MV SM is scalable in the sense that they can be stacked on top of each other to build the HV AWG with an output voltage rating of 100 kV. For testing a single MV SM to its maximum rating of 3 kV, the load capacitance is down-scaled from 10 to 680 nF to keep the same current rating. The design of the arm inductance (L_a) and arm resistance (R_a) is determined as per the design guidelines discussed above and their values are 27 mH and 150 Ω, respectively. The value of arm inductance is higher since there is only one SMs per arm in the current experimental setup, which needs higher inductance to filter the voltage harmonics. In addition, the value of arm resistance is reduced lower than the overdamped system discussed in (16) to limit the losses in the laboratory-scale setup to 40 W.

This hardware setup is controlled using the OPAL-RT simulator (OP5600). Each SM receives an enable and four gate pulse signals and transmits back the SM capacitor voltage, fault signal, and arm current measurements via a digital voltage oscillator and fiber optics. The output voltage and arm currents are measured using the HV differential probe

TABLE 4. System Parameters of the MMC-Based AWG With a Single MV SM

No	Description	Symbol	Values
1.	DC-link voltage	V_{DC}	0.8—2.7 kV
2.	Output voltage	V_a	0.2—1.2 kV
3.	Modulation index	m_a	0.3—0.9
4.	Number of SMs	N	3
5.	Switching frequency	F_s	7011 Hz/9011 Hz
6.	SM capacitance	C_s	310 µF
7.	Arm inductance	L_a	27 mH
8.	Arm resistance	R_a	150 Ω
9.	Load capacitance	C_{load}	680 nF

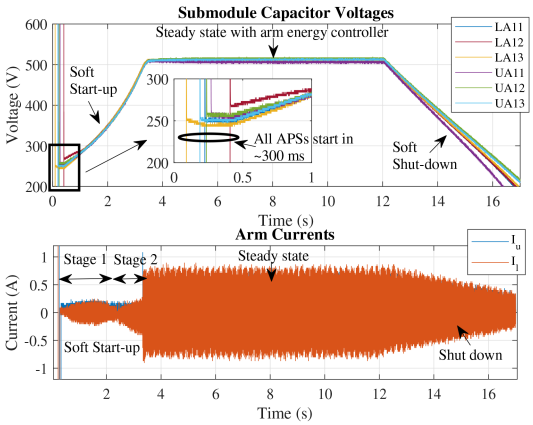


FIGURE 24. Soft start-up and soft shutdown of the MMC-based AWG with a single MV SM.

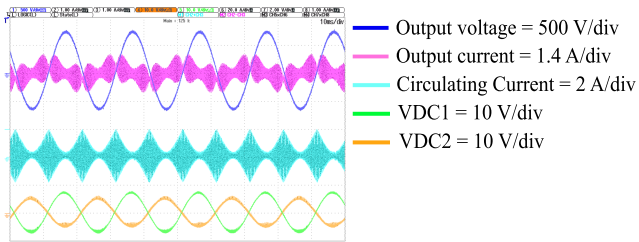


FIGURE 25. Steady-state performance of the MMC-based AWG with a single MV SM.

(CT4072) and current probes (N2782B). The above-discussed system parameters are summarized in Table 4. In this table, the switching frequency (F_s) is chosen as 7011 or 9011 Hz for balancing the SM capacitor voltage naturally. In addition, Fig. 23(a) shows the basic fundamental block of the MV SM, which is SM PCB, and Fig. 23(b) displays the experimental setup of HV AWG.

First, the dynamic performance of the MMC-based AWG with a single MV SM has showcased in Fig. 24 with 1.55-kV dc-link voltage. Hence, the steady-state SM capacitor voltages are properly balanced between 500 and 520 V, which concludes that the implemented arm energy controller is working correctly. In addition, the soft start-up algorithm discussed in Section IV-B is working properly that the SM capacitor voltages are slowly rising from ($V_{DC}/2N$) to (V_{DC}/N) without

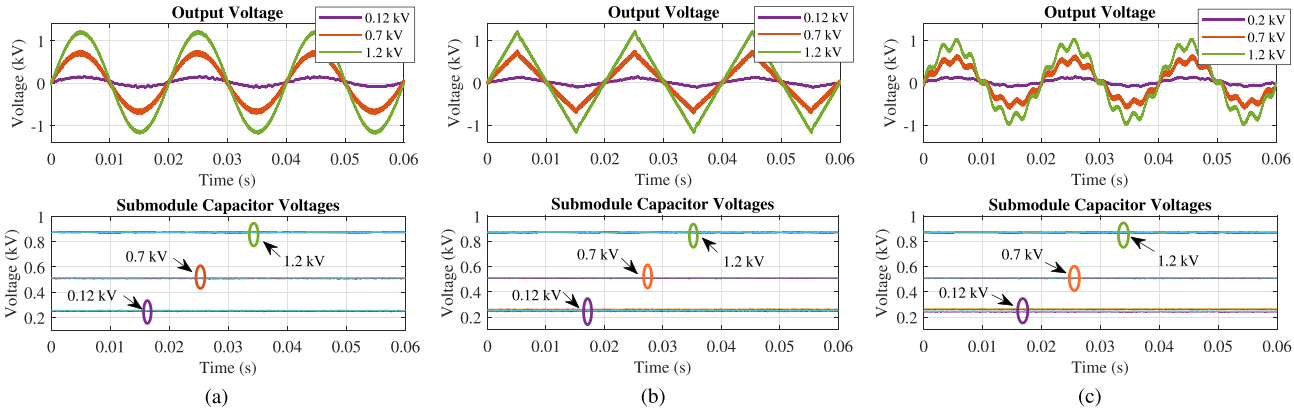


FIGURE 26. **Experimental results with wide output voltage range. (a) 50 Hz sinusoidal. (b) 50 Hz triangular. (c) 50 Hz sinusoidal superimposed with 400 Hz sinusoidal.**

drawing large charging current. The model developed in Section IV-B is verified with the experimental results shown in Fig. 24. A sufficient large charging time (T_c) of 3 s is chosen so that the average current drawn from the HVDC source is limited to 80 mA, which is almost the same as the experimentally obtained value of 78 mA. Moreover, the detailed model of maximum peak-to-peak charging current is found to be 420 mA, while the model predicted it to be 480 mA. In addition, the zoomed picture of the start-up shows that the delay between the first APS and the last APS turning ON is 300 ms. Fig. 25 shows the output voltage, output current, and circulating current during steady-state operation at 1.555 kV with 0.9 modulation index, which generates 700-V peak sinusoidal. The higher values of steady-state arm currents are supplied by the dc-link capacitors with a small voltage ripple, as shown in Fig. 25, with green V_{DC1} and orange waveform V_{DC2}.

Second, the performance of the MMC-based AWG with a single MV SM per arm is showcased for the wide output voltage range. Though the MV SM was aimed to operate from 0.3 to 3 kV, the issues with lower voltage are discussed in Section IV in detail, and those issues can be solved with a larger minimum voltage of 0.8 kV (3×0.267 kV). Earlier, when the minimum voltage per SM could go to as small as 0.3 kV, the MMC-based AWG with a single MV SM could have an output voltage from 0.135 to 1.35 kV considering a 0.9 modulation index. Since the minimum operable voltage of the MMC is elevated to 0.8 kV, the lower voltages are obtained with a 0.3 modulation index. Hence, the minimum obtained output voltage is 0.12 kV, and the performance of the MMC-based AWG at this output voltage for different wave shapes is shown in Fig. 26(a)–(c). In addition, a midrange of 0.7 kV is chosen with 1.55-kV dc-link voltage and 0.9 modulation index. The highest voltage is chosen to be 1.2 kV, operating at 88% of the full-rated MV SM for safety reasons. Each figure displays the output voltage and the SM capacitor voltages at different operating conditions. It can be observed that the series operation of the three SMs is working properly for different wave shapes at different operating voltages as required. In addition, though the obtained waveforms are only with a single MV SM without any output voltage control, their quality is acceptable with THD around 5%. The THD for the nonsinusoidal waveform is obtained as

$$\text{THD}_{\text{nonsin}} = \frac{\sqrt{\sum_{h=0}^{\infty}(V_{h,\text{ref}} - V_{h,\text{out}})^2}}{V_{1,\text{out}}}. \tag{17}$$

Apart from the wide voltage range, Fig. 27(a) and (f) shows the operation of MMC-based AWG when the reference waveform is varying from 1 to 600 Hz. As discussed in Section IV, the large ripple of roughly 30 V is visible in Fig. 27(a). The large capacitor voltage ripple of 30 V exists only because of the APS consumption, as per the calculations from (15). The capacitor voltage ripple is reducing from 10 to 600 Hz waveform since the APS consumption is negligible due to the minimum period with high frequency. Note that the SM capacitor voltages are shown for 1 s irrespective of the frequency of the waveform, and all the SM capacitors are balanced well. With only a single SM per arm, the current harmonics are not filtered in any of the waveforms shown, and the switching harmonics are distinctively visible in 600 Hz since the ratio of switching frequency to reference waveform is lowered. In addition, the THD of all waveforms shown in Fig. 27 is within 5%. The fastest rise obtained from the MMC-based HV AWG is found to be 170 μs when 800-V dc voltage is applied with a modulation index of 0.9. Its performance is shown in Fig. 28, and the obtained slew rate is 2.35 V/μs. The rise time generated from the MMC-based HV AWG is limited since the arm inductor is present, and switches have limited current capability [30]. After verifying the start-up, steady-state, and shutdown operation of the MMC-based HV AWG, the FRT capability of the test source is verified in Fig. 29. Here, the load capacitor is shorted using an HV relay with a small resistance of 40 Ω. When such an event occurs, the arm current increases, and the overcurrent protection operates when the current crosses the set point of 1 A. As discussed in Section IV-D, the fault protection operates within 40 μs and protects the MMC hardware.

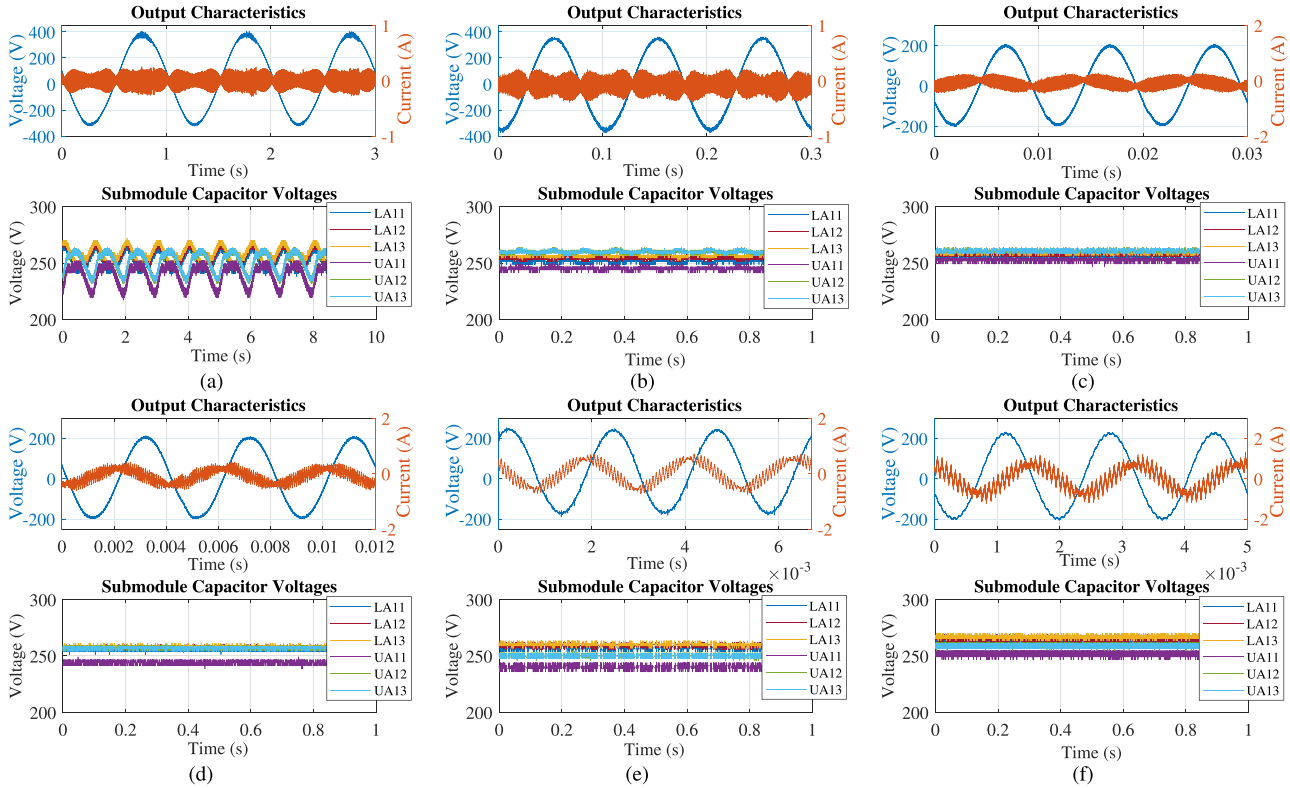


FIGURE 27. Experimental results with wide output frequency range. (a) 1 Hz sinusoidal. (b) 10 Hz sinusoidal. (c) 100 Hz sinusoidal. (d) 250 Hz sinusoidal. (e) 450 Hz sinusoidal. (f) 600 Hz sinusoidal.

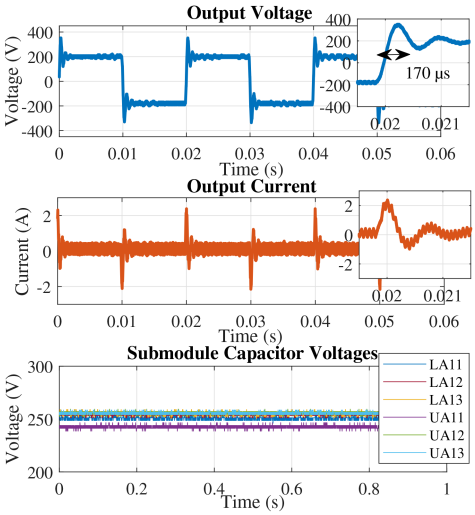


FIGURE 28. Square pulse waveform.

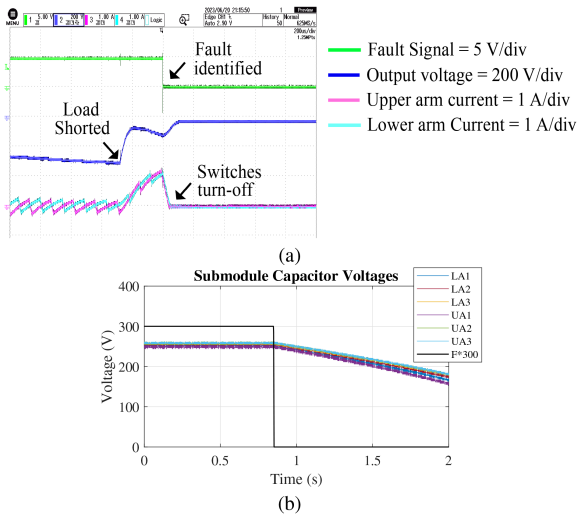


FIGURE 29. FRT performance. (a) Output characteristics. (b) SM capacitor voltages.

VI. GUIDELINES FOR THE FULL-SCALE PROTOTYPE

The experimental results prove the feasibility of the series operation of three SMs to create an MV SM, and this MV SM is scalable to stack more of these to create 100-kV rated MMC-based HV AWG. Since the MV SM is realized using the commercially available component, the production of the MMC-based HV AWG is possible and cost-effective. One of the major challenges faced was the APS and its mismatch in the start-up. A hardware solution to control the start of all APSs together will be helpful. Then, the demonstration of the MV SM is done with a central controller where all data of the SM capacitor voltage, fault, enable, and gate pulse data are exchanged with the central controller. For the full-scale prototype, it will be important to move to a distributed controller, as shown in Fig. 30. The arm energy controller shown in

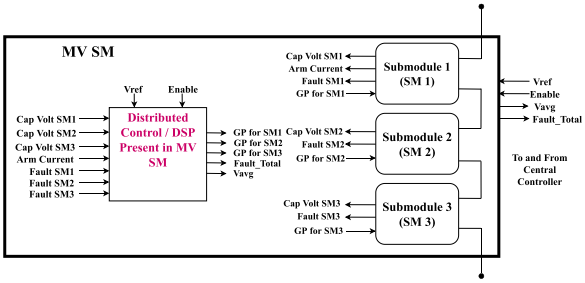


FIGURE 30. Overall control architecture for an MV SM.

Fig. 12 should be implemented in the local DSP to reduce the total required fiber-optic communication units. In the current system, each SM has seven to eight fiber optics, and the total fiber-optic elements for the MV SM will be 23–24 fiber-optic elements. The distributed control system will reduce the number of fiber-optic elements to 4 per HV module.

Currently, the input of the MMC-based HV AWG is implemented using a Glassman HV source (EQ series with 10-kV voltage rating and 120-mA current rating) and two split capacitors with 50 μF. A similar structure is proposed for the full-scale prototype of the HV AWG, where the split capacitors are reduced to lower values, such as a few microfarads. However, an HVDC source with a variable voltage range from 20 to 200 kV is needed. For such an implementation, there is a traditional cascaded rectifier design [10] or transformer and diode rectifier-based design [47]. With these existing solutions, the MMC-based HV AWG can be realized, providing the flexibility to generate different complex waveforms for dielectric testing of HV grid assets.

VII. CONCLUSION

To test HV equipment with increasingly complex transients obtained from various power system studies, this article demonstrates the performance of the scalable series-connected MV SM design for the MMC-based HV AWG. The proposed MV SM generates a wide output voltage range of 0.12–1.2 kV to satisfy the requirement posed by the HV AWG application. In addition, the proposed design of SM capacitance works for different arbitrary wave shapes with a wide output frequency range from 1 to 600 Hz. With the extensive quantitative analysis of the system parameters affecting the start-up behavior, a new and comprehensive start-up procedure is formulated for the proper operation of the MMC-based HV AWG. During the steady-state operation, the series connection of three SMs works as expected with the designed control system for a wide SM voltage range and different wave shapes with different frequencies. Overall, this MV SM fulfills HV test requirements, and the design behaves as expected and can generate bipolar voltage waveforms for dielectric testing of various insulating materials and HV equipment. With the MV SM realized using the off-the-shelf component, the proposed design is recommended to develop the MMC-based HV AWG for testing for MV class equipment.

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